19-1268; Rev 0; 8/97

EVALUATION KIT AVAILABLE

Low-Voltage, Precision Step-Down Controller for Portable CPU Power

General Description

The MAX1636 is a synchronous, buck, switch-mode, power-supply controller that generates the CPU supply voltage in battery-powered systems. It achieves ±1% output voltage accuracy and offers the excellent load-transient response needed by upcoming generations of dynamic-clock CPUs.

Up to 95% efficiency is achieved through synchronous rectification and Maxim's proprietary Idle Mode™ control scheme. Efficiency is greater than 80% over a 1000:1 load-current range, extending battery life in system-suspend or standby modes. Excellent dynamic response corrects output load transients caused by the latest dynamic-clock CPUs within five 300kHz clock cycles. Strong, 1A, on-board gate drivers ensure fast, external N-channel MOSFET switching.

The MAX1636 features a logic-controlled and synchronizable, fixed-frequency, pulse-width-modulation (PWM) operating mode that reduces noise and RF interference in sensitive mobile communications and pen-entry applications. Holding $\overline{SKIP}$ high forces fixed-frequency mode for lowest noise under all load conditions.

For a low-cost version that omits the +5V VL linear-regulator block and comes in a smaller 16-pin QSOP package, refer to the MAX1637 data sheet.

Applications

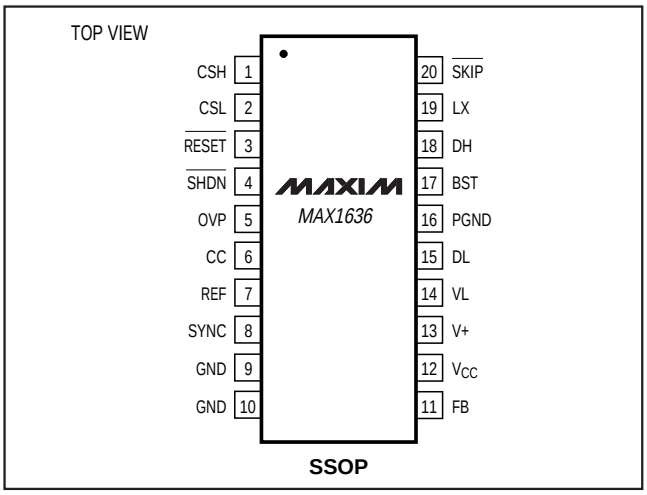
Notebook Computers

Subnotebook Computers

Desktop Computers

Bus-Termination Supplies

Pin Configuration



Idle Mode is a trademark of Maxim Integrated Products.

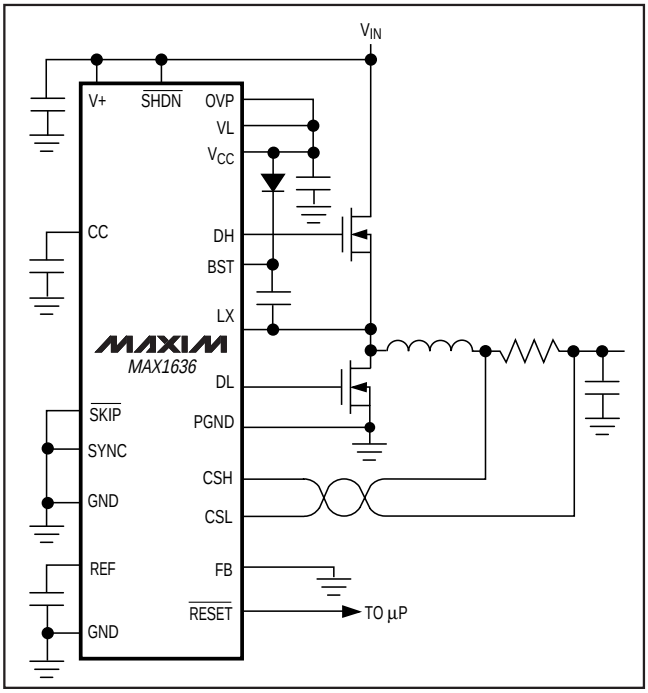
Features

- ♦ **±1% DC Accuracy (Adjustable Mode)**
- ♦ **Output Overvoltage Crowbar Protection**
- ♦ **Output Undervoltage Shutdown**
- ♦ **Adjustable Switching Frequency to 340kHz**
- ♦ **Low-Dropout Operation**
- ♦ **Idle Mode Pulse-Skipping Operation**
- ♦ **1.10V to 5.5V Adjustable Output Voltage**
- ♦ **2.5V/3.3V Dual-Mode Fixed-Output Settings**
- ♦ **Internal Digital Soft-Start**
- ♦ **1.1V ±1% Reference Output**
- ♦ **3µA (typ) Shutdown Current**
- ♦ **Open-Drain Power-Good Output ($\overline{RESET}$)**
- ♦ **20-Pin SSOP Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1636EAP	-40°C to +85°C	20 SSOP

Typical Operating Circuit



Low-Voltage, Precision Step-Down Controller for Portable CPU Power

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to 36V
GND to PGND.....±2V
$\overline{SHDN}$ to GND. ..... -0.3V to 36V
LX, BST to GND. ..... -0.3V to 36V
DH, BST to LX.....-0.3V to 6V
VL, V_{CC}, CSL, CSH, FB, $\overline{SKIP}$ to GND ..... -0.3V to 6V
DL to GND.. .....-0.3V to (VL + 0.3V)
REF, $\overline{RESET}$, SYNC, CC, OVP to GND. ..... -0.3V to (V_{CC} + 0.3V)
VL Output Current... .....50mA
VL Short Circuit to GND.....Momentary

REF Output Current 20mA
REF Short Circuit to GND ....Indefinite
Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Range
MAX1636EAP. .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 15V, SYNC = VL = V_{CC}, I_{VL} = 0mA, I_{REF} = 0mA, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SMPS CONTROLLER					
Input Voltage Range, V+	Input source for VL regulator	4.5		30	V
Input Voltage Range, VL	Gate-driver supply rail	4.2		5.5	V
Input Voltage Range, V_{CC}	Internal chip supply rail	3.15		5.5	V
Output Voltage, Adj Mode	FB tied to V_{OUT}, 0mV < (CSH - CSL) < 80mV, 4.5V < V+ < 30V (includes line and load regulation)	1.090	1.100	1.110	V
Output Voltage, Fixed 2.5V Mode	FB tied to V_{CC}, 0mV < (CSH - CSL) < 80mV, 4.5V < V+ < 30V (includes line and load regulation)	2.486	2.55	2.614	V
Output Voltage, Fixed 3.3V Mode	FB tied to GND, 0mV < (CSH - CSL) < 80mV, 4.5V < V+ < 30V (includes line and load regulation)	3.282	3.366	3.450	V
Output Adjustment Range	V_{CC} = VL = 5V	V_{REF}		5.5	V
	V_{CC} = 3.3V, VL = 5V	V_{REF}		3.6	
Current-Limit Threshold	Positive direction	80	100	120	mV
	Negative direction	-145	-100	-55	
Power Consumption	V_{CC} = 5V, output not switching			2.0	mW
	V_{CC} = 3.3V, output not switching			1.5	
Shutdown Supply Current (V+)	$\overline{SHDN}$ = GND, OVP = GND		3	10	µA
FB Input Current	FB forced to REF	-50		50	nA
Soft-Start Ramp Time	$\overline{SHDN}$ to full current limit, five levels		512		clks
Idle Mode Switchover Threshold	CSH - CSL	20	30	40	mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, SYNC = VL = V_{CC}, I_{VL} = 0mA, I_{REF} = 0mA, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL VL REGULATOR AND REFERENCE					
Regulator Supply Current (V+)	V_{CC} = 5V, I(VL) = 0			60	µA
	V_{CC} = 5V, I(VL) = 0, V+ = 4.5V (includes PNP base current)			500	
Standby Supply Current (V+)	$\overline{SHDN}$ = GND, OVP = V_{CC}			60	µA
VL Output Voltage	I(VL) = 0 to 25mA, 5V < V+ < 30V	4.5	5.0	5.3	V
	I(VL) = 0 to 25mA, 6V < V+ < 30V	4.7	5.0	5.3	
VL Undervoltage Lockout Threshold	Rising edge, hysteresis = 25mV	3.45	3.60	3.75	V
VL/ V_{CC} Switchover Threshold	Rising edge, hysteresis = 25mV		3.15		V
REF Output Voltage	No REF load	1.090	1.100	1.110	V
REF Load Regulation	REF load = 0 to 50µA			10	mV
REF Line Regulation	V_{CC} = 3.3V to 5.5V			3	mV
OSCILLATOR					
Oscillator Frequency	SYNC = V_{CC}	270	300	330	kHz
	SYNC = GND	170	200	230	
Maximum Duty Factor	SYNC = V_{CC}	91	94		%
	SYNC = GND	93	96		
Maximum Duty Factor, Dropout Mode	SYNC = GND	98	99		%
SYNC Input Pulse Width High		200			ns
SYNC Input Pulse Width Low		200			ns
SYNC Input Rise/Fall Time	Guaranteed by design			200	ns
SYNC Input Frequency Range		240		340	kHz
OVERVOLTAGE PROTECTION					
Overvoltage Trip Threshold	FB, with respect to regulation point	4	7	10	%
Overvoltage Fault Propagation Delay	FB to DL delay, 22mV overdrive, C_{GATE} = 2000pF		1.25		µs
Thermal Shutdown Threshold	Hysteresis = 10°C		150		°C
Catastrophic Output Undervoltage Lockout Threshold	% of nominal output	60	70	80	%
Catastrophic Output Undervoltage Lockout Delay	From shutdown or power-on-reset state		6144		clks
$\overline{RESET}$ Trip Threshold	Falling edge (hysteresis = 1%)	-6		-3	%
$\overline{RESET}$ Delay Time			32768		clks
INPUTS AND OUTPUTS					
Logic Input Voltage High	$\overline{SHDN}$, $\overline{SKIP}$, OVP, SYNC	2.4			V
Logic Input Voltage Low	$\overline{SHDN}$, $\overline{SKIP}$, OVP, SYNC			0.8	V
Logic Input Bias Current	Pin at GND or V_{CC}; $\overline{SKIP}$, OVP, SYNC	-1		1	µA
$\overline{SHDN}$ Input Bias Current	$\overline{SHDN}$ = GND or V+	-3		3	µA
$\overline{RESET}$ Output Voltage Low	I_{SINK} = 4mA			0.4	V
$\overline{RESET}$ Output Leakage Current	+5.5V stress voltage applied			1	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, SYNC = VL = V_{CC}, I_{VL} = 0mA, I_{REF} = 0mA, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Sense Input Leakage Current	CSH = CSL = 5V, V+ = VL = V_{CC} = GND, either CSH or CSL input			10	µA
Gate-Driver Sink/Source Current	DH or DL forced to 2V		1		A
Gate-Driver On-Resistance	High or low, DH or DL			7	Ω

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 15V, SYNC = VL = V_{CC}, I_{VL} = 0mA, I_{REF} = 0mA, **T_A =-40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SMPS CONTROLLER					
Input Voltage Range, V+	Input source for VL regulator	4.5		30	V
Input Voltage Range, VL	Gate-driver supply rail	4.2		5.5	V
Input Voltage Range, V_{CC}	Internal chip supply rail	3.15		5.5	V
Output Voltage, Adj Mode	FB tied to V_{OUT}, 0mV < (CSH - CSL) < 80mV, 4.5V < V+ < 30V (includes line and load regulation)	1.086		1.114	V
Output Voltage, Fixed 2.5V Mode	FB tied to V_{CC}, 0mV < (CSH - CSL) < 80mV, 4.5V < V+ < 30V (includes line and load regulation)	2.432		2.635	V
Output Voltage, Fixed 3.3V Mode	FB tied to GND, 0mV < (CSH - CSL) < 80mV, 4.5V < V+ < 30V (includes line and load regulation)	3.195		3.497	V
Output Adjustment Range	V_{CC} = VL = 5V	V_{REF}		5.5	V
	V_{CC} = 3.3V, VL = 5V	V_{REF}		3.6	
Current-Limit Threshold	Positive direction	70		130	mV
Power Consumption	V_{CC} = 5V, output not switching			2.0	mW
	V_{CC} = 3.3V, output not switching			1.5	
INTERNAL VL REGULATOR AND REFERENCE					
Regulator Supply Current (V+)	V_{CC} = 5V, I(VL) = 0			60	µA
	V_{CC} = 5V, I(VL) = 0, V+ = 4.5V (includes PNP base current)			500	
Standby Supply Current (V+)	$\overline{SHDN}$ = GND, OVP = V_{CC}			60	µA
VL Output Voltage	I(VL) = 0 to 25mA, 5V < V+ < 30V	4.5		5.3	V
	I(VL) = 0 to 25mA, 6V < V+ < 30V	4.7		5.3	
VL Undervoltage Lockout Threshold	Rising edge, hysteresis = 25mV	3.45		3.91	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, SYNC = VL = V_{CC}, I_{VL} = 0mA, I_{REF} = 0mA, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

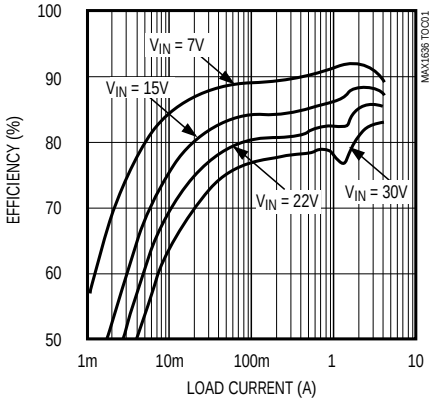
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR					
Oscillator Frequency	SYNC = V_{CC}	270		330	kHz
	SYNC = GND	170		230	
SYNC Input Pulse Width High		200			ns
SYNC Input Pulse Width Low		200			ns
SYNC Input Rise/Fall Time	Guaranteed by design			200	ns
SYNC Input Frequency Range		240		340	kHz
OVERVOLTAGE PROTECTION					
Overvoltage Trip Threshold	FB, with respect to regulation point	3.5		10	%
Catastrophic Output Undervoltage Lockout Threshold	% of nominal output	60		80	%
$\overline{\text{RESET}}$ Trip Threshold	Falling edge (hysteresis = 1%)	-7		-1.5	%
INPUTS AND OUTPUTS					
Logic Input Voltage High	$\overline{\text{SHDN}}$, $\overline{\text{SKIP}}$, OVP, SYNC	2.4			V
Logic Input Voltage Low	$\overline{\text{SHDN}}$, $\overline{\text{SKIP}}$, OVP, SYNC			0.8	V
$\overline{\text{RESET}}$ Output Voltage Low	I_{SINK} = 4mA			0.4	V
Gate-Driver On-Resistance	High or low, DH or DL			7	Ω

Note 1: Specifications to -40°C are guaranteed by design and not production tested.

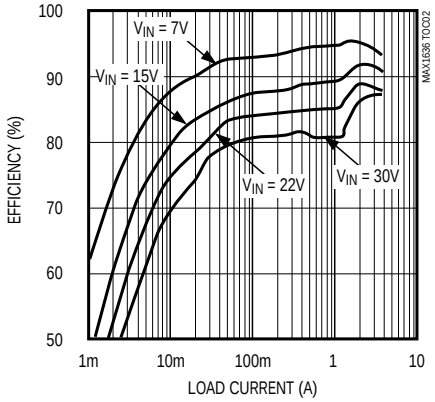
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 7V, T_A = +25°C, unless otherwise noted.)

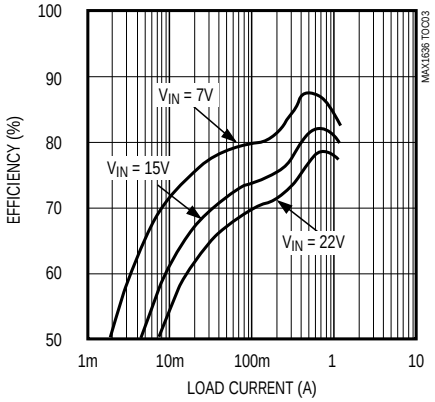
EFFICIENCY vs. LOAD CURRENT (3.3V/3A CIRCUIT)



EFFICIENCY vs. LOAD CURRENT (5V/3A CIRCUIT)



EFFICIENCY vs. LOAD CURRENT (1.8V/1A CIRCUIT)

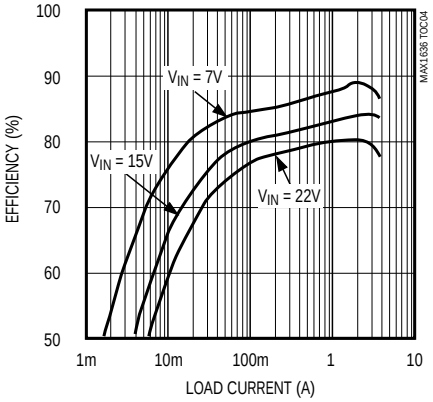


Low-Voltage, Precision Step-Down Controller for Portable CPU Power

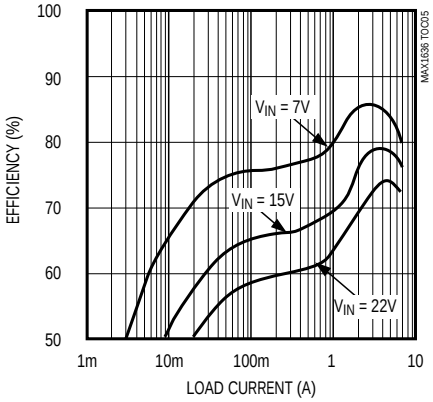
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 7V, T_A = +25°C, unless otherwise noted.)

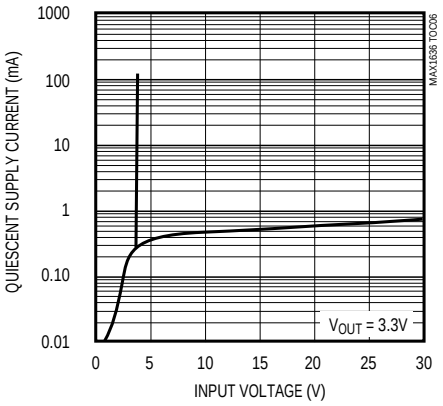
EFFICIENCY vs. LOAD CURRENT (1.8V/4A CIRCUIT)



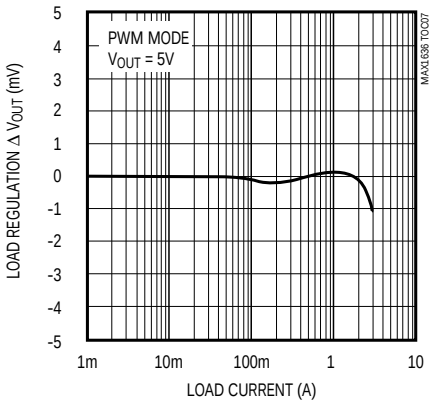
EFFICIENCY vs. LOAD CURRENT (1.8V/7A CIRCUIT)



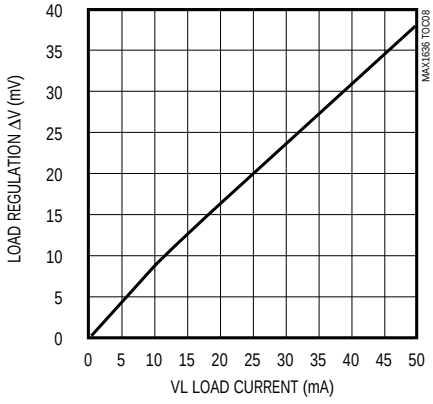
QUIESCENT SUPPLY CURRENT vs. INPUT VOLTAGE



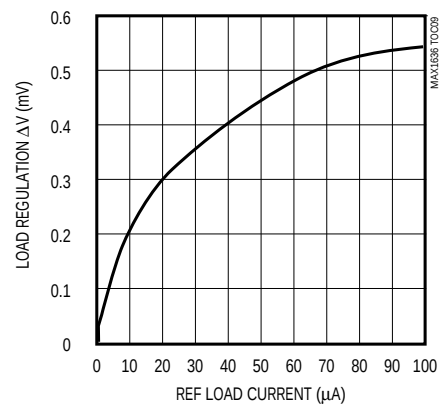
LOAD REGULATION vs. LOAD CURRENT



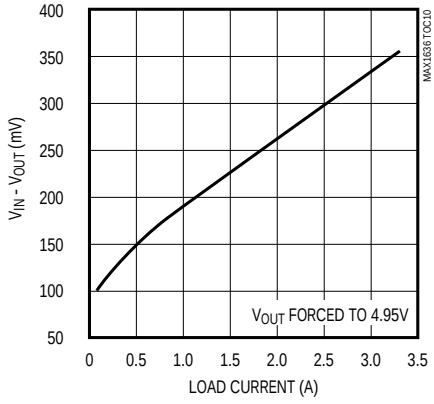
VL LOAD-REGULATION ERROR vs. VL LOAD CURRENT



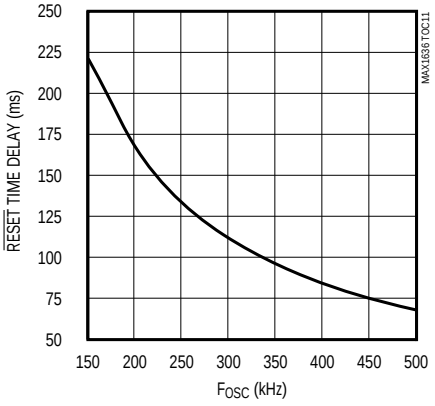
REF LOAD-REGULATION ERROR vs. REF LOAD CURRENT



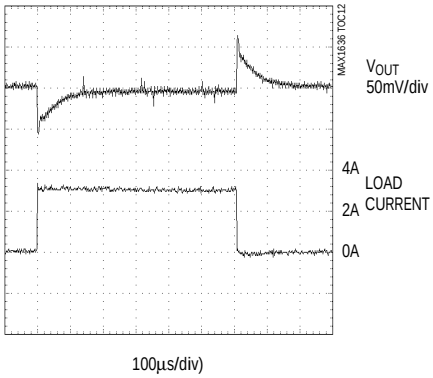
DROPOUT VOLTAGE vs. LOAD CURRENT



$\overline{\text{RESET}}$ TIME DELAY vs. OSC FREQUENCY



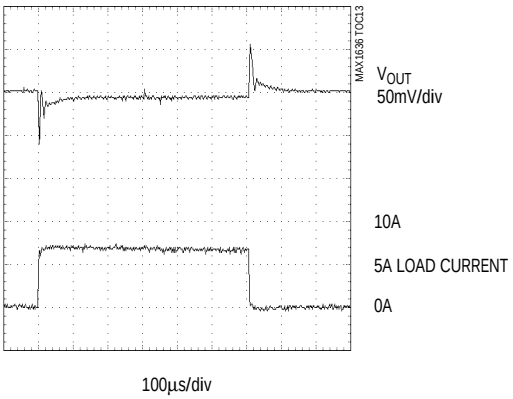
LOAD-TRANSIENT RESPONSE (3.3V/3A, PWM MODE)



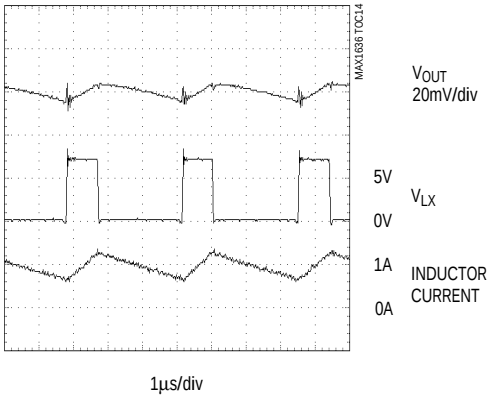
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 7V, T_A = +25°C, unless otherwise noted.)

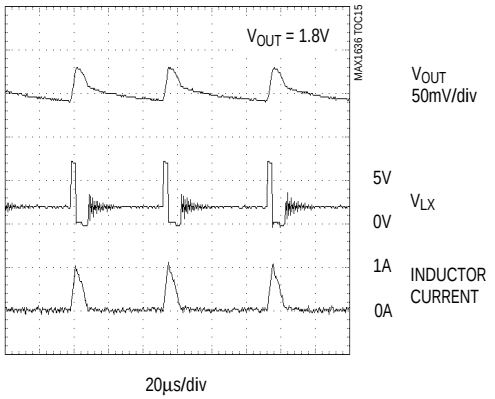
LOAD-TRANSIENT RESPONSE (1.8V, PWM MODE)



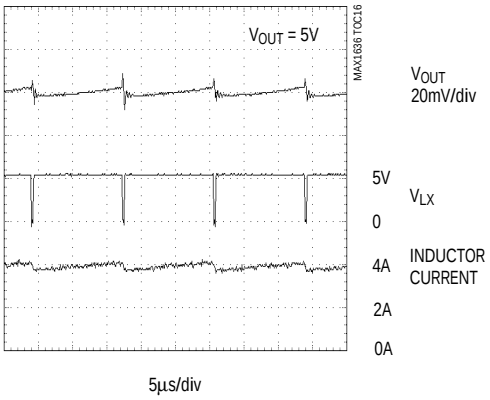
SWITCHING WAVEFORMS (PWM MODE)



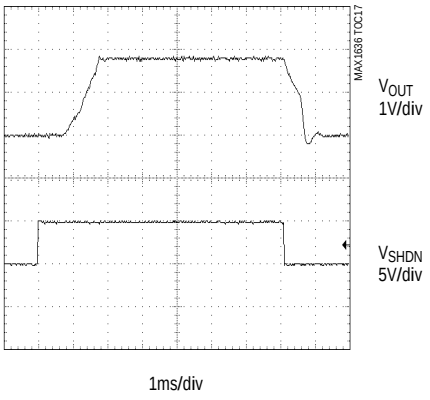
SWITCHING WAVEFORMS (PFM MODE)



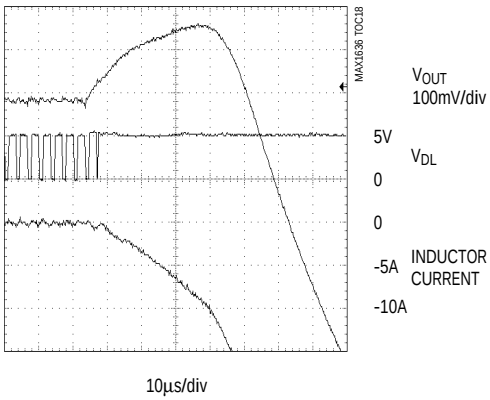
SWITCHING WAVEFORMS (DROPOUT OPERATION)



STANDBY AND STARTUP RESPONSE (V_{OUT} = 1.8V, NO LOAD)



OVERVOLTAGE-PROTECTION WAVEFORMS (V_{IN} SHORTED TO V_{OUT} THROUGH a 0.5Ω RESISTOR)



Pin Description

PIN	NAME	FUNCTION
1	CSH	Current-Sense Input, High Side
2	CSL	Current-Sense Input, Low Side. Also serves as a feedback input in fixed output modes.
3	$\overline{\text{RESET}}$	Timed Reset Output. Low for at least 100ms after output voltage is valid, then goes high impedance (open drain).
4	$\overline{\text{SHDN}}$	Shutdown Control Input. Puts chip in shutdown or standby mode, depending on OVP (Table 5).
5	OVP	Overvoltage Protection Enable/Disable. Tie to GND to disable OVP; tie to V_{CC} to enable OVP.
6	CC	Compensation pin. Connect a small capacitor to GND to set the integration time constant.
7	REF	1.100V Reference Output. Capable of sourcing 50µA for external loads; bypass with a 0.22µF (min) capacitor.
8	SYNC	Oscillator Frequency Select and Synchronization Input. Tie to V_{CC} for 300kHz operation; tie to GND for 200kHz operation.
9, 10	GND	Analog Ground
11	FB	Feedback Input. Tie to GND for fixed 3.3V output; tie to V_{CC} for fixed 2.5V output; tie to resistor divider for adjustable mode.
12	V_{CC}	Main Supply Voltage Input. Powers the PWM controller, logic, and reference. Input range is +3.15V to +5.5V.
13	V+	5V VL Linear-Regulator Input. The VL linear regulator automatically shuts off if V+ is left open or shorted to V_L. Bypass V+ to GND with a 0.1µF capacitor close to the IC.
14	VL	5V Linear-Regulator Output. Powers the DL low-side gate driver. Bypass with a 2.2µF (min) capacitor.
15	DL	Low-Side Gate-Driver Output
16	PGND	Power Ground
17	BST	Boost-Capacitor Connection
18	DH	High-Side Gate-Driver Output
19	LX	Inductor Connection
20	$\overline{\text{SKIP}}$	Low-Noise Mode Control. Forces fixed-frequency PWM operation when high.

Standard Application Circuit

The basic MAX1636 buck converter (Figure 1) is easily adapted to meet a wide range of applications with inputs up to 30V by substituting components from Table 1. These circuits represent a good set of trade-offs between cost, size, and efficiency, while staying within the worst-case specification limits for stress-related parameters, such as capacitor ripple current. Do not change the circuits' switching frequency without first recalculating component values (particularly inductance value at maximum battery voltage). Adding a Schottky rectifier across the synchronous rectifier improves circuit efficiency by approximately 1%. This rectifier is otherwise not needed because the MOSFET required typically incorporates a high-speed silicon diode from drain to source. Use a Schottky rectifier rated at a DC current equal to at least one-third of the load current.

Table 1. Component Selection for Standard Applications

COMPONENT	LOAD CURRENT				
	1A	4A	7A (EV KIT)	3A	3A
Input Voltage Range	7V to 22V	7V to 22V	7V to 22V	4.75V to 30V	6V to 30V
Output Voltage Range	1.8V	1.8V	1.25V to 2V	3.3V	5V
Application	CPU I/O	CPU Core	CPU Core		
Frequency	300kHz	300kHz	300kHz	300kHz	300kHz
Q1 High-Side MOSFET	1/2 Si4902DY or 1/2 MMDF3NO3HD	International Rectifier IRF7413, Fairchild NDS8410A, or Siliconix Si4410DY	International Rectifier IRF7403 or Siliconix Si9804DY	International Rectifier IRF7413, Fairchild NDS8410A, or Siliconix Si4410DY	International Rectifier IRF7413, Fairchild NDS8410A, or Siliconix Si4410DY
Q2 Low-Side MOSFET	1/2 Si4902DY or 1/2 MMDF3NO3HD	International Rectifier IRF7413, Fairchild NDS8410A, or Siliconix Si4410DY	Fairchild FDS6680 or Siliconix Si4420DY	International Rectifier IRF7413, Fairchild NDS8410A, or Siliconix Si4410DY	International Rectifier IRF7413, Fairchild NDS8410A, or Siliconix Si4410DY
C1 Input Capacitor	4.7µF, 25V ceramic Tokin C34Y5U1E475Z or Marcon/United Chemicon THCR40E1E475Z	2 x 10µF, 25V ceramic Tokin C34Y5U1E106Z or Marcon/United Chemicon THCR50E1E106ZT	4 x 10µF, 25V ceramic Tokin C34Y5U1E106Z or Marcon/United Chemicon THCR50E1E106ZT	2 x 22µF, 35V AVX TPSE226M035R0300 or Sprague 593D226X0035E2W	2 x 22µF, 35V AVX TPSE226M035R0300 or Sprague 593D226X0035E2W
C2 Output Capacitor	220µF, 6.3V tantalum Sprague 595D227X96R3C2	2 x 470µF, 4V low-ESR Sprague 594D477X0004R2T	4 x 390µF, 6.3V low-ESR, Sprague 594D397X06R3R2T, or 4 x 470µF, 4V Sprague 594D477X0004R2T	2x 220µF Sprague 594D 594D227X0010D2T	2x 220µF Sprague 594D 594D227X0010D2T
R1 Resistor	0.070Ω, 1% (1206) Dale WSL-1206-R070F	0.015Ω, 1% (2512) Dale WSL-2512-R015F	0.010Ω, 1% (2512) Dale WSL-2512-R010F	0.020Ω, 1% (2010) Dale WSL-2010-R020F	0.020Ω, 1% (2010) Dale WSL-2010-R020F
L1 Inductor	15µH Sumida CD54-150	4.6µH Panasonic ETQP1F4R6H, Sumida CDRH127-4R7, Coiltronics UP2-4R7, or Coilcraft DO3316P-472	2.2µH Panasonic P1F2R0HL, Sumida CDRH127-2R4, Coiltronics UP4-2R2, or Coilcraft DO5022P-222HC	10µH Sumida CDRH125-100, Coiltronics UP2-100, or Coilcraft DO3316-103	10µH Sumida CDRH125-100, Coiltronics UP2-100, or Coilcraft DO3316-103

Low-Voltage, Precision Step-Down Controller for Portable CPU Power

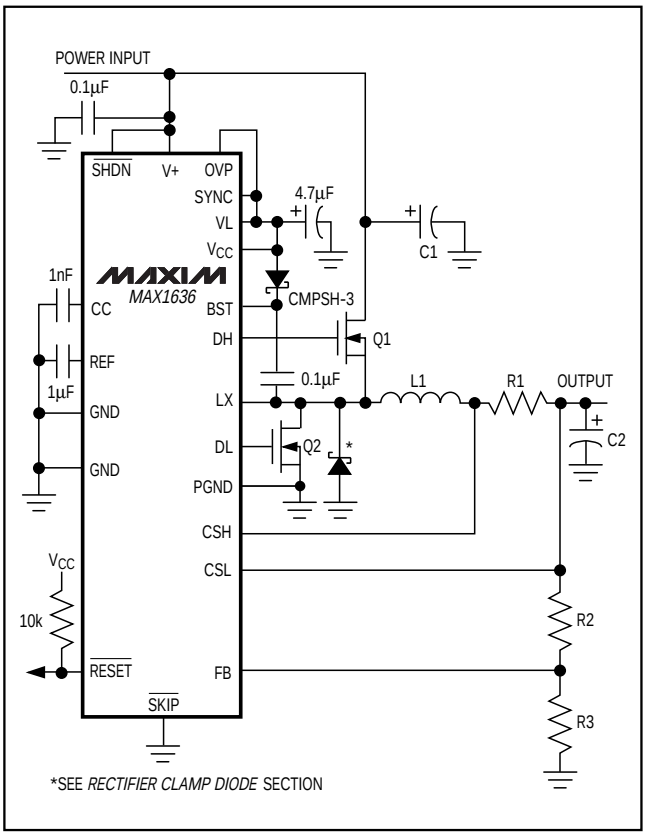


Figure 1. Standard Application Circuit

Table 2. Component Suppliers

COMPANY	FACTORY FAX (COUNTRY CODE)	USA PHONE
AVX	(1) 803-626-3123	(803) 946-0690
Central Semiconductor	(1) 516-435-1824	(516) 435-1110
Coilcraft	(1) 847-639-1469	(847) 639-6400
Coiltronics	(1) 561-241-9339	(561) 241-7876
Dale	(1) 605-665-1627	(605) 668-4131
Fairchild	(1) 408-721-1635	(408) 721-2181
International Rectifier (IR)	(1) 310-322-3332	(310) 322-3331
IRC	(1) 512-992-3377	(512) 992-7900
Marcon/United Chemi-Con	(1) 847-696-9278	(847) 696-2000
Matsuo	(1) 714-960-6492	(714) 969-2491
Motorola	(1) 602-994-6430	(602) 303-5454
Panasonic	(1) 714-373-7183	(714) 373-7939
Sanyo	(81) 7-2070-1174	(619) 661-6835
Siliconix	(1) 408-970-3950	(408) 988-8000
Sprague	(1) 603-224-1430	(603) 224-1961
Sumida	(81) 3-3607-5144	(847) 956-0666
TDK	(1) 847-390-4428	(847) 390-4373
Tokin	(1) 408-434-0375	(408) 432-8020

Detailed Description

The MAX1636 is a BiCMOS, switch-mode, power-supply controller designed primarily for buck-topology regulators in battery-powered applications where high efficiency and low quiescent supply current are critical. Light-load efficiency is enhanced by automatic Idle Mode operation, a variable-frequency, pulse-skipping mode that reduces transition and gate-charge losses. The step-down, power-switching circuit consists of two N-channel MOSFETs, a rectifier, and an LC output filter. The output voltage is the average AC voltage at the switching node, which is regulated by changing the duty cycle of the MOSFET switches. The gate-drive signal to the N-channel high-side MOSFET, which must exceed the battery voltage, is provided by a flying-capacitor boost circuit that uses a 100nF capacitor between BST and LX. The MAX1636 contains 10 major circuit blocks (Figure 2).

The pulse-width-modulation (PWM) controller consists of a Dual Mode™ feedback network and multiplexer, a multi-input PWM comparator, high-side and low-side gate drivers, and logic. The MAX1636 contains fault-protection circuits that monitor the PWM output for undervoltage and overvoltage. Bias generator blocks include the 5V (VL) linear regulator and the 1.1V precision reference. The PWM uses a 200kHz/300kHz synchronizable oscillator. The circuit blocks are powered from an internal IC power rail that receives power from either VL or V_{CC}. The synchronous-switch gate driver is powered directly from VL, while the high-side-switch gate driver is powered indirectly from VL via an external diode-capacitor boost circuit.

Dual Mode is a trademark of Maxim Integrated Products.

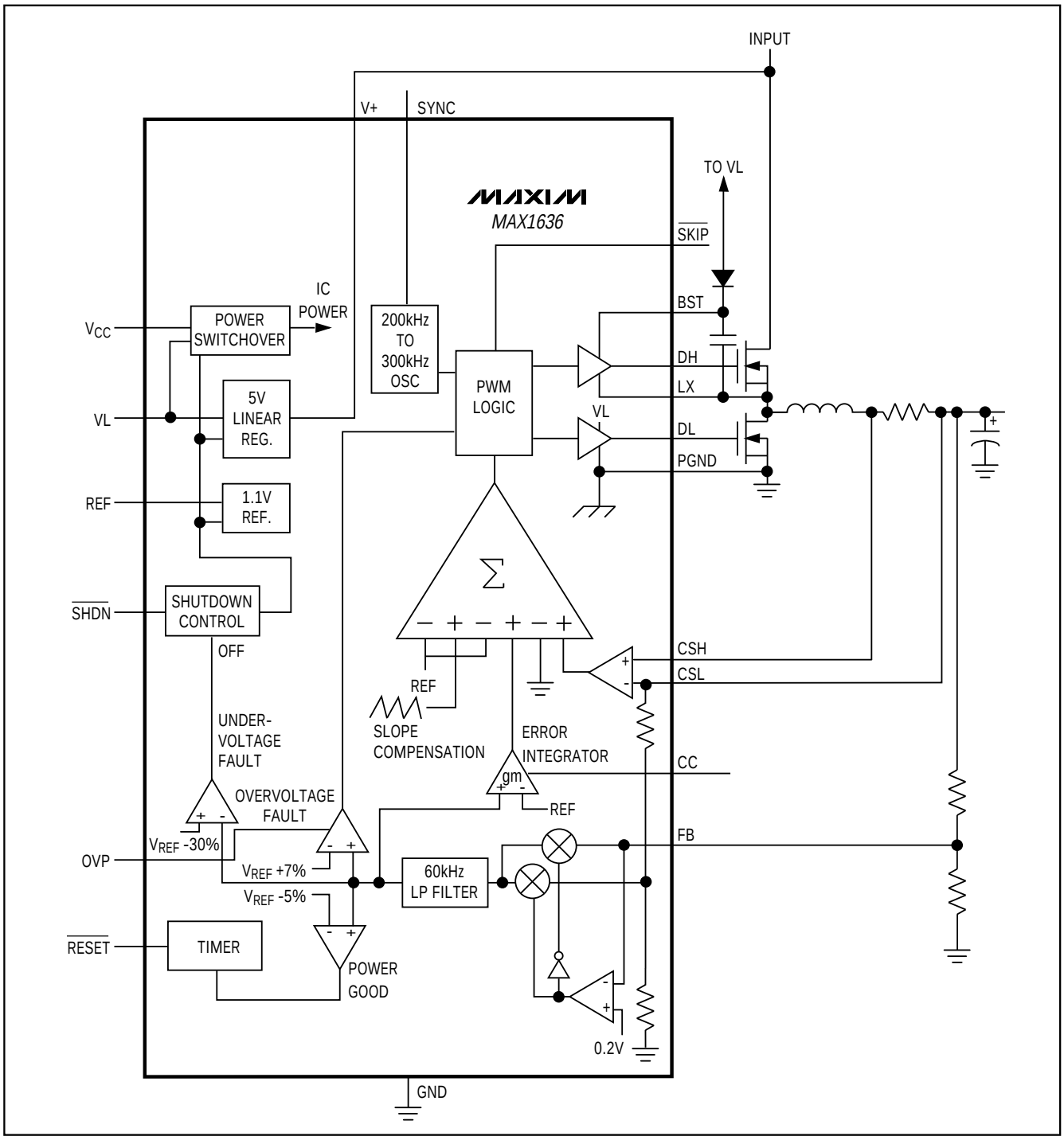


Figure 2. Functional Diagram

Table 3. $\overline{SKIP}$ PWM Table

$\overline{SKIP}$	LOAD CURRENT	MODE	DESCRIPTION
Low	Light	Idle	Pulse-skipping, discontinuous inductor current
Low	Heavy	PWM	Constant-frequency PWM, continuous inductor current
High	Light	PWM	Constant-frequency PWM, continuous inductor current
High	Heavy	PWM	Constant-frequency PWM, continuous inductor current

PWM Controller

The heart of the current-mode PWM controller is a multi-input, open-loop comparator that sums four signals: the output voltage error signal with respect to the reference voltage, the current-sense signal, the integrated voltage-feedback signal, and the slope-compensation ramp (Figure 3).

The PWM controller is a direct-summing type, lacking a traditional error amplifier and the phase shift associated with it. This direct-summing configuration approaches ideal cycle-by-cycle control over the output voltage (Figure 4).

When $\overline{SKIP}$ = low, Idle Mode circuitry automatically optimizes efficiency throughout the load-current range. Idle Mode dramatically improves light-load efficiency

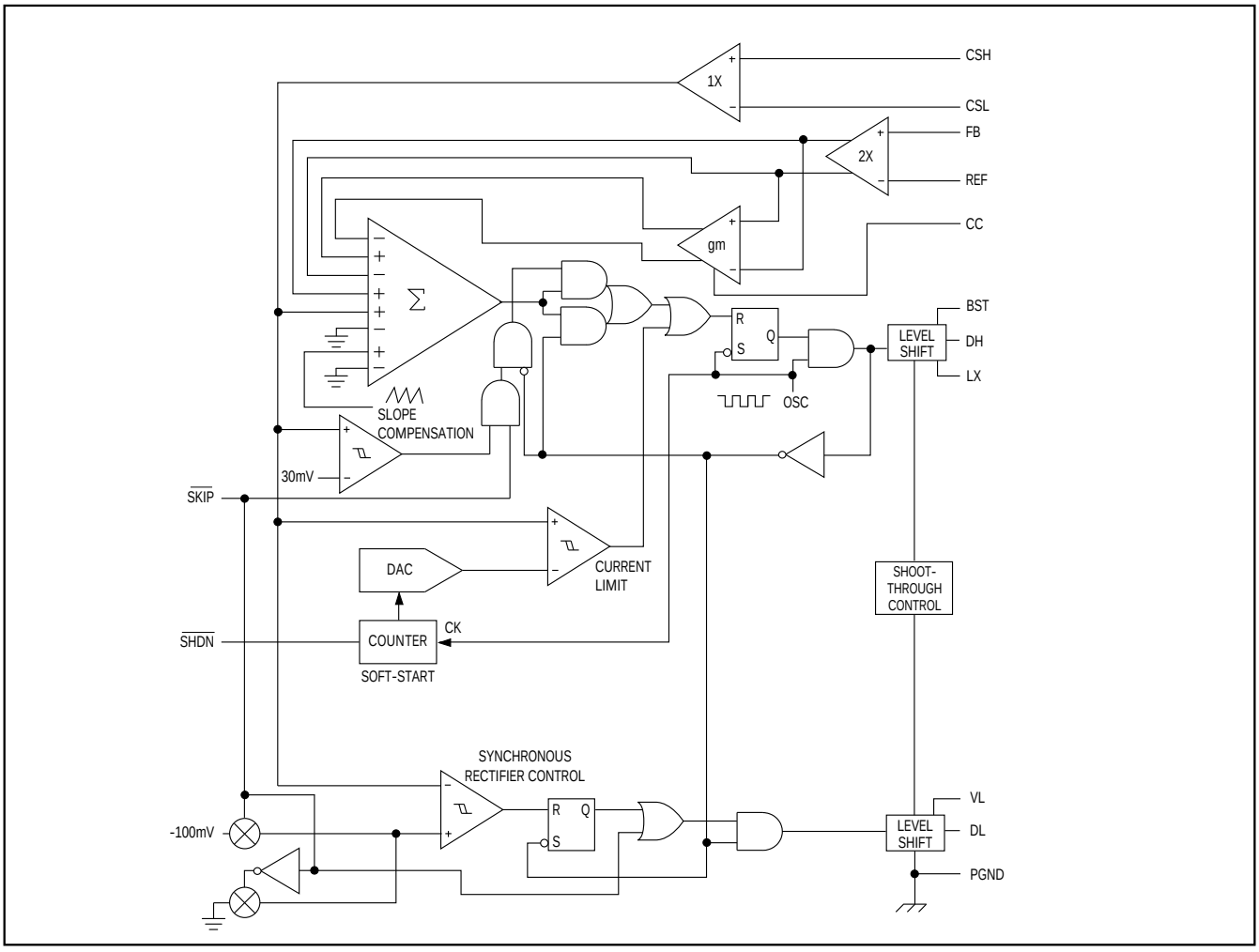


Figure 3. PWM Controller Functional Diagram

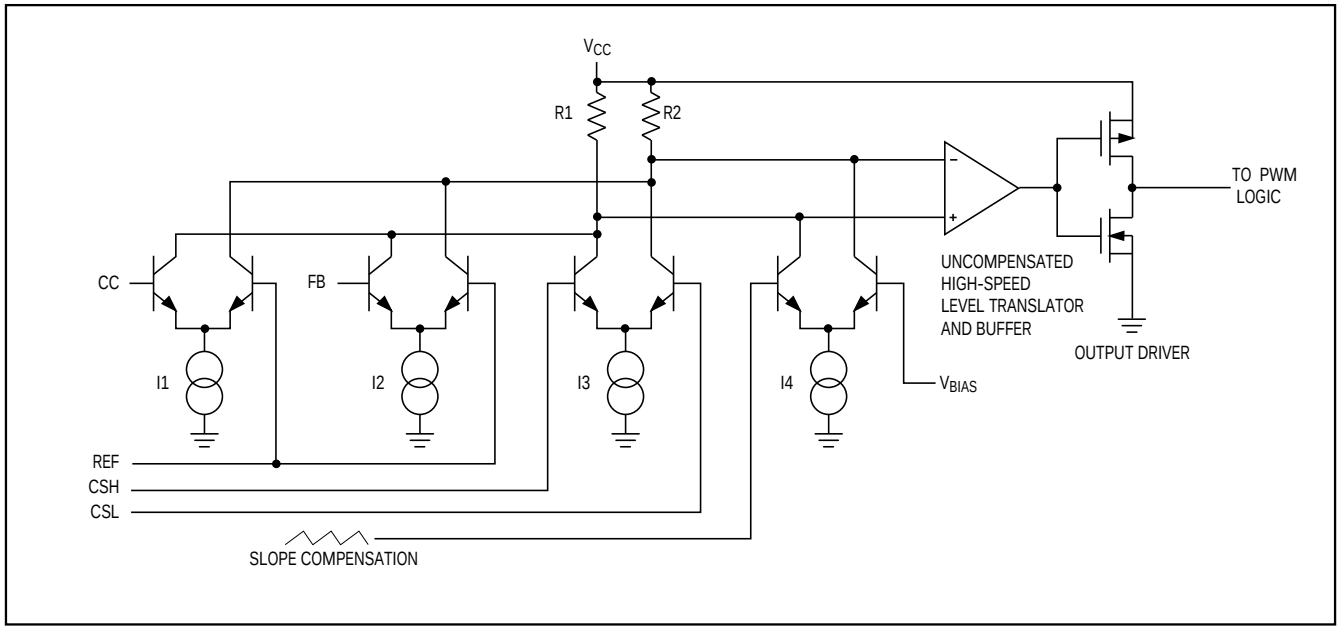


Figure 4. Main PWM Comparator Functional Diagram

by reducing the effective frequency, subsequently reducing switching losses. It forces the peak inductor current to ramp to 30% of the full current limit, delivering extra energy to the output and allowing subsequent cycles to be skipped. Idle Mode transitions seamlessly to fixed-frequency PWM operation as load current increases.

With $\overline{SKIP}$ = high, the controller always operates in fixed-frequency PWM mode for lowest noise. Each pulse from the oscillator sets the main PWM latch that turns on the high-side switch for a period determined by the duty factor (approximately V_{OUT} / V_{IN}). As the high-side switch turns off, the synchronous rectifier latch sets; 60ns later, the low-side switch turns on. The low-side switch stays on until the beginning of the next clock cycle.

In PWM mode, the controller operates as a fixed-frequency, current-mode controller in which the duty factor is set by the input/output voltage ratio. The current-mode feedback system regulates the peak inductor current value as a function of the output voltage error signal. In continuous-conduction mode, the average inductor current is nearly the same as the peak current, so the circuit acts as a switch-mode transconductance amplifier. This pushes the second output LC filter pole, normally found in a duty-factor-controlled (voltage-mode) PWM, to a higher frequency. To preserve inner-loop stability and eliminate regenerative inductor current "staircasing," a slope-compensation ramp is summed into the main PWM comparator to make the apparent duty factor less than 50%.

The relative gains of the voltage-sense and current-sense inputs are weighted by the values of current sources that bias four differential input stages in the main PWM comparator (Figure 4). The voltage sense into the PWM has been conditioned by an integrated component of the feedback voltage, yielding excellent DC output voltage accuracy. See the *Output Voltage Accuracy* section for more information.

Synchronous Rectifier Driver (DL)

Synchronous rectification reduces conduction losses in the rectifier by shunting the normal Schottky catch diode with a low-resistance MOSFET switch. Also, the synchronous rectifier ensures proper start-up of the boost gate-driver circuit. If the synchronous power MOSFET is omitted for cost or other reasons, replace it with a small-signal MOSFET, such as a 2N7002.

If the circuit is operating in continuous-conduction mode, the DL drive waveform is simply the complement of the DH high-side-drive waveform (with controlled dead time to prevent cross-conduction or "shoot-through"). In discontinuous (light-load) mode, the synchronous switch is turned off as the inductor current falls through zero.

Table 4. Powering the MAX1636

AVAILABLE POWER SOURCES	V_{CC} CONNECTS TO	V+ CONNECTS TO	VL CONNECTS TO	COMMENT
Battery, 3.3V, and 5V	3.3V	5V	5V	Most efficient
Battery and 5V	5V	5V	5V	
Battery and 3.3V	3.3V	Battery	Bypass capacitor only	
Battery only	VL	Battery	Bypass capacitor only	Least efficient

REF and VL Supplies and V_{CC} Input

The 1.1V reference (REF) is accurate to ±1% over temperature, making REF useful as a precision system reference. Bypass REF to GND with a 0.22µF (min) capacitor. REF can supply up to 50µA for external loads. Loading REF reduces the main output voltage slightly because of the reference load-regulation error. The 5V VL linear-regulator output can be tied to the system +5V supply in order to obtain gate-drive power from an efficient source. The two supply pins (V_{CC} and VL) are independent of each other (no protection diodes or sequencing requirements), allowing you to choose the most efficient sources for chip biasing from among existing system supply voltages without having to worry about sequencing or latch-up problems (Table 4).

The V_{CC} input runs the chip if the V_{CC} voltage is greater than 3.15V. Otherwise, the chip supply is powered from VL via the internal V_{CC}-VL switchover circuit. If a system supply between 3.3V and 5V is not available, tie V_{CC} directly to VL.

In shutdown mode, the VL regulator and reference are completely turned off. In standby mode, the VL regulator and DL stay alive so that the overvoltage-protection circuit can operate (Table 5).

Important: Ensure that VL and V_{CC} do not exceed 6V. Measure VL with the main output fully loaded. If it is pumped above 5.5V, either excessive boost-diode capacitance or excessive ripple at V+ is the probable cause. Use only small-signal diodes for the boost circuit (10mA to 100mA Schottky or 1N4148 are preferred) and bypass VL to PGND with a 4.7µF capacitor directly at the package pins.

Shutdown and Standby Modes

Holding $\overline{SHDN}$ low puts the IC into its 3µA shutdown mode. $\overline{SHDN}$ is a logic input with a threshold of about 1V (the VTH of an internal N-channel MOSFET). For automatic start-up, tie $\overline{SHDN}$ to V+.

Standby operation is entered when $\overline{SHDN}$ = low and OVP = high (Table 5). In standby mode, the VL regulator stays active, and the DL output is forced high to provide overvoltage protection by clamping the output to GND. However, DL is not forced high until the output sags below V_{REF}, so that the output can be held high by external keep-alive supplies.

$\overline{RESET}$* *Power-Good Voltage Monitor

The power-good monitor generates a system-reset signal. The $\overline{RESET}$ output is an open drain that needs to be pulled up to the appropriate logic supply. At first power-up, $\overline{RESET}$ is held low until output is in regulation. At this point, an internal timer begins counting oscillator pulses, and $\overline{RESET}$ continues to be held low until 32,000 cycles have elapsed. After this timeout period (107ms at 300kHz or 160ms at 200kHz), the $\overline{RESET}$ output is released.

Output Undervoltage Lockout

The output undervoltage-lockout circuit is similar to foldback current limiting but employs a timer rather than a variable current limit. The SMPS has an undervoltage-protection circuit that is activated 6144 clock cycles after the SMPS is enabled. If the SMPS output is under 70% of the nominal value, output is latched off and does not restart until $\overline{SHDN}$ is toggled or until V+ power is cycled below 1V. Note that undervoltage protection can make prototype troubleshooting difficult, since only 20ms or 30ms elapse before the SMPS is latched off.

The output undervoltage lockout circuit protects against heavy overloads and shorts to the main SMPS output. The circuit trips if the output is less than 70% of the nominal output value any time after the timeout has expired upon start-up. When the comparator trips, the output is turned off (the SMPS stops switching). This state is similar to thermal shutdown and can be exited by a power-on reset or by a rising edge on $\overline{SHDN}$. The overvoltage crowbar is disabled in output undervoltage or thermal shutdown modes.

Table 5. Operating Modes

MODE	$\overline{SHDN}$	OVP	HOW ENTERED	STATUS	NOTES
Run	High	High		All circuit blocks active	Normal operation
Standby	Low	High		VL = on REF = off DL = high $\overline{RESET}$ = high-Z (high state)	DL = high to enforce overvoltage protection
Shutdown	Low	Low		All circuit blocks inactive	Lowest possible quiescent consumption
Overvoltage (crowbar)	High	High	V_{OUT} > 7% too high	VL = on REF = off DL = high $\overline{RESET}$ = low	Cycling $\overline{SHDN}$ or a power-on reset exits crowbar.
Output UVLO	High	Don't care	V_{OUT} < 70% of nominal after 20–30ms timeout expires	VL = on REF = off DL = low $\overline{RESET}$ = low	Cycling $\overline{SHDN}$ or a power-on reset exits output UVLO.
Thermal Shutdown	High	High	T_J > +150°C	VL = on REF = off DL = high $\overline{RESET}$ = low	Cycling $\overline{SHDN}$ or a power-on reset exits thermal shutdown.
Thermal Shutdown	High	Low	T_J > +150°C	All circuit blocks inactive	Cycling $\overline{SHDN}$ or a power-on reset exits thermal shutdown.

Output Overvoltage Protection (OVP)

The overvoltage crowbar protection circuit is intended to blow a fuse in series with the battery if the main SMPS output rises significantly higher than its preset level. In normal operation, the output is compared to the internal precision reference voltage. If the output goes 7% above nominal, the synchronous rectifier MOSFET turns on 100% (the high-side MOSFET is simultaneously forced off) in order to draw massive amounts of battery current to blow the fuse. This safety feature does not protect the system against a failure of the controller IC itself but is intended primarily to guard against a short across the high-side MOSFET. A crowbar event is latched and can only be reset by a rising edge on $\overline{SHDN}$ (or by removal of the V+ supply voltage). The overvoltage-detection decision is made relative to the regulation point.

The overvoltage comparators are kept inactive in standby mode. Instead, the DL driver is simply left in the high state. However, DL does not turn on until the output has decayed to less than 1V. This prevents conflicts in systems where the output is held up by an external source in suspend or backup mode. The OVP pin has an internal pulldown resistor that is only turned on during the reset phase. The OVP pin's state is then sampled and stored internally. A floating OVP pin implies no overvoltage protection.

Boost High-Side Gate-Drive Supply (BST)

Gate-drive voltage for the high-side N-channel switch is generated by a flying-capacitor boost circuit (Figure 2). The capacitor between BST and LX is alternately charged from the VL supply and placed parallel to the high-side MOSFET's gate-source terminals.

On start-up, the synchronous rectifier (low-side MOSFET) forces LX to 0V and charges the boost capacitor to 5V. On the second half-cycle, the SMPS turns on the high-side MOSFET by closing an internal switch between BST and DH. This provides the necessary enhancement voltage to turn on the high-side switch, an action that boosts the 5V gate-drive signal above the battery voltage.

Ringing at the high-side MOSFET gate (DH) in discontinuous-conduction mode (light loads) is a natural operating condition. It is caused by residual energy in the tank circuit, formed by the inductor and stray capacitance at the switching node, LX. The gate-drive negative rail is referred to LX, so any ringing there is directly coupled to the gate-drive output.

Current-Limiting and Current-Sense Inputs (CSH and CSL)

The current-limit circuit resets the main PWM latch and turns off the high-side MOSFET switch whenever the voltage difference between CSH and CSL exceeds 100mV. This limiting is effective for both current flow directions, putting the threshold limit at ±100mV. The tolerance on the positive current limit is ±20%, so the external low-value sense resistor (R1) must be sized for 80mV/I_{PEAK}, where I_{PEAK} is the required peak inductor current to support the full load current. Components must be designed to withstand continuous current stresses of 120mV/R1.

For breadboarding or for very high current applications, it may be useful to wire the current-sense inputs with a twisted pair rather than PC traces (two pieces of wrapped wire twisted together are sufficient.) This reduces the noise picked up at CSH and CSL, which can cause unstable switching and reduced output current.

Oscillator Frequency and Synchronization (SYNC)

The SYNC input controls the oscillator frequency. Low selects 200kHz; high selects 300kHz. SYNC can also be used to synchronize with an external 5V CMOS or TTL clock generator. SYNC has a guaranteed 240kHz to 340kHz capture range. A high-to-low transition on SYNC initiates a new cycle.

Operation at 300kHz optimizes the application circuit for component size and cost. Operation at 200kHz provides increased efficiency, lower dropout, and improved load-transient response at low input-output voltage differences (see the *Low-Voltage Operation* section).

Output Voltage Accuracy (GND, CC)

Output voltage error is guaranteed to be within ±1% over all conditions of line, load, and temperature. The DC load regulation is typically better than 0.1% due to the integrator amplifier. Transient response is optimized by providing a feedback signal that has a direct path from the output to the main summing PWM comparator. The integrated feedback signal is also summed into the PWM comparator, with the gain weighted so that the integrated signal has only enough gain to correct the DC inaccuracies. The integrator's response time is determined by the time constant set by the capacitor placed on the CC pin. The time constant should not be so fast that the integrator responds to the normal V_{OUT} ripple or too slow to negate the integrator's effect. A 470pF to 1500pF CC capacitor is sufficient for 200kHz to 300kHz frequencies.

Figure 5 shows the output voltage response to a 0A to 3A load transient with and without the integrator. With the integrator, the output voltage returns to within 0.1% of its no-load value with only a small AC excursion. Without the integrator, the typical load-transient response with the AC and DC output voltage changes. Asymmetrical clamping at the integrator output prevents worsening of load transients during pulse-skipping mode.

Internal Digital Soft-Start Circuit

Soft-start allows a gradual increase of the internal current-limit level at start-up to reduce input surge currents. The SMPS contains an internal digital soft-start circuit controlled by a counter, a digital-to-analog converter (DAC), and a current-limit comparator. In shutdown or standby mode, the soft-start counter is reset to zero. When the SMPS is enabled, its counter starts counting oscillator pulses, and the DAC begins incrementing the comparison voltage applied to the current-limit comparator. The DAC output increases from 0mV to 100mV in five equal steps as the count increases to 512 clocks. As a result, the main output capacitor charges up relatively slowly. The exact time of the output rise depends on output capacitance and load current, but it is typically 1ms with a 300kHz oscillator.

Overload and Dropout Operation

Dropout (low input-output differential) operation is enhanced by stretching the clock pulse width to increase the maximum duty factor. The algorithm follows: If the output voltage (V_{OUT}) drops out of regulation without the current limit having been reached, the SMPS skips an off-time period (extending the on-time). At the end of the cycle, if the output is still out of regulation, the SMPS skips another off-time period. This action can continue until three off-time periods are skipped, effectively dividing the clock frequency by as much as four. This behavior also slightly improves load-transient response. Dividing the clock frequency by four raises the maximum duty factor to above 98%. The typical PWM minimum off-time is 300ns, regardless of the operating frequency.

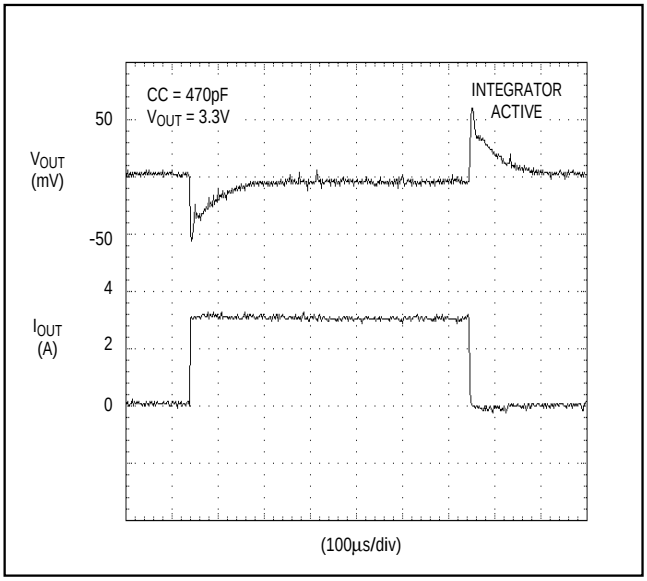


Figure 5a. Load-Transient Response with Integrator Active

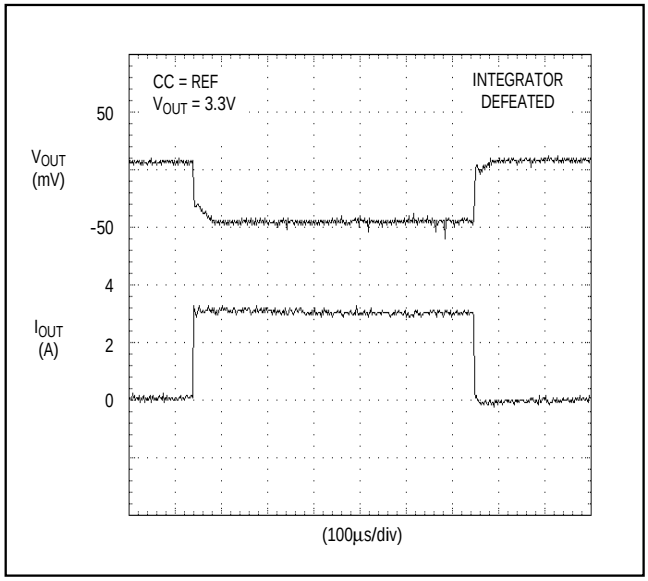


Figure 5b. Load-Transient Response with Integrator Defeated

Adjustable-Output Feedback (Dual-Mode FB)

A fixed, preset output voltage of 2.5V and 3.3V is selected when FB is connected to V_{CC} or ground. In this mode, internal resistors monitor the voltage on CSL. For voltages other than the fixed-output options, adjust the output voltage through a resistor divider connected to FB (Figure 2). Calculate the output voltage with the following formula:

$$V_{OUT} = V_{REF} (1 + R1 / R2)$$

where V_{REF} = 1.1V nominal. Recommended normal values for R2 range from 5kΩ to 100kΩ. To achieve a 1.1V nominal output, simply connect FB directly to CSL.

Remote output voltage sensing is not possible in fixed output mode due to the combined nature of the voltage-sense and current-sense inputs (CSL). It is, however, easy to do in adjustable mode by using the top of the external resistor divider as the remote sense point.

Low-Noise Operation (PWM Mode)

PWM mode ($\overline{SKIP}$ = high) minimizes RF and audio interference in noise-sensitive applications such as hi-fi multimedia-equipped systems, cellular phones, RF communicating computers, and electromagnetic pen-entry systems. See the summary of operating modes in Table 5. $\overline{SKIP}$ can be driven from an external logic signal.

PWM mode forces a constant switching frequency, reducing interference due to switching noise by concentrating the emissions at a known frequency outside the system audio or IF bands. Choose an oscillator frequency for which switching frequency harmonics do not overlap a sensitive frequency band. If necessary, synchronize the oscillator to a tight-tolerance external clock generator. To extend the output voltage-regulation range, constant operating frequency is not maintained under overload or dropout conditions (see the *Overload and Dropout Operation* section).

PWM mode ($\overline{SKIP}$ = high) forces two changes on the PWM controller. First, it disables the minimum-current comparator, ensuring fixed-frequency operation. Second, it changes the detection threshold for reverse-current limit from 0mV to -100mV, allowing the inductor current to reverse at light loads. This results in fixed-frequency operation and continuous inductor-current flow. PWM mode eliminates discontinuous-mode inductor ringing and improves cross-regulation of transformer-coupled, multiple-output supplies.

In most applications, tie $\overline{SKIP}$ to GND to minimize quiescent supply current. VL supply current with $\overline{SKIP}$ high is typically 20mA, depending on external MOSFET gate capacitance and switching losses.

Low-Voltage, Precision Step-Down Controller for Portable CPU Power

Design Procedure

The five predesigned standard application circuits (Figure 1 and Table 1) contain ready-to-use solutions for common application needs. Use the following design procedure to optimize these basic schematics for different voltage or current requirements. But before beginning a design, firmly establish the following:

- Maximum input (battery) voltage, $V_{IN(MAX)}$. This value should include the worst-case conditions, such as no-load operation when a battery charger or AC adapter is connected but no battery is installed. $V_{IN(MAX)}$ must not exceed 30V.
- Minimum input (battery) voltage, $V_{IN(MIN)}$. This should be taken at full load under the lowest battery conditions. If $V_{IN(MIN)}$ is less than 4.5V, use an external circuit to externally hold VL above the VL undervoltage lockout threshold. If the minimum input-output difference is less than 1.5V, the filter capacitance required to maintain good AC load regulation increases (see *Low-Voltage Operation* section).

Inductor Value

The exact inductor value is not critical and can be freely adjusted to make trade-offs between size, cost, and efficiency. Lower inductor values minimize size and cost but reduce efficiency due to higher peak-current levels. The smallest inductor is achieved by lowering the inductance until the circuit operates at the border between continuous and discontinuous mode. Further reducing the inductor value below this crossover point results in discontinuous-conduction operation even at full load. This helps lower output filter capacitance requirements, but efficiency suffers due to high I^2R losses. On the other hand, higher inductor values mean greater efficiency, but resistive losses due to extra wire turns eventually exceed the benefit gained from lower peak-current levels. Also, high inductor values can affect load-transient response (see the V_{SAG} equation in the *Low-Voltage Operation* section). The equations in this section are for continuous-conduction operation.

Three key inductor parameters must be specified: inductance value (L), peak current (I_{PEAK}), and DC resistance (R_{DC}). The following equation includes a constant, LIR, which is the ratio of inductor peak-to-peak AC current to DC load current. A higher LIR value allows smaller inductance but results in higher losses and higher ripple. A good compromise between size and losses is a 30% ripple-current to load-current ratio (LIR = 0.3), which corresponds to a peak inductor current 1.15 times higher than the DC load current.

$$L = V_{OUT}(V_{IN(MAX)} - V_{OUT}) / (V_{IN(MIN)} \times f \times I_{OUT} \times LIR)$$

where f = switching frequency, normally 200kHz or 300kHz, and I_{OUT} = maximum DC load current. The peak current can be calculated by:

$$I_{PEAK} = I_{LOAD} + [V_{OUT}(V_{IN(MAX)} - V_{OUT}) / (2 \times f \times L \times V_{IN(MAX)})]$$

The inductor's DC resistance should be low enough that $R_{DC} \times I_{PEAK} < 100mV$, as it is a key parameter for efficiency performance. If a standard, off-the-shelf inductor is not available, choose a core with an LI^2 rating greater than $L \times I_{PEAK}^2$ and wind it with the largest diameter wire that fits the winding area. For 300kHz applications, ferrite-core material is strongly preferred; for 200kHz applications, Kool-Mu® (aluminum alloy) or even powdered iron is acceptable. If light-load efficiency is unimportant (in desktop PC applications, for example), then low-permeability iron-powder cores may be acceptable, even at 300kHz. For high-current applications, shielded-core geometries, such as toroidal or pot core, help keep noise, EMI, and switching-waveform jitter low.

Current-Sense Resistor Value

The current-sense resistor value is calculated according to the worst-case, low-current-limit threshold voltage (from the *Electrical Characteristics* table) and the peak inductor current:

$$R_{SENSE} = 80mV / I_{PEAK}$$

Use I_{PEAK} from the second equation in the *Inductor Value* section. Use the calculated value of R_{SENSE} to size the MOSFET switches and specify inductor saturation-current ratings according to the worst-case high-current-limit threshold voltage:

$$I_{PEAK} = 120mV / R_{SENSE}$$

Low-inductance resistors, such as surface-mount metal film, are recommended.

Input Capacitor Value

Connect low-ESR bulk capacitors directly to the drain on the high-side MOSFET. The bulk input filter capacitor is usually selected according to input ripple current requirements and voltage rating, rather than capacitor value. Electrolytic capacitors with low enough equivalent series resistance (ESR) to meet the ripple-current requirement invariably have sufficient capacitance values. Aluminum electrolytic capacitors, such as Sanyo OS-CON or Nichicon PL, are superior to tantalum types, which risk power-up surge-current failure, especially when connecting to robust AC adapters or low-impedance batteries. RMS input ripple current (I_{RMS}) is

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determined by the input voltage and load current, with the worst case occurring at V_{IN} = 2 x V_{OUT}:

$$I_{RMS} = I_{LOAD} \times \sqrt{V_{OUT}(V_{IN} - V_{OUT})} / V_{IN}$$

Therefore, when V_{IN} is 2 x V_{OUT}:

$$I_{RMS} = I_{LOAD} / 2$$

Output Filter Capacitor Value

The output filter capacitor values are generally determined by the ESR and voltage-rating requirements rather than actual capacitance requirements for loop stability. In other words, the low-ESR electrolytic capacitor that meets the ESR requirement usually has more output capacitance than is required for AC stability. Use only specialized low-ESR capacitors intended for switching-regulator applications, such as AVX TPS, Sprague 595D, Sanyo OS-CON, or Nichicon PL series. To ensure stability, the capacitor must meet both minimum capacitance and maximum ESR values as given in the following equations:

$$C_{OUT} > V_{REF}(1 + V_{OUT} / V_{IN(MIN)}) / V_{OUT} \times R_{SENSE} \times f$$

$$R_{ESR} < R_{SENSE} \times V_{OUT} / V_{REF}$$

where R_{ESR} can be multiplied by 1.5, as discussed below.

These equations are worst case, with 45 degrees of phase margin to ensure jitter-free, fixed-frequency operation, and provide a nicely damped output response for zero to full-load step changes. Some cost-conscious designers may wish to bend these rules with less-expensive capacitors, particularly if the load lacks large step changes. This practice is tolerable if some bench testing over temperature is done to verify acceptable noise and transient response.

No well-defined boundary exists between stable and unstable operation. As phase margin is reduced, the first symptom is timing jitter, which shows up as blurred edges in the switching waveforms where the scope does not quite sync up. Technically speaking, this jitter (usually harmless) is unstable operation, since the duty factor varies slightly. As capacitors with higher ESRs are used, the jitter becomes more pronounced, and the load-transient output voltage waveform starts looking ragged at the edges. Eventually, the load-transient waveform has enough ringing on it that the peak noise levels exceed the allowable output voltage tolerance. Note that even with zero phase margin and gross instability, the output voltage noise never gets much worse than I_{PEAK} x R_{ESR} (under constant loads).

Designers of RF communicators or other noise-sensitive analog equipment should be conservative and stay within the guidelines. Designers of notebook computers and similar commercial-temperature-range digital systems can multiply the R_{ESR} value by a factor of 1.5 without hurting stability or transient response.

The output voltage ripple, which is usually dominated by the filter capacitor's ESR, can be approximated as I_{RIPPLE} x R_{ESR}. There is also a capacitive term, so the full equation for ripple in continuous-conduction mode is $V_{NOISE(p-p)} = I_{RIPPLE} \times [R_{ESR} + 1 / (2 \times p \times f \times C_{OUT})]$. In Idle Mode, the inductor current becomes discontinuous, with high peaks and widely spaced pulses, so the noise can actually be higher at light load (compared to full load). In Idle Mode, calculate the output ripple as follows:

$$V_{NOISE(p-p)} = \frac{0.02 \times R_{ESR}}{R_{SENSE}} + \frac{0.0003 \times L \times \left[1/V_{OUT} + 1/(V_{IN} - V_{OUT})\right]}{(R_{SENSE})^2 \times C_F}$$

Selecting Other Components

MOSFET Switches

The high-current N-channel MOSFETs must be logic-level types with guaranteed on-resistance specifications at VGS = 4.5V. Lower gate-threshold specifications are better (i.e., 2V max rather than 3V max). Drain-source breakdown voltage ratings must at least equal the maximum input voltage, preferably with a 20% derating factor. The best MOSFETs have the lowest on-resistance per nanocoulomb of gate charge. Multiplying $R_{DS(ON)}$ by Q_g provides a good figure of merit for comparing various MOSFETs. Newer MOSFET process technologies with dense cell structures generally perform best. The internal gate drivers tolerate >100nC total gate charge, but 70nC is a more practical upper limit to maintain best switching times.

In high-current applications, MOSFET package power dissipation often becomes a dominant design factor. I^2R power losses are the greatest heat contributor for both high-side and low-side MOSFETs. I^2R losses are distributed between Q1 and Q2 according to duty factor as shown in the equations below. Generally, switching losses affect only the upper MOSFET, since the Schottky rectifier usually clamps the switching node before the synchronous rectifier turns on. Gate-charge losses are dissipated by the driver and do not heat the MOSFET. Calculate the temperature rise according to package thermal-resistance specifications to ensure

that both MOSFETs are within their maximum junction temperature at high ambient temperature. The worst-case dissipation for the high-side MOSFET occurs at both extremes of input voltage, and the worst-case dissipation for the low-side MOSFET occurs at maximum input voltage.

$$Duty = (V_{OUT} + V_{Q2}) / (V_{IN} - V_{Q1})$$

$$PD\ (upper\ FET) = I_{LOAD}^2 \times R_{DS(ON)} \times Duty + V_{IN} \times I_{LOAD} \times f \times [(V_{IN} \times C_{RSS}) / I_{GATE} + 20ns]$$

$$PD\ (lower\ FET) = I_{LOAD}^2 \times R_{DS(ON)} \times (1 - Duty)$$

where on-state voltage drop $V_Q = I_{LOAD} \times R_{DS(ON)}$, C_{RSS} = MOSFET reverse transfer capacitance, I_{GATE} = DH driver peak output current capability (1A typ), and 20ns = DH driver inherent rise/fall time. The MAX1636's output undervoltage shutdown protects the synchronous rectifier under output short-circuit conditions. To reduce EMI, add a 0.1µF ceramic capacitor from the high-side switch drain to the low-side switch source.

Rectifier Clamp Diode

The rectifier is a clamp across the low-side MOSFET that catches the negative inductor swing during the 60ns dead time between turning one MOSFET off and each low-side MOSFET on. The latest generations of MOSFETs incorporate a high-speed silicon body diode, which serves as an adequate clamp diode if efficiency is not of primary importance. A Schottky diode can be placed in parallel with the body diode to reduce the forward voltage drop, typically improving efficiency 1% to 2%. Use a diode with a DC current rating equal to one-third of the load current; for example, use an MBR0530 (500mA-rated) type for loads up to 1.5A, a 1N5819 type for loads up to 3A, or a 1N5822 type for loads up to 10A. The rectifier's rated reverse-breakdown voltage must be at least equal to the maximum input voltage, preferably with a 20% derating factor.

Boost-Supply Diode

A signal diode such as a 1N4148 works well in most applications. If the input voltage can go below +6V, use a small (20mA) Schottky diode for slightly improved efficiency and dropout characteristics. Do not use large power diodes, such as 1N5817 or 1N4001, since high junction capacitance can pump up VL to excessive voltages.

Low-Voltage Operation

Low input voltages and low input-output differential voltages each require extra care in their design. Low absolute input voltages can cause the VL linear regulator to enter dropout and eventually shut itself off. Low V_{IN} - V_{OUT} differentials can cause the output voltage to sag when the load current changes abruptly. The sag's amplitude is a function of inductor value and maximum duty factor (D_{MAX}, an *Electrical Characteristics* parameter, 98% guaranteed over temperature at f = 200kHz) as follows:

$$V_{SAG} = \frac{(I_{STEP})^2 \times L}{2 \times C_F \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

Table 6 is a low-voltage troubleshooting guide. The cure for low-voltage sag is to increase the output capacitor's value. For example, at V_{IN} = +5.5V, V_{OUT} = 5V, L = 10µH, f = 200kHz, and I_{STEP} = 3A, a total capacitance of 660µF keeps the sag less than 200mV. Note that only the capacitance requirement increases; the ESR requirements do not change. Therefore, the added capacitance can be supplied by a low-cost bulk capacitor in parallel with the normal low-ESR capacitor.

Applications Information

Heavy-Load Efficiency Considerations

The major efficiency-loss mechanisms under loads are as follows, in the usual order of importance:

- $P(I^2R) = I^2R$ losses
- P(tran) = transition losses
- P(gate) = gate-charge losses
- P(diode) = diode-conduction losses
- P(cap) = capacitor ESR losses
- P(IC) = losses due to the IC's operating supply current

Inductor core losses are fairly low at heavy loads because the inductor's AC current component is small. Therefore, they are not accounted for in this analysis. Ferrite cores are preferred, especially at 300kHz, but powdered cores, such as Kool-Mu, can also work well.

$$Efficiency = P_{OUT} / P_{IN} \times 100\%$$

$$= P_{OUT} / (P_{OUT} + P_{TOTAL}) \times 100\%$$

$$P_{TOTAL} = P(I^2R) + P(tran) + P(gate) + P(diode) + P(cap) + P(IC)$$

$$P = (I^2R) = (I_{LOAD})^2 \times (R_{DC} + R_{DS(ON)} + R_{SENSE})$$

Table 6. Low-Voltage Troubleshooting Chart

SYMPTOM	CONDITION	ROOT CAUSE	SOLUTION
Sag or droop in V_{OUT} under step-load change	Low V_{IN}-V_{OUT} differential, <1.5V	Limited inductor-current slew rate per cycle.	Increase bulk output capacitance per formula (see *Low-Voltage Operation* section). Reduce inductor value.
Dropout voltage is too high (V_{OUT} follows V_{IN} as V_{IN} decreases)	Low V_{IN}-V_{OUT} differential, <1V	Maximum duty-cycle limits exceeded.	Reduce operation to 200kHz. Reduce MOSFET on-resistance and coil DCR.
Unstable—jitters between different duty factors and frequencies	Low V_{IN}-V_{OUT} differential, <0.5V	Normal function of internal low-dropout circuitry.	Increase the minimum input voltage or ignore.
Poor efficiency	Low input voltage, <5V	VL linear regulator is going into dropout and isn't providing good gate-drive levels.	Use a small 20mA Schottky diode for boost diode. Supply VL from an external source.
Won't start under load or quits before battery is completely dead	Low input voltage, <4.5V	VL output is so low that it hits the VL UVLO threshold.	Supply VL from an external source other than V_{IN}, such as the system +5V supply.

where R_{DC} is the DC resistance of the coil, $R_{DS(ON)}$ is the MOSFET on-resistance, and R_{SENSE} is the current-sense resistor value. The $R_{DS(ON)}$ term assumes identical MOSFETs for the high-side and low-side switches because they time-share the inductor current. If the MOSFETs are not identical, their losses can be estimated by averaging the losses according to duty factor.

$$PD(tran) = \text{transition loss} = V_{IN} \times I_{LOAD} \times f \times 3/2 \times [(V_{IN} C_{RSS} / I_{GATE}) + 20ns]$$

where C_{RSS} is the reverse transfer capacitance of the high-side MOSFET (a data-sheet parameter), I_{GATE} is the DH gate-driver peak output current (1.5A typ), and 20ns is the rise/fall time of the DH driver (20ns typ).

$$P(gate) = Q_g \times f \times VL$$

where VL is the internal logic-supply voltage (+5V), and Q_g is the sum of the gate-charge values for low-side and high-side switches. For matched MOSFETs, Q_g is twice the data-sheet value of an individual MOSFET. If V_{OUT} is set to less than 4.5V, replace VL in this equation with V_{BATT}. In this case, efficiency can be improved by connecting VL to an efficient 5V source, such as the system +5V supply.

$$P(diode) = \text{diode conduction losses} = I_{LOAD} \times V_{FWD} \times t_D \times f$$

where t_D is the diode-conduction time (120ns typ), and V_{FWD} is the forward voltage of the diode. This power is dissipated in the MOSFET body diode if no external Schottky diode is used.

$$P(cap) = \text{input capacitor ESR loss} = I_{RMS}^2 \times R_{ESR}$$

where I_{RMS} is the input ripple current as calculated in the *Input Capacitor Value* section.

Light-Load Efficiency Considerations

Under light loads, the PWM operates in discontinuous mode, where the inductor current discharges to zero at some point during the switching cycle. This makes the inductor current's AC component high compared to the load current, which increases core losses and I^2R losses in the output filter capacitors. For best light-load efficiency, use MOSFETs with moderate gate-charge levels and use ferrite, MPP, or other low-loss core material. Avoid powdered-iron cores; even Kool-Mu (aluminum alloy) is not as good as ferrite.

PC Board Layout Considerations

Good PC board layout is required in order to achieve specified noise, efficiency, and stable performance. The PC board layout artist must be given explicit instructions, preferably a pencil sketch showing the placement of power-switching components and high-current routing. See the PC board layout in the MAX1636 evaluation kit manual for examples. A ground plane is essential for optimum performance. In most applications, the circuit will be located on a multi-layer board, and full use of the four or more copper layers is recommended. Use the top layer for high-current

Low-Voltage, Precision Step-Down Controller for Portable CPU Power

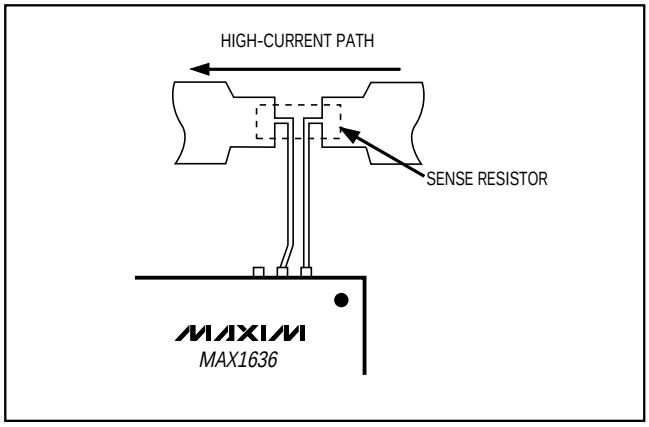


Figure 6. Kelvin Connections for the Current-Sense Resistors

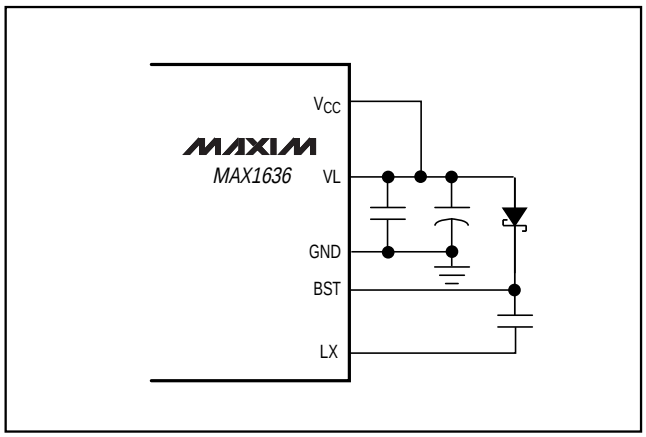


Figure 7. Capacitor Placement

connections, the bottom layer for quiet connections (REF, CC, GND), and the inner layers for an uninterrupted ground plane. Use the following step-by-step guide:

1) Place the high-power components (C1, C2, Q1, Q2, D1, L1, and R1) first, with their grounds adjacent.
   - *Minimize current-sense resistor trace lengths* and ensure accurate current sensing with Kelvin connections (Figure 6).
   - *Minimize ground trace lengths* in the high-current paths.
   - *Minimize other trace lengths* in the high-current paths.
     - — Use >5mm-wide traces.
     - — CIN to high-side MOSFET drain: 10mm max length
     - — Rectifier diode cathode to low side
     - — MOSFET: 5mm max length
     - — LX node (MOSFETs, rectifier cathode, inductor): 15mm max length

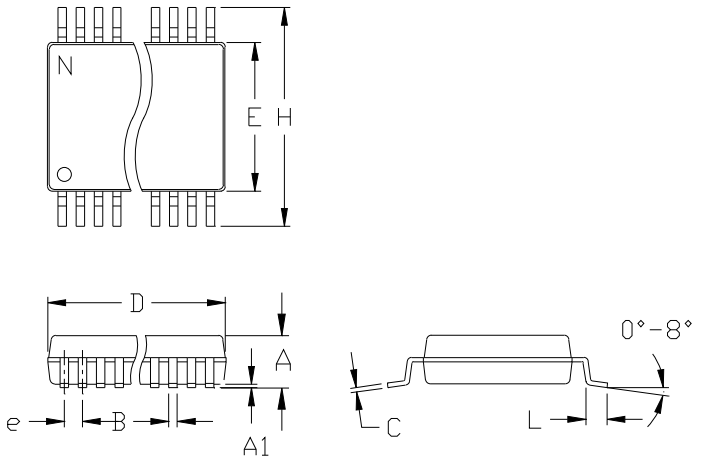
Ideally, surface-mount power components are butted up to one another with their ground terminals almost touching. These high-current grounds are then connected to each other with a wide, filled zone of top-layer copper so they do not go through vias. The resulting top-layer subground plane is connected to the normal inner-layer ground plane at the output ground terminals, which ensures that the IC's analog ground is sensing at the supply's output terminals without interference from IR drops and ground noise. Other high-current paths should also be minimized, but focusing primarily on short ground and current-sense connections eliminates about 90% of all PC board layout problems (see the PC board layouts in the MAX1636 evaluation kit manual for examples).

2) Place the IC and signal components. Keep the main switching nodes (LX nodes) away from sensitive analog components (current-sense traces and REF capacitor). Place the IC and analog components on the opposite side of the board from the power-switching node. **Important**: The IC must be no further than 10mm from the current-sense resistors. Keep the gate-drive traces (DH, DL, and BST) shorter than 20mm and route them away from CSH, CSL, and REF. Place ceramic bypass capacitors close to the IC. The bulk capacitors can be placed further away. If using VL to power V_{CC}, minimize noise by placing a 0.1µF capacitor close to the V_{CC} pin and placing the 4.7µF capacitor further away, but closer than the boost diode (Figure 7).
3) Use a single-point star ground where the input ground trace, power ground (subground plane), and normal ground plane meet at the supply's output ground terminal. Connect both IC ground pins and all IC bypass capacitors to the normal ground plane.

Chip Information

TRANSISTOR COUNT: 3472

SSOP.EPS



ADDED TO SSOP.DWG FILE*

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.005	0.009	0.13	0.22
e	0.0256		0.65	
E	0.205	0.212	5.20	5.38
H	0.301	0.311	7.65	7.90
L	0.022	0.037	0.55	0.95

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.278	0.289	7.07	7.33	20
D	0.317	0.328	8.07	8.33	24
D	0.397	0.407	10.07	10.33	28

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION

TITLE: PACKAGE FAMILY OUTLINE: SSOP .200" x .65mm | 1/1 | 21-0039 A DOCUMENT CONTROL NUMBER REV