Features

- **Programmable Driver Current Regulation**
- **Antenna Driver Stage for 1 A Peak Current**
- **LF Baudrates between 1 kbaud to 8 kbaud**
- **Integrated Oscillator for Ceramic Resonators**
- **Two Inputs for Push-button Switches**
- **Bi-directional Single-wire Interface**
- **Diagnosis Function and Overtemperature Protection**
- **Quick Start Control (QSC) for Fast Oscillation Build-up and Decay Timing**
- **Operation Temperature -40°C to +85°C**
- **Carrier Frequency Range from 100 kHz to 150 kHz**
- **Amplitude Shift Keying (ASK) Modulation**
- **Phase Shift Keying (PSK) Modulation**
- **Power Supply Range 7 V to 16 V Direct Battery Input (6 V and 28 V with Limited Function Range)**
- **EMI and ESD According to Automotive Requirements**
- **Highly Integrated — Less External Components Required**

Applications

- **Car Access**

Benefits

- **Dedicated for Decentralized Systems**
- **Constant Magnetic Field Strength**

Electrostatic sensitive device.
Observe precautions for handling.

Description

The circuit is an integrated BCDMOS antenna driver IC dedicated as a transmitter for Passive Entry/Go (PEG) car applications and for other handsfree access control applications.

It includes the full functionality to generate a magnetic LF field in conjunction with an antenna coil to transmit data to a receiver in a key fob, card or transponder. The transmission can be controlled via an one wire I/O interface (DIO) by an external control unit.

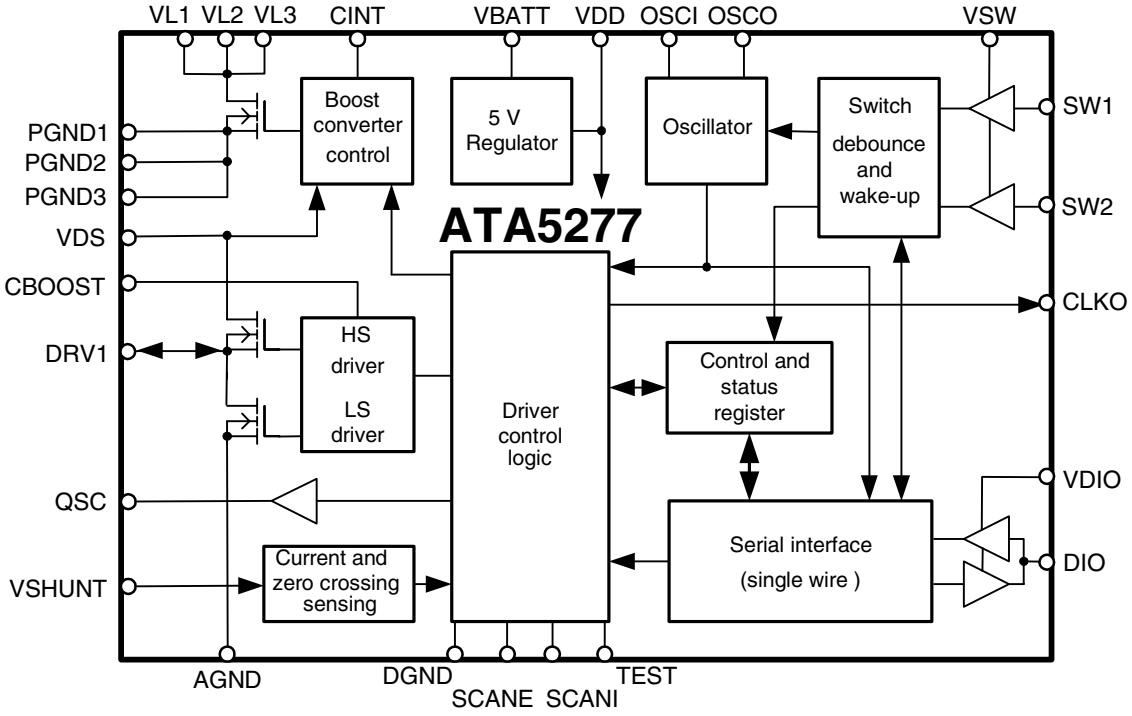
Stand-alone Antenna Driver

ATA5277

Preliminary

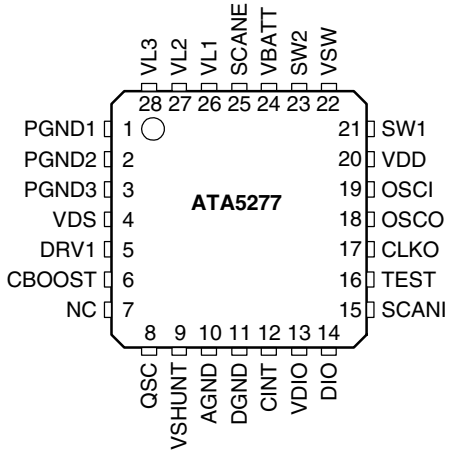
Rev. 4669B–RKE–10/03

Figure 1. Block Diagram



Pin Configuration

Figure 2. Pinning QFN 28



Pin Description

Pin	Symbol	Function
1	PGND1	Power supply ground
2	PGND2	Power supply ground
3	PGND3	Power supply ground
4	VDS	Driver voltage supply input
5	DRV1	Antenna driver stage output
6	CBOOST	External bootstrap capacitor connection
7	NC	Not connected
8	QSC	QSC transistor driver stage output
9	VSHUNT	Antenna current sensing
10	AGND	Analog ground (sensoric and antenna driver)
11	DGND	Digital ground (logic)
12	CINT	External integrator capacitor connection
13	VDIO	DIO line interface supply voltage
14	DIO	One-wire serial interface line
15	SCANI	For test purposes only
16	TEST	For test purposes only
17	CLKO	Clock output
18	OSCO	Oscillator output (for resonator/crystal connection)
19	OSCI	Oscillator input (for external source or resonator/crystal)
20	VDD	5 V supply output (for filter capacitor only)
21	SW1	Door switch input 1
22	VSW	Door switch interface supply voltage
23	SW2	Door switch input 2
24	VBATT	Battery supply voltage 7 V to 16 V (28 V jump start)
25	SCANE	For test purposes only
26	VL1	Coil input of the switch mode power supply
27	VL2	Coil input of the switch mode power supply
28	VL3	Coil input of the switch mode power supply

Functional Description

General Description

The IC contains a half-bridge coil driver stage with a special driver voltage regulator and control logic with diagnosis circuitry. Further it contains a one-wire bi-directional microcontroller interface for the carrier modulation and the mode selection. An integrated oscillator for ceramic resonators generates the clock signal for the control logic. Additionally, the IC contains two connectors for switches to wake-up the IC.

The IC generates an electromagnetic LF field in combination with an LC antenna circuitry. The carrier frequency for the antenna is generated by the oscillator and prescaler logic.

The LF field can be modulated to transmit data to a suitable receiver. There are two modulation modes available, Amplitude Shift Keying (ASK) and 180° Phase Shift Keying (PSK). A microcontroller or another control unit must be used to control the transmitter via the bi-directional single-wire interface.

A boost converter power supply is used to supply the driver half-bridge and the antenna with a high voltage and a regulated current even if the battery voltage is low. The antenna current is programmable in 16 steps to support a transmission with various field strengths.

The driver circuitry is Short Circuit (SC) protected and the driver logic contains diagnosis functions for short circuit and open wire detection at the antenna outputs.

Operation Modes

Three different operation modes are defined:

- Standby
- Command mode
- Modulation mode

After power-on reset, the ATA5277 is in standby mode. To achieve minimum power consumption, only the internal 5-V supply, the DIO-line interface and the door switch inputs are active. The IC can be activated either by the external control unit via the serial interface or by one of the switch inputs. A low signal at the DIO-line or at the switch inputs (SW1, SW2) powers up the IC. If this is done at a switch input, a low signal is generated on the DIO-line which can be used as a wake-up signal for the connected microcontroller.

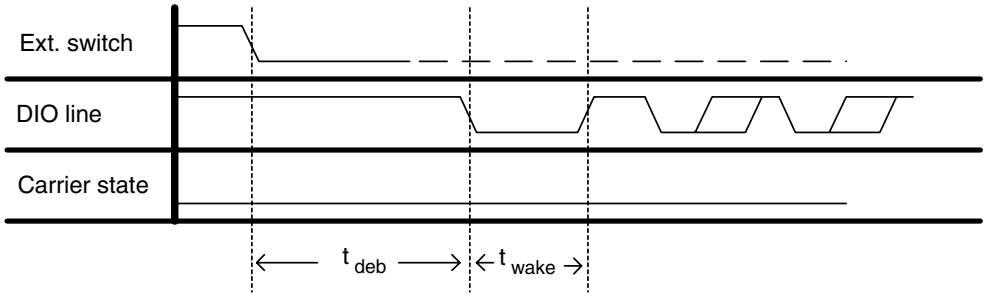
In command mode, the IC can be configured and diagnostics can be run. This mode is always activated after wake-up from standby mode and after leaving modulation mode. The communication is based on a one-wire serial interface (DIO-line) with the connected microcontroller being the master and ATA5277 being the slave. In this mode, the antenna driver stage is disabled, except if the automatic field generation after wake-up is selected.

In modulation mode, the antenna driver stage is activated (if enabled) and the data applied to the DIO-line modulates the LF field (in ASK or PSK). This mode is activated after the command mode and remains active as long as data is applied to the DIO-line (i.e., until a timeout has occured). After that, the IC falls back to command mode.

Standby and Wake-up

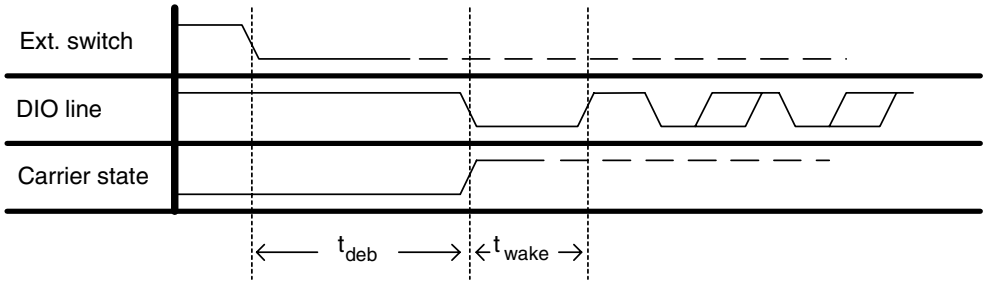
There are two different wake-up modes. In the default mode the antenna driver stage remains off after wake-up. The second mode can be programmed by a control command. Here, also the driver output stage is enabled. The IC generates the carrier signal for the antenna immediately.

Figure 3. Wake-up by External Switch



In Figure 3, the IC is woken up by an external switch (pulled to ground). After a debouncing time t_{deb}, the IC leaves sleep mode and sends a wake-up impulse to a connected microcontroller via the DIO line. Note that this impulse is already the start bit of the first command. After that, the ATA5277 waits for a control or status command from the microcontroller. The carrier remains off as the configuration bit M_Wake (see control command 2) is '0'.

Figure 4. Wake-up by External Switch, Automatic Field Generation



The wake-up event as shown in Figure 4 is the same as in Figure 3, except for the configuration bit M_Wake which is '1'. The driver stage will start operation after the wake-up command has been confirmed. This behaviour can be used to build up an LF field independently of the connected microcontroller.

Figure 5. Wake-up by Connected Microcontroller, Automatic Field Generation

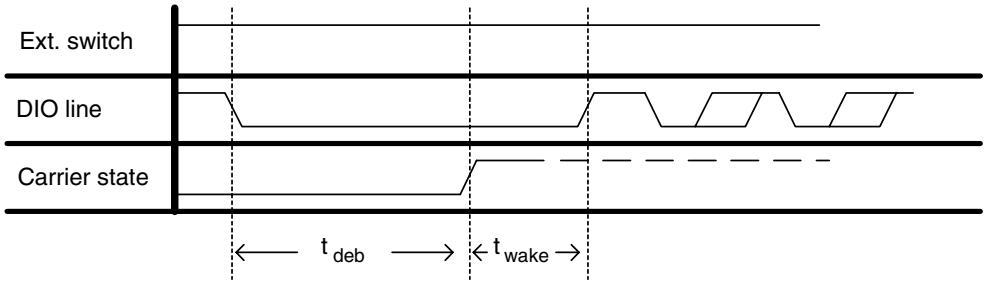


Figure 5 shows a wake-up event triggered by the connected microcontroller, which now pulls the DIO line to ground. To prevent the ATA5277 from waking up due to noise on the DIO line, there is also a debouncing time before it will start operation. In this example, M_Wake is again '1', so the driver stage starts operation after the wake-up event has been confirmed.

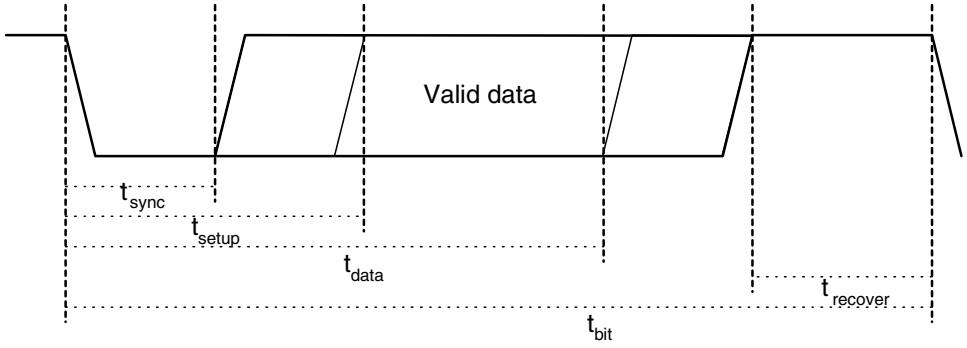
There are two ways to enter standby mode. One is to keep the DIO-line at a high level for more than 32 ms while the IC is in command mode. A low signal at the DIO line keeps the IC active and resets the standby timer. As the clock output CLKO remains active, this configuration can be used to supply a clock signal to a connected microcontroller.

The second way to shut down the ATA5277 is to set the STBY bit to control command 0. Note that the IC will switch off operation immediately after receiving the last data bit (bit 3) of the control command. The rest of the telegram (i.e., acknowledge and stop bit) is then omitted.

Command Mode Protocol

As described above, the communication between a controlling unit and the ATA5277 is done via a one-wire serial interface. Figure 6 shows the structure of one communication bit.

Figure 6. Structure of One Communication Bit



All bits start with a falling edge. This pull-down has to be done by the microcontroller and maintained for at least $t_{sync,minimum}$. After that, the setup for the data bit itself has to be performed. If the ATA5277 is the receiver, the microcontroller has to change the state of the DIO-line according to the bit it wants to transmit. The maximum time for this setup is $t_{setup,maximum}$. This state should then be applied for a time of at least $t_{data,minimum}$. Independent of the former state of the DIO-line, it has to return to '1' and keep this state for a minimum time of $t_{recover,minimum}$. If the ATA5277 is the transmitter of the data, the IC will apply the bit to the DIO-line after $t_{sync,minimum}$ (i.e., activate the internal pull-down when a '0' needs to be transmitted). This signal on the DIO-line is then valid for $t_{data,maximum}$.

Generally, the following conditions have to be met in all cases:

- $t_{sync,minimum} \leq t_{sync} < t_{setup,maximum}$
- $t_{setup} \leq t_{setup,maximum}$
- $t_{data} \leq t_{data,maximum}$
- $t_{recover} \geq t_{recover,minimum}$
- $t_{bit} \geq t_{bit,minimum}$

The timing values can be found in the electrical characteristics section for the DIO interface.

A command consists of a start bit followed by four command bits and four control or status bits respectively. It ends with an acknowledge bit and, if no further commands are to be transmitted, a stop bit.

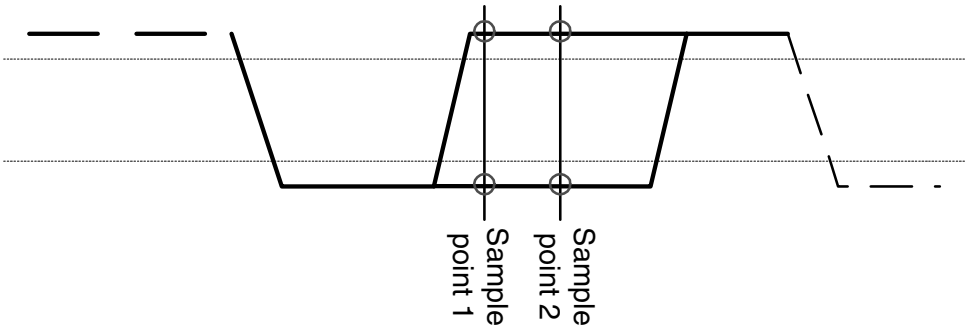
Any command is preceded by a start bit. Note again that, if the ATA5277 is woken up by one of the external switches, the wake-up signal from the ATA5277 (slave) to the microcontroller (master) on the DIO-line is already the start bit of the first command.

It is followed by the command bits CMD0...CMD3. Bits CMD0 to CMD2 are used to select one of the eight registers of control and status bits. These registers have a depth of four bits and are used to configure the ATA5277 and to check its status. The CMD3 bit is used to select the operation mode of the ATA5277 after the current command has been processed (i.e., switch to modulation mode or stay in command mode).

The next four bits of the protocol (Bit0 to Bit3) are the data bits. Depending on the selected register, these bits are to be transmitted by the microcontroller (for control commands) or by ATA5277 (for status commands). Note that even if data is transmitted by ATA5277, the initial falling edge for any bit has to be transmitted by the microcontroller, as it is the master of the transmission.

Furthermore, the IC has a built-in bit error check for input bits. If no errors are detected during a command transfer, the IC acknowledges the command with N_ACKN = 0. If a bit error is detected, the transfer is not acknowledged (N_ACKN =1), the received data is dismissed and the command has to be sent again immediately.

Figure 7. Data Consistency Check



As can be seen in Figure 7, the state of the DIO line is sampled twice during the data-valid time. During this time, the state must not change, both samples must result in the same value. If they differ, the N_ACKN bit is set to '1' and thus a fault is reported at the end of the sequence. The bit is reset after each control/status command (i.e., after it is transmitted to the microcontroller).

If the controller receives a ’1’ acknowledge bit, it has to repeat the command immediately (i.e., without transmitting the stop bit), starting again with the start bit.

The stop bit is used to end the command mode. After receiving the stop bit, the IC switches to modulation mode. Note that this bit is omitted if the CMD3 bit has been sent as a '1' (i.e., another command is to be transmitted).

Figure 8. Control/Status Command Structure

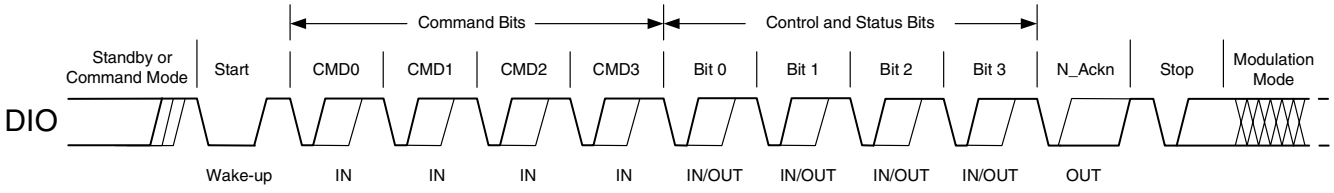


Figure 8 shows a typical sequence for data communication with the ATA5277. Any status/command sequence is started with a start bit. The shown sequence requires the CMD3 bit to be '0', as the protocol ends with the stop bit and after that, modulation mode is activated. If another command should be transmitted, the CMD3 bit of the preceding command must be '1' and the new command, which starts again with a start bit, is applied right after the acknowledge bit of the preceding command.

Usually, the driver output stage is disabled during command mode. But as described above, by setting the M_Wake bit to '1', the driver stage will be enabled together with the command mode after wake-up. Note that this is only happening after a wake-up from standby mode. The driver stage will be disabled when switching back from modulation mode to command mode, even with the M_Wake bit set to '1'.

If the DIO-line is kept in a passive state (i.e., '1') for more than 32 ms, the IC will fall into sleep mode.

Command Tables

The following tables contain the description of the eight ATA5277 commands.

Table 1. Control Command 0

Bit	Name/Value	Type	Function 1	Function 2
CMD0	0	Cmd bit	Command selection	–
CMD1	0	Cmd bit	Command selection	–
CMD2	0	Cmd bit	Command selection	–
CMD3	X	Cmd bit	'0' Return to modulation mode	'1' Keep command mode
Bit0	C_ON	Ctrl bit	'0' Carrier/driver off(1)	'1' Carrier/driver on
Bit1	STBY	Ctrl bit	'0' No effect(1)	'1' Invokes standby mode
Bit2	NASK_PSK	Ctrl bit	'0' ASK modulation mode(1)	'1' PSK modulation mode
Bit3	TMOD_SEL	Ctrl bit	'0' Modulation timeout 2 ms(1)	'1' Modulation timeout 500 µs

Note: 1. Default values after power-on reset

Table 2. Control Command 1

Bit	Name/Value	Type	Function 1	Function 2
CMD0	1	Cmd bit	Command selection	–
CMD1	0	Cmd bit	Command selection	–
CMD2	0	Cmd bit	Command selection	–
CMD3	X	Cmd bit	'0' Return to modulation mode	'1' Keep command mode
Bit0	I_coil0	Ctrl bit	Bit0 of the current control stage(1)	–
Bit1	I_coil1	Ctrl bit	Bit1 of the current control stage(1)	–
Bit2	I_coil2	Ctrl bit	Bit2 of the current control stage(1)	–
Bit3	I_coil3	Ctrl bit	Bit3 of the current control stage(1)	–

Note: 1. See coil current adjustment, default all bits '1'

Table 3. Control Command 2

Bit	Name/Value	Type	Function 1	Function 2
CMD0	0	Cmd bit	Command selection	–
CMD1	1	Cmd bit	Command selection	–
CMD2	0	Cmd bit	Command selection	–
CMD3	X	Cmd bit	'0' Return to modulation mode	'1' Keep command mode
Bit0	PS_CLK	Ctrl bit	'0' Disable prescaler for CLKO-pin	'1' Enable prescaler (/2) for CLKO-pin(1)
Bit1	M_Wake	Ctrl bit	'0' Carrier off after wake-up(1)	'1' Carrier on after wake-up
Bit2	DIS_SW1	Ctrl bit	'0' SW1 input pull-up on(1)	'1' SW1 input pull-up off
Bit3	DIS_sw2	Ctrl bit	'0' SW2 input pull-up on(1)	'1' SW2 input pull-up off

Note: 1. Default values after power on reset

Table 4. Status Command 3

Bit	Name/Value	Type	Function 1	Function 2
CMD0	1	Cmd bit	Command selection	–
CMD1	1	Cmd bit	Command selection	–
CMD2	0	Cmd bit	Command selection	–
CMD3	X	Cmd bit	'0' Return to modulation mode	'1' Keep command mode
Bit0	SW1	Status bit	Logical level at SW1 input (low: 0; high: 1)	–
Bit1	SW2	Status bit	Logical level at SW2 input (low: 0; high: 1)	–
Bit2	–	–	Not used	–
Bit3	–	–	Not used	–

Table 5. Status Command 4

Bit	Name/Value	Type	Function 1	Function 2
CMD0	0	Cmd bit	Command selection	–
CMD1	0	Cmd bit	Command selection	–
CMD2	1	Cmd bit	Command selection	–
CMD3	X	Cmd bit	'0' Return to modulation mode	'1' Keep command mode
Bit0	DIAG0	Status bit	Diagnosis bit0	–
Bit1	DIAG1	Status bit	Diagnosis bit0	–
Bit2	DIAG2	Status bit	Diagnosis bit0	–
Bit3	–	–	Not used	–

Table 6. Status Command 5

Bit	Name/Value	Type	Function 1	Function 2
CMD0	1	Cmd bit	Command selection	–
CMD1	0	Cmd bit	Command selection	–
CMD2	1	Cmd bit	Command selection	–
CMD3	X	Cmd bit	'0' return to modulation mode	'1' Keep command mode
Bit0	C_ON	Status bit	'0' carrier/driver off	'1' Carrier/driver on
Bit1	STBY	Status bit	'0'	–
Bit2	NASK_PSK	Status bit	'0' ASK modulation selected	'1' PSK modulation selected
Bit3	TMOD_SEL	Status bit	'0' modulation timeout is 2 ms	'1' Modulation timeout is 500 µs

Table 7. Status Command 6

Bit	Name/Value	Type	Function 1	Function 2
CMD0	0	Cmd bit	Command selection	–
CMD1	1	Cmd bit	Command selection	–
CMD2	1	Cmd bit	Command selection	–
CMD3	X	Cmd bit	'0' Return to modulation mode	'1' Keep command mode
Bit0	I_coil0	Status bit	Bit0 of the current control stage	–
Bit1	I_coil1	Status bit	Bit1 of the current control stage	–
Bit2	I_coil2	Status bit	Bit2 of the current control stage	–
Bit3	I_coil3	Status bit	Bit3 of the current control stage	–

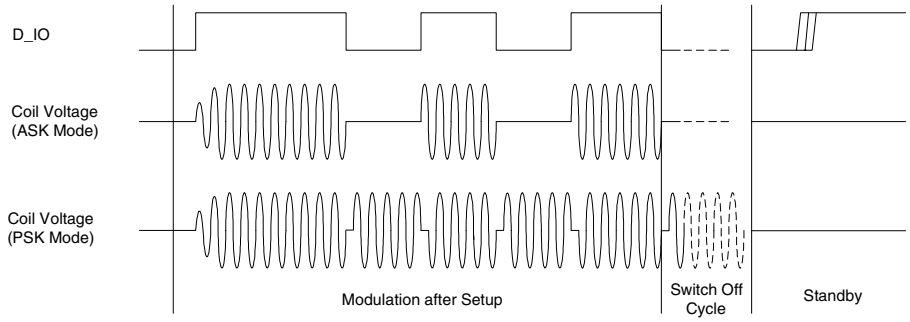
Table 8. Status Command 7

Bit	Name/Value	Type	Function 1	Function 2
CMD0	1	Cmd bit	Command selection	–
CMD1	1	Cmd bit	Command selection	–
CMD2	1	Cmd bit	Command selection	–
CMD3	X	Cmd bit	'0' return to modulation mode	'1' keep command mode
Bit0	PS_CLK	Status bit	'0' prescaler for CLKO-pin disabled	'1' prescaler (/2) for CLKO pin enabled
Bit1	M_Wake	Status bit	'0' carrier off after wake-up	'1' carrier onafter wake-up
Bit2	DIS_SW1	Status bit	'0' SW1 input pull-up on	'1' SW1 input pull-up off
Bit3	DIS_SW2	Status bit	'0' SW2 input pull-up on	'1' SW2 input pull-up off

Modulation

After the IC has woken up and a command has been received, the DIO line is used for LF modulation. The IC has two modulation modes, ASK and PSK. The mode can be selected with the control command '0', bit 2. If ASK modulation mode is selected (NASK_PSK = 0), the IC switches the carrier on and off, depending on the state of the DIO line ('1' is on, '0' is off). Note that, depending on the quality of the connected LF antenna and on the desired LF data rate, the usage of the QSC transistor T1 (see typical applications section) is neccessary. If PSK mode is selected (NASK_PSK = 1), the phase of the carrier is shifted by 180° on any change of the DIO line. Here, the QSC transistor must be used.

Figure 9. Modulation Modes

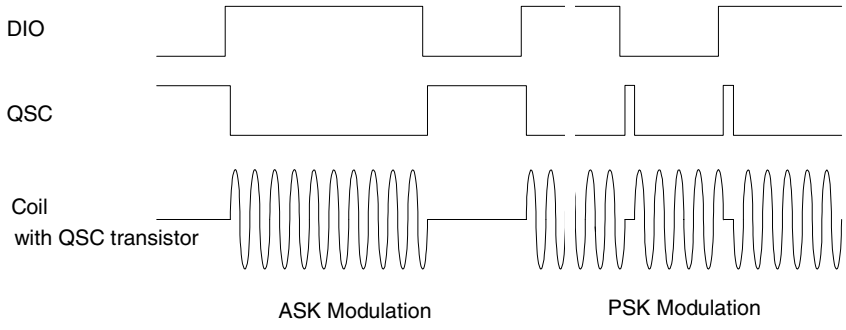


The IC switches from modulation mode to command mode if the DIO-line has not been changed for a time peraiod longer than t_{modsel}.

QSC Feature

The Quick Start Control (QSC) feature supports a short oscillation build up and decay timing during LF data modulation. An external high-voltage MOS transistor is used as a switch to close and open the current loop of the antenna. By synchronizing this switch to the zero-crossing events of the antenna current, very short build-up and decay times for the LF-field and hence high data baud rates can be achieved.

Figure 10. QSC Operation



The external transistor (T1 in the typical applications section) is driven by the QSC pin. It provides a fast and synchronized gate-driver signal.

Coil Driver

The coil driver is composed of a power MOS stage in half-bridge configuration, which is supplied by a current regulated boost converter. The driver generates a square-wave output signal to supply the antenna circuit with the carrier frequency. The antenna coil current is regulated by the voltage of the switch mode power supply. The current is therefore sensed by a shunt resistor connected between the VSHUNT and the GND pins of the IC.

To avoid damages in case of short circuits and high currents, the driver is switched off by the integrated fault detection unit.

Current Adjustment

To provide an adjustable coil current, the IC is equipped with a voltage regulator composed of a Switch Mode Power Supply (SMPS), which is used if the supply voltage is too low to reach the desired antenna coil current. In this case, the driver stage voltage is brought up to the required level (maximum 40 V). The IC contains the control logic and the switching transistor for the boost converter. All other components like the choke coil and the capacitor have to be applied externally.

The antenna coil current can be adjusted in 16 steps by modifying the I_Coil0 to I_Coil3 bits in the control register. According to the selected current, the pulse width of the antenna coil driver signal is adjusted in order to enlarge the control range for the voltage regulator. The 16 steps are scaled logarithmically and have the follwing current ratings:

Table 9. Current Settings

Step	Current [mA]	I_Coil0	I_Coil1	I_Coil2	I_Coil3	P/P Ratio
1	$I_{maximum}/3.158$	0	0	0	0	1/7
2	$I_{maximum}/2.927$	1	0	0	0	1/7
3	$I_{maximum}/2.727$	0	1	0	0	1/7
4	$I_{maximum}/2.5$	1	1	0	0	1/7
5	$I_{maximum}/2.353$	0	0	1	0	2/6
6	$I_{maximum}/2.143$	1	0	1	0	2/6
7	$I_{maximum}/2$	0	1	1	0	2/6
8	$I_{maximum}/1.846$	1	1	1	0	2/6
9	$I_{maximum}/1.714$	0	0	0	1	3/5
10	$I_{maximum}/1.579$	1	0	0	1	3/5
11	$I_{maximum}/1.463$	0	1	0	1	3/5
12	$I_{maximum}/1.367$	1	1	0	1	3/5
13	$I_{maximum}/1.263$	0	0	1	1	4/4
14	$I_{maximum}/1.165$	1	0	1	1	4/4
15	$I_{maximum}/1.081$	0	1	1	1	4/4
16[1]	$I_{maximum}$	1	1	1	1	4/4

Note: 1. Default

The maximum output current can be selected with the external shunt resistor. Its resistance can be calculated with the formula:

$$R_{shunt} = \frac{1}{I_{max,peak}}\Omega$$

where the minimum and maximum ratings for $I_{maximum,peak}$ quoted in the DC characteristics have to be considered. See Figure 11 to determine the antenna´s parameters.

The maximum reachable output current can be calculated as follows:

$$I_{ant,peak} = \frac{V_{DRV} \times 2}{\pi \times |\underline{Z}|}A$$

Here, V_{DRV} is the maximum reachable driver voltage (40 V) and Z the antenna´s impedance (inculding the R_{DSon} of the QSC MOSFET, the shunt resistor and the driver output resistance).

Fault Diagnotics

The IC contains several fault diagnotic stages to protect itself from destruction and to provide diagnostic information. Once there is a fault detected, both the switch mode power supply and the antenna driver stage are switched off and the corresponding fault information is written into the status register. Note that besides shutting down the driver stages, the ATA5277 will not change its behaviour (i.e., it will remain in modulation mode until the DIO line timeout has occured). The fault information can be read out from status command 4, which will also reset the status register.

Following protection and diagnostic mechanisms are defined:

- General
  - The IC is equipped with temperature measurement obilities in order to detect a critical junction temperature
- DRV output
  - Short-circuit protection of the driver stage output is realized by means of voltage monitoring. Thus, the output voltage is compared to a corresponding threshold (depeding on the active transistor in the power MOS half-bridge). If this threshold is surpassed for several oscillations, a Short Circuit (SC) fault is detected;
  - Open load or QSC transistor SC to GND is detected with the external current sensing resistor R_{Shunt}. If there is no signal at this point even if the output is active, there is at least one of those two faults present. There is no possibility to determine the exact fault source.

The diagnostic bits contain the information as given in Table 10 on page 14.

Table 10. Diagnostic Bits

DIAG0	DIAG1	DIAG2	Fault Type
0	0	0	No fault detected
1	0	0	Open load or QSC transistor SC to GND
0	1	0	Overtemperature
1	1	0	Antenna driver SC to GND
0	0	1	Antenna driver SC to V_{BATT}
1	0	1	QSC transistor SC to V_{BATT}
0	1	1	Not defined
1	1	1	Not defined

Switch Inputs

The switch inputs SW1 and SW2 can be used to connect switches, e.g., the door handle contactors. These inputs are equipped with pull-ups, capable of driving currents up to 20 mA per pin. The pull-up voltage can be selected with the VSW input pin, which has to be connected either to V_{DD} (5 V) for 5 V operation or to V_{BATT} for 12 V operation.

The state of the switches is determined by the voltage level at the corresponding pin. This information can be read out via the DIO-line during the status command 3. If the IC is in the standby mode, it wakes up if an input is pulled to ground. After a debounce time the IC generates a low signal at the DIO-line (wake-up). This signal can be used to wake up and request a microcontroller to read the switches with a setup cycle. Once the IC has woken up or during normal operation mode, a low state at a switch input (i.e., the switch is triggered) is stored until the status command 3 has been read out or ALYA enters standby mode. This enables the microcontroller to determine which of the two switch inputs was triggered, independant of the time it needs for processing status command 3.

To prevent high standby currents caused by a hanging door switch or a short-circuited line, the pull-ups can be disabled individually by setting the DIS_SW1 and the DIS_SW2 bits in the command register 2.

CLKO Output Pin

The clock output pin CLKO on the ATA5277 can be used to supply an onboard microcontroller with a clock signal (either 8 or 4 MHz). Due to this frequency and the 5-V output stage, this signal is not suited to supply any device beyond the PCB boundaries.

This clock signal is directly derived from the clock source connected to the OSCI/OSCO pins of the ATA5277 and is available as long as ATA5277 is not in standby mode. The frequency can be selected with the PS_CLK bit of control command 2, which is '0' for full clock rate (typical 8 MHz) or '1' for the half clock rate (4 MHz).

Application Hints

Figure 11. Antenna Coil Inductance versus Quality

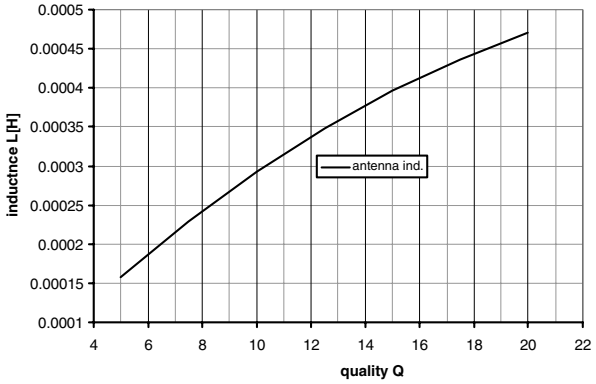


Figure 11 shows the maximum usable antenna coil inductance in order to meet the requirements (maximum output voltage of 40 V square wave, output peak current of 1 A, maximum frequency deviation of antenna is ±2.5%).

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Supply voltage	V_{BATT}	-0.3 to +44	V
Input voltage	V_{IN}	V_{SS}-0.3 ≤ V_{IN} ≤ 44	V
Power dissipation (IC, QFN)	P_{tot}	2	W
Emission	EMI	250	V/M
Minimum ESD protection (100 pF through 1.5 k)	ESD	2 (onboard pins) 4 (offboard pins)	kV
Junction temperature	T_J	150	°C
Storage temperature range	T_{stg}	-55 to +150	°C

Note: 1. Voltages are given relative to V_{SS}.

Thermal Resistance

Parameters	Symbol	Value	Unit
Thermal resistance junction-case	R_{thJC}	5	K/W
Thermal resistance junction-ambient (QFN28)	R_{thJA}	32	K/W

Operating Range

Parameters	Symbol	Value	Unit
Power supply range	V_{BATT}	7 to 16.5	V
Operating temperature range	T_{amb}	-40 to +85	°C

Electrical Characteristics (1)

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Power Supply**								
1.1	Operating voltage		24	V_{BATT}	7 (2)		16.5 (2)	V	D
1.2	SMPS voltage range		4	V_{VDS}	16.5		40	V	D
1.3	Switching frequency		26, 27, 28	f_{SMPS}		$2 \times f_{CF}$		kHz	C
1.4	Current regulation set up time			t_{reg}		1	1,5	ms	D
1.5	Supply current	V_S = 7 V		I_{SUP}			3.5	A_{eff}	D
1.6	Standby current	IC in standby, V_{BATT} = 12 V	24	I_{STB}			TBD	µA	A
1.7	Power on reset V_{BATT}		24	V_{POR}	4.2		4.7	V	A
1.8	OV discharger	IC in standby, V_{BATT} > 23 V	24	I_{DIS}			9.5	mA	A
1.9	Internal 5 V supply		20	V_{VDD}	4.7		5.3	V	A
1.10	Integrator current	After fusing = $2 \times I_{REF}$	12	I_{CINT}	18		22	µA	A
1.11	dV_{CP} for high side	Clamping V_{BOOST}	6	dV_{CP}	7.7		8.9	V	A
1.12	Thermal shutdown temperature	Temperature reference = V_{SCANI}	15	T_{jsd}		155		°C	B
2	**Serial Interface**								
2.1	Data output current		14	I_{DIO}		10	20	mA	A
2.2	Output low level	I_{DIO} = 20 mA	14	V_{Lout}		1.2	1.5	V	A
2.3	Input impedance		14	R_{in}	0.6		3.5	MΩ	A
2.4	Input low level	$5 V \le V_{DIO} \le V_{BATT}$	14	V_{Lin}			$0.4 \times V_{DIO}$	V	A
2.5	Input high level	$5 V \le V_{DIO} \le V_{BATT}$	14	V_{Hin}	$0.7 \times V_{DIO}$			V	A
2.6	Serial Interface baud rate		14	Bd_{IF}			5	kbit/s	D
2.7	Signal rise-time (L to H)		14	t_{rise}	0		1	µs	A
2.8	Signal fall-time (H to L)		14	t_{fall}	0		1	µs	A
2.9	Wake-up debounce time		14	t_{deb}	550			µs	D
2.10	Wake-up impulse length		14	t_{wake}	20		50	µs	D
2.11	Minimum synchronize time		14	t_{sync}	20			µs	D
2.12	Maximum set-up time		14	t_{setup}			50	µs	D
2.13	Data valid time for input		14	$t_{data,in}$	140			µs	D
2.14	Data valid time for output		14	$t_{data,out}$	140		160	µs	D
2.15	Recovery time		14	$t_{recover}$	20			µs	D
2.16	Bit length		14	t_{bit}	200			µs	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. $7 V < V_{BATT} < 16.5 V$; T_{amb} = 25°C unless otherwise specified; all values refer to GND pins
2. 6 V possible with approximately 30% decrease of maximum output power; 28 V operation possible (jump start), but output current stability is not guranteed

Electrical Characteristics (1) (Continued)

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3	**Driver Stage**								
3.1	Coil driver output voltage	Square wave	4	V_{VDS}	V_{BATT}		40	V	A
3.2	Coil driver output current	Depends on antenna inductance	5	$I_{DRV,peak}$			1	A_{peak}	D
3.3	Coil driver resistance		5	R_{DRV}		0.4		Ω	A
3.4	QSC driver output voltage		8	V_{QSC}		10	20	V	A
3.5	QSC driver output current	Short-term loads	8	I_{QSC}			50	mA	A
3.6	QSC driver output highside-impedance		8	R_{QSCh}	3			Ω	A
3.7	QSC driver output lowside-impedance		8	R_{QSCl}		3		Ω	A
3.8	Carrier frequency range		5	f_{CF}	100		150	kHz	D
3.9	LF data baud rate	Bi-phase/ Manchester	5	Bd_{RF}	1		8	kbit/s	D
3.10	Output rise/fall time	Between 10% and 90% of driver supply	26, 27, 28	t_{rf}		TBD		s	A
3.11	Output duty cycle		5	D_{CF}	12.5		50	%	A
4	**Door Switch Inputs**								
4.1	Trigger voltage level	$5\ V \le V_{SW} \le V_{BATT}$	21, 23	V_{SWtrig}			$0.4 \times V_{SW}$	V	A
4.2	Output current (pull-up)		21, 23	I_{SW}	8	20	40	mA	A
4.3	Input debounce time		17	t_{deb}		2		ms	A
4.4	Oscillator set-up time	Dependent on ceramic resonator	17	t_{oscon}		500		µs	D
5	**Oscillator**								
5.1	Input frequency range	Ceramic resonator, crystal or external CLKO source	17	f_{OSC}	6.4		10	MHz	B
5.2	CLKO-output frequency	SCANI change	17	f_{OUT}	$f_{OSC}/2$	4	f_{OSC}	MHz	A
5.3	CLKO high level		17	V_{HCLKO}	4.4		7.1	V	A
5.4	CLKO low level		17	V_{LCLKO}			2.2	V	A

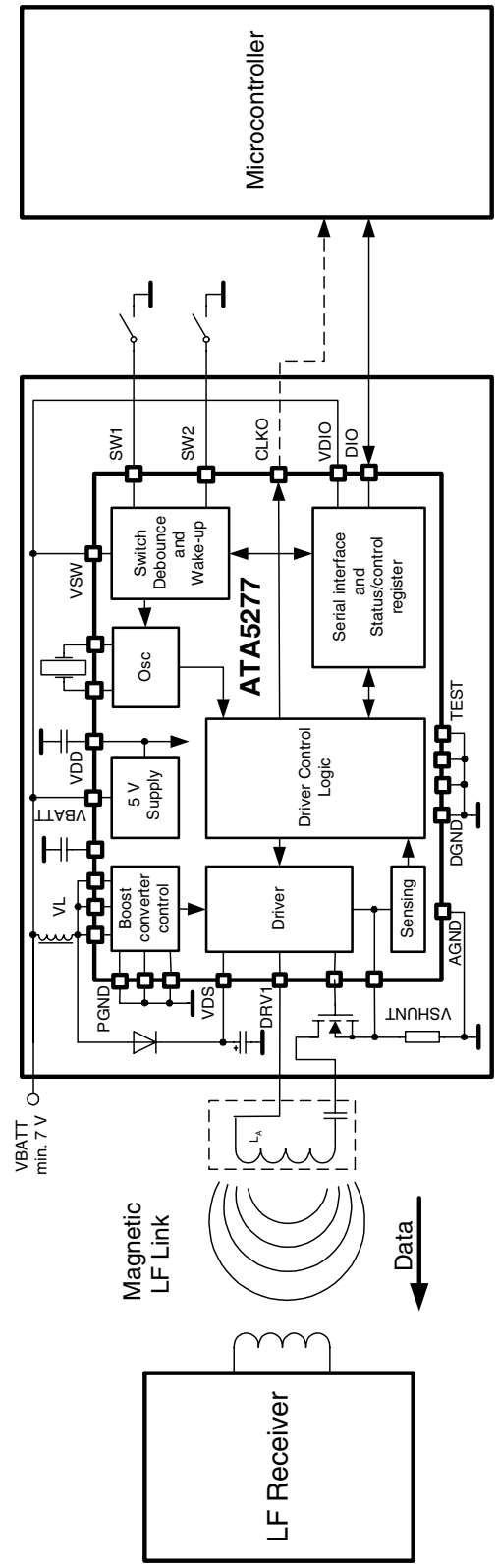
*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. $7\ V < V_{BATT} < 16.5\ V$; $T_{amb} = 25°C$ unless otherwise specified; all values refer to GND pins
2. 6 V possible with approximately 30% decrease of maximum output power; 28 V operation possible (jump start), but output current stability is not guranteed

Soldering Recommendations

Parameters	Symbol	Value	Unit
Maximum heating rate	T_D	1 to 3	°C/s
Peak temperature in preheat zone	Z_{PH}	100 to 140	°C
Duration of time above melting point of solder	t_{MP}	10 min/75 max	s
Peak reflow temperature	T_{Peak}	220 to 225	°C
Maximum cooling rate	T_{rPeak}	2 to 4	°C/s

Figure 12. Application Circuit



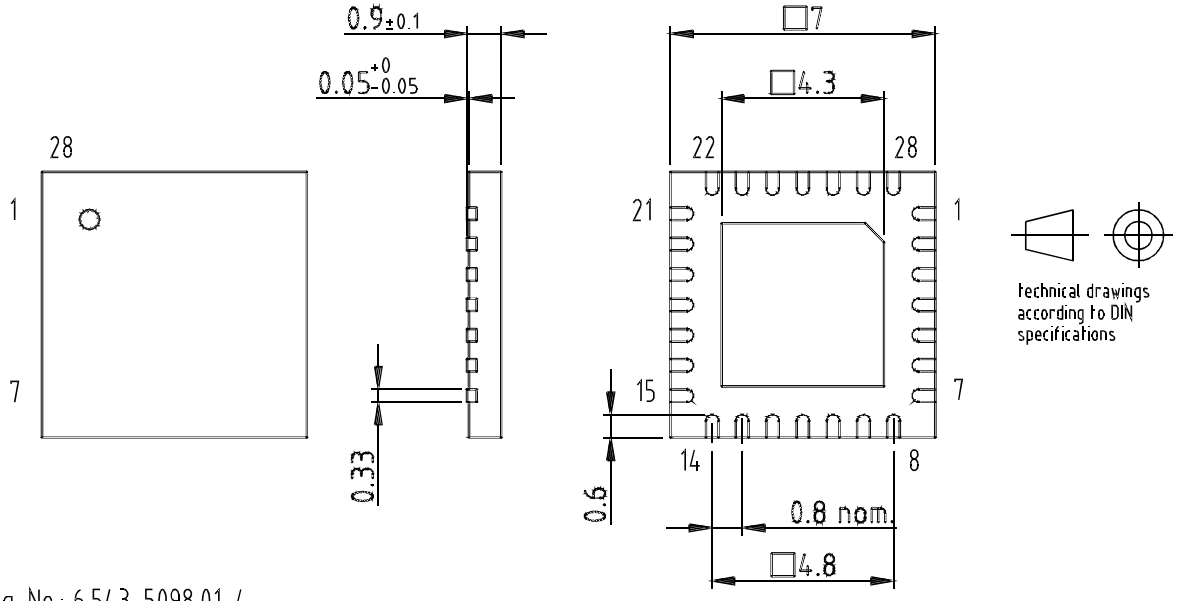
Ordering Information

Extended Type Number	Package	Remarks
ATA5277-PCQ	QFN28	7 mm × 7 mm

Package Information

Package: QFN 28 - 7x7
Exposed pad 4.3x4.3
(acc. JEDEC OUTLINE No. MO-220)
Dimensions in mm

Not indicated tolerances ±0.05



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