



## +3V, 8-Bit ADC with 1 $\mu$ A Power-Down

### ABSOLUTE MAXIMUM RATINGS

V <sub>DD</sub> to GND .....	-0.3V to +7V	Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
V <sub>SS</sub> to GND .....	+0.3V to -7V	Plastic DIP (derate 11.11mW/°C above +70°C) .....	889mW
Digital Input Voltage to GND .....	-0.3V, (V <sub>DD</sub> + 0.3V)	Wide SO (derate 10.00mW/°C above +70°C) .....	800mW
Digital Output Voltage to GND .....	-0.3V, (V <sub>DD</sub> + 0.3V)	SSOP (derate 8.00mW/°C above +70°C) .....	640mW
VREF+ to GND .....	(V <sub>SS</sub> - 0.3V) to (V <sub>DD</sub> + 0.3V)	CERDIP (derate 11.11mW/°C above +70°C) .....	889mW
VREF- to GND .....	(V <sub>SS</sub> - 0.3V) to (V <sub>DD</sub> + 0.3V)	Operating Temperature Ranges:	
V <sub>IN</sub> to GND .....	(V <sub>SS</sub> - 0.3V) to (V <sub>DD</sub> + 0.3V)	MAX152C__ .....	0°C to +70°C
		MAX152E__ .....	-40°C to +85°C
		MAX152MJP .....	-55°C to +125°C
		Storage Temperature Range .....	-65°C to +150°C
		Lead Temperature (soldering, 10sec) .....	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS

(Unipolar input range, V<sub>DD</sub> = 3.0V to 3.6V, GND = 0V, V<sub>SS</sub> = GND, VREF+ = 3.0V, VREF- = GND, specifications are given for RD mode (pin 7 = GND), T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>ACCURACY</b> (Note 1)						
Resolution	N		8			Bits
Total Unadjusted Error	TUE	Unipolar range			±1	LSB
Differential Nonlinearity	DNL	No-missing-codes guaranteed			±1	LSB
Zero-Code Error (Note 2)		Unipolar and bipolar modes			±1	LSB
Full-Scale Error (Note 2)		Unipolar and bipolar modes			±1	LSB
<b>DYNAMIC PERFORMANCE</b> (Note 3)						
Signal-to-Noise Plus Distortion Ratio	S/(N+D)	MAX152C/E, f <sub>SAMPLE</sub> = 400kHz, f <sub>IN</sub> = 30.273kHz	45			dB
		MAX152M, f <sub>SAMPLE</sub> = 340kHz, f <sub>IN</sub> = 30.725kHz	45			
Total Harmonic Distortion	THD	MAX152C/E, f <sub>SAMPLE</sub> = 400kHz, f <sub>IN</sub> = 30.273kHz			-50	dB
		MAX152M, f <sub>SAMPLE</sub> = 340kHz, f <sub>IN</sub> = 30.725kHz			-50	
Spurious-Free Dynamic Range		MAX152C/E, f <sub>SAMPLE</sub> = 400kHz, f <sub>IN</sub> = 30.273kHz	50			dB
		MAX152M, f <sub>SAMPLE</sub> = 340kHz, f <sub>IN</sub> = 30.725kHz	50			
Input Full-Power Bandwidth		V <sub>IN</sub> = 3.0V <sub>p-p</sub>		0.3		MHz
Maximum Input Slew Rate, Tracking			0.28	0.5		V/μs
<b>ANALOG INPUT</b>						
Input Voltage Range	V <sub>IN</sub>		VREF-		VREF+	V
Input Leakage Current	I <sub>IN</sub>	V <sub>SS</sub> < V <sub>IN</sub> < V <sub>DD</sub>			±3	μA
Input Capacitance	C <sub>IN</sub>			22		pF
<b>REFERENCE INPUT</b>						
Reference Resistance	RREF		1	2	4	kΩ
VREF+ Input Voltage Range			VREF-		V <sub>DD</sub>	V
VREF- Input Voltage Range			V <sub>SS</sub>		VREF+	V

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### ELECTRICAL CHARACTERISTICS (continued)

(Unipolar input range,  $V_{DD} = 3.0V$  to  $3.6V$ ,  $GND = 0V$ ,  $V_{SS} = GND$ ,  $V_{REF+} = 3.0V$ ,  $V_{REF-} = GND$ , specifications are given for RD mode (pin 7 = GND),  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>LOGIC INPUTS</b>						
Input High Voltage	$V_{INH}$	CS, WR, RD, PWRDN	2.0			V
		MODE	2.4			
Input Low Voltage	$V_{INL}$	CS, WR, RD, PWRDN			0.66	V
		MODE			0.8	
Input High Current	$I_{INH}$	CS, RD, PWRDN			$\pm 1$	$\mu A$
		WR			$\pm 3$	
		MODE		15	100	
Input Low Current	$I_{INL}$	CS, WR, RD, PWRDN, MODE			$\pm 1$	$\mu A$
Input Capacitance (Note 4)	$C_{IN}$	CS, WR, RD, PWRDN, MODE		5	8	pF
<b>LOGIC OUTPUTS</b>						
Output Low Voltage	$V_{OL}$	INT, D0-D7, $I_{SINK} = 20\mu A$			0.1	V
		INT, D0-D7, $I_{SINK} = 400\mu A$			0.4	
		RDY, $I_{SINK} = 1mA$			0.4	
Output High Voltage	$V_{OH}$	INT, D0-D7, $I_{SOURCE} = 20\mu A$	$V_{DD}-0.1$			V
		INT, D0-D7, $I_{SOURCE} = 400\mu A$	$V_{DD}-0.4$			
Floating-State Current	$I_{LKG}$	D0-D7, RDY			$\pm 3$	$\mu A$
Floating Capacitance (Note 4)	$C_{OUT}$	D0-D7, RDY		5	8	pF
<b>POWER REQUIREMENTS</b>						
Positive Supply Voltage	$V_{DD}$		3.0		3.6	V
Negative Supply Voltage	$V_{SS}$	Unipolar operation		GND		V
		Bipolar operation (Note 2)	-3.6		-3.0	
Positive Supply Current	$I_{DD}$	$V_{DD} = 3.6V$	MAX152C, CS = RD = 0, PWRDN = $V_{DD}$	2.5	5	mA
			MAX152E/M, CS = RD = 0, PWRDN = $V_{DD}$	2.5	6	
		$V_{DD} = 3.0V$	MAX152C, CS = RD = 0, PWRDN = $V_{DD}$	1.5	3	
			MAX152E/M, CS = RD = 0, PWRDN = $V_{DD}$	1.5	3.5	
Power-Down $V_{DD}$ Current (Note 5)		$\overline{CS} = \overline{RD} = V_{DD}$ , PWRDN = 0		1	50	$\mu A$
Negative Supply Current	$I_{SS}$	CS = RD = 0, PWRDN = $V_{DD}$		1	50	$\mu A$
Power-Down $V_{SS}$ Current		CS = RD = $V_{DD}$ , PWRDN = 0		1	25	$\mu A$
Power-Supply Rejection	PSR	$V_{DD} = 3.3V \pm 10\%$		$\pm 1/16$	$\pm 1/4$	LSB

**Note 1:** Accuracy measurements performed at  $V_{DD} = 3.0V$ , unipolar mode. Operation over supply range is guaranteed by power-supply rejection test.

**Note 2:** Bipolar tests are performed with  $V_{REF+} = +1.5V$ ,  $V_{REF-} = -1.5V$ ,  $V_{SS} = -3.0V$ .

**Note 3:** Unipolar input range,  $V_{IN} = 3.0V_{P-P}$ , WR-RD mode,  $V_{DD} = 3.0V$

**Note 4:** Guaranteed by design.

**Note 5:** Power-down current increases if control inputs are not driven to ground or  $V_{DD}$ .

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### TIMING CHARACTERISTICS

(Unipolar input range,  $V_{DD} = 3V$ ,  $V_{SS} = 0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	ALL GRADES $T_A = +25^\circ C$			MAX152C/E $T_A = T_{MIN}$ to $T_{MAX}$		MAX152M $T_A = T_{MIN}$ to $T_{MAX}$		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Conversion Time (WR-RD Mode)	$t_{CWR}$	$t_{RD} < t_{INTL}$ , $C_L = 100pF$		1.8		2.06		2.4	$\mu s$	
Conversion Time (RD Mode)	$t_{CRD}$			2.0		2.3		2.6	$\mu s$	
Power-Up Time	$t_{UP}$			0.9		1.2		1.4	$\mu s$	
CS to RD,WR Setup Time	$t_{CSS}$		0			0		0	ns	
CS to RD,WR Hold Time	$t_{CSH}$		0			0		0	ns	
CS to RDY Delay	$t_{RDY}$	$C_L = 50pF$ , $R_L = 5.1k\Omega$ to $V_{DD}$		100		120		140	ns	
Data Access Time (RD Mode) (Note 7)	$t_{ACC0}$	$C_L = 100pF$		$t_{CRD} + 100$		$t_{CRD} + 130$		$t_{CRD} + 150$	ns	
RD to INT Delay (RD Mode)	$t_{INTH}$	$C_L = 50pF$	100	160		170		180	ns	
Data Hold Time (Note 8)	$t_{DH}$			100		130		150	ns	
Delay Time Between Conversions	$t_p$		450			600		700	ns	
WR Pulse Width	$t_{WR}$		0.6	10		0.66	10	0.8	$\mu s$	
Delay Time Between WR and RD Pulses	$t_{RD}$		0.8			0.9		1.0	$\mu s$	
RD Pulse Width	$t_{READ1}$	WR-RD mode, determined by $t_{ACC1}$ (Figure 6)	400			500		600	ns	
Data Access Time (Note 7)	$t_{ACC1}$	WR-RD mode, $t_{RD} < t_{INTL}$ , $C_L = 100pF$ (Figure 6)		400		500		600	ns	
RD to INT Delay	$t_{RI}$			300		340		400	ns	
WR to INT Delay	$t_{INTL}$	$C_L = 50pF$		0.7	1.45		1.6	1.8	$\mu s$	
RD Pulse Width	$t_{READ2}$	WR-RD mode, $t_{RD} > t_{INTL}$ , determined by $t_{ACC2}$ (Figure 5)	180			220		250	ns	
Data Access Time (Note 7)	$t_{ACC2}$	WR-RD mode, $t_{RD} < t_{INTL}$ , $C_L = 100pF$ (Figure 5)		180		220		250	ns	
WR to INT Delay	$t_{IHWR}$	Stand-alone mode, $C_L = 50pF$		180		200		240	ns	
Data Access Time After INT (Note 7)	$t_{ID}$	Stand-alone mode, $C_L = 100pF$		100		130		150	ns	

**Note 6:** Input control signals are specified with  $t_r = t_f = 5ns$ , 10% to 90% of +3.0V, and timed from a voltage level of 1.3V. Timing delays get shorter at higher supply voltages. See the Conversion Time vs. Supply Voltage graph in the *Typical Operating Characteristics* to extrapolate timing delays at other power-supply voltages.

**Note 7:** See Figure 1 for load circuit. Parameter defined as the time required for the output to cross 0.66V or 2.0V.

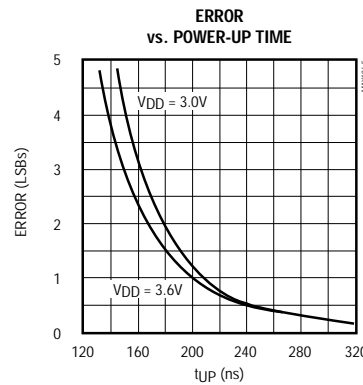
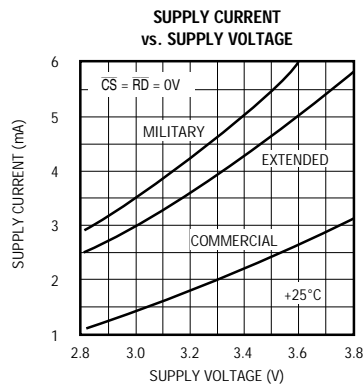
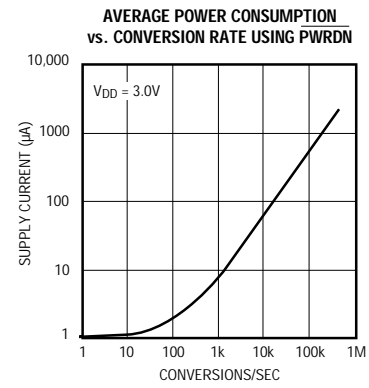
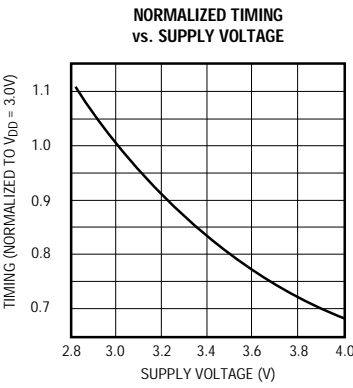
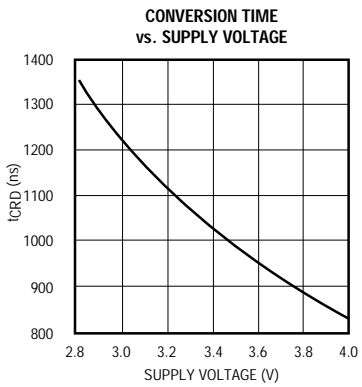
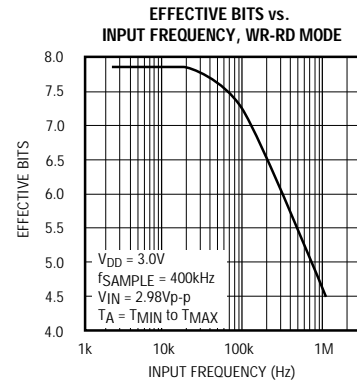
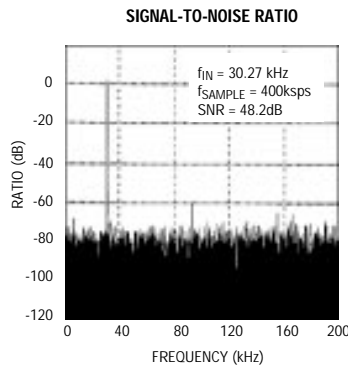
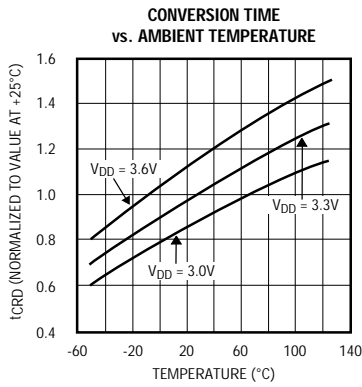
**Note 8:** See Figure 2 for load circuit. Parameter defined as the time required for the data lines to change 0.5V.

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## Typical Operating Characteristics

(T<sub>A</sub> = +25°C, unless otherwise noted).

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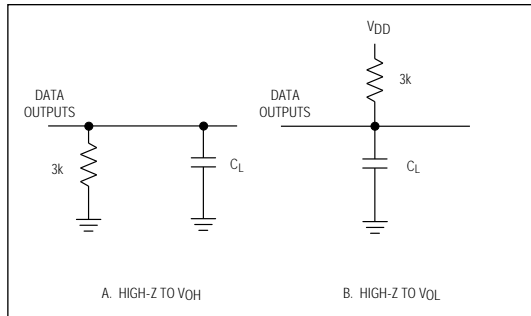


Figure 1. Load Circuits for Data-Access Time Test

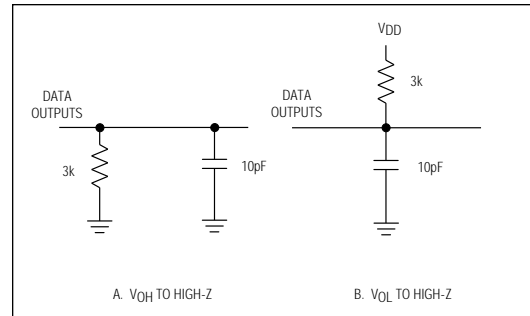


Figure 2. Load Circuits for Data-Hold Time Test

### Pin Description

PIN	NAME	FUNCTION
1	$V_{IN}$	Analog Input. Range is $V_{REF-} \leq V_{IN} \leq V_{REF+}$ .
2	D0	Three-State Data Output (LSB)
3-5	D1-D3	Three-State Data Outputs
6	WR/RDY	Write Control Input/Ready Status Output*
7	MODE	Mode Selection Input is internally pulled low with a 15 $\mu$ A current source. MODE = 0 activates read mode. MODE = 1 activates write-read mode*
8	RD	Read Input must be low to access data.*
9	INT	Interrupt Output goes low to indicate end of conversion.*
10	GND	Ground
11	VREF-	Lower limit of reference span. Sets the zero-code voltage. Range is $V_{SS} \leq V_{REF-} < V_{REF+}$ .
12	VREF+	Upper limit to reference span. Sets the full-scale input voltage. Range is $V_{REF-} < V_{REF+} \leq V_{DD}$ .
13	CS	Chip-Select Input must be low for the device recognize WR or RD inputs.
14-16	D4-D6	Three-State Data Outputs
17	D7	Three-State Data Output (MSB)
18	PWRDN	Powerdown Input reduces supply current when low.
19	$V_{SS}$	Negative Supply. Unipolar: $V_{SS} = 0V$ , Bipolar: $V_{SS} = -3V$ .
20	$V_{DD}$	Positive Supply, +3V.

\*See Digital Interface Section.

### Detailed Description

#### Converter Operation

The MAX152 uses a half-flash conversion technique (see *Functional Diagram*) in which two 4-bit flash ADC sections achieve an 8-bit result. Using 15 comparators, the flash ADC compares the unknown input voltage to the reference ladder and provides the upper 4 data bits.

An internal digital-to-analog converter (DAC) uses the 4 most significant bits (MSBs) to generate the analog result from the first flash conversion and a residue voltage that is the difference between the unknown input and the DAC voltage. The residue is then compared again with the flash comparators to obtain the lower 4 data bits (LSBs).

The MAX152 is characterized for operation between +3.0V and +3.6V. Conversion times decrease as the supply voltage increases. The supply current decreases rapidly with decreasing supply voltage. (See *Typical Operating Characteristics*.)

#### Power-Down Mode

In burst-mode or low sample-rate applications, the MAX152 can be shut down between conversions, reducing supply current to microamp levels (see *Typical Operating Characteristics*). A logic low on the PWRDN pin shuts the device down, reducing supply current to typically 1 $\mu$ A when powered from a single 3V supply. A logic high on PWRDN wakes up the MAX152. A new conversion can be started within 900ns of the PWRDN pin being driven high (this includes both the power-up delay and the track/hold acquisition time). If power-down mode is not required, connect PWRDN to  $V_{DD}$ .

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Once the MAX152 is in power-down mode, lowest supply current is drawn with MODE low (RD mode) due to an internal pull-down resistor at this pin. In addition, for minimum current consumption, other digital inputs should remain high in power-down. Refer to the *Reference* section for information on reducing reference current during power-down.

### Digital Interface

The MAX152 has two basic interface modes set by the status of the MODE input pin. When MODE is low, the converter is in the RD mode; when MODE is high, the converter is set up for the WR-RD mode.

#### Read Mode (MODE = 0)

In RD mode, conversion control and data access are controlled by the  $\overline{\text{RD}}$  input (Figure 3). The comparator inputs track the analog input voltage for the duration of  $t_p$ . A conversion is initiated by driving  $\overline{\text{RD}}$  low. With  $\mu$ Ps that can be forced into a wait state, hold  $\overline{\text{RD}}$  low until output data appears. The  $\mu$ P starts the conversion, waits, and then reads data with a single read instruction.

$\overline{\text{WR}}/\text{RDY}$  is configured as a status output (RDY) in RD mode, where it can drive the ready or wait input of a  $\mu$ P. RDY is an open-collector output (with no internal pull-up) that goes low after the falling edge of  $\overline{\text{CS}}$  and goes high at the end of the conversion. If not used, the  $\overline{\text{WR}}/\text{RDY}$  pin can be left unconnected. The  $\overline{\text{INT}}$  output goes low at the end of the conversion and returns high on the rising edge of  $\overline{\text{CS}}$  or  $\overline{\text{RD}}$ .

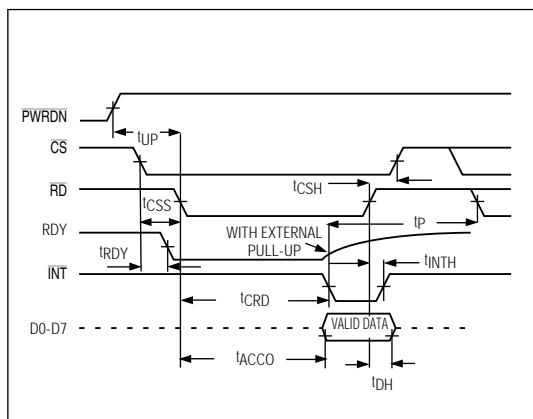


Figure 3. RD Mode Timing (MODE = 0)

#### Write-Read Mode (MODE = 1)

Figures 4 and 5 show the operating sequence for the write-read (WR-RD) mode. The comparator inputs track the analog input voltage for the duration of  $t_p$ . The conversion is initiated by a falling edge of  $\overline{\text{WR}}$ . When  $\overline{\text{WR}}$  returns high, the 4 MSBs' flash result is latched into the output buffers and the 4 LSBs' conversion begins.  $\overline{\text{INT}}$  goes low, indicating conversion end, and the lower 4 data bits are latched into the output buffers. The data is then accessible after  $\overline{\text{RD}}$  goes low (see *Timing Characteristics*).

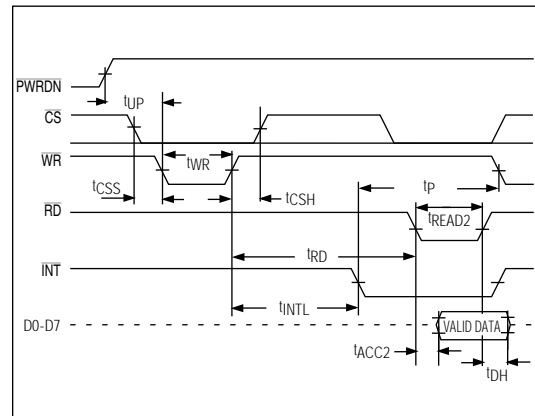


Figure 4. WR-RD Mode Timing ( $t_{RD} > t_{INTL}$ ) (MODE = 1)

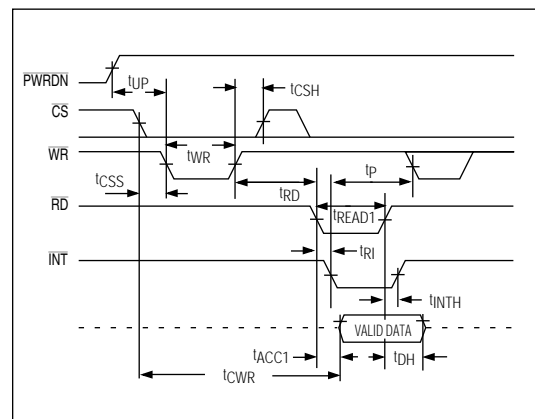


Figure 5. WR-RD Mode Timing ( $t_{RD} < t_{INTL}$ ), Fastest Operating Mode (MODE = 1)

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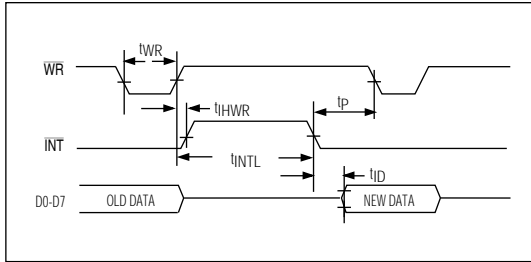


Figure 6. Stand-Alone Mode Timing ( $\overline{CS} = \overline{RD} = 0$ ) (MODE = 1)

A minimum acquisition time ( $t_p$ ) is required from  $\overline{INT}$  going low to the start of another conversion ( $\overline{WR}$  going low).

Options for reading data from the converter include the following:

### Using Internal Delay

The  $\mu P$  waits for the  $\overline{INT}$  output to go low before reading the data (Figure 4).  $\overline{INT}$  goes low after the rising edge of  $\overline{WR}$ , indicating that the conversion is complete and the result is available in the output latch. With  $\overline{CS}$  low, data outputs D0-D7 can be accessed by pulling  $\overline{RD}$  low.  $\overline{INT}$  is then reset by the rising edge of  $\overline{CS}$  or  $\overline{RD}$ .

### Fastest Conversion: Reading Before Delay

An external method of controlling the conversion time is shown in Figure 5. The internally generated delay  $t_{INTL}$  varies slightly with temperature and supply voltage, and can be overridden with  $\overline{RD}$  to achieve the fastest conversion time.  $\overline{RD}$  is brought low after the rising edge of  $\overline{WR}$ , but before  $\overline{INT}$  goes low. This completes the conversion and enables the output buffers (D0-D7) that contain the conversion result.  $\overline{INT}$  also goes low after the falling edge of  $\overline{RD}$  and is reset on the rising edge of  $\overline{RD}$  or  $\overline{CS}$ . The total conversion time is therefore:  $t_{CWR} = t_{WR} (600ns) + t_{RD} (800ns) + t_{ACC1} (400ns) = 1800ns$ .

### Stand-Alone Operation

Besides the two standard WR-RD mode options, stand-alone operation can be achieved by connecting  $\overline{CS}$  and  $\overline{RD}$  low (Figure 6). A conversion is initiated by pulling  $\overline{WR}$  low. Output data can be read by either edge of the next  $\overline{WR}$  pulse.

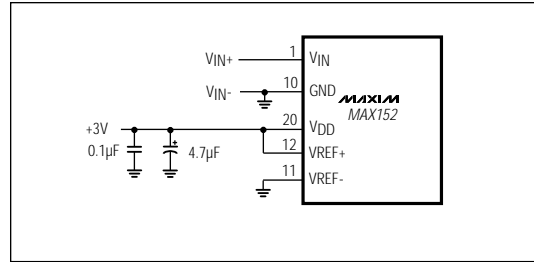


Figure 7a. Power Supply as Reference

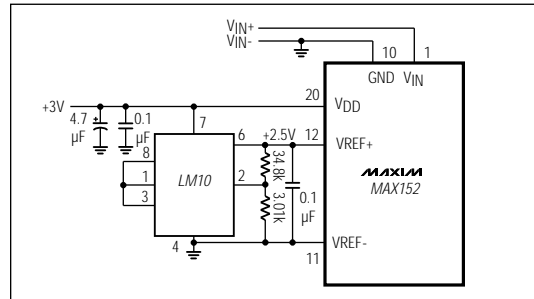


Figure 7b. External Reference, +2.5V Full Scale

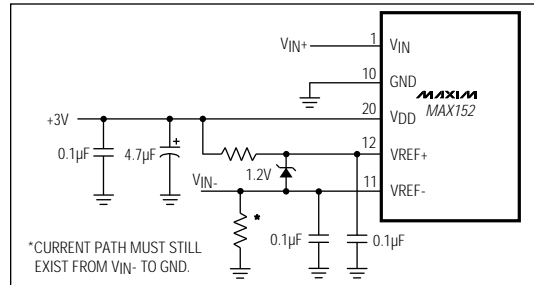


Figure 7c. Input Not Referenced to GND

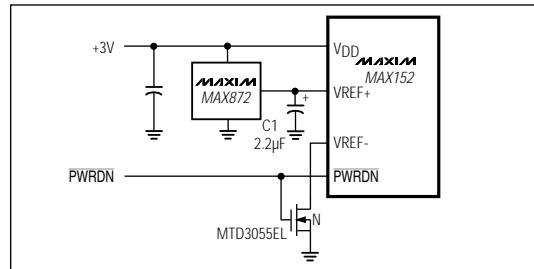


Figure 7d. An N-channel MOSFET switches off the reference load during power-down.



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### \_\_\_\_\_ Analog Considerations

#### Reference

Figures 7a-7c show some reference connections. VREF+ and VREF- inputs set the full-scale and zero-input voltages of the ADC. The voltage at VREF- defines the input that produces an output code of all zeros, and the voltage at VREF+ defines the input that produces an output code of all ones.

The internal resistance from VREF+ to VREF- may be as low as 1k $\Omega$ , and current will flow through it even when the MAX152 is shut down. Figure 7d shows how an N-channel MOSFET may be connected to VREF- to break this path during power-down. The FET should have an on resistance < 2 $\Omega$  with a 3V gate drive.

Although VREF+ is frequently connected to VDD, this circuit uses a low current, low-dropout, 2.5V voltage reference – the MAX872. Since the MAX872 cannot continuously furnish enough current for the reference resistance, this circuit is intended for applications where the MAX152 is normally in standby and is turned on in order to make measurements at intervals greater than 20 $\mu$ s. The capacitor C1 connected to VREF+ is slowly charged by the MAX872 during the standby period and furnishes the reference current during the short measurement period.

The 2.2 $\mu$ F value of C1 is chosen so that its voltage drops by less than 1/2LSB during the conversion process. Larger capacitors reduce the error still further. Use ceramic or tantalum capacitors for C1.

When VREF- is switched, as in Figure 7d, a new conversion can be initiated after waiting a time equal to the power-up delay ( $t_{UP}$ ) plus the turn-on time of the N-channel FET.

#### Bypassing

A 4.7 $\mu$ F electrolytic in parallel with a 0.1 $\mu$ F ceramic capacitor should be used to bypass VDD to GND. These capacitors should have minimal lead length.

The reference inputs should be bypassed with 0.1 $\mu$ F capacitors, as shown in Figures 7a-7c.

#### Input Current

Figure 8 shows the equivalent circuit of the converter input. When the conversion starts and  $\overline{WR}$  is low,  $V_{IN}$  is connected to sixteen 0.6pF capacitors. During this acquisition phase, the input capacitors charge to the input voltage through the resistance of the internal analog switches. In addition, about 12pF of stray capacitance must be charged. The input can be modeled as an equivalent RC network (Figure 9). As source impedance increases, the capacitors take longer to charge.

The typical 22pF input capacitance allows source resistance as high as 2.2k $\Omega$  without setup problems. For larger resistances, the acquisition time ( $t_p$ ) must be increased.

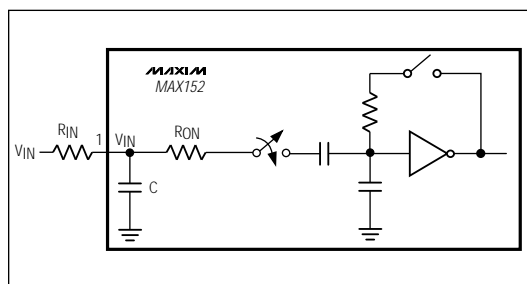


Figure 8. Equivalent Input Circuit

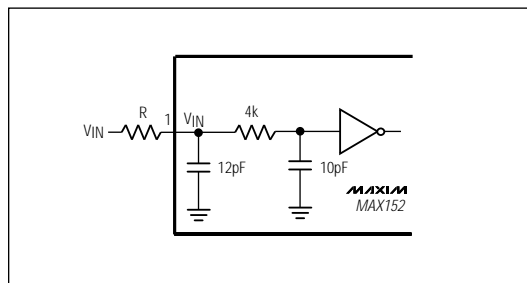


Figure 9. RC Network Equivalent Input Model

## +3V, 8-Bit ADC with 1 $\mu$ A Power-Down

### Conversion Rate

The maximum sampling rate ( $f_{\max}$ ) for the MAX152 is achieved in the WR-RD mode ( $t_{RD} < t_{INTL}$ ) and is calculated as follows:

$$f_{\max} = \frac{1}{t_{WR} + t_{RD} + t_{RI} + t_P}$$

e.g. at  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +3.0\text{V}$ :

$$f_{\max} = \frac{1}{600\text{ns} + 800\text{ns} + 300\text{ns} + 450\text{ns}}$$

$$f_{\max} = 465\text{kHz}$$

where  $t_{WR}$  = Write pulse width

$t_{RD}$  = Delay between WR and RD pulses

$t_{RI}$  =  $\overline{\text{RD}}$  to  $\overline{\text{INT}}$  delay

$t_P$  = Delay time between conversions.

### Signal-to-Noise Ratio and Effective Number of Bits

Signal-to-noise plus distortion ratio (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS amplitude of all other ADC output signals. The output band is limited to frequencies above DC and below one-half the ADC sample rate.

The theoretical minimum A/D noise is caused by quantization error, and results directly from the ADC's resolution:  $\text{SNR} = (6.02N + 1.76)\text{dB}$ , where N is the number of bits of resolution. Therefore, a perfect 8-bit ADC can do no better than 50dB.

The FFT plot (*Typical Operation Characteristics*) shows the result of sampling a pure 30.27kHz sinusoid at a 400kHz rate. This FFT plot of the output shows the output level in various spectral bands.

The effective resolution, or "effective number of bits," the ADC provides can be measured by transposing the equation that converts resolution to SNR:  $N = (\text{SINAD} - 1.76)/6.02$  (see *Typical Operating Characteristics*).

### Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one-half the sample rate) to the fundamental itself. This is expressed as:

$$\text{THD} = 20 \log \left[ \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + \dots + V_N^2)}}{V_1} \right]$$

where  $V_1$  is the fundamental RMS amplitude, and  $V_2$  to  $V_N$  are the amplitudes of the 2nd through Nth harmonics.

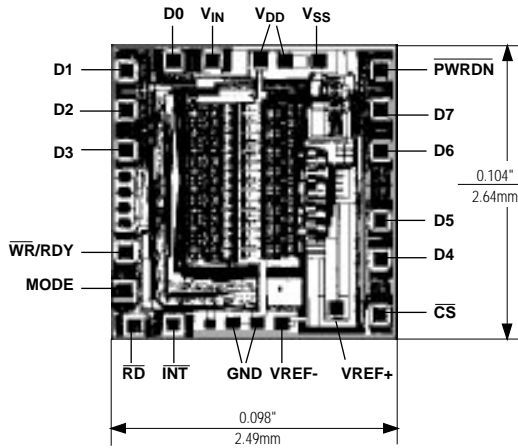
### Spurious-Free Dynamic Range

Spurious-free dynamic range is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually the next largest spectral component occurs at some harmonic of the input frequency. However, if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor. See "Signal to Noise Ratio" plot in *Typical Operating Characteristics*.

# +3V, 8-Bit ADC with 1µA Power-Down

## Chip Topography

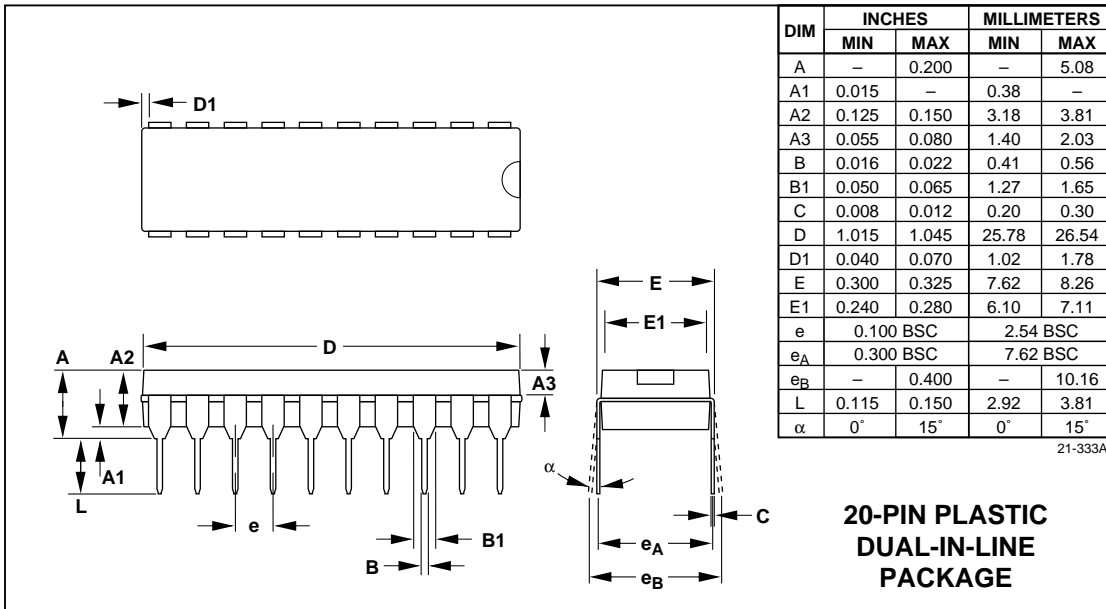
MAX152



TRANSISTOR COUNT: 1856  
SUBSTRATE CONNECTED TO V<sub>DD</sub>

MAX152

## Package Information



# +3V, 8-Bit ADC with 1 $\mu$ A Power-Down

MAX152

Package Information (continued)

