

MAXIM

300kHz 10-Bit A/D Converter with Reference and T/H

MAX151

General Description

The MAX151 is a high-speed, easy-to-use, microprocessor (μ P) compatible 10-bit Analog-to-Digital Converter (ADC) with Track-and-Hold (T/H). Half-flash techniques allow a typical conversion time of 1.9 μ s with a Total Unadjusted Error (TUE) of ± 1 LSB (Max). The converter has a 0V to +5V analog input voltage range and uses ± 5 V supplies.

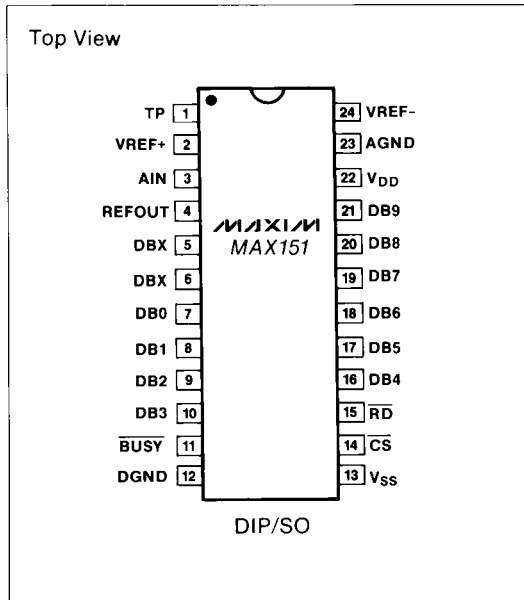
The MAX151 internally tracks and holds the analog input signal, eliminating the need for an external T/H when digitizing high-speed AC input signals. The MAX151 also contains an internal 4V reference, making the part a complete, low-cost ADC. Power consumption is typically 275mW.

The MAX151 interfaces directly to a μ P by appearing as a memory location or Input/Output (I/O) port. Read (RD) and Chip Select (CS) inputs control three-state outputs. Two interface modes ensure compatibility with most popular μ Ps. The MAX151 is available in both 0.3" DIP and Wide SO packages.

Applications

- Digital Signal Processing
- High-Speed Data Acquisition
- Telecommunications
- High-Speed Servo Loops
- Audio Systems

Pin Configuration



Features

- ◆ 10-Bit Resolution and Accuracy
- ◆ ± 1 LSB Total Unadjusted Error
- ◆ 2.5 μ s Max Conversion Time (0.5 μ s Input Acquisition Time)
- ◆ 300kHz Sampling Rate
- ◆ Internal 60ppm/ $^{\circ}$ C Reference
- ◆ 1ppm/ $^{\circ}$ C Gain and Offset Drift
- ◆ Internal Clock
- ◆ ± 5 V Supplies with 275mW Power Dissipation
- ◆ 24-Pin 0.3" DIP and Wide SO Packages
- ◆ Tested for DC and Dynamic Specifications

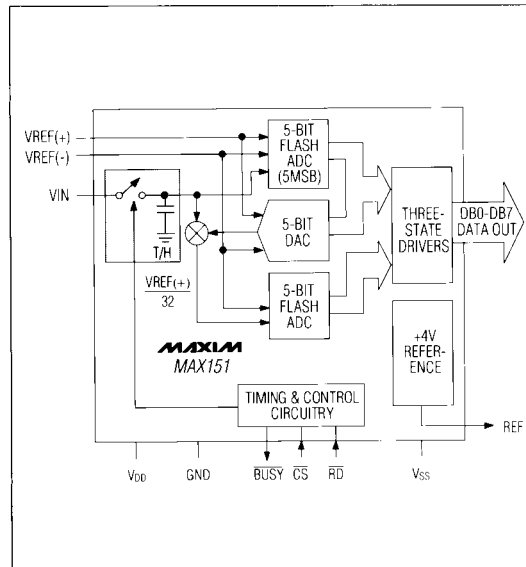
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	TUE (LSB)
MAX151ACNG	0 $^{\circ}$ C to +70 $^{\circ}$ C	24 Plastic DIP	1.0
MAX151BCNG	0 $^{\circ}$ C to +70 $^{\circ}$ C	24 Plastic DIP	1.5
MAX151ACWG	0 $^{\circ}$ C to +70 $^{\circ}$ C	24 Wide SO	1.0
MAX151BCWG	0 $^{\circ}$ C to +70 $^{\circ}$ C	24 Wide SO	1.5
MAX151BC/D	0 $^{\circ}$ C to +70 $^{\circ}$ C	Dice*	1.5

* Consult factory for dice specification.

Ordering information continued on page 11.

Block Diagram



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300kHz 10-Bit A/D Converter with Reference and T/H

ABSOLUTE MAXIMUM RATINGS

V _{DD} to DGND	-0.3V, +6V	Max Junction Temperature	
V _{DD} to V _{SS}	-0.3V, +12V	MAX151C, MAX151E	150°C
V _{DD} to AGND	-0.3V, +6V	MAX151M	175°C
Digital Outputs and Inputs to DGND	-0.3V, V _{DD} +0.3V	Operating Temperature Ranges	
Analog Inputs to V _{SS}	-0.3V, V _{DD} +0.3V	MAX151C	0°C to +70°C
REFOUT Current	Indefinite Short to V _{DD} or AGND	MAX151E	-40°C to +85°C
Power Dissipation (Any Package) to +75°C	1000mW	MAX151M	-55°C to +125°C
Derate Above 75°C by	10mW/°C	Storage Temperature Range	-65°C to +160°C
		Lead Temperature Range (Soldering, 10 sec.)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = -5V; VREF- = 0V, VREF+ = +5V; Slow Memory Mode; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC ACCURACY						
Resolution			10			Bits
Differential Nonlinearity	DNL	No missing codes guaranteed			±1	LSB
Total Unadjusted Error	TUE	MAX151A MAX151B			±1 ±1.5	LSB
Power-Supply Rejection		V _{DD} = ±5% V _{SS} fixed V _{SS} = ±5% V _{DD} fixed			±1/4 ±1/4	LSB
DYNAMIC PERFORMANCE (f _s = 300kHz, V _{IN} = 5V _{P-P} at 40kHz)						
Signal-to-Noise Plus Distortion Ratio	S/(N+D)		55	58		dB
Total Harmonic Distortion	THD	First 5 harmonics		-70	-60	dB
Peak Harmonic or Spurious Noise				-70	-60	dB
Full-Power Input Bandwidth	FPBW			5		MHz
ANALOG INPUT						
Analog Input Range			VREF-		VREF+	V
Input Resistance	RIN			10		MΩ
Input Capacitance	CAIN	In series with 150Ω		150		pF
Input Current	I _{AIN}	A _{IN} = 0V to V _{DD}			±10	μA
REFERENCE INPUT						
Ladder Resistance		VREF+ to VREF-	0.5	1		kΩ
Negative Reference Voltage			V _{AGND} -0.1		V _{AGND} +0.1	V
Reference Voltage (Note 2)		VREF+ to VREF-	1		V _{DD}	V
INTERNAL REFERENCE						
Output Voltage		T _A = 25°C	3.970	4.000	4.030	V
Temperature Coefficient (Note 3)					60	ppm/°C
External Load Current		Must not change during conversion (In addition to ladder current)			2	mA
Power-Supply Rejection		V _{DD} = ±5% V _{SS} fixed V _{SS} = ±5% V _{DD} fixed			±3 ±2	mV
Output Impedance				0.4	1.5	Ω

300kHz 10-Bit A/D Converter with Reference and T/H

MAX151

ELECTRICAL CHARACTERISTICS (Continued)

($V_{DD} = +5V$, $V_{SS} = -5V$; $V_{REF-} = 0V$, $V_{REF+} = +5V$; Slow Memory Mode; $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
Input High Voltage	V_{IH}	\overline{CS} , \overline{RD}	2.4			V
Input Low Voltage	V_{IL}	\overline{CS} , \overline{RD}			0.8	V
Input Current	I_{IN}	\overline{CS} , \overline{RD} ; $V_{IN} = 0V$ to V_{DD}			± 10	μA
Input Capacitance (Note 1)	C_{IN}	\overline{CS} , \overline{RD}			10	pF
LOGIC OUTPUTS						
Output Low Voltage	V_{OL}	\overline{BUSY} , DB0-DB9 $I_{SINK} = 1.6mA$			0.4	V
Output High Voltage	V_{OH}	\overline{BUSY} , DB0-DB9 $I_{SRC} = 200\mu A$	4.0			V
Floating State Current	I_{LKG}	DB0-DB9 $V_{OUT} = 0V$ to V_{DD}			± 10	μA
Floating Capacitance (Note 1)	C_{OUT}				15	pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}		4.75		5.25	V
Negative Supply Voltage	V_{SS}		-4.75		-5.25	V
Positive Supply Current	I_{VDD}	$\overline{CS} = \overline{RD} = 0$, $A_{IN} = 0V$ REFOUT connected to V_{REF+}		30	45	mA
Negative Supply Current	I_{VSS}	$\overline{CS} = \overline{RD} = 0$, $A_{IN} = 0V$ REFOUT connected to V_{REF+}		25	40	mA
Power Dissipation	PD	$\overline{CS} = \overline{RD} = 0$, $A_{IN} = 0V$, Including Ladder; REFOUT connected to V_{REF+}		275	425	mW

TIMING CHARACTERISTICS

($V_{DD} = +5V$, $V_{SS} = -5V$; Guaranteed by design, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	$T_A = +25^\circ C$			$T_A = T_{MIN}$ to T_{MAX}		UNITS
			MIN	TYP	MAX	MIN	MAX	
\overline{CS} to \overline{RD} Setup Time	t_{CS}		0			0		ns
\overline{CS} to \overline{RD} Hold Time	t_{CH}		0			0		ns
Data Access Time (Notes 4, 5)	t_{RD}	$C_L = 100pF$		70	120		180	ns
Bus Relinquish Time (Notes 4, 5)	t_{DH}				70		100	ns
Conversion Time (Note 4)	t_{CONV}			1.9	2.5		2.5	μs
\overline{RD} to \overline{BUSY} Delay (Note 4)	t_{BUSY}	$C_L = 100pF$		70	140		200	ns
Data Setup Time After \overline{BUSY} (Notes 4, 5)	t_B				30		50	ns
Delay Between Conversions	t_D	With $R_S < 50\Omega$		500		500		ns
		With $R_S < 1k\Omega$		1.5		1.5		μs
\overline{RD} Pulse Width	t_{RPW}	To minimize digital coupling in ROM Mode			300		300	ns
Aperture Delay	t_{AP}			30				ns
Aperture Jitter				100				ps

Note 1: Guaranteed by design, not 100% tested.

Note 2: Reduce accuracy at low reference voltages. See Typical Operating Characteristics.

Note 3: $V_{REF} \text{ Tempco} = \Delta V_{REF} / \Delta T$, where ΔV_{REF} is the change in the reference voltage from $T_A = 25^\circ C$ to T_{MIN} or T_{MAX} .

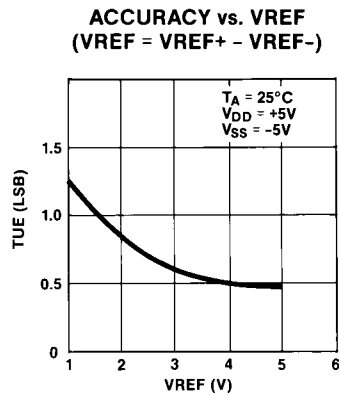
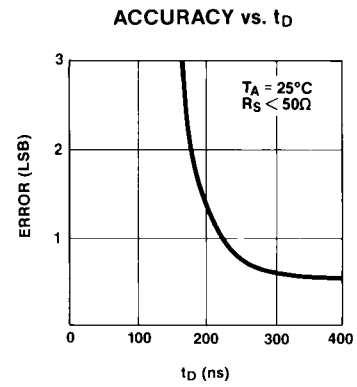
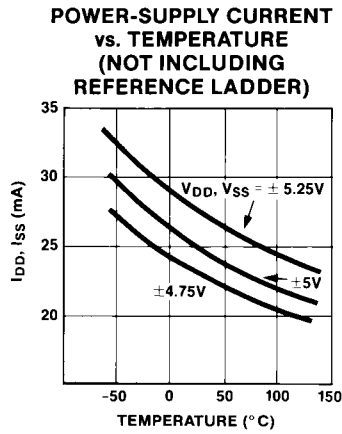
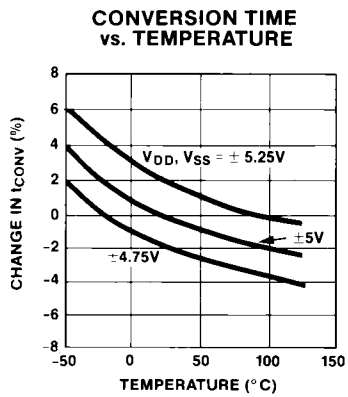
Note 4: 100% production tested.

Note 5: All input control signals are specified with $t_r = t_f = 5ns$ (10% to 90% of +5V) and timed from a voltage level of +1.6V. t_{RD} and t_B are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V. t_{DH} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

MAXIM

300kHz 10-Bit A/D Converter with Reference and T/H

Typical Operating Characteristics



300kHz 10-Bit A/D Converter with Reference and T/H

Pin Description

MAX151

PIN	NAME	FUNCTION
1	TP	Test Pin, leave open.
2	VREF+	Positive Ladder Input, upper limit of reference span. Set the full-scale input voltage. Range: 1V to V _{DD} .
3	AIN	(Sampling) Analog Input
4	REFOUT	+4V Reference Output, usually connected to VREF+.
5-6	DBX	(Reserved for DB0-1, future 12-bit version, = LOW.)
7-10	DB0-DB3	Three-State Data Output, Bits 0-3
11	BUSY	Busy Status Output, low when conversion is in progress.
12	DGND	Digital Ground.

PIN	NAME	FUNCTION
13	V _{SS}	Negative Supply, -5V.
14	$\overline{\text{CS}}$	Chip Select Input, must be low for the ADC to recognize RD.
15	$\overline{\text{RD}}$	Active Low Read Input, starts conversion when $\overline{\text{CS}}$ is low. $\overline{\text{RD}}$ also enables the output drivers when $\overline{\text{CS}}$ is low.
16-21	DB4-DB9	Three-State Data Output, Bits 4-9
22	V _{DD}	Positive Supply, +5V
23	AGND	Analog Ground
24	VREF-	Negative Voltage Ladder Input, lower limit of reference span. Set the zero-code voltage. Range: AGND \pm 0.1V.

Detailed Description

ADC Operation

The MAX151 half-flash A/D converter contains 31 comparators. The analog input is sampled by each comparator and compared to a resistive ladder DAC. A 5-bit coarse conversion result is then generated from the ladder DAC, subtracted from the analog input, and compared to a 2nd resistive ladder. 5 coarse and 5 fine bits are output in 10-bit wide parallel output format.

The voltage at the top and the bottom of the reference ladder determines the MAX151's zero-scale and full-scale input voltage. The analog input can range from 0V to +5V. An internal reference provides a 4.000V nominal output and is used by connecting REFOUT to VREF+ and VREF- to AGND. The reference provides up to 2mA of external load current in addition to the current it supplies to the internal ladder. Figure 3 shows the MAX151 in a typical application.

Analog Input - T/H

The MAX151 input can be modeled as a 150pF load in series with 150 Ω (Figure 4). The comparator's input capacitance acts as a "hold" capacitor and must be completely charged by the input signal with every A/D conversion.

The input signal sees AIN as a capacitor which is switched between itself and AGND. Between conversions, the signal is tracked by connecting the capacitor to AIN. When a conversion begins, the capacitor disconnects from the analog input, and the A/D performs its conversion. At the end of the conversion, it reconnects to the input and charges to the input signal.

The MAX151 can digitize a variety of high-speed input signals without an external sample-and-hold. Although the conversion time for the MAX151 is 1.9 μ s, the time the input must be stable is much less.

The time needed for the T/H to acquire an input signal is a function of how quickly the input capacitance can be charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. Acquisition time is calculated by:

$$t_{ACQ} = 10(R_S + 150\Omega)150\text{pF}$$

(but never less than 500ns)

Where R_S = source impedance of the input signal.

The MAX151 samples the analog input approximately 30ns after RD and CS (which are internally NANDed) are pulled low. This aperture delay is caused by the propagation delay of the internal logic. The variation in this delay from one conversion to the next is called aperture jitter, and it is typically less than 100ps.

The architecture of the MAX151 allows signals with high slew rates to be converted without error (Figure 4). The errors caused by fast input signals are far less than the errors caused in a conventional SAR type ADC without sample-and-hold: a 1 μ s SAR converter would be unable to measure a 1kHz, 5V sine wave without using an external sample-and-hold. With no external sample-and-hold, the MAX151 can typically measure 5V_{p-p}, 100kHz waveforms.

300kHz 10-Bit A/D Converter with Reference and T/H

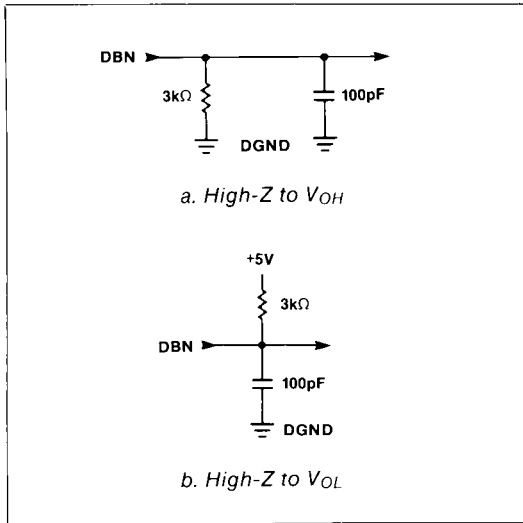


Figure 1. Load Circuits for Data Access Time Test

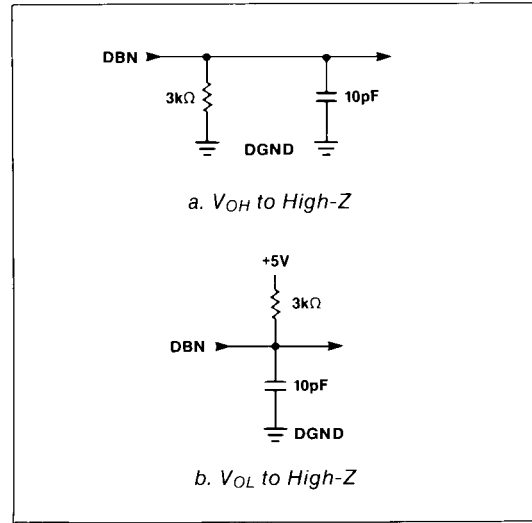


Figure 2. Load Circuits for Bus Relinquish Time Test

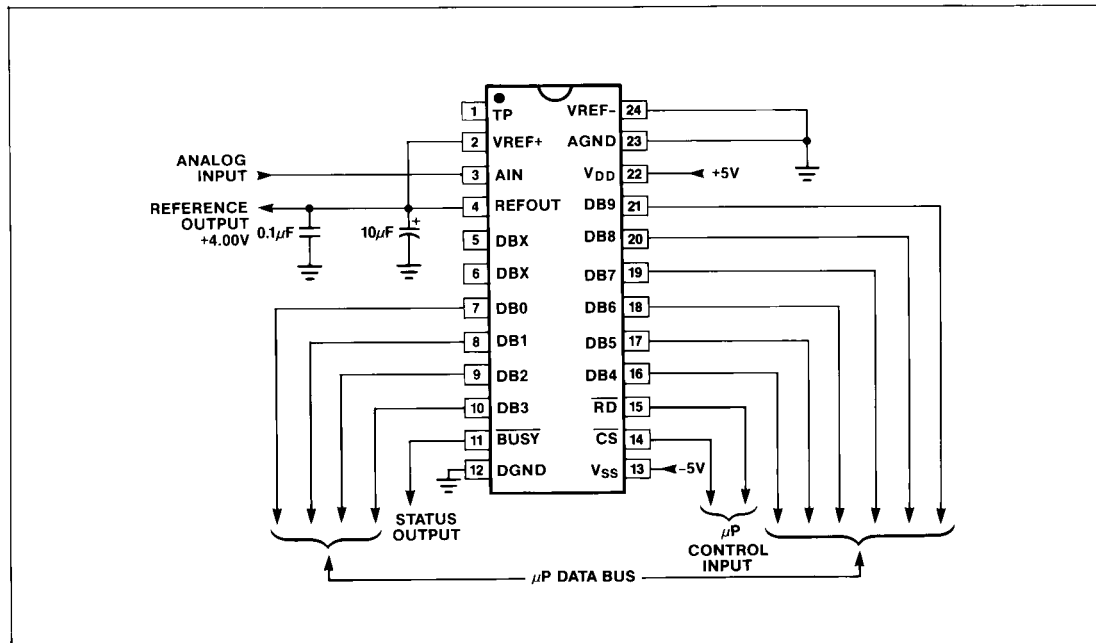


Figure 3. MAX151 Operational Diagram

300kHz 10-Bit A/D Converter with Reference and T/H

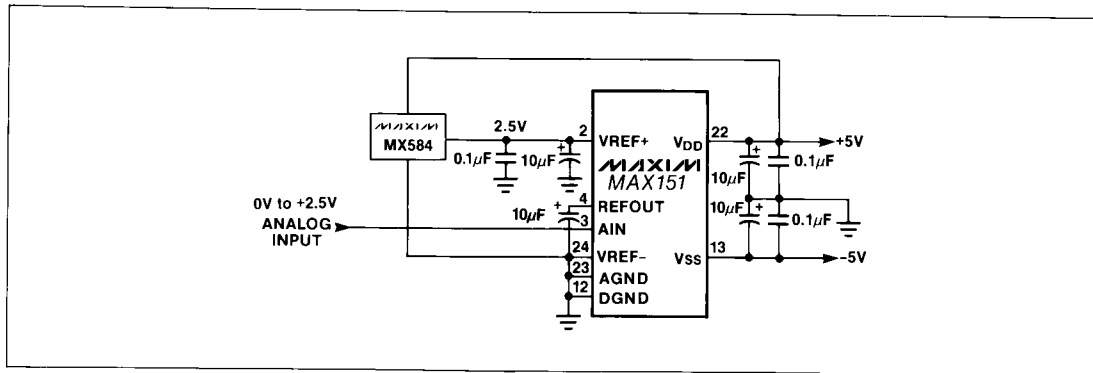


Figure 8. External Reference 2.5V Full-Scale

The VREF+ and VREF- inputs set the full-scale and zero-input voltages of the A/D. More precisely, the voltage at VREF- defines the input which produces an output code of all 0s, and the voltage at VREF+ defines the input which produces an output code of all 1s (Figure 9).

Gain and Offset Adjustment

Figure 9 shows the nominal unipolar transfer function of the MAX151. Code transitions occur at successive integer Least Significant Bit (LSB) values. Output coding is natural binary with 1LSB = 3.91mV (4V/1024) for a 4V reference.

End-point errors are very low. But, if the end points (offset and full scale) need to be adjusted to compensate for errors from other components in the system, use the following techniques. In applications where full-scale adjustment is required, the connection in Figure 10 provides $\pm 0.5\%$, or ± 5 LSBs of adjustment range. If both offset and full-scale range need adjustment, the circuit in Figure 11 is recommended. Offset should be adjusted before full-scale. For the MAX151 (0V to +4V input range), apply 1/2 LSB (2mV) to the analog input and adjust R12 so the digital output code changes between 00000 00000 and 00000 00001. To adjust full-scale, apply FS-3/2LSB (3.994mV) and adjust R8 until the output code changes between 11111 11110 and 11111 11111. There may be slight interaction between adjustments. If an input gain of 2 is acceptable, the connection in Figure 11 can be simplified by removing R5 and R6.

Starting a Conversion

The ADC is controlled by the CS and RD inputs. The T/H holds the value of the input signal, and a conversion is triggered by the falling edge of CS and RD. The BUSY output goes low as soon as the conversion starts. BUSY goes high at the end of the conversion, and the result is latched into three-state output buffers.

Digital Interface

The MAX151 has two basic interface modes: The Slow

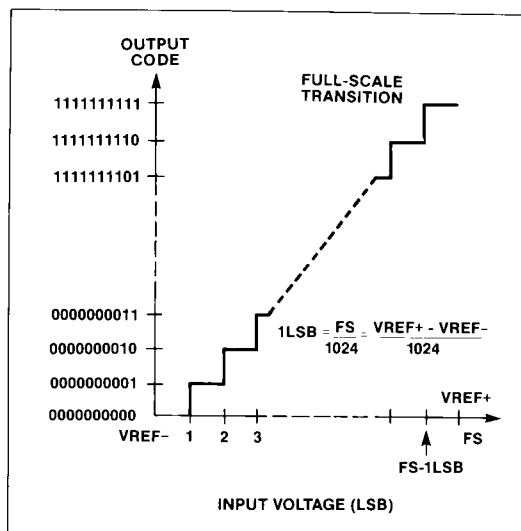


Figure 9. Ideal Transfer Function

Memory Mode requires handshaking, but the ROM Mode does not. The length of the RD pulse tells the chip which mode is anticipated. In both modes, conversions are initiated by a falling RD and CS signal.

In the Slow Memory Mode, the μ P actively holds RD low until a complete conversion has been performed. During the conversion, the data outputs are active with the data from the previous conversion. After the conversion ends (t_{CONV}), the μ P can read the result of the conversion. The BUSY signal is used as a handshake to tell the μ P when a conversion ends.

In the ROM Mode, a short RD pulse starts a conversion and reads the result of the previous conversion. Note, the width of this pulse should not exceed 300ns.

300kHz 10-Bit A/D Converter with Reference and T/H

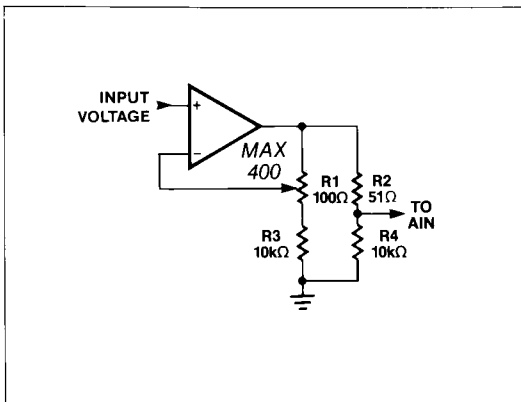


Figure 10. Trim Circuit for Full-Scale Only ($\pm 0.5\%$)

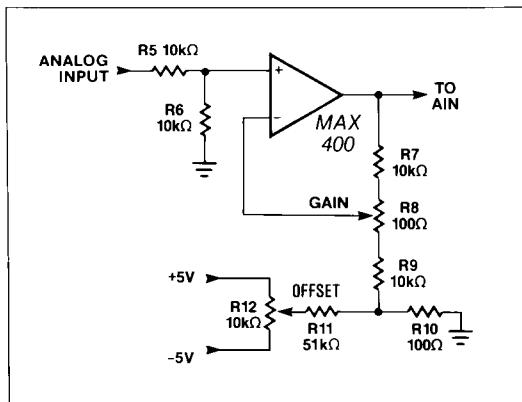


Figure 11. Offset ($\pm 20\text{mV}$) and Gain ($\pm 0.5\%$) Trim Circuit

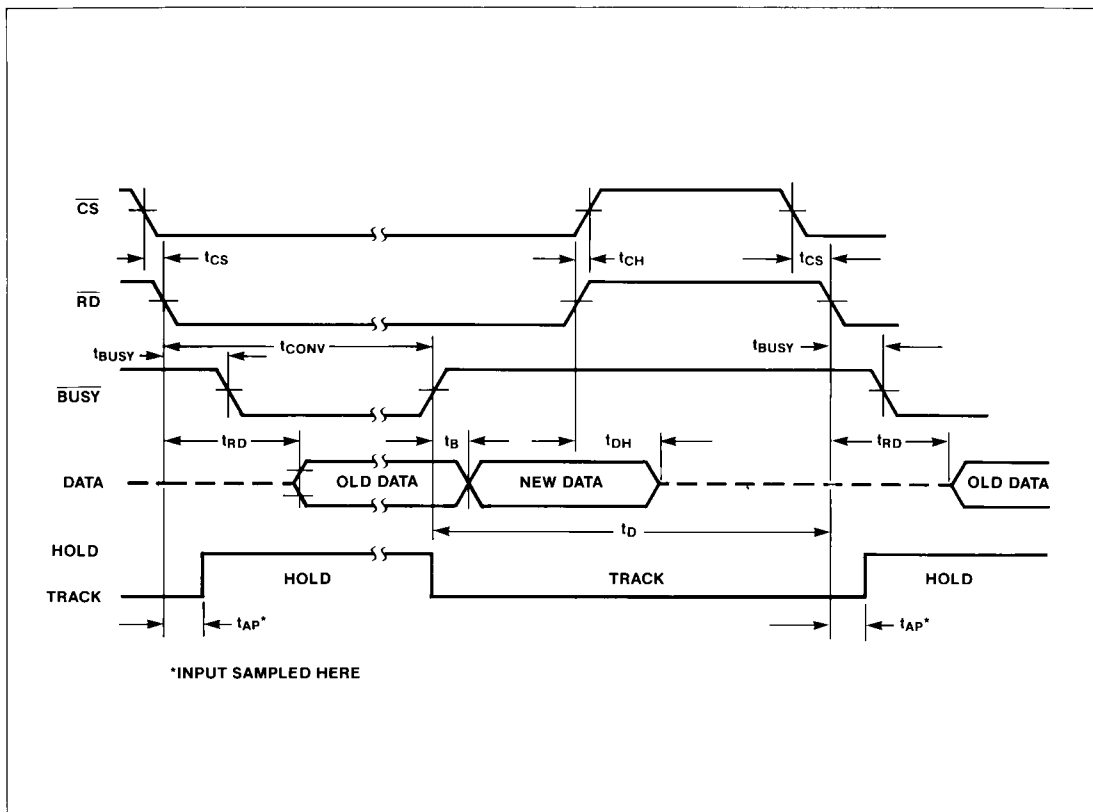


Figure 12. Timing Diagram—Slow Memory Mode

300kHz 10-Bit A/D Converter with Reference and T/H

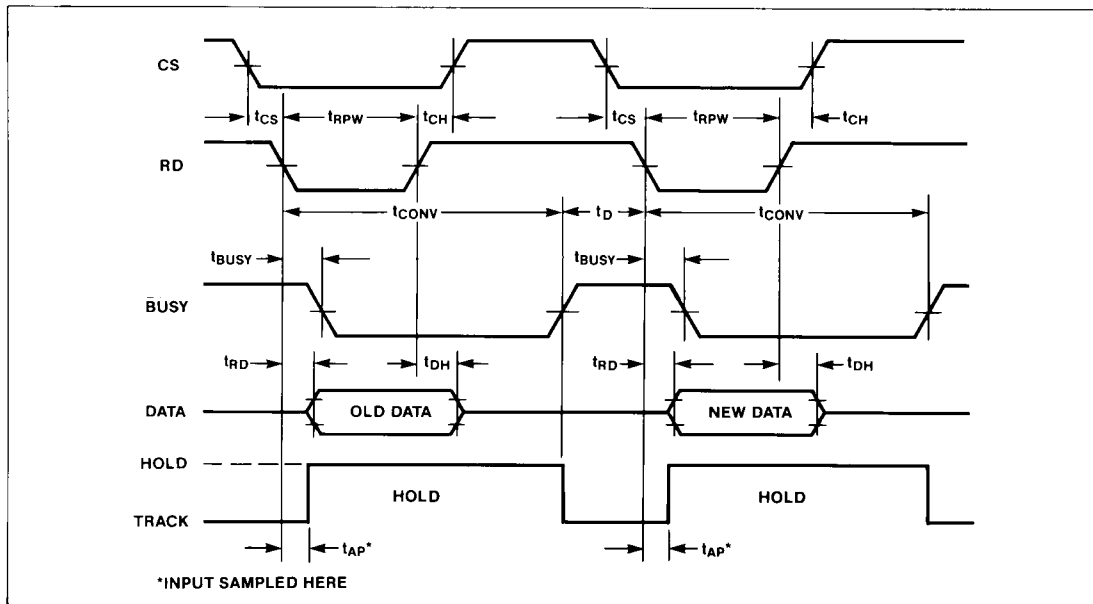


Figure 13. Timing Diagram—ROM Mode

Layout, Grounding and Bypassing

For best system performance, printed circuit boards should be used (wire-wrap boards are not recommended). In layout, separate the digital and analog signal lines as much as possible. Analog and digital lines should not run parallel, and digital lines should not run underneath the ADC package.

Figure 14 shows the recommended power-supply grounding connections. A single-point analog STAR ground should be established at AGND separate from the logic ground. All other analog grounds and DGND should be connected to this STAR ground. No other digital system grounds should be connected here. The ground return to the power supply from this STAR ground should be low impedance and as short as possible for noise-free operation.

Power supplies should be bypassed to the analog STAR ground with $0.1\mu\text{F}$ and $10\mu\text{F}$ bypass capacitors. Capacitor leads should have minimum length for best noise rejection.

Dynamic Performance

ADCs have traditionally been evaluated by specifications such as zero and full-scale error, Integral Nonlinearity (INL), and Differential Nonlinearity (DNL). Such parameters are accepted for specifying performance with DC and slowly varying signals, but less useful in signal processing where the A/D's impact on the system transfer is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

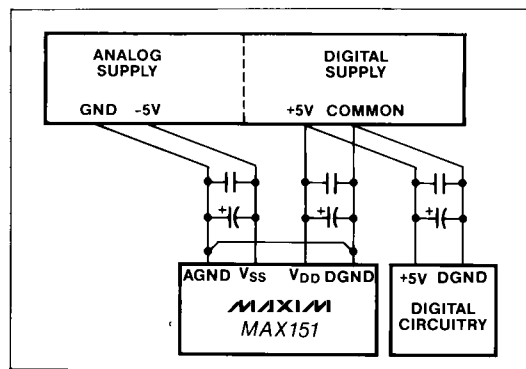


Figure 14. Power-Supply Grounding Practice

High-speed sampling capability and up to 333 ksamples/sec throughput make the MAX151 ideal for wide-band signal processing. To support these and other related applications, Fast Fourier Transform (FFT) test techniques are used to guarantee the A/D's dynamic frequency response, distortion and noise at the rated throughput. This involves applying a low-distortion sine wave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm to determine spectral content. Conversion errors are seen as spectral elements outside of the fundamental input frequency.

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MAX151

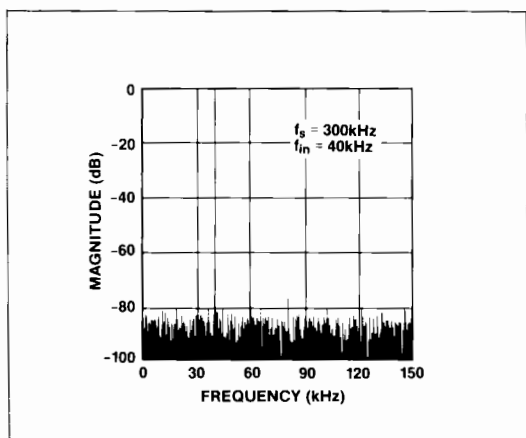


Figure 15. FFT Plot for the MAX151

Signal-to-Noise Ratio and Effective Number of Bits

The ratio of the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other A/D output signals is the Signal-to-Noise Ratio (SNR). This includes distortion and noise components. For this reason, the ratio is also referred to as $S/(N + D)$, or Signal-to-Noise plus Distortion.

The theoretical minimum A/D noise is caused by quantization error and a direct result of the A/D's resolution:

$$\text{SNR} = (6.02N + 1.76)\text{dB}$$

where N is the number of bits of resolution. A perfect 10-bit A/D can do no better than 62dB. Figure 15 shows the result of sampling a pure 40kHz sinusoid at a 300kHz rate. The FFT plot of the output shows the output level in various spectral bands (Figure 15).

By transposing the equation which converts resolution to SNR, the effective resolution or the "Effective Number of Bits" the A/D provides can be determined from the measured SNR:

$$N = (\text{SNR} - 1.76) / 6.02$$

Figure 16 shows the Effective Number of Bits as a function of the input frequency for the MAX151.

Total Harmonic Distortion

The ratio of the RMS sum of all harmonics of the input signal to the fundamental itself is Total Harmonic Distortion (THD). This is expressed as:

$$\text{THD} = 20\text{Log}[\sqrt{(V_2^2 + V_3^2 + V_4^2 + \dots + V_N^2)} / V_1]$$

where V_1 is the fundamental RMS amplitude and V_2 to V_N are the amplitudes of the 2nd through n th harmonics.

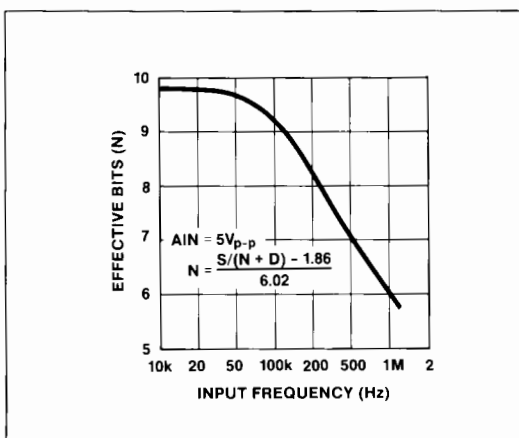


Figure 16. Effective Bits Curve

Peak Harmonic or Spurious Noise

The ratio of the RMS amplitude of the fundamental input frequency to the amplitude of the next largest spectral component is referred to as the Peak Harmonic or Spurious Noise. Usually this peak occurs at some harmonic of the input frequency. But, if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor.

Ordering Information (continued)

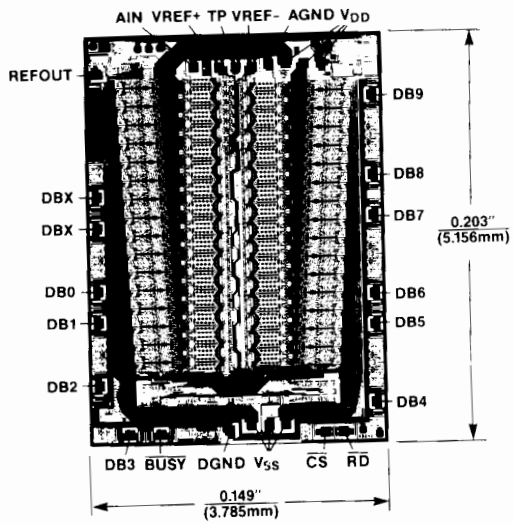
PART	TEMP.RANGE	PIN-PACKAGE	TUE (LSB)
MAX151AENG	-40°C to +85°C	24 Plastic DIP	1.0
MAX151BENG	-40°C to +85°C	24 Plastic DIP	1.5
MAX151AEWG	-40°C to +85°C	24 Wide SO	1.0
MAX151BEWG	-40°C to +85°C	24 Wide SO	1.5
MAX151AMRG	-55°C to +125°C	24 CERDIP	1.0
MAX151BMRG	-55°C to +125°C	24 CERDIP	1.5

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MAX151

Chip Topography



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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