19-1271; Rev 0; 8/97

MAXIM

12-Bit, 100Msps ECL DAC

General Description

The MAX5012 is a 12-bit, 100Msps digital-to-analog converter (DAC) designed for digital modulation, direct digital synthesis, high-resolution imaging, and arbitrary-waveform-generation applications. This device is pin-for-pin compatible with the AD9712 with significantly improved settling time and glitch-energy performance.

The MAX5012 is an ECL-compatible device. It features a fast 13ns settling time and low 15pV-s glitch impulse energy, which results in excellent spurious-free dynamic range characteristics.

The MAX5012 is available in a 28-pin plastic DIP or PLCC package in the -40°C to +85°C extended-industrial temperature range.

Features

- ♦ **12-Bit, 100Msps DAC**
- ♦ **ECL-Compatible Inputs**
- ♦ **Low Power: 600mW**
- ♦ **1/2LSB DNL**
- ♦ **40MHz Multiplying Bandwidth**
- ♦ **Extended-Industrial Temperature Range**
- ♦ **Superior Performance over AD9712:**
  Improved Settling Time: 13ns
  Improved Glitch Energy: 15pV-s
  Master/Slave Latches

Applications

Fast-Frequency-Hopping Spread-Spectrum Radios

Direct-Sequence Spread-Spectrum Radios

Digital RF/IF Modulation

Microwave and Satellite Modems

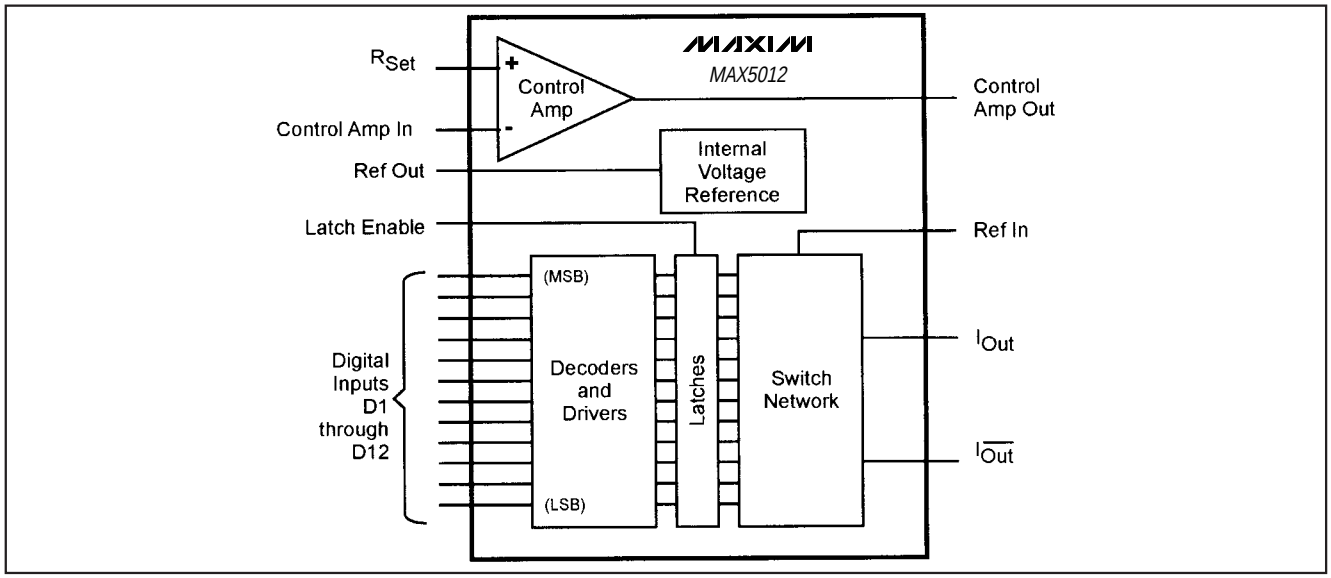
Test and Measurement Instrumentation

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX5012AEPI	-40°C to +85°C	28 Plastic DIP
MAX5012BEPI	-40°C to +85°C	28 Plastic DIP
MAX5012AEQI	-40°C to +85°C	28 PLCC
MAX5012BEQI	-40°C to +85°C	28 PLCC

Pin Configurations appear at end of data sheet.

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltages
  Negative Supply Voltage (V_{EE}) .....-7V
  A/D Ground Voltage Differential.....0.5V
Input Voltages
  Digital Input Voltage (D1–D12, Latch Enable) .....0V to V_{EE}
  Control Amp Input Voltage Range.....0V to -4V
  Reference Input Voltage Range (V_{REF}) .....-3.7V to V_{EE}
Output Currents
  Internal-Reference Output Current 500µA
  Control-Amplifier Output Current.....±2.5mA
Continuous Power Dissipation
  Plastic DIP (derate 14.29mW/°C above +70°C) 1.14W
  PLCC (derate 10.53mW/°C above +70°C) 842mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10sec) .....+300°C
Storage Temperature Range .....-65 to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_{SET} = 7.5kΩ, CONTROL AMP IN = REF OUT, V_{OUT} = 0V, T_A = T_{MIN} - T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MAX5012A MIN	MAX5012A TYP	MAX5012A MAX	MAX5012B MIN	MAX5012B TYP	MAX5012B MAX	UNITS
DC PERFORMANCE									
Resolution				12			12		Bits
Differential Nonlinearity		I		±0.5	±0.75		±1.0	±1.25	LSB
	Max at full temperature	VI			±1.5			±2.0	
Integral Nonlinearity	Best fit	I		±0.75	±1.0		±1.0	±1.5	LSB
	Max at full temperature	VI			±1.75			±2.0	
Output Capacitance	T_A = +25°C	V		10			10		pF
Gain Error (Note 1)	T_A = +25°C	I		1.0	5.0		1.0	5.0	% F.S.
	Full temperature	VI			8.0			8.0	
Gain-Error Tempco	Full temperature	V		150			150		ppm/°C
Zero-Scale Offset Error	T_A = +25°C	I		0.5	2.5		0.5	2.5	µA
	Full temperature	VI			5.0			5.0	
Offset Drift Coefficient	Full temperature	V		0.01			0.01		µA/°C
Output Compliance Voltage	T_A = +25°C	IV	-1.2		2.0	-1.2		2.0	V
Equivalent Output Resistance	T_A = +25°C	IV	0.8	1.0	1.2	0.8	1.0	1.2	kΩ
DYNAMIC PERFORMANCE									
Conversion Rate	T_A = +25°C	IV	100			100			Msps
Settling Time (t_{ST}) (Note 2)	T_A = +25°C	V		13			13		ns
Output Propagation Delay (t_D) (Note 3)	T_A = +25°C	V		1			1		ns
Glitch Energy (Note 4)	T_A = +25°C	V		15			15		pV-s
Full-Scale Output Current (Note 5)	T_A = +25°C	V		20.48			20.48		mA
Spurious-Free Dynamic Range	T_A = +25°C								
1.23MHz; 10Msps	2MHz span	V		70			70		dBc
5.055MHz; 20Msps				68			68		
10.1MHz; 50Msps				68			68		
16MHz; 40Msps	10MHz span			68			68		
Rise/Fall Time	R_L = 50Ω	V		2			2		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = -5.2V, R_{SET} = 7.5kΩ, CONTROL AMP IN = REF OUT, V_{OUT} = 0V, T_A = T_{MIN} - T_{MAX}, unless otherwise noted.)

PARAMETERS	CONDITIONS	TEST LEVEL	MAX5012A MIN	MAX5012A TYP	MAX5012A MAX	MAX5012B MIN	MAX5012B TYP	MAX5012B MAX	UNITS
POWER-SUPPLY REQUIREMENTS									
Negative Supply Voltage		IV	-5.46	-5.2	-4.94	-5.46	-5.2	-4.94	V
Negative Supply Current (-5.2V)	T_A = +25°C	I		115	140		115	140	mA
	Full temperature	VI			148			148	
Nominal Power Dissipation		V		600			600		mW
Power-Supply Rejection Ratio	±5% of V_{EE}, external reference, T_A = +25°C	I		30	100		30	100	µA/V
VOLTAGE INPUT AND CONTROL									
Reference Input Impedance	T_A = +25°C	V		3			3		kΩ
Reference Multiplying Bandwidth	T_A = +25°C	V		40			40		MHz
Internal Reference Voltage		VI	-1.15	-1.20	-1.25	-1.15	-1.20	-1.25	V
Internal Reference Voltage Drift		V		50			50		ppm/°C
Amplifier Input Impedance	T_A = +25°C	V		3			3		MΩ
Amplifier Input Bandwidth	T_A = +25°C	V		1			1		MHz
DIGITAL INPUTS									
Logic 1 Voltage	Full temperature	VI	-1.0	-0.8		-1.0	-0.8		V
Logic 0 Voltage	Full temperature	VI	-1.7	-1.5		-1.7	-1.5		V
Logic 1 Current	Full temperature	VI			20			20	µA
Logic 0 Current	Full temperature	VI			10			10	µA
Input Capacitance	T_A = +25°C	V		3			3		pF
Input Setup Time (t_S)	T_A = +25°C	IV	3	2		3	2		ns
	Full temperature	IV	3.5			3.5			ns
Input Hold Time (t_H)	T_A = +25°C	IV	0.5	0		0.5	0		ns
	Full temperature	IV	0.5			0.5			ns
Latch Pulse Width (t_{PWL}, t_{PWH})	T_A = +25°C	IV	5.0	4.0		5.0	4.0		ns

Note 1: Gain is measured as a ratio of the full-scale current to I_{SET}. The ratio is nominally 128.
Note 2: Measured as voltage at mid-scale transition to ±0.024%; R_L = 50Ω.
Note 3: Measured from the rising edge of Latch Enable to where the output signal has left a 1LSB error band.
Note 4: Glitch is measured as the largest single transient.

Note 5: Calculated using $I_{FS} = 128 \times \left(\frac{\text{Control Amp In}}{R_{SET}}\right)$

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any black section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25°C. Parameter is guaranteed over specified temperature range.

Pin Description

PIN	NAME	FUNCTION
1–10	D2–D11	Digital Input Bits 2–11
11	D12 (LSB)	Digital Input Bit 12 (LSB)
12, 21	Digital V_{EE}	Digital Negative Supply (-5.2V)
13	Analog Return	Analog Return Ground
14	I_{OUT}	Analog Current Output
15, 25	Analog V_{EE}	Analog Negative Supply (-5.2V)
16	$\overline{I_{OUT}}$	Complementary Analog Current Output
17	Ref In	Voltage Reference Input
18	Control Amp Out	Internal Control Amplifier Output. Control Amp Out is normally connected to Ref In.
19	Control Amp In	Internal Control Amplifier Input. Control Amp In is normally connected to Ref Out (if not connected to external reference).
20	Ref Out	Internal Voltage Reference Output. Ref Out is normally connected to Control Amp In.
22	Ref GND	Ground Return for Internal Voltage Reference and Amplifier
23	N.C.	No Connection. Not internally connected.
24	R_{SET}*	Connection for External Resistance Reference. R_{SET} is used with the internal amplifier (nominally 7.5kΩ).
26	Latch Enable	Latch Control Line
27	DGND	Digital Ground Return
28	D1 (MSB)	Digital Input Bit 1 (MSB)

**Full-Scale Current Out = 128 (Control Amp In/R_{SET})*

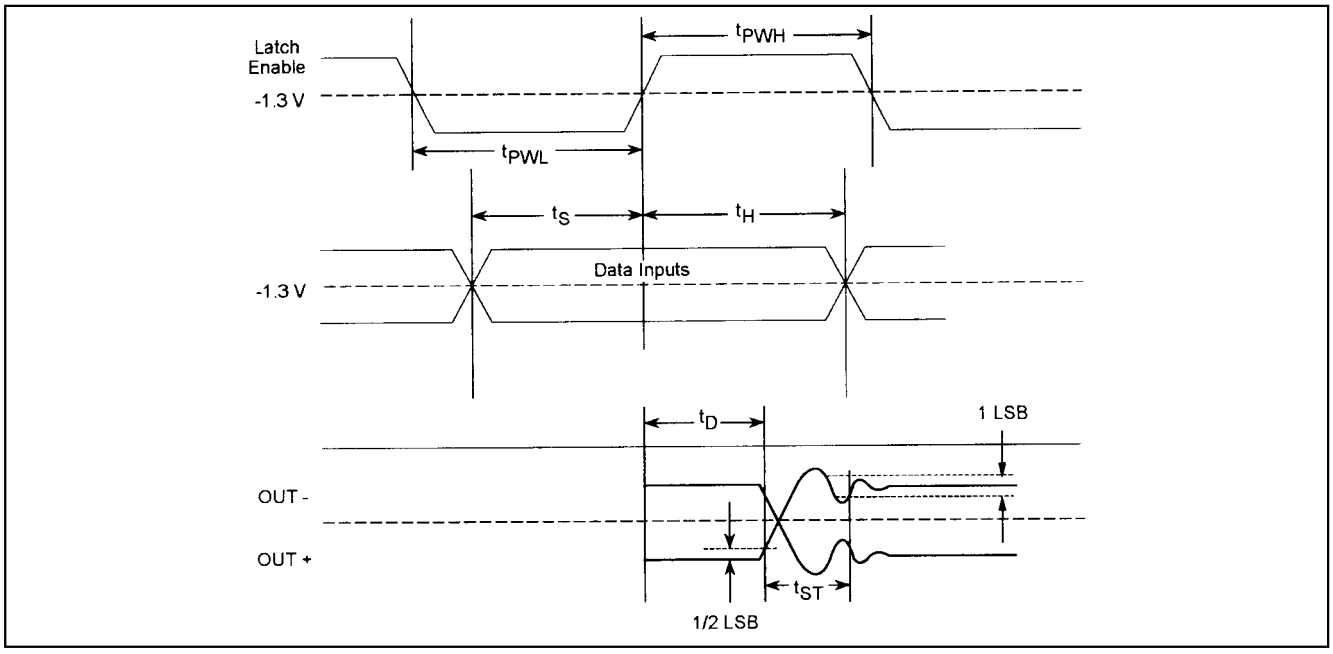


Figure 1. Timing Diagram

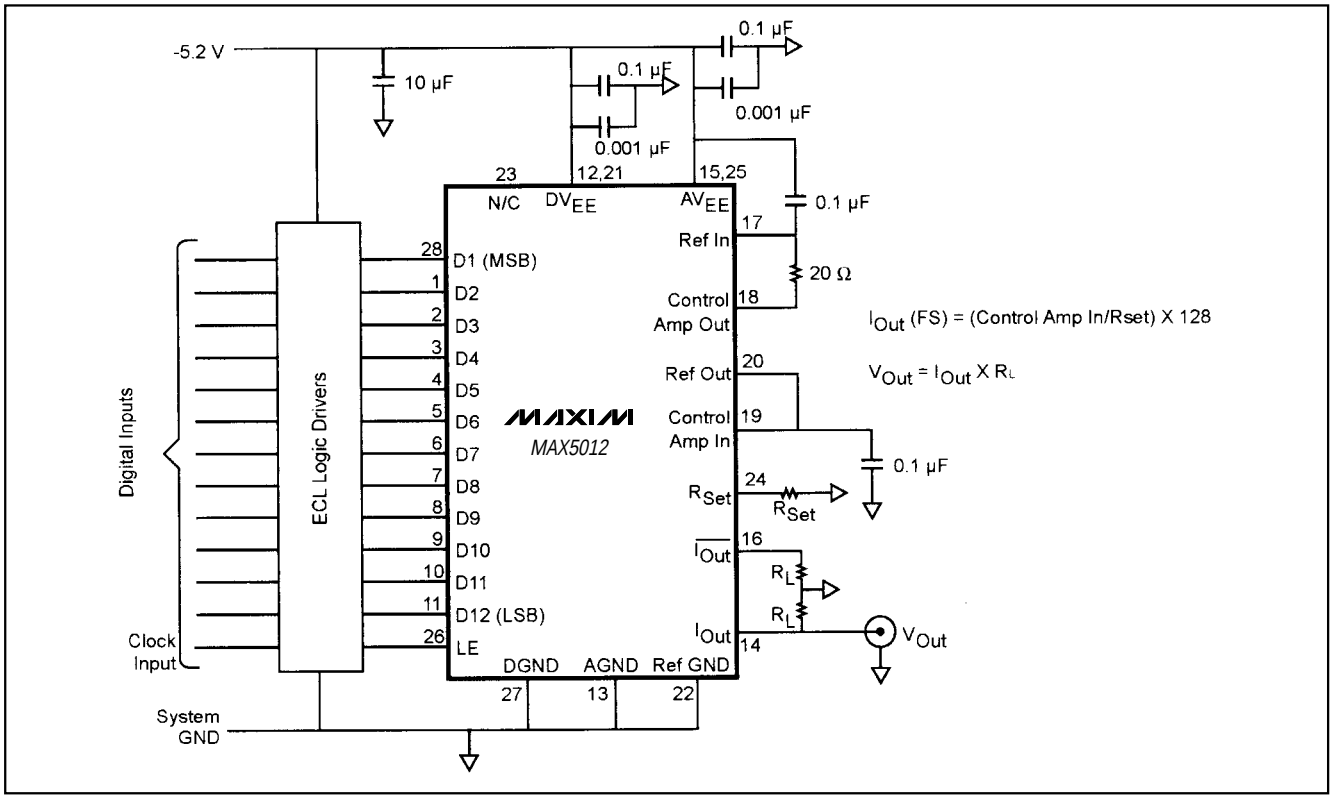
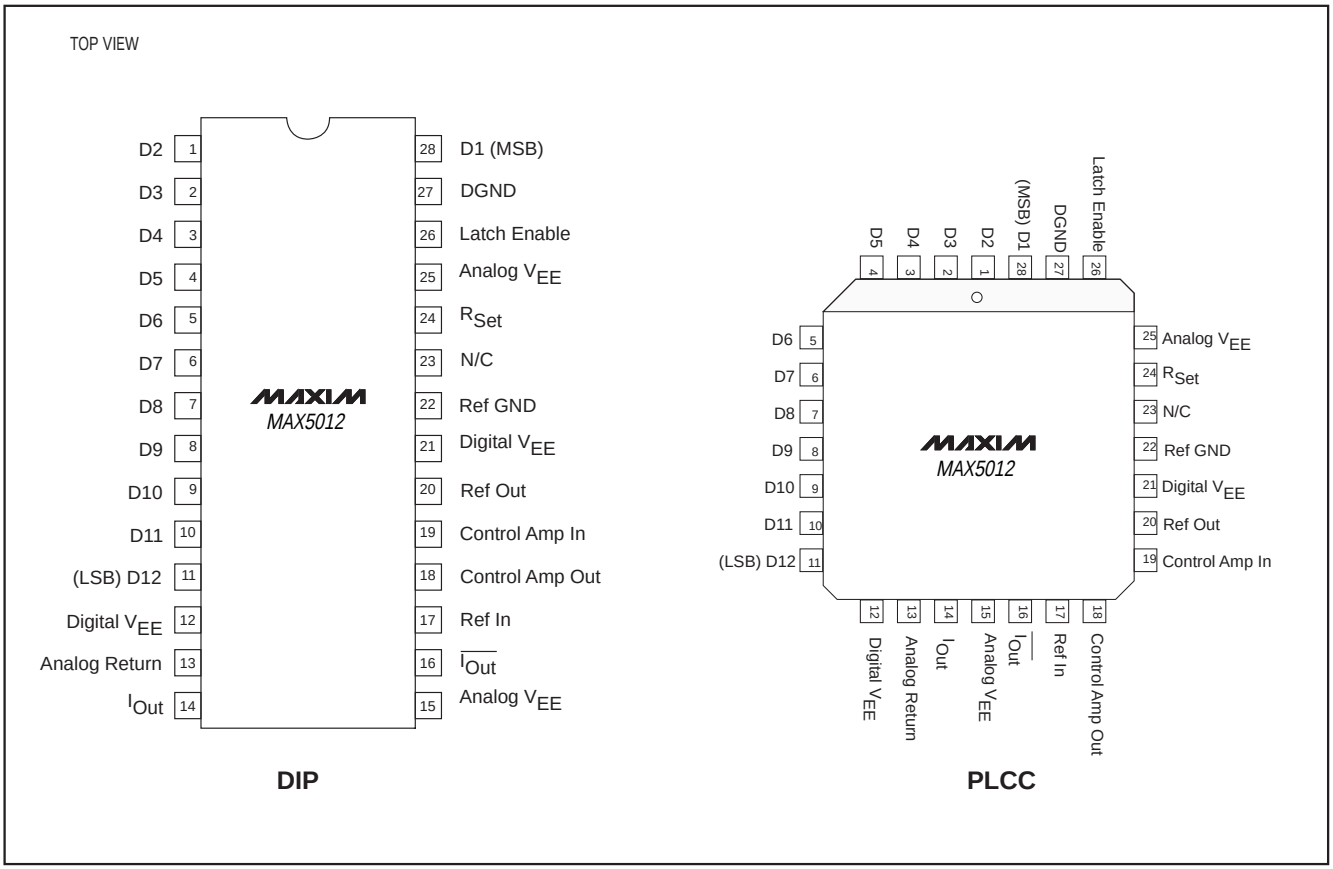
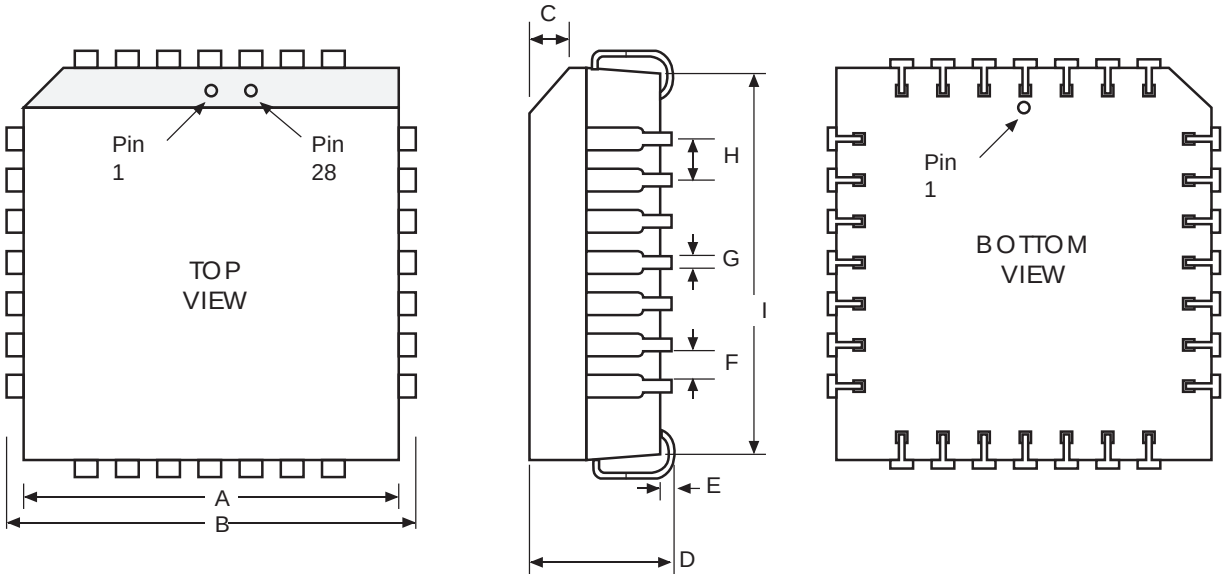


Figure 2. Typical Interface Circuit

Pin Configurations



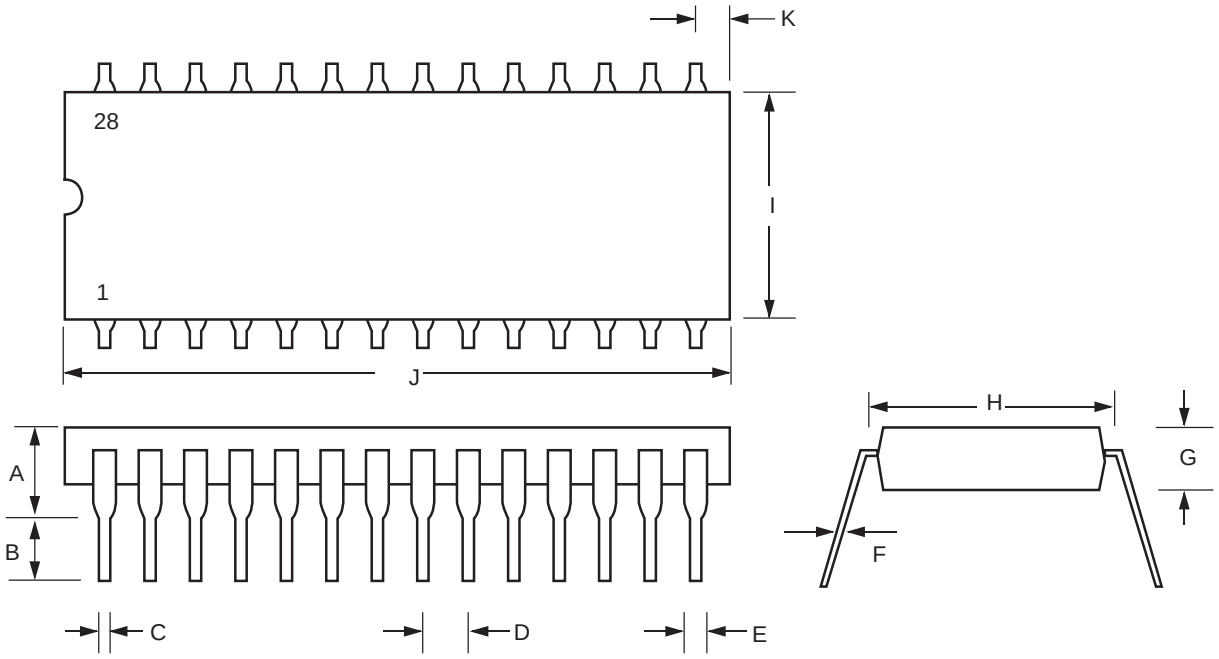
28L PLCC



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.450	0.456	11.43	11.58
B	0.485	0.495	12.32	12.57
C	45°		45°	
D	0.165	0.175	4.19	4.45
E		0.010		0.25
F	0.022 typ		.56 typ	
G	0.18 typ		4.57 typ	
H	0.05 typ		1.27 typ	
I	0.039	0.430	0.99	10.92

Package Information (continued)

28L Plastic DIP



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.200		5.08
B	0.120	0.135	3.05	3.43
C		0.020		0.51
D		0.100		2.54
E		0.067		1.70
F		0.013		0.33
G	0.170	0.180	4.32	4.57
H		0.622		15.80
I		0.555		14.10
J		1.460		37.08
K		0.085		2.16