AVAXIAV $\pm 5 \mathrm{~V}, 1 \mathrm{Gsps}, 8$-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

General Description
The MAX104 PECL-compatible, 1 Gsps, 8-bit analog-todigital converter (ADC) allows accurate digitizing of analog signals with bandwidths to 2.2 GHz . Fabricated on Maxim's proprietary advanced GST-2 bipolar process, the MAX104 integrates a high-performance track/hold (T/H) amplifier and a quantizer on a single monolithic die.
The innovative design of the internal $\mathrm{T} / \mathrm{H}$, which has an exceptionally wide 2.2 GHz full-power input bandwidth, results in high performance (greater than 7.5 effective bits) at the Nyquist frequency. A fully differential comparator design and decoding circuitry reduce out-ofsequence code errors (thermometer bubbles or sparkle codes) and provide excellent metastable performance of one error per $10^{16}$ clock cycles. Unlike other ADCs that can have errors resulting in false full- or zero-scale outputs, the MAX104 limits the error magnitude to 1LSB.
The analog input is designed for either differential or single-ended use with a $\pm 250 \mathrm{mV}$ input voltage range. Dual, differential, PECL-compatible output data paths ensure easy interfacing and include an 8:16 demultiplexer feature that reduces output data rates to one-half the sampling clock rate. The PECL outputs can be operated from any supply between +3 V to +5 V for compatibility with +3.3 V or +5 V referenced systems. Control inputs are provided for interleaving additional MAX104 devices to increase the effective system sampling rate.
The MAX104 is packaged in a $25 \mathrm{~mm} \times 25 \mathrm{~mm}$, 192-contact Enhanced Super-Ball Grid Array (ESBGA ${ }^{\top M}$ ) and is specified over the commercial $\left(0^{\circ} \mathrm{C}\right.$ to $\left.+70^{\circ} \mathrm{C}\right)$ temperature range.

Applications<br>Digital RF/IF Signal Processing<br>Direct RF Downconversion<br>High-Speed Data Acquisition<br>Digital Oscilloscopes<br>High-Energy Physics<br>Radar/Sonar/ECM Systems<br>ATE Systems

Typical Operating Circuit appears at end of data sheet.

ESBGA is a trademark of Amkor/Anam.

Features

- 1Gsps Conversion Rate
- 2.2GHz Full-Power Analog Input Bandwidth
- >7.5 Effective Bits at $\mathrm{fin}=500 \mathrm{MHz}$ (Nyquist Frequency)
- $\pm 0.25$ LSB INL and DNL
- $50 \Omega$ Differential Analog Inputs
- $\pm 250 \mathrm{mV}$ Input Signal Range
- On-Chip, +2.5V Precision Bandgap Voltage Reference
- Latched, Differential PECL Digital Outputs
- Low Error Rate: 10-16 Metastable States at 1Gsps
- Selectable 8:16 Demultiplexer
- Internal Demux Reset Input with Reset Output
- 192-Contact ESBGA Package

Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE |
| :---: | :---: | :--- |
| MAX 104 CHC | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 192 ESBGA |

## 192-Contact ESBGA Ball Assignment Matrix



# $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 

## ABSOLUTE MAXIMUM RATINGS




Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

$\left(\mathrm{V}_{\mathrm{CC}} \mathrm{A}=\mathrm{V}_{\mathrm{CCI}}=\mathrm{V}_{\mathrm{CC}} \mathrm{D}=+5.0 \mathrm{~V} \pm 5 \%, \mathrm{~V}_{\mathrm{EE}}=-5.0 \mathrm{~V} \pm 5 \%, \mathrm{~V}_{\mathrm{CCO}}=+3.0 \mathrm{~V}\right.$ to $\mathrm{V}_{\mathrm{CC}} \mathrm{D}$, REFIN connected to REFOUT, $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}$ to $\mathrm{T}_{\mathrm{MAX}}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ACCURACY |  |  |  |  |  |  |
| Resolution | RES |  | 8 |  |  | Bits |
| Integral Nonlinearity (Note 1) | INL | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -0.5 | $\pm 0.25$ | 0.5 | LSB |
| Differential Nonlinearity (Note 1) | DNL | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -0.5 | $\pm 0.25$ | 0.5 | LSB |
| Missing Codes |  | No missing codes guaranteed |  |  | None | Codes |
| ANALOG INPUTS |  |  |  |  |  |  |
| Full-Scale Input Range | $\mathrm{V}_{\text {FSR }}$ | Note 1 | 475 | 500 | 525 | mVp-p |
| Common-Mode Input Range | $\mathrm{V}_{\text {CM }}$ | Signal + offset w.r.t. GNDI |  | $\pm 0.8$ |  | V |
| Input Resistance | Rin | VIN+ and VIN- to GNDI, $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | 49 | 50 | 51 | $\Omega$ |
| Input Resistance Temperature Coefficient | TCR |  |  | 150 |  | ppm $/{ }^{\circ} \mathrm{C}$ |
| VOS ADJUST CONTROL INPUT |  |  |  |  |  |  |
| Input Resistance (Note 2) | Rvos |  | 14 | 25 |  | $\mathrm{k} \Omega$ |
| Input Vos Adjust Range |  | VOSADJ = 0 to 2.5 V | $\pm 4$ | $\pm 5.5$ |  | LSB |
| REFERENCE INPUT AND OUTPUT |  |  |  |  |  |  |
| Reference Output Voltage | REFOUT | Driving REFIN input only | 2.475 | 2.50 | 2.525 | V |
| Reference Output Load Regulation | $\triangle$ REFOUT | $0<$ ISOURCE $<2.5 \mathrm{~mA}$ |  |  | 5 | mV |
| Reference Input Resistance | RREF | Referenced to GNDR | 4 | 5 |  | $\mathrm{k} \Omega$ |

## $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

DC ELECTRICAL CHARACTERISTICS (continued)
$\left(\mathrm{V}_{C C} \mathrm{~A}=\mathrm{V}_{C C} \mathrm{I}=\mathrm{V}_{C C} \mathrm{D}=+5.0 \mathrm{~V} \pm 5 \%, \mathrm{~V}_{E E}=-5.0 \mathrm{~V} \pm 5 \%, \mathrm{~V}_{C C O}=+3.0 \mathrm{~V}\right.$ to $\mathrm{V}_{C C} \mathrm{D}$, REFIN connected to REFOUT, $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}$ to $\mathrm{T}_{\mathrm{MAX}}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CLOCK INPUTS (Note 3) |  |  |  |  |  |  |
| Clock Input Resistance | RCLK | CLK+ and CLK- to CLKCOM, $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | 48 | 50 | 52 | $\Omega$ |
| Input Resistance Temperature Coefficient | TCR |  |  | 150 |  | ppm $/{ }^{\circ} \mathrm{C}$ |

TTL/CMOS CONTROL INPUTS (DEMUXEN, DIVSELECT)

| High-Level Input Voltage | VIH |  | 2.0 |  |  | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Low-Level Input Voltage | VIL |  |  |  | 0.8 | V |
| High-Level Input Current | IIH | $\mathrm{V}_{\mathrm{IH}}=2.4 \mathrm{~V}$ |  |  | 50 | $\mu \mathrm{A}$ |
| Low-Level Input Current | IIL | V IL $=0$ | -1 |  | 1 | $\mu \mathrm{A}$ |
| DEMUX RESET INPUT (Note 4) |  |  |  |  |  |  |
| Digital Input High Voltage | VIH |  | -1.165 |  |  | V |
| Digital Input Low Voltage | VIL |  |  |  | -1.475 | V |
| PECL DIGITAL OUTPUTS (Note 5) |  |  |  |  |  |  |
| Digital Output High Voltage | VOH |  | -1.025 |  | -0.880 | V |
| Digital Output Low Voltage | VOL |  | -1.810 |  | -1.620 | V |
| POWER REQUIREMENTS |  |  |  |  |  |  |
| Positive Analog Supply Current | IccA |  |  | 480 | 780 | mA |
| Positive Input Supply Current | Iccl |  |  | 108 | 150 | mA |
| Negative Input Supply Current | IEE |  | -290 | -210 |  | mA |
| Digital Supply Current | IccD |  |  | 205 | 340 | mA |
| Output Supply Current (Note 6) | IccO |  |  | 75 | 115 | mA |
| Power Dissipation (Note 6) | PDISS |  |  | 5.25 |  | W |
| Common-Mode Rejection Ratio (Note 7) | CMRR | $\mathrm{VIN}+=\mathrm{VIN}-= \pm 0.1 \mathrm{~V}$ | 40 | 68 |  | dB |
| Positive Power-Supply Rejection Ratio (Note 8) | PSRR+ | (Note 9) | 40 | 73 |  | dB |
| Negative Power-Supply Rejection Ratio (Note 8) | PSRR- | (Note 10) | 40 | 68 |  | dB |

## $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

## AC ELECTRICAL CHARACTERISTICS

$\left(\mathrm{V}_{\mathrm{CC}} \mathrm{A}=\mathrm{V}_{\mathrm{CC}} \mathrm{I}=\mathrm{V}_{\mathrm{CC}} \mathrm{D}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CCO}}=+3.3 \mathrm{~V}\right.$, REFIN connected to REFOUT, fS $=1 \mathrm{Gsps}, \mathrm{f}_{\mathrm{IN}}$ at $-1 \mathrm{dBFS}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS |  | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ANALOG INPUT |  |  |  |  |  |  |  |
| Analog Input Full-Power Bandwidth | BW-3dB |  |  |  | 2.2 |  | GHz |
| Analog Input VSWR | VSWR | $\mathrm{fiN}^{\text {a }}$ = 500MHz |  | 1.1:1 |  |  | V/V |
| Transfer Curve Offset | Vos | VOSADJ control input open |  | -1.5 | 0 | +1.5 | LSB |
| DYNAMIC SPECIFICATIONS |  |  |  |  |  |  |  |
| Effective Number of Bits (Note 11) | ENOB1000 | $\mathrm{f} / \mathrm{N}=1000 \mathrm{MHz}$ | Differential |  | 7.52 |  | Bits |
|  |  |  | Single-ended |  | 7.40 |  |  |
|  | ENOB500 | $\mathrm{fIN}=500 \mathrm{MHz}$ | Differential | 7.2 | 7.55 |  |  |
|  |  |  | Single-ended |  | 7.49 |  |  |
|  | ENOB125 | $\mathrm{fIN}=125 \mathrm{MHz}$ | Differential | 7.4 | 7.74 |  |  |
|  |  |  | Single-ended |  | 7.73 |  |  |
| Signal-to-Noise Ratio (No Harmonics) | SNR1000 | $\mathrm{f} / \mathrm{N}=1000 \mathrm{MHz}$ | Differential |  | 46.4 |  | dB |
|  |  |  | Single-ended |  | 46.4 |  |  |
|  | SNR500 | $\mathrm{fIN}=500 \mathrm{MHz}$ | Differential | 43.5 | 47.0 |  |  |
|  |  |  | Single-ended |  | 47.1 |  |  |
|  | SNR125 | $\mathrm{fin}^{\mathrm{I}}=125 \mathrm{MHz}$ | Differential | 44.2 | 47.4 |  |  |
|  |  |  | Single-ended |  | 47.4 |  |  |
| Total Harmonic Distortion (Note 12) | THD 1000 | $\mathrm{f}_{\mathrm{IN}}=1000 \mathrm{MHz}$ | Differential |  | -52.6 |  | dB |
|  |  |  | Single-ended |  | -49.6 |  |  |
|  | THD500 | $\mathrm{fin}^{\prime}=500 \mathrm{MHz}$ | Differential | -50 | -52.5 |  |  |
|  |  |  | Single-ended |  | -51.3 |  |  |
|  | THD ${ }_{125}$ | $\mathrm{fin}^{\mathrm{N}}=125 \mathrm{MHz}$ | Differential | -61 | -66.2 |  |  |
|  |  |  | Single-ended |  | -67.4 |  |  |
| Spurious-Free Dynamic Range | SFDR1000 | $\mathrm{f} \mathrm{N}=1000 \mathrm{MHz}$ | Differential |  | 52.8 |  | dB |
|  |  |  | Single-ended |  | 52.5 |  |  |
|  | SFDR500 | $\mathrm{fin}^{\mathrm{N}}=500 \mathrm{MHz}$ | Differential | 50 | 52.3 |  |  |
|  |  |  | Single-ended |  | 52.3 |  |  |
|  | $\mathrm{SFDR}_{125}$ | $\mathrm{fin}^{\prime}=125 \mathrm{MHz}$ | Differential | 62 | 68.9 |  |  |
|  |  |  | Single-ended |  | 69.5 |  |  |
| Signal-to-Noise Ratio and Distortion (Note 11) | SINAD1000 | $\mathrm{f} \mathrm{I}=1000 \mathrm{MHz}$ | Differential |  | 47.0 |  | dB |
|  |  |  | Single-ended |  | 46.3 |  |  |
|  | SINAD500 | $\mathrm{fin}^{\prime}=500 \mathrm{MHz}$ | Differential | 45.1 | 47.2 |  |  |
|  |  |  | Single-ended |  | 46.9 |  |  |
|  | SINAD ${ }_{125}$ | $\mathrm{fin}^{\prime}=125 \mathrm{MHz}$ | Differential | 46.3 | 48.3 |  |  |
|  |  |  | Single-ended |  | 48.3 |  |  |
| Two-Tone Intermodulation | IMD | $\mathrm{f}_{\mathrm{I}} \mathrm{N} 1=124 \mathrm{MHz}, \mathrm{f}_{\mathrm{I}} \mathrm{N} 2=126 \mathrm{MHz}$, at -7 dB below full-scale |  |  | -57.7 |  | dB |

# $\pm 5 \mathrm{~V}, 1$ Gsps, 8 -Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 

## AC ELECTRICAL CHARACTERISTICS (continued)

$\left(\mathrm{V}_{\mathrm{CC}} \mathrm{A}=\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CC}} \mathrm{D}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CCO}}=+3.3 \mathrm{~V}\right.$, REFIN connected to REFOUT, fS $=1 \mathrm{Gsps}, \mathrm{f}_{\mathrm{IN}}$ at $-1 \mathrm{dBFS}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS |  | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TIMING CHARACTERISTICS |  |  |  |  |  |  |  |
| Maximum Sample Rate | fmax |  |  | 1 |  |  | Gsps |
| Clock Pulse Width Low | tPWL | Figure 17 |  | 0.45 |  |  | ns |
| Clock Pulse Width High | tpWH | Figure 17 |  | 0.45 |  | 5 | ns |
| Aperture Delay | tad | Figure 4 |  |  | 100 |  | ps |
| Aperture Jitter | $t_{\text {AJ }}$ | Figure 4 |  |  | <0.5 |  | ps |
| Reset Input Data Setup Time (Note 13) | tsu | Figure 15 |  | 0 |  |  | ps |
| Reset Input Data Hold Time (Note 13) | thD | Figure 15 |  | 0 |  |  | ps |
| CLK to DREADY Propagation Delay | tpD1 | Figure 17 |  | 2.2 |  |  | ns |
| DREADY to DATA Propagation Delay (Note 14) | tPD2 | Figure 17 |  | -50 | 150 | 350 | ps |
| DATA Rise Time | tRDATA | 20\% to $80 \%, C_{L}=3 p F$ |  |  | 420 |  | ps |
| DATA Fall Time | tFDATA | 20\% to $80 \%, C_{L}=3 p F$ |  |  | 360 |  | ps |
| DREADY Rise Time | trDREADY | 20\% to $80 \%, C L=3 p F$ |  |  | 220 |  | ps |
| DREADY Fall Time | tfdready | 20\% to $80 \%, C_{L}=3 p F$ |  |  | 180 |  | ps |
| Primary Port Pipeline Delay | tpDP | Figures 6, 7, 8 | DIV1, DIV2 modes |  | 7.5 |  | Clock Cycles |
|  |  |  | DIV4 mode |  | 7.5 |  |  |
| Auxiliary Port Pipeline Delay | tPDA | Figures 6, 7, 8 | DIV1, DIV2 modes |  | 8.5 |  | Clock Cycles |
|  |  |  | DIV4 mode |  | 9.5 |  |  |

Note 1: Static linearity parameters are computed from a "best-fit" straight line through the code transition points. The full-scale range (FSR) is defined as $256 \cdot$ slope of the line.
Note 2: The offset control input is a self-biased voltage divider from the internal +2.5 V reference voltage. The nominal open-circuit voltage is +1.25 V . It may be driven from an external potentiometer connected between REFOUT and GNDI.
Note 3: The clock input's termination voltage can be operated between -2.0 V and GNDI. Observe the absolute maximum ratings on the CLK+ and CLK- inputs.
Note 4: Input logic levels are measured with respect to the VccO power-supply voltage.
Note 5: All PECL digital outputs are loaded with $50 \Omega$ to $\mathrm{V}_{\mathrm{Cc}} \mathrm{O}-2.0 \mathrm{~V}$. Measurements are made with respect to the $\mathrm{V}_{\mathrm{cc}} \mathrm{O}$ powersupply voltage.
Note 6: The current in the $\mathrm{V}_{\mathrm{CCO}}$ power supply does not include the current in the digital output's emitter followers, which is a function of the load resistance and the $\mathrm{V}_{\mathrm{T}}$ termination voltage.
Note 7: Common-Mode Rejection Ratio is defined as the ratio of the change in the transfer-curve offset voltage to the change in the common-mode voltage, expressed in dB.
Note 8: Power-Supply Rejection Ratio is defined as the ratio of the change in the transfer-curve offset voltage to the change in power-supply voltage, expressed in dB.
Note 9: Measured with the positive supplies tied to the same potential; $\mathrm{V}_{\mathrm{Cc}} \mathrm{A}=\mathrm{V}_{\mathrm{Cc}} \mathrm{D}=\mathrm{V}_{\mathrm{Cc}} \mathrm{I}$. $\mathrm{V}_{\mathrm{Cc}}$ varies from +4.75 V to +5.25 V .
Note 10: VEE varies from -5.25 V to -4.75 V .

# $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 

Note 11: Effective Number of Bits (ENOB) and Signal-to-Noise Plus Distortion (SINAD) are computed from a curve fit referenced to the theoretical full-scale range.
Note 12: Total Harmonic Distortion (THD) is computed from the first five harmonics.
Note 13: Guaranteed by design with a reset pulse one clock period long or greater.
Note 14: The DREADY to DATA propagation delay is measured from the $50 \%$ point on the rising edge of the DREADY signal (when the output data changes) to the $50 \%$ point on a data output bit. This places the falling edge of the DREADY signal in the middle of the data output valid window, within the differences between the DREADY and DATA rise and fall times, which gives maximum setup and hold time for latching external data latches.

Typical Operating Characteristics
$\left(\mathrm{V}_{C C} \mathrm{~A}=\mathrm{V}_{\mathrm{CC}} \mathrm{I}=\mathrm{V}_{\mathrm{CC}} \mathrm{D}=+5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CCO}}=+3.3 \mathrm{~V}\right.$, REFIN connected to REFOUT, fs $=1 \mathrm{Gsps}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.)


## $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

Typical Operating Characteristics (continued)
$\left(\mathrm{VCCA}=\mathrm{VCCI}=\mathrm{VCCD}_{\mathrm{CC}}=+5 \mathrm{~V}\right.$, $\mathrm{V}_{\mathrm{EE}}=-5 \mathrm{~V}, \mathrm{~V} \mathrm{VCO}=+3.3 \mathrm{~V}$, REFIN connected to REFOUT, fs $=1 \mathrm{Gsps}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.)


EFFECTIVE NUMBER OF BITS vs. CLOCK POWER
( $\mathrm{f} / \mathrm{N}=125 \mathrm{MHz},-1 \mathrm{dBFS}$ )


EFFECTIVE NUMBER OF BITS vs. VEE


SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT FREQUENCY (DIFFERENTIAL ANALOG INPUT DRIVE)


EFFECTIVE NUM BER OF BITS vs. CLOCK FREQUENCY ( $\mathrm{f} / \mathrm{N}=125 \mathrm{MHz},-1 \mathrm{dBFS}$ )


EFFECTIVE NUMBER OF BITS
vs. $V_{C C}=V_{C C A}=V_{C C} D$
( $\mathrm{f} / \mathrm{N}=125 \mathrm{MHz},-1 \mathrm{dBFS}$ )


SPURIOUS-FREE DYNAMIC RANGE
vs. CLOCK POWER
( $\mathrm{f} \mathrm{IN}=125 \mathrm{MHz},-1 \mathrm{dBFS}$ )


## $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

## Typical Operating Characteristics (continued)

$\left(\mathrm{V}_{C C A}=\mathrm{V}_{C C I}=\mathrm{V}_{C C D}=+5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CCO}}=+3.3 \mathrm{~V}\right.$, REFIN connected to REFOUT, fS $=1 \mathrm{Gsps}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise
noted.)


FFT PLOT
( f IN $=494.5068 \mathrm{MHz}$, RECORD LENGTH 8192)


ANALOG INPUT BANDWIDTH
-6dB BELOW FULL-SCALE



FFT PLOT
( $\mathrm{f}_{\mathrm{I}}=1005.0049 \mathrm{MHz}$, RECORD LENGTH 8192)


ANALOG INPUT BANDWIDTH
FULL-POWER


ANALOG INPUT FREQUENCY (MHz)

FFT PLOT
( f IN $=125.8545 \mathrm{MHz}$, RECORD LENGTH 8192)


TWO-TONE INTERM ODULATION
FFT PLOT (fin $1=124 \mathrm{MHz}, \mathrm{f} / \mathrm{N} 2=126 \mathrm{MHz}$,
7dB BELOW FULL-SCALE, RECORD LENGTH 8192)


INTEGRAL NONLINEARITY vs. OUTPUT CODE
(LOW-FREQUENCY SERVO LOOP DATA)


8

# $\pm 5 \mathrm{~V}, 1$ Gsps, 8 -Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 

Typical Operating Characteristics (continued)
$\left(\mathrm{VCCA}=\mathrm{V} C \mathrm{Cl}=\mathrm{VCCD}=+5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-5 \mathrm{~V}, \mathrm{~V} C \mathrm{CO}=+3.3 \mathrm{~V}\right.$, REFIN connected to REFOUT, fs $=1 \mathrm{Gsps}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.) DIFFERENTIAL NONLINEARITY vs. OUTPUT CODE (LOW-FREQUENCY SERVO LOOP DATA)





TOTAL HARM ONIC DISTORTION
vs. $V_{C C I}=V_{C C A}=V_{C C} D$
( $\mathrm{f} \mathrm{IN}=125 \mathrm{MHz},-1 \mathrm{dBFS}$ )


Pin Description

| CONTACT | NAME | FUNCTION |
| :---: | :--- | :--- |
| A1-A4, A6, A7, B1, B2, C1, C2, D1, D2, <br> D3, G1, H1, J2, J3, K1-K3, L2, L3, M1, <br> N1, T2, T3, U1, V1, V2, W1-W4 | GNDI | Analog Ground. For T/H amplifier, clock distribution, bandgap <br> reference, and reference amplifier. |
| A5, B5, C5, H2, H3, M2, M3, U5, V5, W5 | VCCl | Analog Supply Voltage, +5V. Supplies T/H amplifier, clock distri- <br> bution, bandgap reference, and reference amplifier. |
| A8, B8, C8, U6, V6, W6 | GNDA | Analog Ground. For comparator array. |
| A9, B9, C9, U7, V7, W7 | VCcA | Analog Supply Voltage, +5V. Supplies analog comparator array. |
| A10, E17, F2, P3, R17, R18 | TESTPOINT (T.P.) | Test Point. Do not connect. |
| A11, B11, B16, B17, C11, C16, U9, U17, <br> V9, V17, V18, W9 | GNDD | Digital Ground |
| A12-A19, B19, C19, D19, E19, F19, <br> G19, H19, J19, K19, L19, M19, N19, <br> P19, T19, U19, V19, W10-W19 | VCCO | PECL Supply Voltage, +3V to +5V |

## $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with <br> On-Chip 2.2GHz Track/Hold Amplifier

Pin Description (continued)

| CONTACT | NAME | FUNCTION |
| :---: | :---: | :---: |
| B3, B4, C3, C4, E3, F3, G2, G3, N2, N3, U2, U3, U4, V3, V4 | Vee | Analog Supply Voltage, -5 V . Supplies T/H amplifier, clock distribution, bandgap reference, and reference amplifier. |
| B6, B7 | GNDR | Reference Ground. Must be connected to GNDI. |
| B10, B18, C10, C17, C18, T17, T18, U8, U18, V8, W8 | $\mathrm{V}_{\mathrm{cc}} \mathrm{D}$ | Digital Supply Voltage, +5 V |
| B12 | P0+ | Primary Output Data Bit 0 (LSB) |
| B13 | A0+ | Auxiliary Output Data Bit 0 (LSB) |
| B14 | P1+ | Primary Output Data Bit 1 |
| B15 | A1+ | Auxiliary Output Data Bit 1 |
| C6 | REFIN | Reference Input |
| C7 | REFOUT | Reference Output |
| C12 | P0- | Complementary Primary Output Data Bit 0 (LSB) |
| C13 | A0- | Complementary Auxiliary Output Data Bit 0 (LSB) |
| C14 | P1- | Complementary Primary Output Data Bit 1 |
| C15 | A1- | Complementary Auxiliary Output Data Bit 1 |
| D17 | DIVSELECT | TTL/CMOS Demux Divide Selection Input <br> 1: Decimation DIV4 mode <br> 0: Demultiplexed DIV2 mode |
| D18 | AUXEN2 | Tie to $\mathrm{V}_{\mathrm{CCO}}$ to power the auxiliary port. Tie to GNDD to power down. |
| E1 | ICONST | Die Temperature Measurement Test Point. See Die Temperature Measurement section. |
| E2 | IPTAT | Die Temperature Measurement Test Point. See Die Temperature Measurement section. |
| E18 | DEMUXEN | TTL/CMOS Demux Enable Control <br> 1: Enable Demux <br> 0: Disable Demux |
| F1 | VOSADJ | Offset Adjust Input |
| F17 | P2- | Complementary Primary Output Data Bit 2 |
| F18 | P2+ | Primary Output Data Bit 2 |
| G17 | A2- | Complementary Auxiliary Output Data Bit 2 |
| G18 | A2+ | Auxiliary Output Data Bit 2 |
| H17 | P3- | Complementary Primary Output Data Bit 3 |
| H18 | P3+ | Primary Output Data Bit 3 |

# $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 

Pin Description (continued)

| CONTACT | NAME | FUNCTION |
| :---: | :---: | :---: |
| J1 | VIN- | Differential Input Voltage (-) |
| J17 | А3- | Complementary Auxiliary Output Data Bit 3 |
| J18 | A3+ | Auxiliary Output Data Bit 3 |
| K17 | DREADY- | Complementary Data-Ready Clock |
| K18 | DREADY+ | Data-Ready Clock |
| L1 | VIN+ | Differential Input Voltage (+) |
| L17 | P4- | Complementary Primary Output Data Bit 4 |
| L18 | P4+ | Primary Output Data Bit 4 |
| M17 | A4- | Complementary Auxiliary Output Data Bit 4 |
| M18 | A4+ | Auxiliary Output Data Bit 4 |
| N17 | P5- | Complementary Primary Output Data Bit 5 |
| N18 | P5+ | Primary Output Data Bit 5 |
| P1 | CLK- | Complementary Sampling-Clock Input |
| P2 | TESTPOINT (T.P.) | This contact must be connected to GNDI. |
| P17 | A5- | Complementary Auxiliary Output Data Bit 5 |
| P18 | A5+ | Auxiliary Output Data Bit 5 |
| R1, R2, R3 | CLKCOM | $50 \Omega$ Clock Termination Return |
| R19 | AUXEN1 | Tie to VccO to power the auxiliary port. Tie to GNDD to power down. |
| T1 | CLK + | Sampling Clock Input |
| U10 | RSTIN- | Complementary PECL Demux Reset Input |
| U11 | RSTOUT- | Complementary PECL Reset Output |
| U12 | OR- | Complementary PECL Overrange Bit |
| U13 | A7- | Complementary Auxiliary Output Data Bit 7 (MSB) |
| U14 | P7- | Complementary Primary Output Data Bit 7 (MSB) |
| U15 | A6- | Complementary Auxiliary Output Data Bit 6 |
| U16 | P6- | Complementary Primary Output Data Bit 6 |
| V10 | RSTIN+ | PECL Demux Reset Input |
| V11 | RSTOUT+ | PECL Reset Output |
| V12 | OR+ | PECL Overrange Bit |
| V13 | A7+ | Auxiliary Output Data Bit 7 (MSB) |
| V14 | P7+ | Primary Output Data Bit 7 (MSB) |
| V15 | A6+ | Auxiliary Output Data Bit 6 |
| V16 | P6+ | Primary Output Data Bit 6 |

# $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 



Figure 1. Simplified Functional Diagram

## Detailed Description

The MAX104 is an 8-bit, 1Gsps flash analog-to-digital converter (ADC) with on-chip track/hold (T/H) amplifier and differential PECL-compatible outputs. The ADC (Figure 1) employs a fully differential 8-bit quantizer and a unique encoding scheme to limit metastable states to typically one error per $10^{16}$ clock cycles, with no error exceeding 1LSB max.
An integrated 8:16 output demultiplexer simplifies interfacing to the part by reducing the output data rate to one-half the sampling clock rate. This demultiplexer has internal reset capability that allows multiple

MAX104s to be time-interleaved to achieve higher effective sampling rates.
When clocked at 1Gsps, the MAX104 provides a typical effective number of bits (ENOB) of $>7.5$ bits at an analog input frequency of 500 MHz . The analog input of the MAX104 is designed for differential or single-ended use with a $\pm 250 \mathrm{mV}$ full-scale input range. In addition, this ADC features an on-chip +2.5 V precision bandgap reference. If desired, an external reference can also be used.

# $\pm 5 \mathrm{~V}, 1$ Gsps, 8 -Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 

## Princ iple of Operation

The MAX104's flash or parallel architecture provides the fastest multibit conversion of all common integrated ADC designs. The key to this high-speed flash architecture is the use of an innovative, high-performance comparator design. The flash converter and downstream logic translate the comparator outputs into a parallel 8 -bit output code and pass this binary code on to the optional 8:16 demultiplexer, where primary and auxiliary ports output PECL-compatible data at up to 500 Msps per port (depending on how the demultiplexer section is set on the MAX104).
The ideal transfer function appears in Figure 2.

## On-Chip Track/Hold Amplifier

As with all ADCs, if the input waveform is changing rapidly during conversion, effective number of bits (ENOB) and signal-to-noise ratio (SNR) specifications will degrade. The MAX104's on-chip, wide-bandwidth (2.2GHz) T/H amplifier reduces this effect and increases the ENOB performance significantly, allowing precise capture of fast analog data at high conversion rates.
The T/H amplifier buffers the input signal and allows a full-scale signal input range of $\pm 250 \mathrm{mV}$. The T/H amplifier's differential $50 \Omega$ input termination simplifies interfacing to the MAX104 with controlled impedance lines. Figure 3 shows a simplified diagram of the T/H amplifier stage internal to the MAX104.
Aperture width, delay, and jitter (or uncertainty) are parameters that affect the dynamic performance of high-speed converters. Aperture jitter, in particular, directly influences SNR and limits the maximum slew rate ( $\mathrm{dV} / \mathrm{dt}$ ) that can be digitized without contributing significant errors. The MAX104's innovative T/H amplifier design limits aperture jitter typically to less than 0.5ps.

## Aperture Width

Aperture width ( $\mathrm{t} A \mathrm{AW}$ ) is the time the $\mathrm{T} / \mathrm{H}$ circuit requires (Figure 4) to disconnect the hold capacitor from the input circuit (for instance, to turn off the sampling bridge and put the $\mathrm{T} / \mathrm{H}$ unit in hold mode).

## Aperture Jitter

Aperture jitter (tAJ) is the sample-to-sample variation (Figure 4) in the time between the samples.

## Aperture Delay

Aperture delay ( $t_{A D}$ ) is the time defined between the rising edge of the sampling clock and the instant when an actual sample is taken (Figure 4).

## Internal Reference

The MAX104 features an on-chip +2.5 V precision bandgap reference, which can be used by connecting


Figure 2. Transfer Function


Figure 3. Internal Structure of the 2.2 GHz T/H Amplifier


Figure 4. T/H Aperture Timing

# $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 

REFOUT to REFIN. This connects the reference output to the positive input of the reference buffer. The buffer's negative input is internally connected to GNDR. GNDR must be connected to GNDI on the user's application board. REFOUT can source up to 2.5 mA to supply external devices if required.
An adjustable external reference can be used to adjust the ADC's full-scale range. To use an external reference supply, simply connect a high-precision reference to the REFIN pin and leave the REFOUT pin floating. In this configuration, REFOUT must not be simultaneously connected to avoid conflicts between the two references. REFIN has a typical input resistance of $5 \mathrm{k} \Omega$ and accepts input voltages of $+2.5 \mathrm{~V} \pm 200 \mathrm{mV}$. Using the MAX104's internal reference is recommended for best performance.

## Digital Outputs

The MAX104 provides data in offset binary format to differential PECL outputs. A simplified circuit schematic of the PECL output cell is shown in Figure 5. All PECL outputs are powered from $\mathrm{V}_{\mathrm{CCO}}$, which may be operated from any voltage between +3.0 V to VccD for flexible interfacing with either +3.3 V or +5 V systems. The nominal $\mathrm{V}_{\mathrm{CCO}}$ supply voltage is +3.3 V .
All PECL outputs on the MAX104 are open-emitter types and must be terminated at the far end of each transmission line with $50 \Omega$ to $\mathrm{VCCO}-2 \mathrm{~V}$. Table 1 lists all MAX104 PECL outputs and their functions.


Figure 5. Simplified PECL Output Structure

## Demultiplexer Operation

The MAX104 features an internal data demultiplexer that provides for three different modes of operation (see the following sections on Demultiplexed DIV2 Mode, Non-Demultiplexed DIV1 Mode, and Decimation DIV4 Mode) controlled by two TTL/CMOS-compatible inputs: DEMUXEN and DIVSELECT.
DEMUXEN enables or disables operation of the internal 1:2 demultiplexer. A logic high on DEMUXEN activates the internal demultiplexer, and a logic low deactivates it. With the internal demultiplexer enabled, DIVSELECT controls the selection of the operational mode. DIVSELECT low selects demultiplexed DIV2 mode, and DIVSELECT high selects decimation DIV4 mode (Table 2).

## Table 1. PECL Output Functions

| PECL OUTPUT SIGNALS | FUNCTIONAL DESCRIPTION |
| :---: | :--- |
| P0+, P0-, P1+, P1-, P2+, P2-, <br> P3+, P3-, P4+, P4-, P5+, P5-, <br> P6+, P6-, P7+, P7- | Primary-Port Differential Outputs from LSB to MSB. A "+" indicates the true outputs; a "-" <br> denotes the complementary outputs. |
| A0+, A0-, A1+, A1-, A2+, A2-, <br> A3+, A3-, A4+, A4-, A5+, A5-, <br> A6+, A6-, A7+, A7-- | Auxiliary-Port Differential Outputs from LSB to MSB. A "+" indicates the true outputs; a "-" <br> denotes the complementary outputs. |
| DREADY+, DREADY- | Data-Ready Clock True and Complementary Outputs. These signal lines are used to latch <br> the output data from the primary to the auxiliary output ports. Data changes on the rising <br> edge of the DREADY clock. |
| OR+, OR- | Overrange True and Complementary Outputs |
| RSTOUT+, RSTOUT- | Reset Output True and Complementary Outputs |

# $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 

Non-Demultiplexed DIV1 Mode The MAX104 may be operated at up to 500 Msps in nondemultiplexed DIV1 mode (Table 2). In this mode, the internal demultiplexer is disabled, and sampled data is presented to the primary port only, with the data repeated at the auxiliary port but delayed by one clock cycle (Figure 6). Since the auxiliary output port contains the same data stream as the primary output port, the auxiliary port can be shut down to save power by connecting AUXEN1 and AUXEN2 to digital ground (GNDD). This powers down the internal bias cells and causes both outputs (true and complementary) of the auxiliary port to pull up to a logic-high level. To save additional power, the external $50 \Omega$ termination resistors connected to the

PECL termination power supply (VccO-2V) may be removed from all auxiliary output ports.

## Demultiplexed DIV2 Mode

 The MAX104 features an internally selectable DIV2 mode (Table 2) that reduces the output data rate to one-half of the sample clock rate. The demultiplexed outputs are presented in dual 8 -bit format with two consecutive samples appearing in the primary and auxiliary output ports on the rising edge of the data-ready clock (Figure 7). The auxiliary data port contains the previous sample, and the primary output contains the most recent data sample. AUXEN1 and AUXEN2 must be connected to VccO to power-up the auxiliary port PECL output drivers.

Figure 6. Non-Demuxed, DIV1-Mode Timing Diagram


NOTE: THE LATENCY TO THE PRIMARY PORT IS 7.5 CLOCK CYCLES, AND THE LATENCY TO THE AUXILIARY PORT IS 8.5 CLOCK CYCLES BOTH THE PRIMARY AND AUXILIARY DATA PORTS ARE UPDATED ON THE RISING EDGE OF THE DREADY+ CLOCK

Figure 7. Demuxed DIV2-Mode Timing Diagram

# $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 

## Decimation DIV4 Mode

The MAX104 also offers a special decimated, demultiplexed output (Figure 8) that discards every other input sample and outputs data at one-quarter the input sampling rate for system debugging at slower output data rates. With an input clock of 1 GHz , the effective output data rate will be reduced to 250 MHz per output port in the DIV4 mode (Table 2). Since every other sample is discarded, the effective sampling rate is 500 Msps .

## Overrange Operation

A single differential PECL overrange output bit (OR+, OR-) is provided for both primary and auxiliary demultiplexed outputs. The operation of the overrange bit depends on the status of the internal demultiplexer. In demultiplexed DIV2 mode and decimation DIV4 mode,
the OR bit will flag an overrange condition if either the primary or auxiliary port contains an overranged sample (Table 2). In non-demultiplexed DIV1 mode, the OR port will flag an overrange condition only when the primary output port contains an overranged sample.

## Applications Information

Single-Ended Analog Inputs
The MAX104 T/H amplifier is designed to work at full speed for both single-ended and differential analog inputs (Figure 9). Inputs VIN+ and VIN- feature on-chip, laser-trimmed $50 \Omega$ termination resistors to provide excellent voltage standing wave ratio (VSWR) performance.


Figure 8. Decimation DIV4-Mode Timing Diagram

Table 2. Demultiplexer Operation

| DEMUXEN | DIVSELECT | DEMUX MODE | OVERRANGE BIT OPERATION |
| :---: | :---: | :---: | :---: |
| Low | X | DIV1 <br> $500 \mathrm{Msps}(\mathrm{max})$ | Flags overrange data appearing in primary <br> port only. |
| High | Low | DIV2 <br> $500 \mathrm{Msps} /$ port | Flags overrange data appearing in either <br> the primary or auxiliary port. |
| High | High | DIV4 <br> $250 \mathrm{Msps} /$ port |  |

[^0]
# $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 



Figure 9. Simplified Analog Input Structure (Single-Ended/ Differential)

In a typical single-ended configuration, the analog input signal (Figure 10a) enters the T/H amplifier stage at the in-phase input ( $\mathrm{VIN}+$ ), while the inverted phase input (VIN-) is reverse-terminated to GNDI with an external $50 \Omega$ resistor. Single-ended operation allows for an input amplitude of $\pm 250 \mathrm{mV}$. Table 3 shows a selection of input voltages and their corresponding output codes for single-ended operation.

Differential Analog Inputs
To obtain a full-scale digital output with differential input drive (Figure 10b), 250mVp-p must be applied between $\mathrm{VIN}+$ and $\mathrm{VIN}-(\mathrm{VIN}+=+125 \mathrm{mV}$ and $\mathrm{VIN}-=-125 \mathrm{mV})$. Midscale digital output codes (01111111 or 10000000) occur when there is no voltage difference between $\mathrm{VIN}+$ and VIN -. For a zero-scale digital output code, the


Figure 10a. Single-Ended Analog Input Signals


Figure 10b. Differential Analog Input Signals
in-phase ( $\mathrm{VIN}+$ ) input must see -125 mV and the inverted input (VIN-) must see +125 mV . A differential input drive is recommended for best performance. Table 4 represents a selection of differential input voltages and their corresponding output codes.

Table 3. Ideal Input Voltage and Output Code Results for Single-Ended Operation

| VIN + | VIN- | OVERRANGE BIT | OUTPUT CODE |
| :---: | :---: | :---: | :---: |
| +250 mV | 0 V | 1 | 11111111 (full scale) |
| $+250 \mathrm{mV}-1 \mathrm{LSB}$ | 0 V | 0 | 11111111 |
| 0 V | 0 V | 0 | 01111111 <br> toggles <br> 10000000 |
| $-250 \mathrm{mV}+1 \mathrm{LSB}$ | 0 V | 0 | 0000001 |
| -250 mV | 0 V | 0 | 00000000 (zero scale) |

# $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 

Table 4. Ideal Input Voltage and Output Code Results for Differential Operation

| VIN + | VIN- | OVERRANGE BIT | OUTPUT CODE |
| :---: | :---: | :---: | :---: |
| +125 mV | -125 mV | 1 | 11111111 (full scale) |
| $+125 \mathrm{mV}-0.5 \mathrm{LSB}$ | $-125 \mathrm{mV}+0.5 \mathrm{LSB}$ | 0 | 11111111 |
| 0 V | 0 V | 0 | 01111111 |
| toggles |  |  |  |
|  |  | 0 | 0000000 |
| $-125 \mathrm{mV}+0.5 \mathrm{LSB}$ | $+125 \mathrm{mV}-0.5 \mathrm{LSB}$ | 0 | 00000001 |
| -125 mV | +125 mV | 00000000 (zero scale) |  |

## Offset Adjust

The MAX104 provides a control input (VOSADJ) to compensate for system offsets. The offset adjust input is a self-biased voltage divider from the internal +2.5 V precision reference. The nominal open-circuit voltage is onehalf the reference voltage. With an input resistance of typically $25 \mathrm{k} \Omega$, this pin may be driven by an external $10 \mathrm{k} \Omega$ potentiometer (Figure 11) connected between REFOUT and GNDI to correct for offset errors. This control provides a typical $\pm 5.5 \mathrm{LSB}$ offset adjustment range.

Clock Operation The MAX104 clock inputs are designed for either singleended or differential operation (Figure 12) with flexible input drive requirements. Each clock input is terminated with an on-chip, laser-trimmed $50 \Omega$ resistor to CLKCOM (clock-termination return). The CLKCOM termination voltage can be connected anywhere between ground and -2 V for compatibility with standard ECL drive levels.
The clock inputs are internally buffered with a preamplifier to ensure proper operation of the data converter with even small-amplitude sine-wave sources. The MAX104 was designed for single-ended, low-phasenoise sine-wave clock signals with as little as 100 mV amplitude $(-10 \mathrm{dBm})$. This eliminates the need for an external ECL clock buffer and its added jitter.

Single-Ended Clock Inputs (Sine-Wave Drive) Excellent performance is obtained by AC- or DC-coupling a low-phase-noise sine-wave source into a single clock input (Figure 13a, Table 5). For proper DC balance, the undriven clock input should be externally $50 \Omega$ reverse-terminated to GNDI.
The dynamic performance of the data converter is essentially unaffected by clock-drive power levels from


Figure 11. Offset Adjust with External 10k $\Omega$ Potentiometer


Figure 12. Simplified Clock Input Structure (Single-Ended/ Differential)

# $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 

$-10 \mathrm{dBm}(100 \mathrm{mV}$ clock signal amplitude) to $+10 \mathrm{dBm}$ (1V clock signal amplitude). The MAX104 dynamic performance specifications are determined by a singleended clock drive of $+4 \mathrm{dBm}(500 \mathrm{mV}$ clock signal amplitude). To avoid saturation of the input amplifier stage, limit the clock power level to a maximum of +10 dBm .

Differential Clock Inputs (Sine-Wave Drive) The advantages of differential clock drive (Figure 13b, Table 5) can be obtained by using an appropriate balun or transformer to convert single-ended sine-wave sources into differential drives. The precision on-chip, laser-trimmed $50 \Omega$ clock-termination resistors ensure excellent amplitude matching. Refer to Single-Ended Clock Inputs (Sine-Wave Drive) for proper input amplitude requirements.


Figure 13a. Single-Ended Clock Input Signals


Figure 13c. Single-Ended ECL Clock Drive

## Single-Ended Clock Inputs (ECL Drive)

Configure the MAX104 for single-ended ECL clock drive by connecting the clock inputs as shown in Figure 13c (Table 5). A well bypassed VBB supply ( -1.3 V ) is essential to avoid coupling noise into the undriven clock input, which would degrade dynamic performance.

Differential Clock Inputs (ECL Drive) The MAX104 may be driven from a standard differential (Figure 13d, Table 5) ECL clock source by setting the clock termination voltage at CLKCOM to -2V. Bypass the clock-termination return (CLKCOM) as close as possible to the ADC with a $0.01 \mu \mathrm{~F}$ capacitor connected to GNDI.

AC-Coupling Clock Inputs The clock inputs CLK+ and CLK- can also be driven with positive referenced ECL (PECL) logic if the clock


NOTE: CLKCOM = OV

Figure 13b. Differential Clock Input Signals


NOTE: CLKCOM $=-2 \mathrm{~V}$

Figure 13d. Differential ECL Clock Drive

# $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 

## Table 5. DC-Coupled Clock Drive Options

| CLOCK DRIVE | CLK+ | CLK- | CLKCOM | REFERENCE |
| :--- | :---: | :---: | :---: | :--- |
| Single-Ended Sine Wave | -10 dBm to +4 dBm | External $50 \Omega$ to GNDI | GNDI | Figure 13a |
| Differential Sine Wave | -10 dBm to +4 dBm | -10 dBm to +4 dBm | GNDI | Figure 13b |
| Single-Ended ECL | ECL Drive | -1.3 V | -2 V | Figure 13c |
| Differential ECL | ECL Drive | $\overline{\text { ECL Drive }}$ | -2 V | Figure 13d |

inputs are AC-coupled. Under this condition, connect CLKCOM to GNDI. Single-ended ECL/PECL/sine-wave drive is also possible if the undriven clock input is reverse-terminated to GNDI through a $50 \Omega$ resistor in series with a capacitor whose value is identical to that used to couple the driven input.

## Demux Reset Operation

The MAX104 features an internal 1:2 demultiplexer that reduces the data rate of the output digital data to onehalf the sample clock rate. Demux reset is necessary when interleaving multiple MAX104s and/or synchronizing external demultiplexers. The simplified block diagram of Figure 1 shows that the demux reset signal path consists of four main circuit blocks. From input to output, they are the reset input dual latch, the reset pipeline, the demux clock generator, and the reset output. The signals associated with the demux reset operation and the control of this section are listed in Table 6.

## Reset Input Dual Latch

 The reset input dual-latch circuit block accepts differential PECL reset inputs referenced to the same VccO power supply that powers the MAX104 PECL outputs. For applications that do not require a synchronizing reset, the reset inputs can be left open. In this case, they will self-bias to a proper level with internal $50 \mathrm{k} \Omega$ resistors and $20 \mu \mathrm{~A}$ current source. This combination creates a -1V difference between RSTIN+ and RSTINto disable the internal reset circuitry. When driven with PECL logic levels terminated with $50 \Omega$ to ( $\mathrm{VCCO}-2 \mathrm{~V}$ ), the internal biasing network can easily be overdriven. Figure 14 shows a simplified schematic of the reset input structure.To properly latch the reset input data, the setup time (tSU) and the data hold time (tHD) must be met with respect to the rising edge of the sample clock. The timing diagram of Figure 15 shows the timing relationship of the reset input and sampling clock.


Figure 14. Simplified Reset Input Structure


Figure 15. Reset Input Timing Definitions

# $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 

## Table 6. Demux Operating and Reset Control Signal

| SIGNAL NAME | TYPE | FUNCTION |
| :--- | :--- | :--- |
| CLK,+ CLK- | Sampling clock inputs | Master ADC timing signal. The ADC samples on the rising edge of CLK+. |
| DREADY + , DREADY- | Differential PECL outputs | Data-Ready PECL Output. Output data changes on the rising edge of <br> DREADY.+ |
| RSTIN+, RSTIN- | Differential PECL inputs | Demux reset input signals. Resets the internal demux when asserted. |
| RSTOUT + , RSTOUT- | Differential PECL outputs | Reset outputs for resetting additional external demux devices |

## Reset Pipeline

The next section in the reset signal path is the reset pipeline. The purpose of this block is to add clock cycles of latency to the reset signal, to match the latency of the converted analog data through the ADC. In this way, when reset data arrives at the RSTOUT+/ RSTOUT- PECL output, it will be time-aligned with the analog data present in the primary and auxiliary ports at the time the reset input was deasserted at RSTIN+/ RSTIN-.

## Demux Clock Generator

The demux clock generator creates the DIV1, DIV2, or DIV4 clocks required for the different modes of demux and non-demux operation. The TTL/CMOS control inputs DEMUXEN and DIVSELECT control the demuxed mode selection, as described in Table 2. The timing diagrams in Figure 16 and Figure 17 show the output timing and data alignment in DIV1, DIV2, and DIV4 modes, respectively.


Figure 16. CLK and DREADY Timing in Demuxed DIV2 Mode Showing Two Possible DREADY Phases

The phase relationship between the sampling clock at the CLK+/CLK- inputs and the data-ready clock at the DREADY+/DREADY- outputs will be random at device power-up. As with all divide-by-two circuits, two possible phase relationships exist between these clocks. The difference between the phases is simply the inversion of the DIV2-DREADY clock. The timing diagram in Figure 16 shows this relationship.
Reset all MAX104 devices to a known DREADY phase after initial power-up for applications such as interleaving, where two or more MAX104 devices are used to achieve higher effective sampling rates. This synchronization is necessary to set the order of output samples between the devices. Resetting the converters accomplishes this synchronization. The reset signal is used to force the internal counter in the demux clock-generator block to a known phase state.


Figure 17. Output Timing for All Modes (DIV1, DIV2, DIV4)

# $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 

Finally, the reset signal is presented in differential PECL format to the last block of the reset signal path. RSTOUT+/RSTOUT- output the time-aligned reset signal used for resetting additional external demuxes in applications that need further output data rate reduction. Many demux devices require that their reset signal be asserted for several clock cycles while they are clocked. To accomplish this, the MAX104 DREADY clock will continue to toggle while RSTOUT is asserted.
When a single MAX104 device is used, no synchronizing reset is required, because the order of the samples in the output ports is unchanged regardless of the phase of the DREADY clock. In DIV2 mode, the data in the auxiliary port is delayed by 8.5 clock cycles, while the data in the primary port is delayed by 7.5 clock cycles. The older data is always in the auxiliary port, regardless of the phase of the DREADY clock.
The reset output signal, RSTOUT, is delayed by one less clock cycle ( 6.5 clock cycles) than the primary
port. The reduced latency of RSTOUT serves to mark the start of synchronized data in the primary and auxiliary ports. When the RSTOUT signal returns to a zero, the DREADY clock phase is reset.
Since there are two possible phases of the DREADY clock with respect to the input clock, there are two possible timing diagrams to consider. The first timing diagram (Figure 18) shows the RSTOUT timing and data alignment of the auxiliary and primary output ports when the DREADY clock phase is already reset. For this example, the RSTIN pulse is two clock cycles long. Under this condition, the DREADY clock continues uninterrupted, as does the data stream in the auxiliary and primary ports.
The second timing diagram (Figure 19) shows the results when the DREADY phase is opposite from the reset phase. In this case, the DREADY clock "swallows" a clock cycle of the sample clock, resynchronizing to the reset phase. Note that the data stream in the auxiliary and primary ports has reversed. Before reset was


Figure 18. Reset Output Timing in Demuxed DIV2 Mode (DREADY Aligned)

# $\pm 5 \mathrm{~V}, 1$ Gsps, 8 -Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 



Figure 19. Reset Output Timing in Demuxed DIV2 Mode (DREADY Realigned)
asserted, the auxiliary port contained "even" samples while the primary port contained "odd" samples. After the RSTOUT is deasserted (which marks the start of the DREADY clock's reset phase), note that the order of the samples in the ports has been reversed. The auxiliary port also contains an out-of-sequence sample. This is a consequence of the "swallowed" clock cycle that was needed to resynchronize DREADY to the reset phase. Also note that the older sample data is always in the auxiliary port, regardless of the DREADY phase.
These examples illustrate the combinations that result with a reset input signal of two clock cycles. It is also possible to reset the internal MAX104 demux successfully with a reset pulse of only one clock cycle, provided that the setup-time and hold-time requirements are met with respect to the sample clock. However, this is not recommended when additional external demuxes are used.
Note that many external demuxes require that their reset signals be asserted while they are clocked, and may require more than one clock cycle of reset. More importantly, if the phase of the DREADY clock is such that a clock pulse will be "swallowed" to resynchronize,
then no reset output will occur at all. In effect, the RSTOUT signal will be "swallowed" with the clock pulse. The best method to ensure complete system reset is to assert RSTIN for the appropriate number of DREADY clock cycles required to complete reset of the external demuxes.

## Die Temperature Measurement

For applications that require monitoring of the die temperature, it is possible to determine the die temperature of the MAX104 under normal operating conditions by observing the currents ICONST and IPTAT, at contacts ICONST and IPTAT. ICONST and IPTAT are two $100 \mu \mathrm{~A}$ (nominal) currents that are designed to be equal at $+27^{\circ} \mathrm{C}$. These currents are derived from the MAX104's internal precision +2.5 V bandgap reference. ICONST is designed to be temperature independent, while IPTAT is directly proportional to the absolute temperature. These currents are derived from pnp current sources referenced from Vccl and driven into two series diodes connected to GNDI. The contacts ICONST and IPTAT may be left open, because internal catch diodes prevent saturation of the current sources. The simplest method

## $\pm 5 \mathrm{~V}, 1 \mathrm{Gsps}, 8$-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

of determining the die temperature is to measure each current with an ammeter (which shuts off the internal catch diodes) referenced to GNDI. The die temperature in ${ }^{\circ} \mathrm{C}$ is then calculated by the expression:

$$
\mathrm{T}_{\mathrm{DIE}}=300 \cdot\left[\frac{\mathrm{I}_{\mathrm{PTAT}}}{\mathrm{I}_{\mathrm{CONST}}}\right]-273
$$

Another method of determining the die temperature uses the operational amplifier circuit shown in Figure 20. The circuit produces a voltage that is proportional to the die temperature. A possible application for this signal is speed control for a cooling fan, to maintain constant MAX104 die temperature. The circuit operates by converting the ICONST and IPTAT currents to voltages VCONST and VPTAT, with appropriate scaling to account for their equal values at $+27^{\circ} \mathrm{C}$. This voltage difference is then amplified by two amplifiers in an instrumenta-tion-amplifier configuration with adjustable gain. The nominal value of the circuit gain is $4.5092 \mathrm{~V} / \mathrm{V}$. The gain of the instrumentation amplifier is given by the expression:

$$
\begin{aligned}
& A_{V}=\frac{V_{T E M P}}{V_{C O N S T}-V_{\text {PTAT }}} \\
& A_{V}=1+\frac{R 1}{R 2}+2 \cdot \frac{R 1}{R 3}
\end{aligned}
$$



Figure 20. Die Temperature Acquisition Circuit with the MAX479

# $\pm 5 \mathrm{~V}, 1$ Gsps, 8 -Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 

## Table 7. Thermal Performance for MAX104 With or Without Heatsink

| AIRFLOW <br> (linear ft./min.) | MAX104 $\theta \mathbf{J A}\left({ }^{\circ} \mathbf{C} / \mathrm{W}\right)$ |  |
| :---: | :---: | :---: |
|  | WITHOUT <br> HEATSINK | WITH HEATSINK |
| 0 | 16.5 | 12.5 |
| 200 | 14.3 | 9.4 |
| 400 | 13 | 8.3 |
| 800 | 12.5 | 7.4 |

Thermal Performance
The MAX104 has been modeled to determine the thermal resistance from junction to ambient. Table 7 lists the ADC's thermal performance parameters:
Ambient Temperature:
Heatsink Dimensions:
$\mathrm{T}_{\mathrm{A}}=+70^{\circ} \mathrm{C}$
PC Board Size and Layout: $\quad 4^{\prime \prime} \times 4$ "
2 Signal Layers
2 Power Layers
Heatsink Manufacturers
Aavid Engineering and IERC provide open-tool, lowprofile heatsinks, fitting the $25 \mathrm{~mm} \times 25 \mathrm{~mm}$ ESBGA package.
Aavid Engineering, Inc.
Phone: 714-556-2665
Heatsink Catalog \#: 335224B00032
Heatsink Dimensions: $25 \mathrm{~mm} \times 25 \mathrm{~mm} \times 10 \mathrm{~mm}$
International Electronic Research Corporation (IERC)
Phone: 818-842-7277
Heatsink Catalog \#: BDN09-3CB/A01
Heatsink Dimensions: $23.1 \mathrm{~mm} \times 23.1 \mathrm{~mm} \times 9 \mathrm{~mm}$

## Bypassing/Layout/Power Supply

Grounding and power-supply decoupling strongly influence the MAX104's performance. At 1GHz clock frequency and 8-bit resolution, unwanted digital crosstalk may couple through the input, reference, power supply, and ground connections and adversely influence the dynamic performance of the ADC. Therefore, closely follow the grounding and power-supply decoupling guidelines (Figure 22).


Figure 21. MAX104 Thermal Performance
Maxim strongly recommends using a multilayer printed circuit board (PCB) with separate ground and powersupply planes. Since the MAX104 has separate analog and digital ground connections (GNDA, GNDI, GNDR, and GNDD, respectively), the PCB should feature separate analog and digital ground sections connected at only one point (star ground at the power supply). Digital signals should run above the digital ground plane, and analog signals should run above the analog ground plane. Keep digital signals far away from the sensitive analog inputs, reference inputs, and clock inputs. Highspeed signals, including clocks, analog inputs, and digital outputs, should be routed on $50 \Omega$ microstrip lines, such as those employed on the MAX104EVKIT.
The MAX104 has separate analog and digital powersupply inputs: $V_{E E}(-5 \mathrm{~V}$ analog and substrate supply) and $\mathrm{V}_{\mathrm{ccl}}(+5 \mathrm{~V}$ ) to power the $\mathrm{T} / \mathrm{H}$ amplifier, clock distribution, bandgap reference, and reference amplifier; VccA ( +5 V ) to supply the ADC's comparator array; $\mathrm{VccO}(+3 \mathrm{~V}$ to VccD$)$ to establish power for all PECLbased circuit sections; and $\mathrm{V}_{\mathrm{cc}} \mathrm{D}(+5 \mathrm{~V})$ to supply all logic circuits of the data converter.
The MAX104 VEE supply contacts must not be left open while the part is being powered up. To avoid this condition, add a high-speed Schottky diode (such as a Motorola 1N5817) between VEE and GNDI. This diode prevents the device substrate from forward biasing, which could cause latchup.

## $\pm 5 \mathrm{~V}, 1 \mathrm{Gsps}, 8$-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

All supplies should be decoupled with large tantalum or electrolytic capacitors at the point where they enter the PCB. For best performance, bypass all power supplies to the appropriate ground with a $10 \mu \mathrm{~F}$ tantalum capacitor, to filter power-supply noise, in parallel with a $0.01 \mu \mathrm{~F}$ capacitor and a high-quality 47pF ceramic chip capacitor located very close to the MAX104 device, to filter very high-frequency noise.

## Static Parameter Definitions

Integral Nonlinearity (INL)
Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. This straight
line can be either a best-straight-line fit or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX104 are measured using the best-straight-line fit method.

## Differential Nonlinearity (DNL)

 Differential nonlinearity is the difference between an actual step width and the ideal value of 1LSB. A DNL error specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.
NOTE:
LOCATE ALL 47pF CAPACITORS AS CLOSE AS POSSIBLE TO THEMAX104 DEVICE.


$$
V_{C C} A=+4.75 \mathrm{~V} \text { TO }+5.25 \mathrm{~V}
$$

$V_{C C} D=+4.75 \mathrm{~V}$ TO +5.25 V
$\mathrm{V}_{\mathrm{CCI}}=+4.75 \mathrm{~V} \mathrm{TO}+5.25 \mathrm{~V}$
$\mathrm{V}_{\mathrm{CC}} \mathrm{O}=+3.0 \mathrm{~V}$ TO $\mathrm{V}_{\mathrm{CC}} \mathrm{D}$
$\mathrm{V}_{\mathrm{EE}}=-4.75 \mathrm{~V}$ TO-5.25V

Figure 22. MAX104 Bypassing and Grounding

# $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 

Bit Error Rates (BER)

Errors resulting from metastable states may occur when the analog input voltage (at the time the sample is taken) falls close to the decision point of any one of the input comparators. Here, the magnitude of the error depends on the location of the comparator in the comparator network. If it is the comparator for the MSB, the error will reach full scale. The MAX104's unique encoding scheme solves this problem by limiting the magnitude of these errors to 1LSB; it reduces the probability of these errors occurring to typically one in every $10^{16}$ clock cycles.

## Dynamic Parameter Definitions

Signal-to-Noise Ratio (SNR)
For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution ( N bits):

$$
\mathrm{SNR}_{(\mathrm{MAX})}=(6.02 \cdot \mathrm{~N}+1.76) \mathrm{dB}
$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is calculated by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Effective Number of Bits (ENOB)
ENOB indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB is calculated from a curve fit referenced to the theoretical full-scale range.

Signal-to-Noise Plus Distortion (SINAD) SINAD is calculated from the effective number of bits (ENOB) as follows:

$$
\text { SINAD }=(6.02 \cdot \mathrm{ENOB})+1.76
$$

Total Harmonic Distortion (THD)
THD is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$
\mathrm{THD}=20 \cdot \log \left(\sqrt{\left(\mathrm{~V}_{2}^{2}+\mathrm{V}_{3}^{2}+\mathrm{V}_{4}^{2}+\mathrm{V}_{5}^{2}\right)} / \mathrm{V}_{1}\right)
$$

where $\mathrm{V}_{1}$ is the fundamental amplitude, and $\mathrm{V}_{2}$ through $\mathrm{V}_{5}$ are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range (SFDR) SFDR is the ratio, expressed in decibels, of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset.

Intermodulation Distortion (IMD)
The two-tone IMD is the ratio, expressed in decibels, of either input tone to the worst 3rd-order (or higher) intermodulation products. The input tone levels are at -7 dB full scale.

## $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

Typical Operating Circuit


# $\pm 5 \mathrm{~V}, 1 \mathrm{Gsps}, 8$-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 



## $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

Package Information


# $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier 

| NOTES: <br> 1. <br> 2. | UNLESS OTHERTISE SPECIFIED <br> all dimensions and tolerances CONFORM TO ANSI Y14.5M-1982. | STANDARD BODY S |  |  |  | SIZE DIMENSION |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | ¢00\% | $25.0 \times 25.0 \mathrm{MM} \mathrm{PACKAGE}$ |  |  | $27.0 \times 27.0 \mathrm{MM}$ PACKAGE |  |  |  |
|  |  | SYMBOL | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | NOTE |
|  | DIIENSION "b" IS MEASURBD AT THE MAXIMUM SOLDER BALL DIAMETER, PARALIEL TO PRIMARY DATUM -C- | A | 1.41 | 1.54 | 1.67 | 1.41 | 1.54 | 1.67 | THVERNLI |
|  |  | A1 | 0.56 | 0.63 | 0.70 | 0.56 | 0.63 | 0.70 | HEALIT |
| $3$ | PRDMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS. | A2 | 0.85 | 0.91 | 0.97 | 0.85 | 0.91 | 0.97 | HMCKOY |
|  |  | D | 24.90 | 25.00 | 25.10 | 26.90 | 27.00 | 27.10 | ¢ |
| 4. |  | D1 | 22.76 | 22.86 | 22.96 | 24.03 | 24.13 | 24.23 | Footitent |
|  | THE 192 BALL $25 \times 25$ MM SBGA has 3 ROWS OF BALLS. tHE 256 ball $27 \times 27$ mM SBga has 4 ROWS OF balls. | E | 24.90 | 25.00 | 25.10 | 26.90 | 27.00 | 27.10 | coiky |
|  |  | E1 | 22.76 | 22.86 | 22.96 | 24.03 | 24.13 | 24.23 | FCotpliw |
| $5 .$ | SHAPE AT CORNER. | M, N | $19 \times 19$ |  |  | $20 \times 20$ |  |  | MATRIX |
|  | - | $b$ | 0.60 | 0.75 | 0.90 | 0.60 | 0.75 | 0.90 | DiAMCLIER |
| 6. |  | $d$ | 0.6 |  |  | 0.6 |  |  | ENCAP TISTAMCES |
|  | $\square$ | e | 1.27 |  |  | 1.27 |  |  | ¢ |
|  | SINGIE FORM | aad |  |  | 0.15 |  |  | 0.15 | coplanaraty |
|  | ALL DIMENSIONS ARE IN MIILMETERS. | bbb |  |  | 0.15 |  |  | 0.15 | Parallel |
|  |  | cec |  |  | 0.20 |  |  | 0.20 | flap |
| $9$ | height from bail seating plane to Plane of encapsulant. | ddd 8 | 0.15 | 0.33 | 0.50 | 0.15 | 0.33 | 0.50 | SEATING PLANE |
|  |  | P | 0.20 | 0.30 | 0.35 | 0.20 | 0.30 | 0.35 | EmCApSLICTION |
|  |  | S | - | - | 0.00 | - | - | 0.635 | Sold |
| " $\mathrm{S}^{\prime}$ IS MEASURED WITH RESPECT TO -AAND -B- AND DEFINES THE POSITHON OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUNBER OF SOLDER BALIS IN THE OUTER ROW "S" $=.000$; WHEN there is an even number of solder balls IN THE OUTER ROW THE VALUE " $\mathrm{S}^{\prime \prime}=\mathrm{e} / 2$. "S" MAY BE ETTHBR . 000 OR e/2 FOR EACH VARIATION. |  |  |  |  |  |  |  |  |  |
| 9. THE DMENSION FROM THE OUTER EDGE OF THERESIN DAM TO THE EDEE OF THE INNERMOST ROWOF SOIDER BALL PADS IS TO BE A MINIMUM OF0.50 mm . |  |  |  |  | ~" |  |  |  |  |
|  |  | ogies. |  |  | PACKAGE QUTLINE, SUPER-BGA |  |  |  |  |
|  |  |  |  |  | NPTOVL |  | $\begin{aligned} & \text { Docurent conina na } \\ & 21-0073 \end{aligned}$ |  | $\begin{array}{\|c\|c\|} \hline \mathrm{Kev} \\ \mathrm{c} & 2 / 2 \\ \hline \end{array}$ |

# $\pm 5 \mathrm{~V}, 1$ Gsps, 8-Bit ADC with <br> On-Chip 2.2GHz Track/Hold Amplifier 

## NOTES

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

32
Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600
© 1999 Maxim Integrated Products
Printed USA MIXINI is a registered trademark of Maxim Integrated Products.


[^0]:    $X=$ Don't care

