FLEX PCI Development Board

November 2001, ver. 1.2 Data Sheet

Features

- Universal 3.3-V/5.0-V 32-bit/64-bit PCI expansion card
- Includes the FLEX® 10KE EPF10K200SFC672 device
- On-board 144-pin small-outline DIMM 32-Mbyte SDRAM module
- On-board standard PCI mezzanine card (PMC) connector
- Operates on 33- or 66-MHz PCI bus
- 84-pin user I/O and prototype area
- External power supply connector for stand-alone application
- Footprint for crystal oscillator (oscillator not included)
- External clock input for local-side function, SDRAM, prototype devices, and expansion
- On-board phase-locked loops (PLLs) to eliminate clock skew
- Joint Test Action Group (JTAG) and passive serial (PS) headers for device configuration with ByteBlasterMV™ or MasterBlaster™ download cables
- Upgradable to the following FLEX 10KE devices:
  - EPF10K100EFC672
  - EPF10K130EFC484
  - EPF10K130EFC672
  - EPF10K200EFC672
  - EPF10K200SFC672

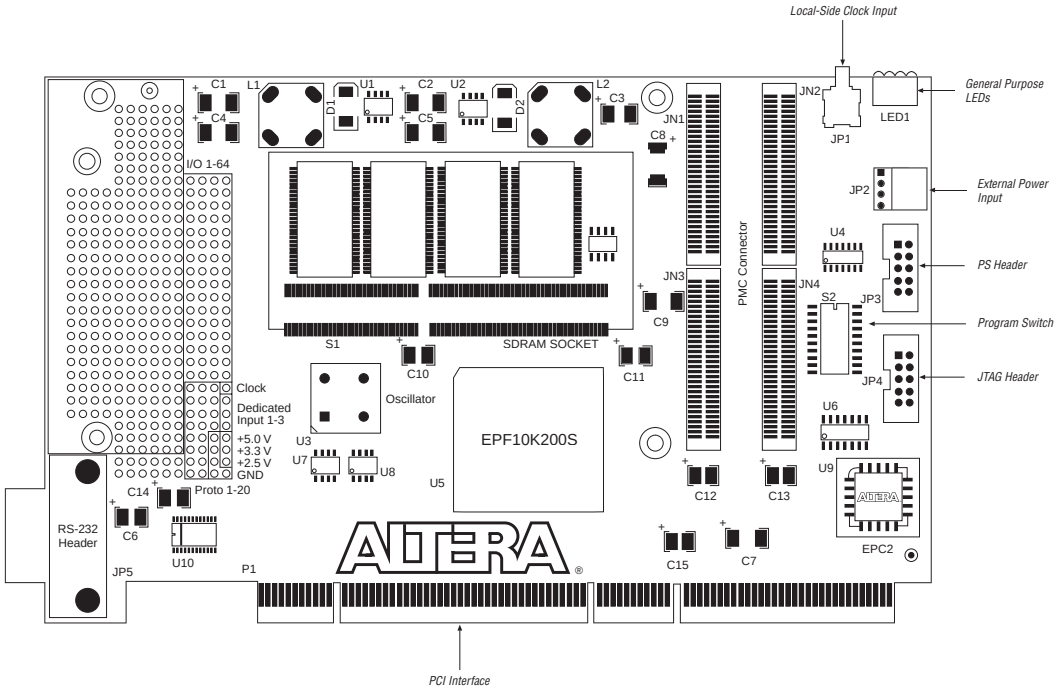
General Description

The PCI development board is designed to work with all Altera® peripheral component interconnect (PCI) MegaCore™ functions, including `pci_mt32`, `pci_t32`, `pci_mt64`, and `pci_t64`. It can be used for product development or demonstration purposes. Users can implement custom local-side functions to interface with the Altera PCI MegaCore function and SDRAM, or an RS-232 port. The PCI development board provides a flexible clock network and in-circuit configuration options. It supports a wide range of FLEX 10KE devices to tailor a user's need for I/O and logic density. This data sheet provides information on signal connections, programming and configuration settings, clock network selection, and board options for the Altera FLEX PCI development board.

Functional Description

Figure 1 shows the FLEX PCI development board block diagram.

Figure 1. PCI Development Board Block Diagram



Programming & Configuration Settings/Defaults

The PCI development board supports on-board configuration device programming and in-circuit configuration for FLEX devices in both JTAG and PS mode with the ByteBlasterMV or MasterBlaster download cable.

Table 1 shows the programming and configuration options available and their settings. Refer to the board schematics for more details.

Table 1. Programming & Configuration Options *Note (1)*

Mode/ Device(s)	EPC2	ByteBlaster/ MasterBlaster	Dip-Switch On	Description
JTAG EPC2	Mounted	Connected to JTAG header	SW1	Programs the EPC2 devices in JTAG mode using the MAX+PLUS II or Quartus II software. The EPC2 devices are device 0 and device 1. This setting is the default for the board.
JTAG EPC2, FLEX	Mounted	Connected to JTAG header	SW2, SW3	Places the EPC2 devices and the FLEX device in the JTAG chain. The EPC2 devices are device 0 and device 1, the FLEX device is device 2, and the PMC device is device 3.
JTAG EPC2, FLEX, Expansion	Mounted	Connected to JTAG header	SW2, SW4, SW5, SW6, SW7	Places the EPC2 device(s), FLEX device, and the PMC connector in the JTAG chain. The EPC2 device(s) are device 0 and device 1, the FLEX device is device 2, and the PMC device is device 3.
PS	Removed	Connected to BitBlaster header	None	Configures the FLEX device in PS mode using the MAX+PLUS II or Quartus II software.
Configuration with EPC2	Mounted	Removed	SW10	Configures the FLEX device with the data programmed into the EPC2 device(s).

Note:
(1) When programming the EPC2 devices, the first Programmer Object File (**.pof**) should target device 0 and the second POF should target device 1.

Clock Network Selection/Default

The clock signal on the PCI development board can arrive from various clocking sources including system clock, external clock, and on-board crystal oscillator (not included). The PLL devices provide zero-delay clock signal distribution throughout the board to minimize clock skew within the same clock network. Clock selection can be done by installing selected resistor(s).

Table 2 shows the available clocks and the corresponding resistor settings.

Table 2. Available Device Clocks & Corresponding Resistor Settings

Source	PLL	Destination	Resistor Settings	Description
System clock	No	FLEX device PCI clock.	R49	The system clock is connected directly to the on-board FLEX device's PCI clock input
System clock	Yes	FLEX device PCI clock.	R45, R41	The system clock is used as a reference voltage to the PLL. An output of the PLL is connected to the FLEX device's PCI clock input
System clock	Yes	SDRAM, expansion connector, prototype clock, FLEX device clock2.	R45, R36	The system clock is used as a reference voltage to the PLL, and outputs of the PLL are connected to SDRAM, FLEX device clock2, expansion connector, and prototype clock.
Crystal oscillator	Yes	SDRAM, expansion connector, prototype clock, FLEX device clock2.	R35	The crystal oscillator (not included) is used as a reference voltage to the PLL, and outputs of the PLL are connected to SDRAM, FLEX device clock2, expansion connector, and prototype clock.
External clock	Yes	SDRAM, expansion connector, prototype clock, FLEX device clock2.	R39	The external clock is used as a reference voltage to the PLL, and outputs of the PLL are connected to SDRAM, FLEX device clock2, expansion connector, and prototype clock.

Resistors R45, R41, and R36 are installed on the board by default.

FLEX 10KE Pin Assignments

Pin assignments to FLEX 10KE devices ensure that its I/Os are properly connected to the defined signals on the board. Before compiling the FLEX 10KE design for the PCI development board, pin assignments must be made to all defined pins.

Signal Connections

Signals pass through the PCI development board via the PCI interface connector, expansion connector, or external sources and connect to various board components. Table 3 defines the schematic references.

Table 3. schematic Reference Definitions

Reference	Definition
P1.A<*n*> or P1.B<*n*>	P1 = PCI interface; A = front of board; B = back of board; <*n*> = pin number
U5.<*Xn*>	U5 = FLEX10KE-672; <*An*> = array pin number
U4.<*n*>	U4 = 74HCT04 inverters; <*n*> = pin number
U10<*n*>	U10 = MAX208 RS232 Interface device; <*n*> = pin number
U1.<*n*>	U1 = MAX750A; <*n*> = pin number
U2.<*n*>	U2 = MAX750A; n = pin number
U7.<*n*>	U7 = Clock distribution device; <*n*> = pin number
U8.<*n*>	U8 = Clock distribution device; <*n*> = pin number
U6.<*n*>	U6 = 74HCT125 tri-state buffers; <*n*> = pin number
U9.<*n*>	U9 = configuration EPC2; <*n*> = pin number
U3.<*n*>	U3 = On-board clock device; <*n*> = pin number
S1.<*n*>	S1 = SDRAM socket; <*n*> = pin number
S2.<*n*>	S2 = Programming/configuration dip-switches; <*n*> = pin number
Jn1.<*n*>	Jn1 = PMC connector; <*n*> = pin number
Jn2.<*n*>	Jn2= PMC connector; <*n*> = pin number
Jn3<*n*>	Jn3= PMC connector; <*n*> = pin number
Jn4<*n*>	Jn4= PMC connector; <*n*> = pin number
JP1<*n*>	JP1 = External Clock connector; <*n*> = pin number
JP2<*n*>	JP2 = External power header; <*n*> = pin number
JP3<*n*>	JP3 = Passive serial configuration header; <*n*> = pin number
JP4<*n*>	JP4 = JTAG programming/configuration header; <*n*> = pin number
LED1<*n*>	LED1 = general purpose LED; <*n*> = pin number
TP<*n*>	TP = User I/O from the FLEX 10KE device; <*n*> = pin number

Table 4 shows the sequence of PCI development board connections.

Table 4. PCI Development Board Connections (Part 1 of 15)

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
JTAG_DATA	P1.A4	P1.B4	–	–	–	–
P5_IO20	TP39.1	U5.F1	–	–	–	–
P5_IO64	TP64.1	U5.AD11	–	–	–	–
P5_IO37	TP101	U5.P2	–	–	–	–
P5_IO42	TP201	U5.U1	–	–	–	–
P5_IO49	TP34.1	U5.Y1	–	–	–	–
P_IDSEL	U5.R10	P1.A26	–	–	–	–
P_REQ#	U5.V21	P1.B18	–	–	–	–
P_AD50	U5.W15	P1.A77	–	–	–	–
P_AD35	U5.AC19	P1.B89	–	–	–	–
P_AD39	U5.W17	P1.B86	–	–	–	–
P_AD3	U5.AC9	P1.B56	–	–	–	–
P5_IO38	TP12.1	U5.P1	–	–	–	–
P5_IO48	TP32.1	U5.W2	–	–	–	–
P5_IO28	TP55.1	U5.L2	–	–	–	–
P5_IO15	TP29.1	U5.D2	–	–	–	–
P5_IO36	TP8.1	U5.N3	–	–	–	–
P5_IO22	TP43.1	U5.G1	–	–	–	–
P5_IO9	TP17.1	U5.B3	–	–	–	–
P5_IO56	TP48.1	U5.AC2	–	–	–	–
P5_IO57	TP50.1	U5.AD2	–	–	–	–
P5_IO53	TP42.1	U5.AB1	–	–	–	–
P5_IO3	TP5.1	U5.A8	–	–	–	–
P_AD36	U5.V18	P1.A88	–	–	–	–
P_AD53	U5.Y15	P1.B75	–	–	–	–
P_AD8	U5.V10	P1.B52	–	–	–	–
P_AD56	U5.Y14	P1.A73	–	–	–	–
P_AD26	U5.U8	P1.A23	–	–	–	–
P5_IO1	TP1.1	U5.D12	–	–	–	–
P5_IO23	TP45.1	U5.H4	–	–	–	–
P5_IO29	TP57.1	U5.L5	–	–	–	–
P5_IO19	TP37.1	U5.F2	–	–	–	–
P5_IO54	TP44.1	U5.U5	–	–	–	–
P_AD62	U5.U13	P1.A68	–	–	–	–
P_REQ64#	U5.Y11	P1.A60	–	–	–	–

Table 4. PCI Development Board Connections (Part 2 of 15)

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
P_AD19	U5.AA7	P1.B30	–	–	–	–
P_AD51	U5.AD16	P1.B77	–	–	–	–
P_AD33	U5.AC20	P1.B90	–	–	–	–
P_AD58	U5.W13	P1.A71	–	–	–	–
P_AD22	U5.W7	P1.A28	–	–	–	–
P_AD54	U5.V14	P1.A74	–	–	–	–
P_AD15	U5.AC7	P1.A44	–	–	–	–
P_LOCK#	U5.U20	P1.B39	–	–	–	–
P_AD11	U5.AB9	P1.A47	–	–	–	–
P5_IO18	TP35.1	U5.E2	–	–	–	–
P5_IO60	TP56.1	U5.AD5	–	–	–	–
P5_IO13	TP25.1	U5.C2	–	–	–	–
P5_IO32	TP63.1	U5.L1	–	–	–	–
P_SERR#	U5.W19	P1.B42	–	–	–	–
P_AD38	U5.AC18	P1.A86	–	–	–	–
P_AD0	U5.W11	P1.A58	–	–	–	–
P_GNT#	U5.AA12	P1.A17	–	–	–	–
P_AD42	U5.Y16	P1.A83	–	–	–	–
P_AD34	U5.W18	P1.A89	–	–	–	–
P_AD24	U5.V6	P1.A25	–	–	–	–
P_AD2	U5.V11	P1.A57	–	–	–	–
P_AD47	U5.AB16	P1.B80	–	–	–	–
P_AD6	U5.W10	P1.A54	–	–	–	–
P_AD13	U5.W9	P1.A46	–	–	–	–
P_FRAME#	U5.AA11	P1.A34	–	–	–	–
P5_IO51	TP38.1	U5.AA1	–	–	–	–
P5_IO47	TP30.1	U5.W3	–	–	–	–
P5_IO61	TP58.1	U5.AB11	–	–	–	–
P5_IO11	TP21.1	U5.A3	–	–	–	–
P5_IO7	TP13.1	U5.C4	–	–	–	–
P5_IO4	TP7.1	U5.A7	–	–	–	–
P5_IO41	TP18.1	U5.R2	–	–	–	–
P5_IO35	TP6.1	U5.N1	–	–	–	–
P5_IO55	TP46.1	U5.AC1	–	–	–	–
P_AD49	U5.AC16	P1.B78	–	–	–	–
P_AD20	U5.AA6	P1.A29	–	–	–	–
P_AD17	U5.AB7	P1.B32	–	–	–	–

Table 4. PCI Development Board Connections (Part 3 of 15)

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
P_AD60	U5.V13	P1.A70	–	–	–	–
P_AD4	U5.AA10	P1.A55	–	–	–	–
P_AD45	U5.V16	P1.B81	–	–	–	–
NCE	U5.G6	R17.1	–	–	–	–
P5_IO44	TP24.1	U5.V1	–	–	–	–
P5_IO14	TP27.1	U5.B1	–	–	–	–
P5_IO24	TP47.1	U5.J2	–	–	–	–
P5_IO52	TP40.1	U5.AB2	–	–	–	–
P_AD18	U5.AA8	P1.A31	–	–	–	–
P_AD40	U5.Y17	P1.A85	–	–	–	–
P_ACK64#	U5.AB12	P1.B60	–	–	–	–
P_AD63	U5.AC12	P1.B68	–	–	–	–
P_AD46	U5.U15	P1.A80	–	–	–	–
P_AD31	U5.T8	P1.B20	–	–	–	–
P_AD32	U5.AA18	P1.A91	–	–	–	–
P5_IO39	TP14.1	U5.P4	–	–	–	–
P5_IO26	TP51.1	U5.K2	–	–	–	–
P5_IO43	TP22.1	U5.U2	–	–	–	–
P5_IO16	TP31.1	U5.D1	–	–	–	–
P5_IO2	TP3.1	U5.A9	–	–	–	–
P5_IO50	TP36.1	U5.AA2	–	–	–	–
P5_IO30	TP59.1	U5.L3	–	–	–	–
P5_IO10	TP19.1	U5.D5	–	–	–	–
P_AD61	U5.AD12	P1.B69	–	–	–	–
P_PAR64	U5.AC22	P1.A67	–	–	–	–
P_AD21	U5.AA5	P1.B29	–	–	–	–
P_AD25	U5.V8	P1.B24	–	–	–	–
P_AD9	U5.AA9	P1.A49	–	–	–	–
P_M66EN	U5.R7	P1.B49	–	–	–	–
P_AD29	U5.U6	P1.B21	–	–	–	–
P_AD43	U5.AA16	P1.B83	–	–	–	–
P5_IO63	TP62.1	U5.AF11	–	–	–	–
P5_IO17	TP33.1	U5.E1	–	–	–	–
P5_IO59	TP54.1	U5.AD7	–	–	–	–
P5_IO5	TP9.1	U5.C7	–	–	–	–
P_AD52	U5.AA15	P1.A76	–	–	–	–
P_AD41	U5.AB17	P1.B84	–	–	–	–

Table 4. PCI Development Board Connections (Part 4 of 15)

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
P_AD37	U5.AA17	P1.B87	–	–	–	–
P_AD57	U5.AA14	P1.B72	–	–	–	–
P_AD30	U5.T6	P1.A20	–	–	–	–
P_AD16	U5.Y8	P1.A32	–	–	–	–
P_AD5	U5.Y10	P1.B55	–	–	–	–
P_AD48	U5.V15	P1.A79	–	–	–	–
P_PAR	U5.AB20	P1.A43	–	–	–	–
P_AD12	U5.AD8	P1.B47	–	–	–	–
P_AD27	U5.U7	P1.B23	–	–	–	–
P_PERR#	U5.W21	P1.B40	–	–	–	–
P5_IO21	TP41.1	U5.G2	–	–	–	–
P5_IO25	TP49.1	U5.J1	–	–	–	–
P5_IO12	TP23.1	U5.C6	–	–	–	–
P5_IO58	TP52.1	U5.AD1	–	–	–	–
P5_IO34	TP4.1	U5.N2	–	–	–	–
P5_IO46	TP28.1	U5.W1	–	–	–	–
P5_IO40	TP16.1	U5.R1	–	–	–	–
P_INTA#	U5.V19	P1.A6	–	–	–	–
P_DEVSEL#	U5.Y12	P1.B37	–	–	–	–
P_AD59	U5.AB13	P1.B71	–	–	–	–
P_AD23	U5.V7	P1.B27	–	–	–	–
P_AD7	U5.AB8	P1.B53	–	–	–	–
P_RST#	U5.G14	P1.A15	–	–	–	–
P_AD1	U5.AC10	P1.B58	–	–	–	–
P_AD28	U5.U9	P1.A22	–	–	–	–
P_AD44	U5.W16	P1.A82	–	–	–	–
P5_IO62	TP601	U5.AC11	–	–	–	–
P5_IO6	TP11.1	U5.C5	–	–	–	–
P_IRDY#	U5.U12	R50.1	P1.B35	–	–	–
P_C/BE#7	U5.Y20	P1.A64	–	–	–	–
P_C/BE#6	U5.Y19	P1.B65	–	–	–	–
P_C/BE#5	U5.AA20	P1.A65	–	–	–	–
P_C/BE#4	U5.AA19	P1.B66	–	–	–	–
P_C/BE#3	U5.AC21	P1.B26	–	–	–	–
P_C/BE#2	U5.U18	P1.B33	–	–	–	–
P_C/BE#1	U5.Y18	P1.B44	–	–	–	–
P_C/BE#0	U5.AB19	P1.A52	–	–	–	–

Table 4. PCI Development Board Connections (Part 5 of 15)

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
P_AD55	U5.W14	P1.B74	–	–	–	–
P_AD10	U5.Y9	P1.B48	–	–	–	–
IN_PCI_TRDY#	U5.U14	R43.2	R47.2	R51.2	–	–
P_AD14	U5.W8	P1.B45	–	–	–	–
PU1	R28.2	R42.1	–	–	–	–
S_DQMB2	S1.115	U5.P1.0	–	–	–	–
S_DQ31	S1.137	U5.G11	–	–	–	–
S_DQ12	S1.47	U5.K7	–	–	–	–
S_DQ48	S1.84	U5.G15	–	–	–	–
S_A13	S1.72	U5.G9	–	–	–	–
S_DQ24	S1.121	U5.G10	–	–	–	–
S_DQ50	S1.88	U5.D16	–	–	–	–
S_CAS#	S1.66	U5.P7	–	–	–	–
P_TRDY#	U5.V12	R51.1	P1.A36	–	–	–
P_STOP#	U5.W12	R521	P1.A38	–	–	–
IN_PCI_STOP#	U5.K13	R44.2	R48.2	R52.2	–	–
IN_PCI_IRDY#	U5.Y13	R42.2	R46.2	R50.2	–	–
PU2	R29.2	R44.1	–	–	–	–
PU3	R26.2	R43.1	–	–	–	–
S_DQ30	S1.135	U5.K12	–	–	–	–
S_DQ11	S1.43	U5.K5	–	–	–	–
S_DQMB1	S1.25	U5.P9	–	–	–	–
S_DQ42	S1.42	U5.H14	–	–	–	–
S_DQ32	S1.4	U5.H12	–	–	–	–
S_DQ1	S1.5	U5.M3	–	–	–	–
S_CKE0	S1.62	U5.R9	–	–	–	–
S_DQ47	S1.54	U5.H15	–	–	–	–
S_A5	S1.34	U5.K9	–	–	–	–
S_DQ58	S1.126	U5.H17	–	–	–	–
S_DQMB3	S1.117	U5.N6	–	–	–	–
S_DQ13	S1.49	U5.L9	–	–	–	–
S_DQ16	S1.83	U5.E7	–	–	–	–
S_DQ37	S1.16	U5.J12	–	–	–	–
S_DQ49	S1.86	U5.F16	–	–	–	–
S_DQMB0	S1.23	U5.P3	–	–	–	–
S_DQ59	S1.128	U5.K21	–	–	–	–
S_DQ0	S1.3	U5.M6	–	–	–	–

Table 4. PCI Development Board Connections (Part 6 of 15)

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
S_DQ29	S1.133	U5.F11	–	–	–	–
S_DQ28	S1.131	U5.J10	–	–	–	–
S_DQ33	S1.6	U5.F12	–	–	–	–
S_DQ2	S1.7	U5.M7	–	–	–	–
S_DQ57	S1.124	U5.J19	–	–	–	–
S_DQ3	S1.9	U5.M8	–	–	–	–
S_DQ17	S1.85	U5.F8	–	–	–	–
S_DQ41	S1.40	U5.J13	–	–	–	–
S_CKE1	S1.68	U5.P6	–	–	–	–
S_DQMB4	S1.24	U5.N8	–	–	–	–
S_DQ14	S1.51	U5.K8	–	–	–	–
S_DQ10	S1.41	U5.L8	–	–	–	–
S_BA1	S1.110	U5.T3	–	–	–	–
S_DQMB5	S1.26	U5.N5	–	–	–	–
S_DQMB6	S1.116	U5.N9	–	–	–	–
S_DQ43	S1.44	U5.J14	–	–	–	–
S_WE#	S1.67	U5.N7	–	–	–	–
S_RAS#	S1.65	U5.P8	–	–	–	–
S_DQ36	S1.14	U5.H13	–	–	–	–
S_DQ18	S1.87	U5.E6	–	–	–	–
S_DQ62	S1.136	U5.K23	–	–	–	–
S_DQ4	S1.13	U5.M9	–	–	–	–
S_A12	S1.70	U5.H8	–	–	–	–
S_DQ55	S1.100	U5.H18	–	–	–	–
S_DQ56	S1.122	U5.H24	–	–	–	–
S_DQ20	S1.93	U5.F9	–	–	–	–
S_A2	S1.33	U5.J6	–	–	–	–
S_DQ38	S1.18	U5.G13	–	–	–	–
S_A6	S1.103	U5.D8	–	–	–	–
S_DQ6	S1.17	U5.K3	–	–	–	–
S_DQMB7	S1.118	U5.N10	–	–	–	–
S_DQ63	S1.138	U5.K19	–	–	–	–
S_DQ8	S1.37	U5.L6	–	–	–	–
S_DQ53	S1.96	U5.H16	–	–	–	–
S_SCL	S1.142	U5.T4	–	–	–	–
S_DQ7	S1.19	U5.L7	–	–	–	–
S_DQ54	S1.98	U5.J21	–	–	–	–

Table 4. PCI Development Board Connections (Part 7 of 15)

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
S_DQ44	S1.48	U5.K14	–	–	–	–
S_DQ22	S1.97	U5.J9	–	–	–	–
S_A8	S1.105	U5.H10	–	–	–	–
S_A1	S1.31	U5.H6	–	–	–	–
S_DQ26	S1.125	U5.J11	–	–	–	–
S_DQ52	S1.94	U5.D17	–	–	–	–
S_DQ39	S1.20	U5.F13	–	–	–	–
S_DQ21	S1.95	U5.F10	–	–	–	–
S_DQ34	S1.8	U5.G12	–	–	–	–
S_DQ40	S1.38	U5.D13	–	–	–	–
S_A4	S1.32	U5.E5	–	–	–	–
S_A3	S1.30	U5.J7	–	–	–	–
S_DQ35	S1.10	U5.C12	–	–	–	–
S_DQ61	S1.134	U5.K20	–	–	–	–
S_DQ27	S1.127	U5.H11	–	–	–	–
S_DQ9	S1.39	U5.K6	–	–	–	–
S_A11	S1.112	U5.F7	–	–	–	–
S_DQ5	S1.15	U5.M10	–	–	–	–
S_DQ25	S1.123	U5.D10	–	–	–	–
S_DQ45	S1.50	U5.D15	–	–	–	–
S_A0	S1.29	U5.J8	–	–	–	–
S_DQ51	S1.90	U5.G16	–	–	–	–
S_BA0	S1.106	U5.T7	–	–	–	–
S_DQ46	S1.52	U5.F15	–	–	–	–
E_SDONE	Jn1.41	U5.P5	–	–	–	–
E_AD14	Jn2.45	U5.D14	–	–	–	–
E_AD8	Jn2.49	U5.E11	–	–	–	–
E_AD57	Jn3.19	U5.U23	–	–	–	–
E_AD34	Jn3.54	U5.M18	–	–	–	–
S_S0#	S1.69	U5.T9	–	–	–	–
E_AD12	Jn1.47	U5.C13	–	–	–	–
S_DQ15	S1.53	U5.H9	–	–	–	–
S_SDA	S1.141	U5.R6	–	–	–	–
S_A10	S1.111	U5.E9	–	–	–	–
S_DQ19	S1.89	U5.D9	–	–	–	–
S_A7	S1.104	U5.H5	–	–	–	–
S_DQ60	S1.132	U5.J18	–	–	–	–

Table 4. PCI Development Board Connections (Part 8 of 15)

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
E_INTD#	Jn1.9	U5.T5	–	–	–	–
E_CBE7	Jn3.4	U5.F21	–	–	–	–
P4_IO2	Jn4.2	U5.B15	–	–	–	–
E_AD27	Jn1.22	U5.L18	–	–	–	–
E_BM1	Jn1.7	U5.AA4	–	–	–	–
E_AD22	Jn1.27	U5.H22	–	–	–	–
E_AD15	Jn1.46	U5.E14	–	–	–	–
E_DEVSEL#	Jn1.37	U5.D20	–	–	–	–
E_AD16	Jn2.31	U5.E15	–	–	–	–
E_AD61	Jn3.13	U5.AD23	–	–	–	–
E_AD37	Jn3.49	U5.L24	–	–	–	–
P4_IO42	Jn4.42	U5.Y25	–	–	–	–
P4_IO57	Jn4.57	U5.AD20	–	–	–	–
S_S1#	S1.71	U5.R8	–	–	–	–
S_A9	S1.109	U5.G8	–	–	–	–
S_DQ23	S1.99	U5.E10	–	–	–	–
E_AD32	Jn3.58	U5.K24	–	–	–	–
P4_IO64	Jn4.64	U5.AD17	–	–	–	–
P4_IO44	Jn4.44	U5.Y26	–	–	–	–
E_INTB#	Jn1.5	U5.V4	–	–	–	–
E_BM3	Jn2.14	U5.W4	–	–	–	–
E_AD41	Jn3.43	U5.M23	–	–	–	–
P4_IO22	Jn4.22	U5.L25	–	–	–	–
P4_IO63	Jn4.63	U5.AF17	–	–	–	–
E_AD17	Jn1.32	U5.C16	–	–	–	–
E_AD19	Jn1.29	U5.G22	–	–	–	–
E_FRAME#	Jn1.33	U5.F19	–	–	–	–
E_AD55	Jn3.23	U5.P1.9	–	–	–	–
E_AD35	Jn3.53	U5.L23	–	–	–	–
P4_IO23	Jn4.23	U5.L26	–	–	–	–
P4_IO19	Jn4.19	U5.J26	–	–	–	–
P4_IO1	Jn4.1	U5.B14	–	–	–	–
+12V	Jn2.1	P1.A2	–	–	–	–
P4_IO52	Jn4.52	U5.AF22	–	–	–	–
P4_IO48	Jn4.48	U5.AB25	–	–	–	–
P4_IO53	Jn4.53	U5.AD26	–	–	–	–
P4_IO21	Jn4.21	U5.K26	–	–	–	–

Table 4. PCI Development Board Connections (Part 9 of 15)

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
P4_IO35	Jn4.35	U5.U26	–	–	–	–
P4_IO17	Jn4.17	U5.H26	–	–	–	–
E_CBE5	Jn3.6	U5.F20	–	–	–	–
E_AD31	Jn1.20	U5.L21	–	–	–	–
E_BM2	Jn2.11	U5.Y4	–	–	–	–
E_CBE1	Jn2.43	U5.H19	–	–	–	–
E_AD60	Jn3.16	U5.AB22	–	–	–	–
E_AD50	Jn3.30	U5.N18	–	–	–	–
P4_IO30	Jn4.30	U5.R25	–	–	–	–
E_PAR	Jn1.43	U5.F22	–	–	–	–
E_AD23	Jn2.26	U5.K18	–	–	–	–
E_REQ#	Jn1.17	U5.C17	–	–	–	–
P4_IO39	Jn4.39	U5.V25	–	–	–	–
P4_IO49	Jn4.49	U5.AC26	–	–	–	–
E_AD29	Jn2.20	U5.L20	–	–	–	–
E_AD49	Jn3.31	U5.P23	–	–	–	–
E_AD33	Jn3.55	U5.M17	–	–	–	–
E_AD48	Jn3.34	U5.P24	–	–	–	–
P4_IO12	Jn4.12	U5.E26	–	–	–	–
P4_IO46	Jn4.46	U5.AA24	–	–	–	–
P4_IO41	Jn4.41	U5.W26	–	–	–	–
P4_IO31	Jn4.31	U5.T22	–	–	–	–
P4_IO11	Jn4.11	U5.E25	–	–	–	–
P4_IO15	Jn4.15	U5.F26	–	–	–	–
P4_IO4	Jn4.4	U5.B18	–	–	–	–
P4_IO20	Jn4.20	U5.K25	–	–	–	–
P4_IO50	Jn4.50	U5.AD25	–	–	–	–
P4_IO47	Jn4.47	U5.AC25	–	–	–	–
P4_IO62	Jn4.62	U5.AC17	–	–	–	–
P4_IO13	Jn4.13	U5.F25	–	–	–	–
E_AD25	Jn1.23	U5.H23	–	–	–	–
E_AD58	Jn3.18	U5.W24	–	–	–	–
E_AD53	Jn3.25	U5.P20	–	–	–	–
E_AD20	Jn2.28	U5.F23	–	–	–	–
E_IRDY#	Jn1.36	U5.E18	–	–	–	–
E_AD62	Jn3.12	U5.AD24	–	–	–	–
E_PAR64	Jn3.10	U5.E22	–	–	–	–

Table 4. PCI Development Board Connections (Part 10 of 15)

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
P4_IO34	Jn4.34	U5.U25	–	–	–	–
P4_IO43	Jn4.43	U5.AA25	–	–	–	–
E_AD10	Jn2.48	U5.D11	–	–	–	–
P4_IO61	Jn4.61	U5.AE18	–	–	–	–
E_AD4	Jn1.55	U5.F5	–	–	–	–
P4_IO26	Jn4.26	U5.N26	–	–	–	–
P4_IO3	Jn4.3	U5.B17	–	–	–	–
E_AD5	Jn1.54	U5.F4	–	–	–	–
P4_IO58	Jn4.58	U5.AF19	–	–	–	–
P4_IO59	Jn4.59	U5.AD19	–	–	–	–
E_STOP#	Jn2.38	U5.C21	–	–	–	–
E_AD0	Jn1.61	U5.F3	–	–	–	–
E_INTA#	Jn1.4	U5.AA3	–	–	–	–
E_GNT#	Jn1.16	U5.G17	–	–	–	–
E_RST#	Jn2.13	U5.W22	–	–	–	–
E_AD51	Jn3.29	U5.P21	–	–	–	–
E_AD52	Jn3.28	U5.R24	–	–	–	–
E_AD40	Jn3.46	U5.N19	–	–	–	–
P4_IO18	Jn4.18	U5.J25	–	–	–	–
P4_IO27	Jn4.27	U5.P25	–	–	–	–
E_AD46	Jn3.36	U5.N23	–	–	–	–
E_AD13	Jn2.46	U5.C14	–	–	–	–
E_SERR#	Jn2.42	U5.E24	–	–	–	–
E_IDSEL	Jn2.25	U5.AC23	–	–	–	–
P4_IO32	Jn4.32	U5.T24	–	–	–	–
P4_IO55	Jn4.55	U5.AD22	–	–	–	–
P4_IO9	Jn4.9	U5.C25	–	–	–	–
E_TRDY#	Jn2.35	U5.C20	–	–	–	–
E_PERR#	Jn2.39	U5.J20	–	–	–	–
E_AD47	Jn3.35	U5.N21	–	–	–	–
E_INTC#	Jn1.6	U5.U4	–	–	–	–
E_AD6	Jn1.53	U5.E8	–	–	–	–
E_AD28	Jn1.21	U5.J24	–	–	–	–
E_AD56	Jn3.22	U5.T23	–	–	–	–
P4_IO14	Jn4.14	U5.G25	–	–	–	–
E_AD2	Jn1.59	U5.E3	–	–	–	–
E_REQ64#	Jn1.64	U5.C22	–	–	–	–

Table 4. PCI Development Board Connections (Part 11 of 15)

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
E_AD9	Jn1.49	U5.C11	–	–	–	–
P4_IO24	Jn4.24	U5.M26	–	–	–	–
E_CBE2	Jn2.32	U5.C23	–	–	–	–
E_AD21	Jn1.28	U5.F24	–	–	–	–
E_AD59	Jn3.17	U5.W23	–	–	–	–
P4_IO38	Jn4.38	U5.V26	–	–	–	–
E_CBE3	Jn1.26	U5.G19	–	–	–	–
E_AD44	Jn3.40	U5.N24	–	–	–	–
P4_IO16	Jn4.16	U5.G26	–	–	–	–
-12V	Jn1.2	P1.B1	–	–	–	–
E_AD54	Jn3.24	U5.R23	–	–	–	–
E_AD38	Jn3.48	U5.M20	–	–	–	–
E_CBE4	Jn3.7	U5.D22	–	–	–	–
E_AD18	Jn2.29	U5.E16	–	–	–	–
E_SBO#	Jn1.42	U5.R4	–	–	–	–
E_BM4	Jn2.16	U5.W5	–	–	–	–
E_ACK64#	Jn2.61	U5.E20	–	–	–	–
E_AD63	Jn3.11	U5.AB21	–	–	–	–
P4_IO6	Jn4.6	U5.B26	–	–	–	–
P4_IO8	Jn4.8	U5.D25	–	–	–	–
P4_IO45	Jn4.45	U5.AB26	–	–	–	–
E_AD1	Jn1.60	U5.G4	–	–	–	–
P4_IO54	Jn4.54	U5.AE26	–	–	–	–
E_AD45	Jn3.37	U5.N22	–	–	–	–
P4_IO10	Jn4.10	U5.D26	–	–	–	–
E_AD24	Jn2.23	U5.G24	–	–	–	–
P4_IO60	Jn4.60	U5.AB18	–	–	–	–
E_AD42	Jn3.42	U5.M24	–	–	–	–
E_LOCK#	Jn1.40	U5.Y22	–	–	–	–
P4_IO29	Jn4.29	U5.R26	–	–	–	–
E_AD26	Jn2.22	U5.J22	–	–	–	–
P4_IO7	Jn4.7	U5.C26	–	–	–	–
A_TDO	S2.3	S.24	U5.H21	–	–	–
E_TDO	S2.5	Jn2.4	–	–	–	–
E_TDI	S2.17	Jn2.5	–	–	–	–
MSEL0	R16.1	R12.2	U5.W6	–	–	–
MSEL1	R13.2	R18.1	U5.Y6	–	–	–

Table 4. PCI Development Board Connections (Part 12 of 15)

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
P4_IO5	Jn4.5	U5.E19	–	–	–	–
P4_IO28	Jn4.28	U5.P26	–	–	–	–
E_CBE6	Jn3.5	U5.E21	–	–	–	–
E_AD36	Jn3.52	U5.M19	–	–	–	–
P4_IO40	Jn4.40	U5.W25	–	–	–	–
P4_IO36	Jn4.36	U5.V22	–	–	–	–
E_CBE0	Jn1.52	U5.D21	–	–	–	–
P4_IO51	Jn4.51	U5.AE24	–	–	–	–
P4_IO37	Jn4.37	U5.V23	–	–	–	–
E_AD30	Jn2.19	U5.L19	–	–	–	–
E_AD39	Jn3.47	U5.M21	–	–	–	–
DATA	R23.2	JP3.9	U6.8	U5.F6	–	–
TDO	JP4.3	S2.20	S2.18	S216	–	–
A_TCK	R33.1	JP4.1	U9.3	S2.6	U5.G20	–
A_TMS	JP4.5	R34.2	U91.9	S2.7	U5.W20	–
A_TRST#	R24.1	S2.8	U5.Y21	–	–	–
A_TDI	S2.19	U5.H7	–	–	–	–
E_TCK	S2.15	Jn1.1	–	–	–	–
E_AD3	Jn1.58	U5.G5	–	–	–	–
P4_IO25	Jn4.25	U5.N25	–	–	–	–
E_AD7	Jn2.51	U5.C9	–	–	–	–
E_AD11	Jn1.48	U5.E12	–	–	–	–
E_AD43	Jn3.41	U5.N20	–	–	–	–
P4_IO56	Jn4.56	U5.AD21	–	–	–	–
P4_IO33	Jn4.33	U5.T26	–	–	–	–
PROTO15	J30.1	U5.AB6	–	–	–	–
PROTO9	J25.1	U5.Y23	–	–	–	–
PROTO8	J21.1	U5.V20	–	–	–	–
PROTO14	J26.1	U5.J4	–	–	–	–
PROTO11	J14.1	U5.U21	–	–	–	–
VNEG	U10.15	C67.2	–	–	–	–
NSTATUS	R22.2	JP3.7	U9.8	U5.AA21	–	–
NCONFIG	R21.2	JP3.5	U9.13	U5.V9	–	–
CONFDONE	JP3.3	R20.2	U6.2	U5.H20	–	–
DCLK	JP3.1	R15.2	U6.11	U5.G7	–	–
E_TRST#	S2.13	Jn2.2	–	–	–	–
E_TMS	S2.14	Jn2.3	–	–	–	–

Table 4. PCI Development Board Connections (Part 13 of 15)

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
NLED2	LED1.2	U4.4	–	–	–	–
R_RTS	JP5.7	U10.24	–	–	–	–
R_CD	JP5.1	U10.16	–	–	–	–
PROTO1	J12.1	U5.K15	–	–	–	–
PROTO5	J28.1	U5.T19	–	–	–	–
PROTO4	J24.1	U5.R17	–	–	–	–
C1POS	U10.10	C70.1	–	–	–	–
UNUSED1	R19.1	U4.11	–	–	–	–
LED3	U4.5	U5.C19	–	–	–	–
RS232_TX	U1.05	U5.T21	–	–	–	–
LED1	U4.1	U5.G18	–	–	–	–
NLED1	U4.2	LED1.1	–	–	–	–
NLED4	LED1.4	U4.8	–	–	–	–
R_DTR	JP5.4	U10.1	–	–	–	–
R_RX	JP5.2	U10.7	–	–	–	–
R_CTS	JP5.8	U10.3	–	–	–	–
R_RI	JP5.9	U10.23	–	–	–	–
PROTO17	J19.1	U5.AC6	–	–	–	–
PROTO19	J27.1	U5.AC4	–	–	–	–
PROTO20	J31.1	U5.AD3	–	–	–	–
PROTO23	J39.1	R47.1	–	–	–	–
PROTO3	J20.1	U5.T18	–	–	–	–
PROTO7	J17.1	U5.Y3	–	–	–	–
UNUSED2	R14.1	U4.13	–	–	–	–
RS232_RTS	U10.19	U5.P1.8	–	–	–	–
RS232_CTS	U10.4	U5.R19	–	–	–	–
RS232_DTR	U10.18	U5.T20	–	–	–	–
R_TX	JP5.3	U10.2	–	–	–	–
PROTO16	J15.1	U5.AD4	–	–	–	–
PROTO12	J18.1	U5.U22	–	–	–	–
PROTO13	J22.1	U5.R21	–	–	–	–
PROTO18	J23.1	U5.AC5	–	–	–	–
PROTO22	J38.1	R48.1	–	–	–	–
RS232_CD	U10.17	U5.N17	–	–	–	–
RS232_RI	U10.22	U5.R20	–	–	–	–
LED4	U4.9	U5.C18	–	–	–	–
C1NEG	C70.2	U10.12	–	–	–	–

Table 4. PCI Development Board Connections (Part 14 of 15)

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
LED2	U4.3	U5.F18	–	–	–	–
RS232_RX	U10.6	U5.P17	–	–	–	–
PROTO2	J16.1	U5.J15	–	–	–	–
PROTO6	J13.1	U5.R18	–	–	–	–
C2POS	U10.13	C66.1	–	–	–	–
C2NEG	C66.2	U10.14	–	–	–	–
E_CLK	U7.5	Jn1.13	–	–	–	–
PROTO_CLK	U7.7	J32.1	–	–	–	–
PCI_CLK3	U8.5	C56.1	–	–	–	–
PCI_CLK0	U8.8	C53.1	–	–	–	–
PCI_REF	U8.1	R45.2	–	–	–	–
PCI_CLK2	U8.2	R41.1	–	–	–	–
PCI_CLK	R45.1	R49.1	P1.B16	–	–	–
NLED3	LED1.3	U4.6	–	–	–	–
S_CK1	U72	S1.74	–	–	–	–
PCI_CLK4	U8.7	C55.1	–	–	–	–
S_CK0	U7.3	S1.61	–	–	–	–
A_CLK2	U7.8	U5.F14	–	–	–	–
PROTO10	J29.1	U5.U19	–	–	–	–
PROTO21	J37.1	R46.1	–	–	–	–
VPOS	U10.11	C69.1	–	–	–	–
REF_1	C29.1	U1.2	–	–	–	–
SS_2	C18.1	U2.3	R4.2	–	–	–
CC_2	U2.4	C19.2	R5.2	R6.1	R7.2	–
REF_2	C26.1	U2.2	–	–	–	–
SS_1	C16.1	U1.3	R3.2	–	–	–
CC_1	U1.4	C25.2	R2.2	R1.1	–	–
LX_1	U1.7	L1.4	L1.1	D1.2	–	–
LX_2	U2.7	L2.4	L2.1	D2.2	–	–
SEL_CLK	U7.1	R35.2	R39.2	R32.2	R36.2	–
PCI_CLK1	R36.1	U8.3	–	–	–	–
OSC_CLK	U3.5	R35.1	–	–	–	–
EXT_CLK	JP1.1	R40.2	R39.1	–	–	–
A_CLKOUT	R32.1	U5.F17	–	–	–	–
A_CLK1	R49.2	R41.2	U5.T13	–	–	–
PROM_SELECT	U6.13	U6.10	U6.1	R25.1	S2.11	–
UNUSED	U6.5	R31.1	–	–	–	–

Table 4. PCI Development Board Connections (Part 15 of 15)

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
UNUSED_TRI	U6.4	R30.1	–	–	–	–
PROM_DATA	U9.2	U6.9	–	–	–	–
PROM_TDO	U9.1	S2.2	S2.1	–	–	–
EXTRA_SWITCH	S2.12	R27.1	U5.J16	–	–	–
TDI	R38.2	JP4.9	U9.11	–	–	–
PROM_DCLK	U9.4	U6.12	–	–	–	–
PROM_CS	U6.3	U9.9	R37.1	–	–	–

Tables 5 through 9 show the board connections for the E_VIO, +5.0 V, +3.3 V, +2.5 V, and GND signals.

Table 5. E_VIO Development Board Connections

Signal	Connections					
E_VIO	Jn1.57	Jn1.45	Jn1.31	Jn1.19	Jn3.9	Jn3.21
	Jn3.39	Jn3.57	R8.2	R9.2	C9.1	C43.1
	C33.1	C27.1	C42.1	C51.1	C47.1	R11.2
	R10.2	–	–	–	–	–

Table 6. +5.0 V Development Board Connections

Signal	Connections					
+5.0V	U1.1	U1.8	C2.1	C17.1	R3.1	U2.1
	U2.8	C5.1	C22.1	R4.1	JP2.1	C14.1
	C15.1	C52.1	C38.1	C30.1	C32.1	C24.1
	C68.1	C35.1	C20.1	C31.1	C28.1	C6.1
	C7.1	U3.8	U4.14	LED1.5	LED1.6	LED1.7
	LED1.8	U10.9	J33.1	JP4.4	JP3.4	Jn1.8
	Jn1.18	Jn1.30	Jn1.38	Jn1.50	Jn1.62	R9.1
	R11.1	P1.B5	P1.A5	P1.B6	P1.A8	P1.B61
	P1.A61	P1.B62	P1.A62	U6.14	–	–

Table 7. +3.3 V Development Board Connections

Signal	Connections					
+3.3V	C25.1	R2.1	C4.1	C10.1	C13.1	C44.1
	C39.1	C46.1	C34.1	C65.1	C41.1	C21.1
	C61.1	C62.1	C40.1	L1.3	L1.2	C36.1
	C57.1	C59.1	C48.1	C1.1	U8.6	U7.6
	J34.1	R21.1	R22.1	R23.1	R13.1	U9.18
	U9.20	U9.14	U9.5	R38.1	R34.1	R12.1
	R24.2	R20.1	R15.1	R37.2	R25.2	R27.2
	JP3.6	JP4.6	Jn2.15	Jn2.27	Jn2.41	Jn2.53
	Jn2.62	Jn2.50	Jn2.36	Jn2.24	Jn2.12	R10.1
	R8.1	S1.130	S1.144	S1.102	S1.82	S1.64
	S1.46	S1.12	S1.28	S1.11	S1.45	S1.143
	S1.129	S1.113	S1.114	S1.101	S1.81	S1.63
	S1.27	R28.1	R26.1	R29.1	U5.C8	U5.C15
	U5.D7	U5.G3	U5.J3	U5.J17	U5.K11	U5.K22
	U5.L13	U5.L15	U5.M11	U5.M13	U5.M16	U5.M22
	U5.N16	U5.P11	U5.R5	U5.R11	U5.R13	U5.R16
	U5.R22	U5.T15	U5.U3	U5.U11	U5.V5	U5.V17
	U5.V24	U5.Y24	U5.Y2	U5.AA26	U5.AD15	–

Table 8. +2.5 V Development Board Connections

Signal	Connections					
+2.5V	C19.1	R5.1	C3.1	R7.1	C11.1	C12.1
	C58.1	C64.1	C49.1	C37.1	C60.1	C63.1
	C23.1	C50.1	C45.1	C54.1	L2.3	L2.2
	C8.1	J35.1	U5.E17	U5.H2	U5.H25	U5.K16
	U5.L10	U5.L12	U5.L14	U5.L17	U5.M2	U5.M25
	U5.N11	U5.N12	U5.N15	U5.P12	U5.P15	U5.P16
	U5.R14	U5.T2	U5.T10	U5.T12	U5.T14	U5.T17
	U5.T25	U5.U16	U5.Y7	U5.AA23	U5.AB10	U5.AC14
	U5.E13	–	–	–	–	–

Table 9. Ground Development Board Connections (Part 1 of 2)

Signal	Connections					
GND	C15.2	C10.2	C13.2	C11.2	C12.2	
	U1.6	C29.2	JP2.3	C22.2	C5.2	R1.2
	C3.2	C2.2	C14.2	R6.2	JP2.2	C18.2
	C4.2	C17.2	C16.2	C26.2	U2.6	D1.1
	D2.1	C52.2	C38.2	C30.2	C32.2	C24.2
	C68.2	C35.2	C20.2	C31.2	C28.2	C41.2
	C34.2	C44.2	C39.2	C46.2	C65.2	C21.2
	C61.2	C40.2	C62.2	C63.2	C37.2	C582.
	C64.2	C49.2	C60.2	C23.2	C50.2	C54.2
	C45.2	C36.2	C57.2	C59.2	C48.2	C1.2
	C6.2	C7.2	C8.2	U8.4	U3.4	U7.4
	C55.2	C53.2	C56.2	R40.1	JP1.4	JP1.5
	JP1.3	JP1.2	U4.7	U1.021	U10.8	C67.1
	C69.2	J36.1	R19.2	R14.2	JP5.5	JP4.2
	JP4.10	JP3.2	JP3.10	U9.10	R33.2	R18.2
	R16.2	R31.2	R30.2	S2.10	S2.9	Jn1.3
	Jn1.11	Jn1.15	Jn1.25	Jn1.35	Jn1.39	Jn1.51
	Jn1.63	Jn1.56	Jn1.44	Jn1.34	Jn1.24	Jn1.4
	Jn2.7	Jn2.21	Jn2.33	Jn2.37	Jn2.47	Jn2.59
	Jn2.63	Jn2.6	Jn2.18	Jn2.30	Jn2.40	Jn2.44
	Jn2.56	Jn3.63	Jn3.51	Jn3.45	Jn3.33	Jn3.27
	Jn3.15	Jn3.3	Jn3.62	Jn3.56	Jn3.50	Jn3.44
	Jn3.38	Jn3.32	Jn3.26	Jn3.20	Jn3.14	Jn3.8
	Jn3.2	C9.2	C43.2	C33.2	C27.2	C42.2
	C51.2	C47.2	S1.2	S1.56	S1.22	S1.76
	S1.92	S1.108	S1.120	S1.140	S1.36	S1.1
	S1.21	S1.35	S1.55	S1.75	S1.91	S1.139
	S1.107	S1.119	U5.P13	U5.P14	U5.P22	U5.R12
	U5.R15	U5.T11	U5.T16	U5.U10	U5.U17	U5.U24
	U5.V3	U5.Y5	U5.AA13	U5.AA22	U5.AB3	U5.AB4
	U5.AB5	U5.AB23	U5.AB24	U5.AC3	U5.AC8	U5.AC24
	U5.AD13	U5.AD18	U5.AE2	U5.AE25	U5.AF2	U5.AF25
	U5.A2	U5.A25	U5.B2	U5.B25	U5.C3	U5.C10
	U5.C24	U5.D3	U5.D4	U5.D19	U5.D23	U5.D24
	U5.E4	U5.E23	U5.G23	U5.J5	U5.J23	U5.K4
	U5.K10	U5.K17	U5.L11	U5.L16	U5.L22	U5.M5
	U5.M12	U5.M14	U5.M15	U5.N13	U5.N14	R17.2

Table 9. Ground Development Board Connections (Part 2 of 2)

Signal	Connections					
GND	P1.B3	P1.B15	P1.B17	P1.A18	P1.B22	P1.A24
	P1.B28	P1.A30	P1.B34	P1.A35	P1.A37	P1.B38
	P1.A42	P1.B46	P1.A48	P1.A56	P1.B57	P1.A90
	P1.A87	P1.A81	P1.A78	P1.A72	P1.A69	P1.A63
	P1.A93	P1.B94	P1.B91	P1.B85	P1.B82	P1.B76
	P1.B73	P1.B67	P1.B64	P1.B9	MH1.1	PMC1.1
	MH2.1	U6.7	–	–	–	–

Supported Components

Table 10 lists all components supported by the PCI development board; however, not all components are shipped with the board. See "Board Options" on page 25 for more information.

Table 10. Supported Components (Part 1 of 3)

Component	Manufacturer Part Number	Quantity	Schematic Reference
CAPACITOR, 0.01UF, 0805	AVX:08055E104ZAT	46	C16, C18, C20, C21, C23, C24, C27, C28, C30, C31, C32, C33, C34,C35, C36, C37,C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C54, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70
CAPACITOR, 10PF, 0805	AVX:08055A100KAT	3	C53, C55, C56
CAPACITOR, 330PF, 0805	AVX:08055A331KAT	2	C19, C25
CAPACITOR, 0.01UF, 0805	AVX:08055E103ZAT	2	C26, C29
CAPACITOR, 1.0UF, 1206	AVX:12063G105ZAT	2	C17, C22
CAPACITOR, 10UF, TAN, B-SIZE	AVX:TAJB107M016	7	C9, C10, C11, C12, C13, C14, C15
CAPACITOR, 47UF, TAN, D-SIZE	AVX:TAJC477M010	8	C1, C2, C3, C4, C5, C6, C7, C8
RESISTOR, 0 ¾, 0805	AVX:CR21-000	22	R8, R9, R10, R11, R16, R18, R32, R35, R36, R39, R41,R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52
RESISTOR, 150 ¾, 0805	AVX:CR21-151J	1	R40
RESISTOR, 510 ¾, 0805	AVX:CR21-511J	2	R3, R4

Table 10. Supported Components (Part 2 of 3)

Component	Manufacturer Part Number	Quantity	Schematic Reference
RESISTOR, 1 K¾, 0805	AVX:CR21-102J	22	R12, R13, R14, R15, R17, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R33, R34, R37, R38
RESISTOR, 13.0 K¾, 1%, 0805	AVX:CR21-1302F	2	R1, R6
RESISTOR, 22.1 K¾, 1%, 0805	AVX:CR21-2212F	2	R2, R5
RESISTOR, 37.5 K¾, 1%, 0805	AVX:CR21-3572F	1	R7
DIODE, SCHOTTKY, 30 V, 1.0 A, SMT	MOTOROLA:MBRS130LT3	2	D1, D2
LED, 4-DIODE_PACK, SMT	DIALIGHT:555-4003	1	LED1
INDUCTOR, 50 UH, 1.0 A	COILTRONICS:CTX50-2P	2	L1, L2
IC, PWM-VOLTAGE-REGULATOR, S08	MAXIM:MAX750ACSA	2	U1, U2
IC, RS232-INTERFACE, S024W	MAXIM:MAX208CWG	1	U10
IC, HEX-INVERTER, HCT, S014	TI:SN74HCT04D	1	U4
IC, QUAD3-STATE_BUF, HCT, S014	TI:SN74HCT125D	1	U6
IC, FLEX 10KE, 484/672-PIN_BGA	ALTERA	1	U5
IC, SERIAL_EPROM, PLCC20	ALTERA	1	U9
IC, ZERO-DELAY_BUFFER, S08	CYPRESS:CY2305-1H	2	U7, U8
SOCKET, 8-PIN_DIP	SAMTEC:ICO-308-SST	1	U3
SOCKET, 20-PIN, PLCC	SAMTEC:PLCC-020-F-N	1	Z2
CONNECTOR, DB-9, MALE	AMP:747250-4	1	JP5
CONNECTOR, 4-PIN, LOCK, RA	AMP:176153-4	1	JP2
SOCKET, 144-PIN, SO-DIMM, RA	AMP:390114-1	1	S1
CONNECTOR, PMC, RECEPTACLE	AMP:120521-1	4	Jn1, Jn2, Jn3, Jn4

Table 10. Supported Components (Part 3 of 3)

Component	Manufacturer Part Number	Quantity	Schematic Reference
CONNECTOR, SMB	AMP:414026-3	1	JP1
HEADER, 5 × 2-PIN, SHROUDED	SAMTEC:TST-105-07-S-D	2	JP3, JP4
SWITCH, DECADE, SMT	CTS:218-10LPST	1	S2

Board Options

The PCI development board schematics illustrate optional items and configuration modes. Not all components in the block diagram are shipped with the board. Tables 11 through 13 show clock, SDRAM, and FLEX 10KE device options for the development board.

Table 11. Clock Options

Options	Part Number	Register Installed	Description
User-defined clock device	–	R35	Other frequency
Suggested clock device	EPSON SG-531PH-66.000MC	R35	Suggested 66-MHz clock device

Table 12. SDRAM Options

Part Number	Configuration	Maximum Access Time (ns)	Maximum Operating Current (mA)
MT4LSDT464HG-662	4 Mbytes × 64	9	420
MT4LSDT464HG-662	8 Mbytes × 64	9	840

Table 13. FLEX 10KE Device Options

Part Number	Number of Pins	Package Type
EPF10K50EFC484-1	484	FineLine BGA™
EPF10K100EFC484-1	484	FineLine BGA
EPF10K100EFC672-1	672	FineLine BGA
EPF10K130EFC484-1	484	FineLine BGA
EPF10K130EFC672-1	672	FineLine BGA
EPF10K200EFC672-1	672	FineLine BGA

References

Refer to the following Altera documents for more information:

- ***PCI MegaCore Function User Guide***
- *AN 116 (Configuring SRAM-Based LUT Devices)*
- *FLEX 10KE Programmable Logic Device Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *MasterBlaster Serial/USB Communications Cable Data Sheet*

Other references include:

- PCI-SIG. ***PCI Local Bus Specification, Revision 2.2***, Portland, Oregon: PCI Special Interest Group, December 1998.
- Micron Technology, inc. Small-Outline SDRAM Module MT4LSDT464H, MT4LSDT864H Data Sheet. **http://www.micron.com/mti/msp/html/modds.html**.

Schematics

Schematic foldouts are shown on sheets 1 through 9.

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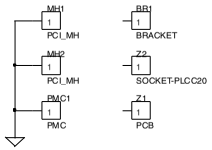
SHEET INDEX

UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE: CHIP RESISTORS - 0805 PACKAGE
   .10 WATT, 5%, 200PPM/C
2. ALL .1uF CAPS ARE: CHIP CAPS - 0805 PACKAGE
   Z5U DIELECTRIC, 20%, 50V

SPARES

MECHANICAL



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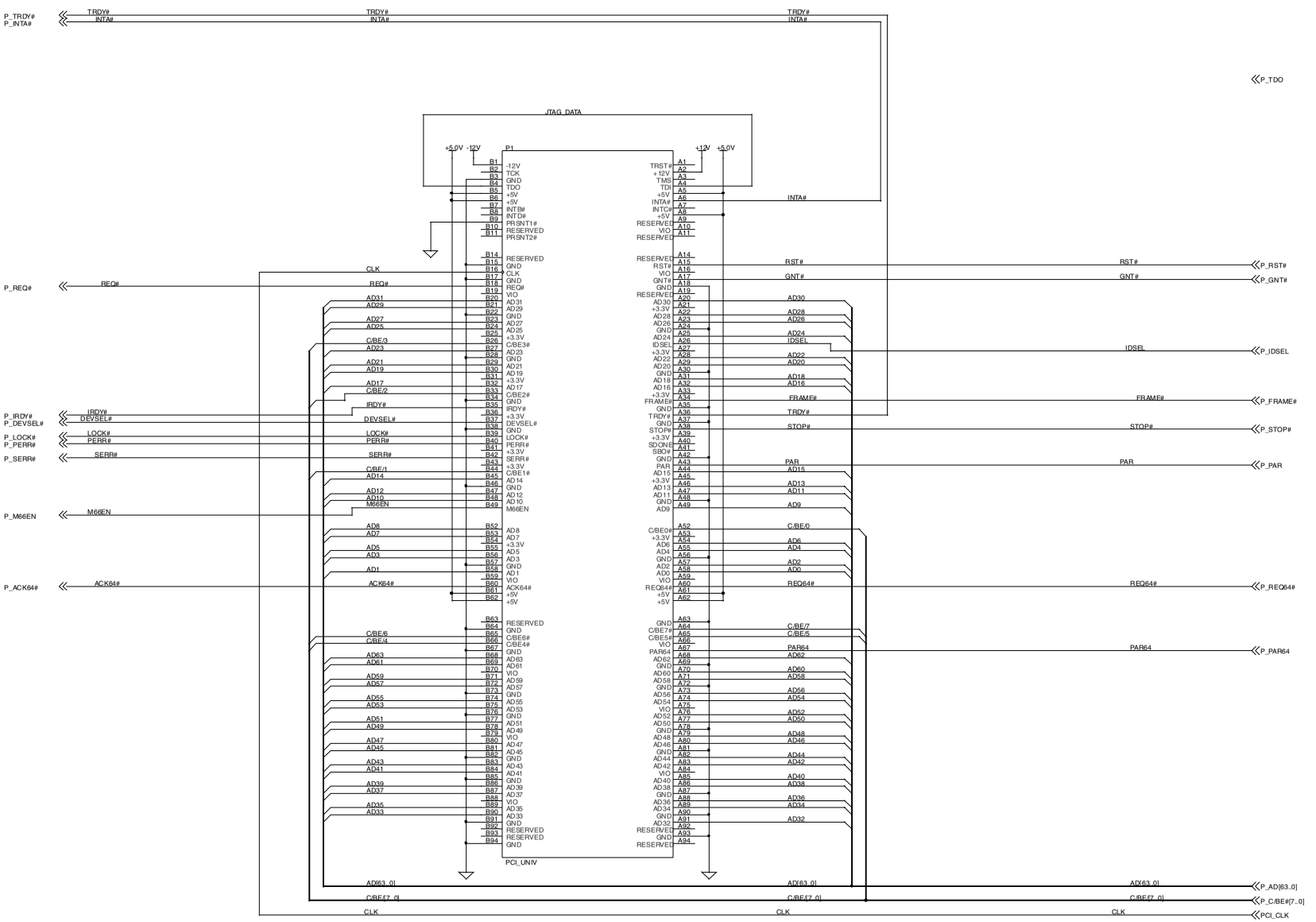

PCI CONNECTOR

Altera Corporation - FLEX 10KE PCI Development Board Data Sheet		
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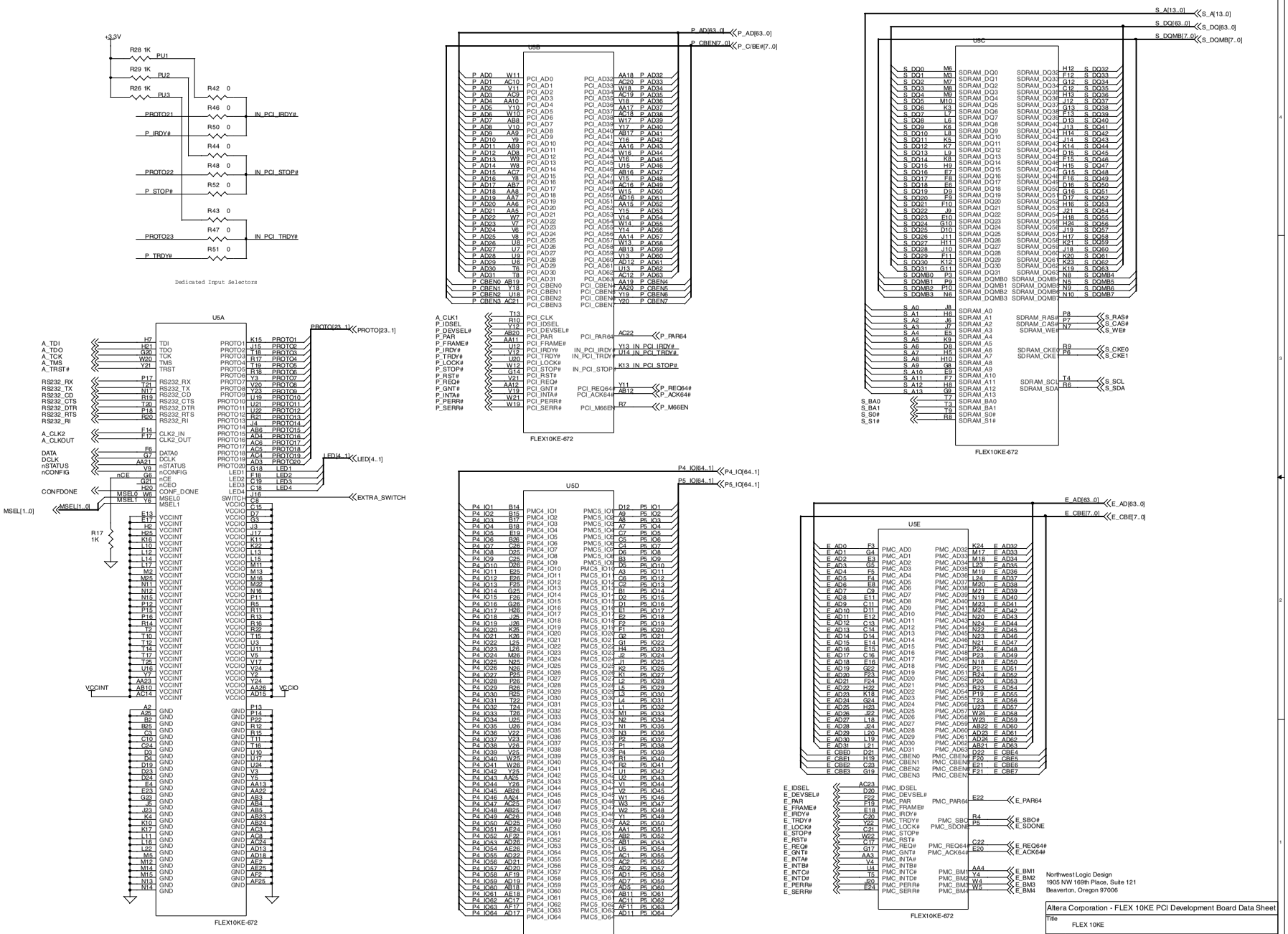
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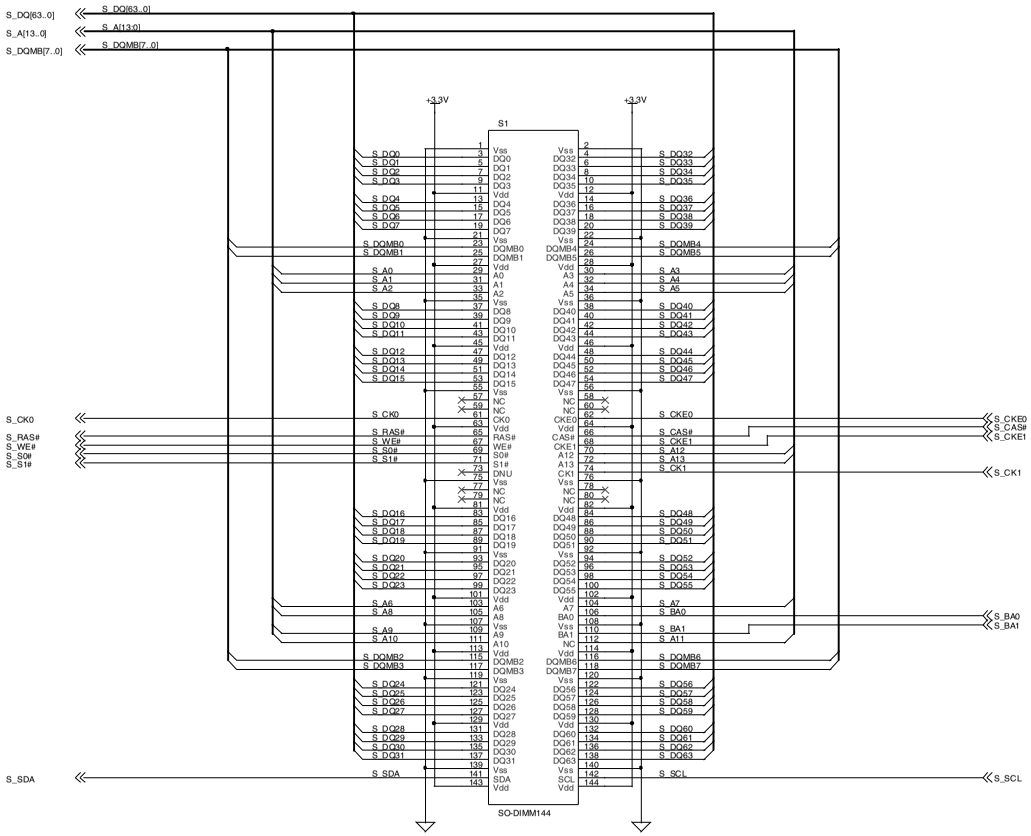

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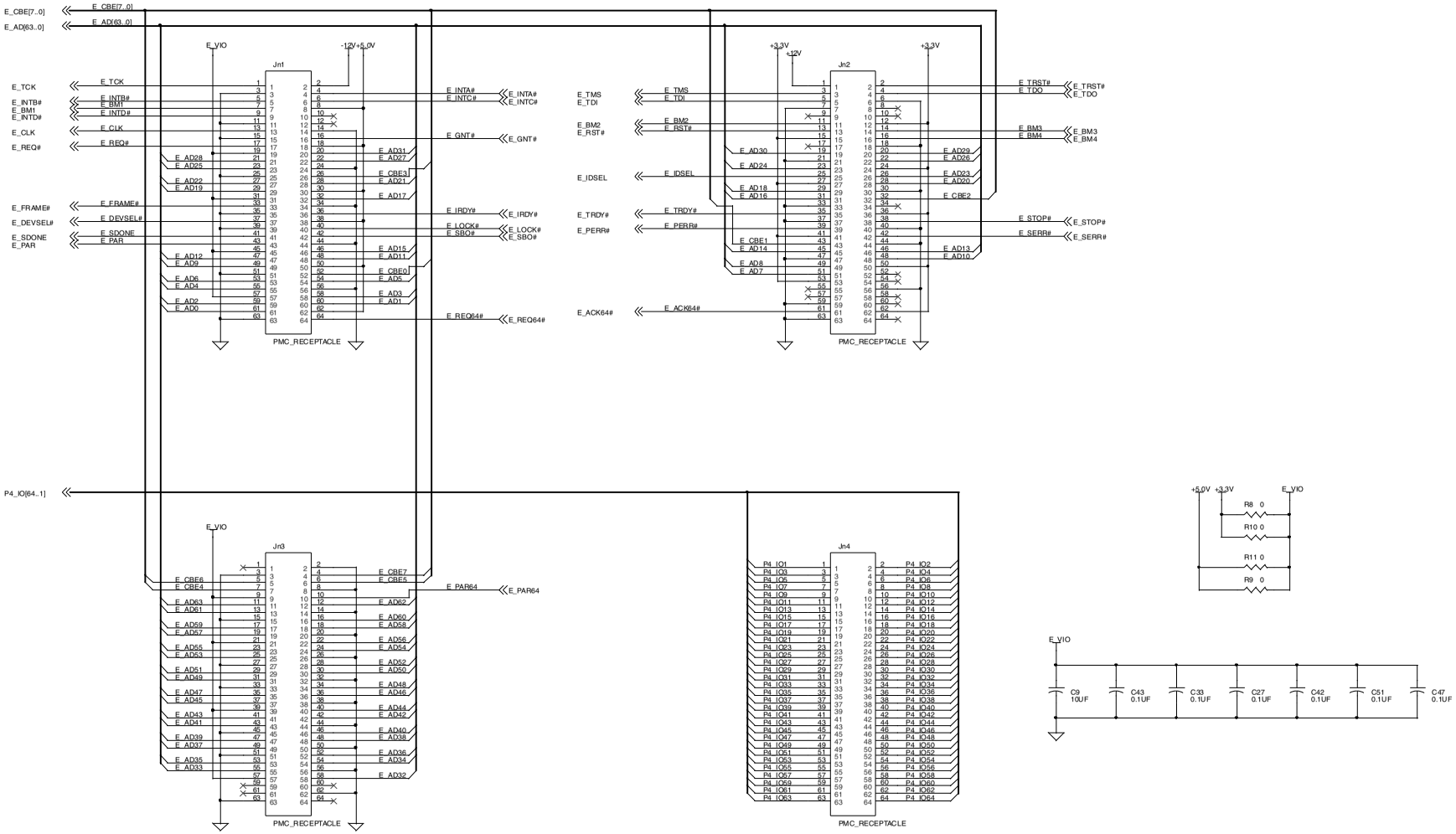

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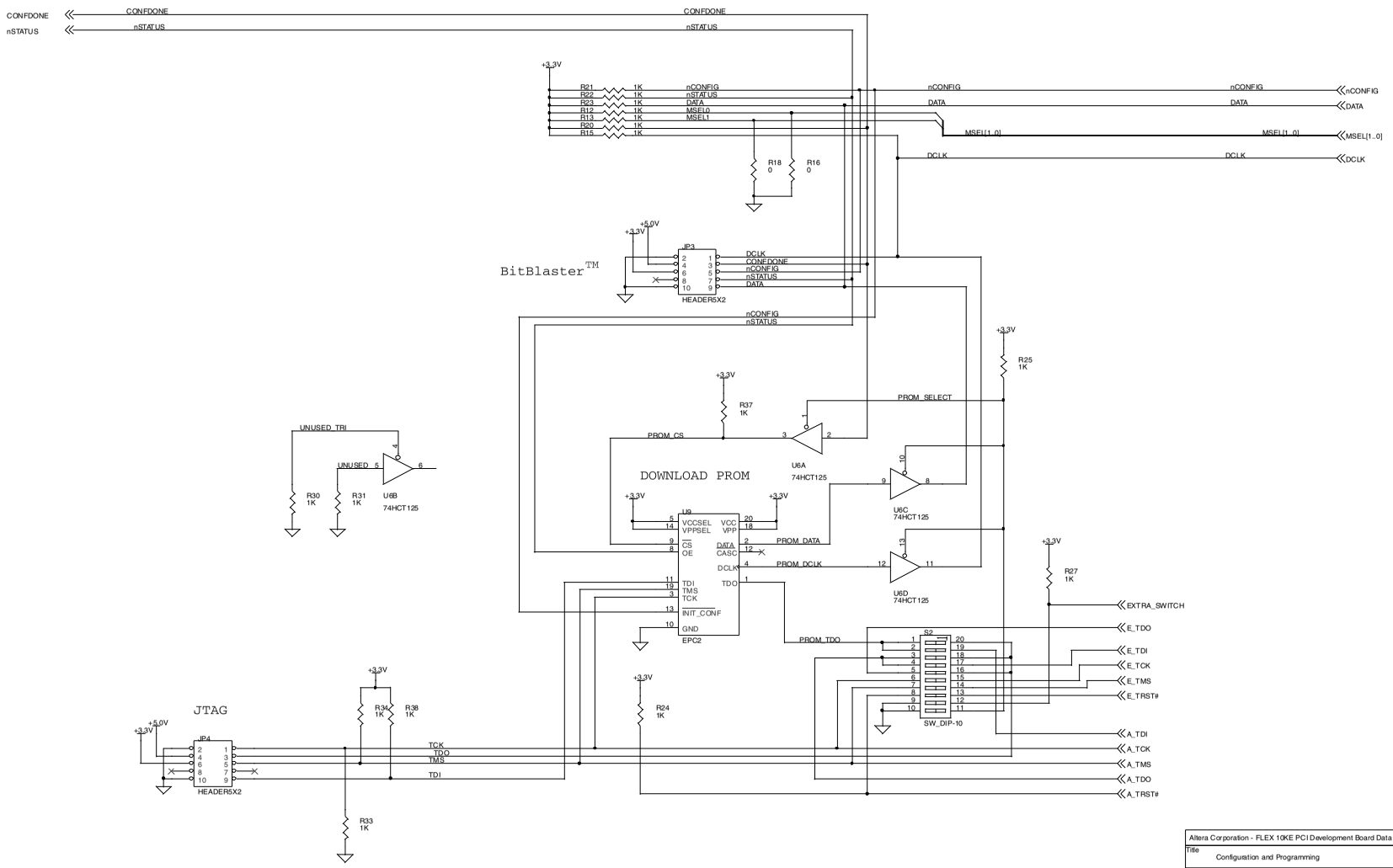
CONFIGURATION LOGIC AND JTAG



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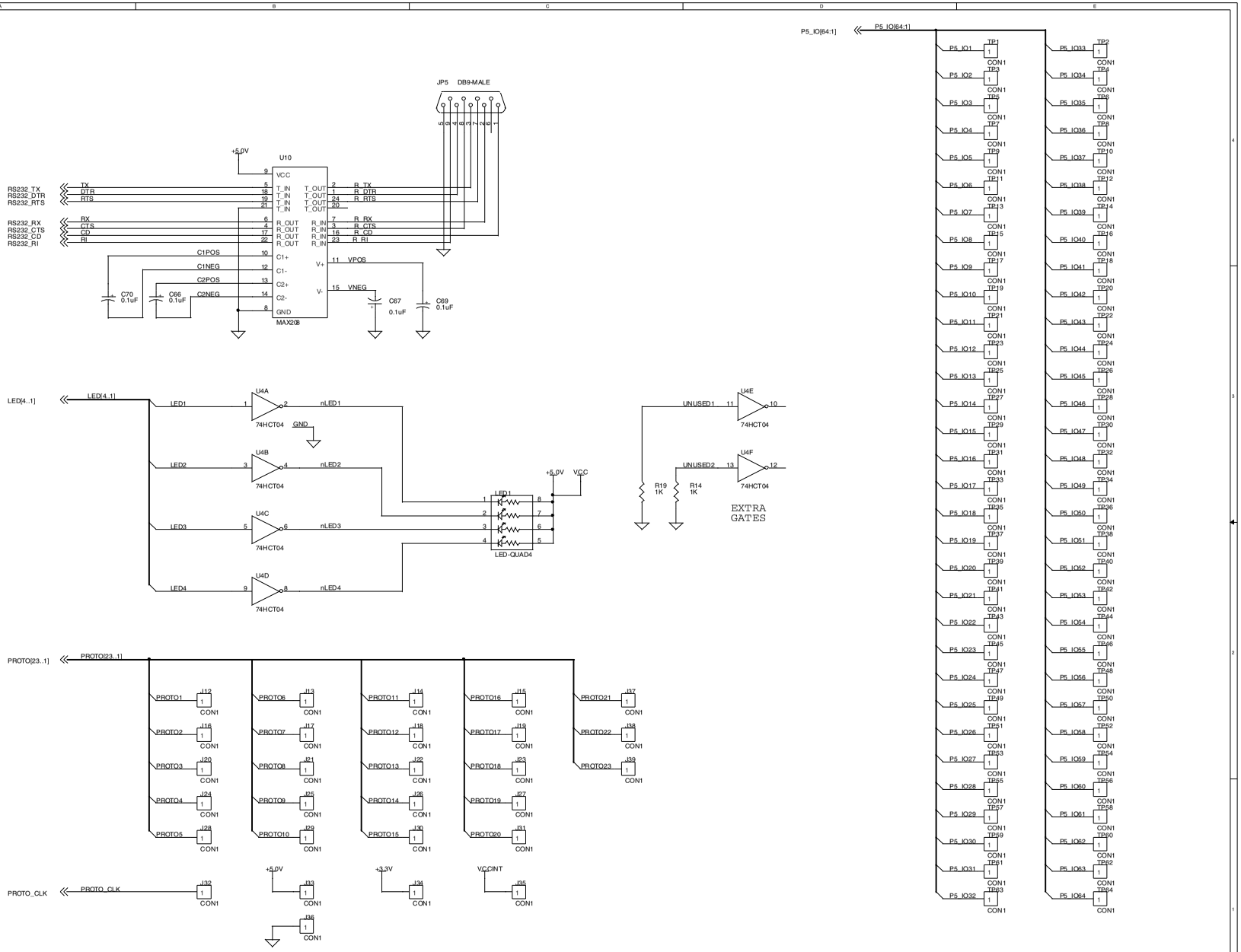

Altera Corporation - FLEX 10KE PCI Development Board Data Sheet	
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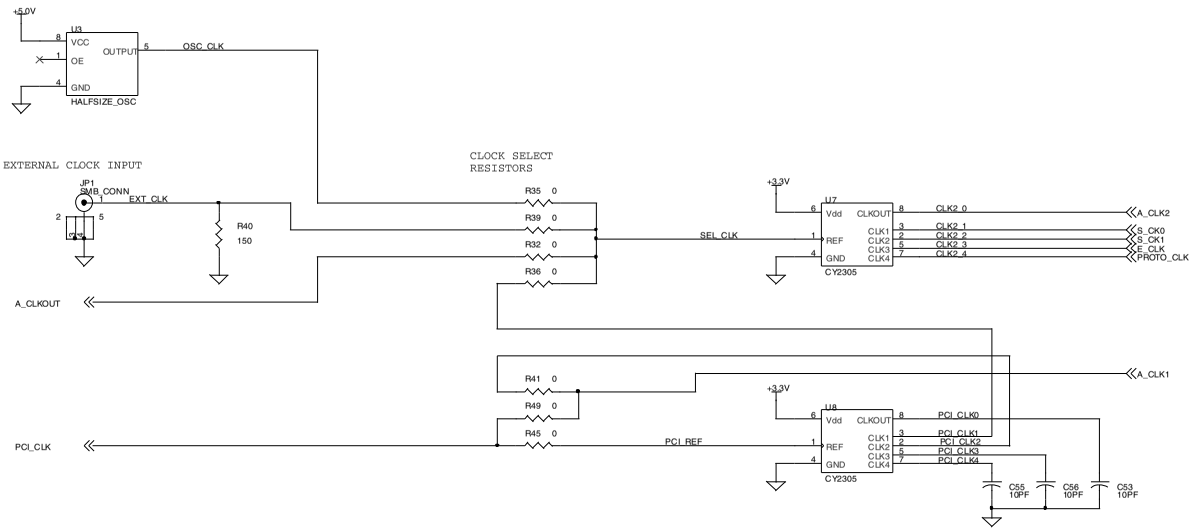

Altera Corporation - FLEX 10KE PCI Development Board Data Sheet		
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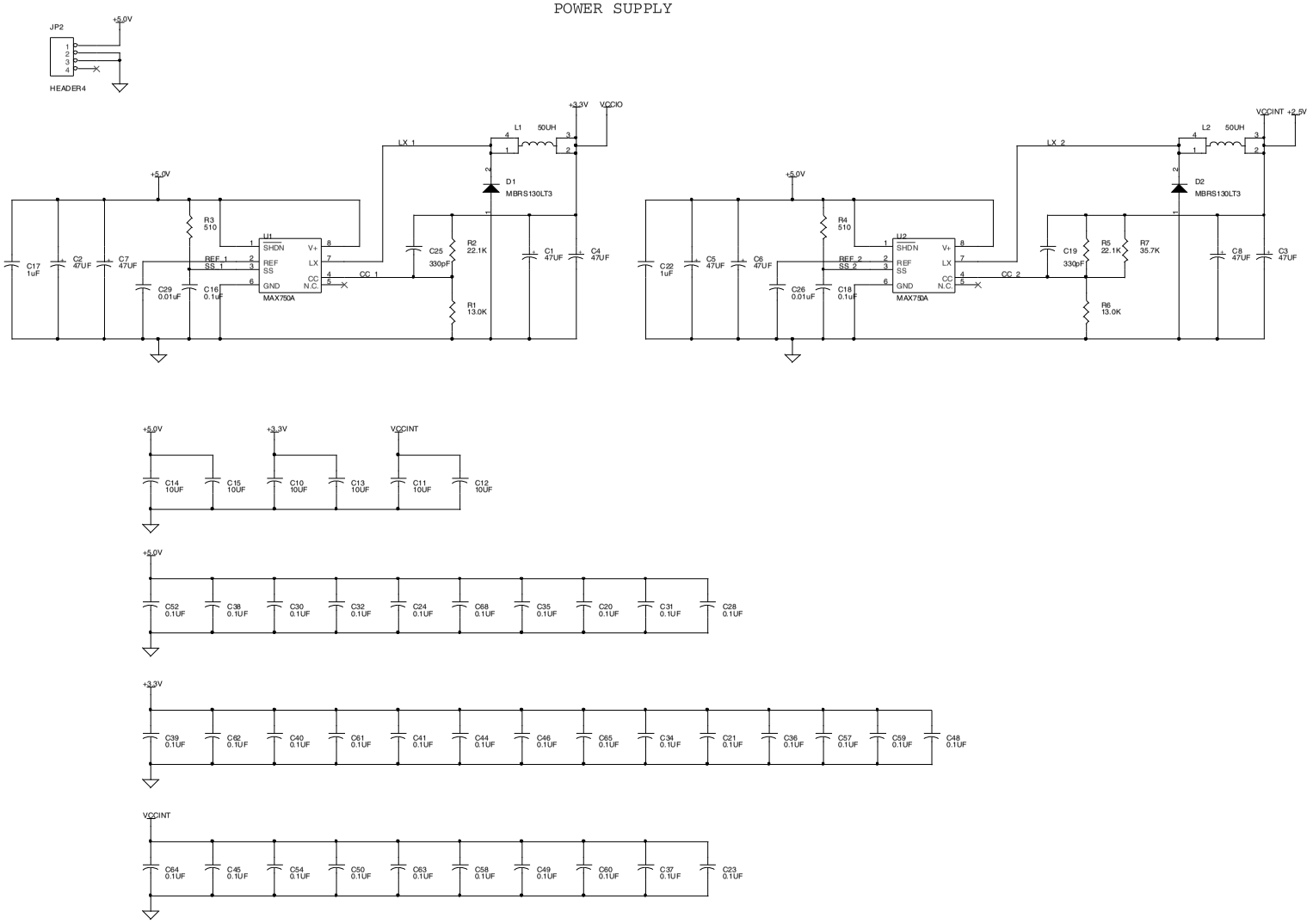
POWER SUPPLY



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Title: Power Supplies		
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