PCMCIA Flash Memory Card ***8 MEGABYTE through 64 MEGABYTE (AMD based)***

General Description

WEDC's PCMCIA Flash memory cards offer the highest density, linear Flash solid state storage solutions for code and data storage, high performance disk emulation and execute in place (XIP) applications in mobile PC and dedicated (embedded) equipment.

Packaged in a PCMCIA type I housing, each card contains a connector, an array of Flash memories packaged in TSOP packages and card control logic. The card control logic provides the system interface and controls the internal Flash memories. Combined with file management software, such as Flash Translation Layer (FTL), WEDC Flash cards provide removable high-performance disk emulation.

The WEDC FLE series is based on AMD Flash memories. The FLE series offers byte wide and word wide operation, low power modes and Card Information Structure (CIS) for easy identification of card characteristics.

Note: Standard options include attribute memory. Cards without attribute memory are available. Cards are also available with or without a hardware write protect switch.

Features

- Very High Density Linear Flash Card
- Supports 5V only systems
- Based on AMD Flash Components
  - -low standby power without entering reset mode
  - -allows standard access from standby mode
- Fast Read Performance
  - 150ns Maximum Access Time
- x8/ x16 Data Interface
- High Performance Random Writes
  - 7µs Typical Word Write Time
- Automated Write and Erase Algorithms
  - AMD Command Set
- 1,000,000 Erase Cycles per Block
- 64K word (128kB) symmetrical Block Architecture
- PC Card Standard Type I Form Factor

Architecture Overview

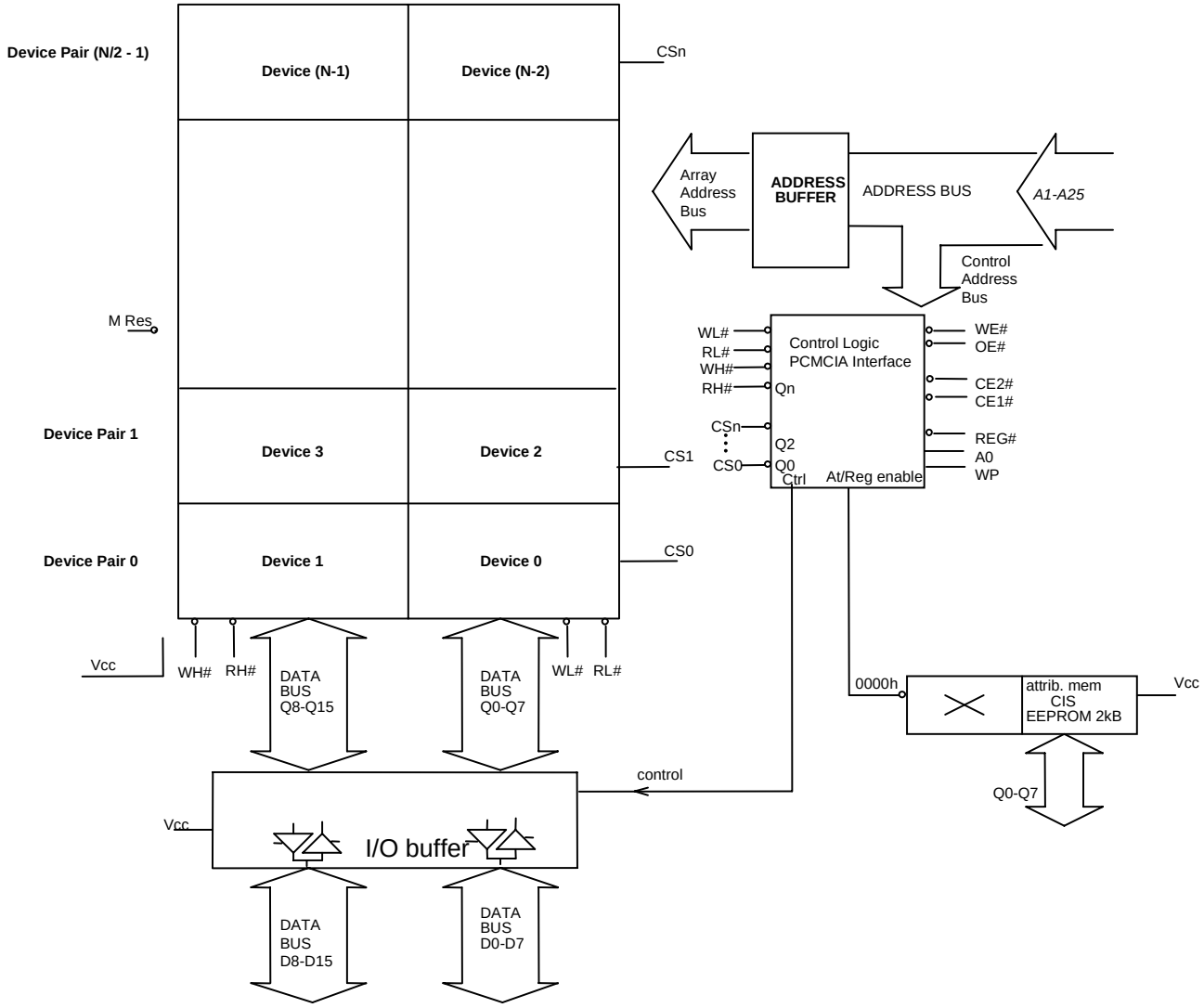
WEDC's FLE series is designed to support up to twenty (see Block diagram) 32Mb components, providing a wide range of density options. Cards are based on the Am29F032 (32Mb) device for 5V only applications. The device code for the Am29F032 is 41h and the manufacturer's ID is 01h. Systems should be able to recognize these codes. Cards utilizing 32Mb components provide densities ranging from 8MB to 64MB in 8MB increments.

In support of the PC Card (PCMCIA) standard for word wide access, devices are paired. Therefore, the Flash array is structured in 64K word blocks. Write, read and block erase operations can be performed as either a word or byte wide operation . By multiplexing A0, CE1# and CE2#, 8-bit hosts can access all data on data lines DQ0 - DQ7. The FLE series cards conform with the PC Card Standard (formerly PCMCIA) and supported JEIDA, providing electrical and physical compatibility. The PC Card form factor offers an industry standard pinout and mechanical outline, allowing density upgrades without system design changes.

WEDC's standard cards are shipped with WEDC's silkscreen design. Cards are also available with blank housings (no silkscreen). The blank housings are available in both a recessed (for label) and flat housing. Please contact your WEDC sales representative for further information on Custom artwork.

Block Diagram

Device type	Manuf ID	Device ID
Am29F032	01_H	41_H



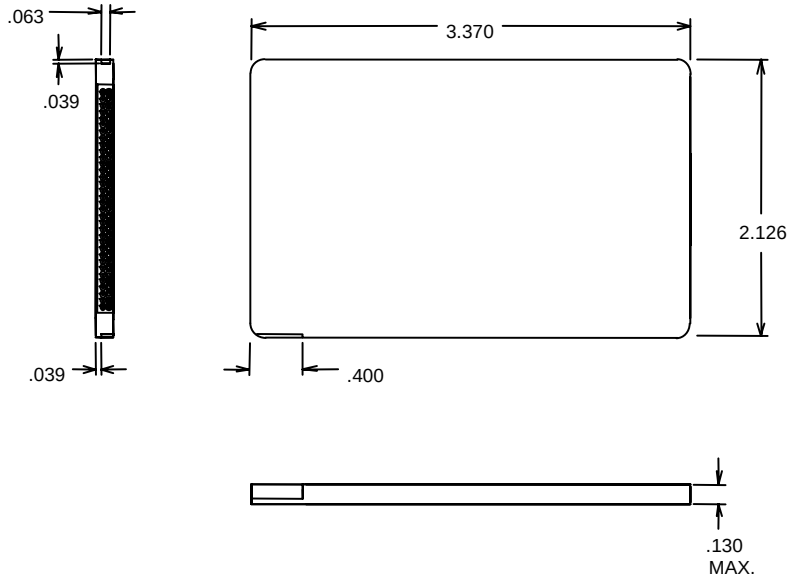
Pinout

Pin	Signal name	I/O	Function	Active
1	GND		Ground	
2	DQ3	I/O	Data bit 3	
3	DQ4	I/O	Data bit 4	
4	DQ5	I/O	Data bit 5	
5	DQ6	I/O	Data bit 6	
6	DQ7	I/O	Data bit 7	
7	CE1#	I	Card enable 1	LOW
8	A10	I	Address bit 10	
9	OE#	I	Output enable	LOW
10	A11	I	Address bit 11	
11	A9	I	Address bit 9	
12	A8	I	Address bit 8	
13	A13	I	Address bit 13	
14	A14	I	Address bit 14	
15	WE#	I	Write Enable	LOW
16	RDY/BSY#	O	Ready/Busy	LOW
17	Vcc		Supply Voltage	
18	Vpp1		Prog. Voltage	N.C.
19	A16	I	Address bit 16	
20	A15	I	Address bit 15	
21	A12	I	Address bit 12	
22	A7	I	Address bit 7	
23	A6	I	Address bit 6	
24	A5	I	Address bit 5	
25	A4	I	Address bit 4	
26	A3	I	Address bit 3	
27	A2	I	Address bit 2	
28	A1	I	Address bit 1	
29	A0	I	Address bit 0	
30	DQ0	I/O	Data bit 0	
31	DQ1	I/O	Data bit 1	
32	DQ2	I/O	Data bit 2	
33	WP	O	Write Potect	HIGH
34	GND		Ground	

Pin	Signal name	I/O	Function	Active
35	GND		Ground	
36	CD1#	O	Card Detect 1	LOW
37	DQ11	I/O	Data bit 11	
38	DQ12	I/O	Data bit 12	
39	DQ13	I/O	Data bit 13	
40	DQ14	I/O	Data bit 14	
41	DQ15	I	Data bit 15	
42	CE2#	I	Card Enable 2	LOW
43	VS1	O	Voltage Sense 1	N.C.
44	RFU		Reserved	
45	RFU		Reserved	
46	A17	I	Address bit 17	
47	A18	I	Address bit 18	
48	A19	I	Address bit 19	
49	A20	I	Address bit 20	
50	A21	I	Address bit 21	
51	Vcc		Supply Voltage	
52	Vpp2		Prog. Voltage	N.C.
53	A22	I	Address bit 22	8MB(3)
54	A23	I	Address bit 23	16MB(3)
55	A24	I	Address bit 24	32MB(3)
56	A25	I	Address bit 25	64MB(3)
57	VS2	O	Voltage Sense 2	N.C.
58	RST	I	Card Reset	HIGH
59	Wait#	O	Extended Bus cycle	LOW(2)
60	RFU		Reserved	
61	REG#	I	Attrib Mem Select	
62	BVD2	O	Bat. Volt. Detect 2	(2)
63	BVD1	O	Bat. Volt. Detect 1	(2)
64	DQ8	I/O	Data bit 8	
65	DQ9	I/O	Data bit 9	
66	DQ10	O	Data bit 10	
67	CD2#	O	Card Detect 2	LOW
68	GND		Ground	

Notes:
1. RDY/BSY is an open drain output, external pull-up resistor is required.
2. Wait#, BVD1 and BVD2 are driven high for compatibility.
3. Shows density for which specified address bit is MSB. Higher order address bits are no connects (i.e., 16MB A23 is MSB A24, A25 are NC).

Mechanical



Card Signal Description

Symbol	Type	Name and Function
A0 - A25	INPUT	**ADDRESS INPUTS:** A0 through A25 enable direct addressing of up to 64MB of memory on the card. Signal A0 is not used in word access mode. A25 is the most significant bit
DQ0 - DQ15	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** DQ0 THROUGH DQ15 constitute the bi-directional databus. DQ15 is the MSB.
CE1#, CE2#	INPUT	**CARD ENABLE 1 AND 2:** CE1# enables even byte accesses, CE2# enables odd byte accesses. Multiplexing A0, CE1# and CE2# allows 8-bit hosts to access all data on DQ0 - DQ7.
OE#	INPUT	**OUTPUT ENABLE:** Active low signal gating read data from the memory card.
WE#	INPUT	**WRITE ENABLE:** Active low signal gating write data to the memory card.
RDY/BSY#	OUTPUT	**READY/BUSY OUTPUT:** Indicates status of internally timed erase or program algorithms. A high output indicates that the card is ready to accept accesses. A low output indicates that one or more devices in the memory card are busy with internally timed erase or write activities.
CD1#, CD2#	OUTPUT	**CARD DETECT 1 and 2:** Provide card insertion detection. These signals are connected to ground internally on the memory card. The host socket interface circuitry shall supply 10K-ohm or larger pull-up resistors on these signal pins.
WP	OUTPUT	**WRITE PROTECT:** Write protect reflects the status of the Write Protect switch on the memory card. WP set to high = write protected, providing internal hardware write lockout to the Flash array. If card does not include optional write protect switch, this signal will be pulled low internally indicating write protect = "off".
VPP1, VPP2	N.C.	**PROGRAM/ERASE POWER SUPPLY:** Not connected for 5V only card.
VCC		**CARD POWER SUPPLY:** 5.0V for all internal circuitry.
GND		**GROUND:** for all internal circuitry.
REG#	INPUT	**ATTRIBUTE MEMORY SELECT :** provides access to Flash memory card registers and Card Information Structure in the Attribute Memory Plane.
RST	INPUT	**RESET:** Active high signal for placing card in Power-on default state. Reset can be used as a Power-Down signal for the memory array.
WAIT#	OUTPUT	**WAIT:** This signal is pulled high internally for compatibility. No wait states are generated.
BVD1, BVD2	OUTPUT	**BATTERY VOLTAGE DETECT:** These signals are pulled high to maintain SRAM card compatibility.
VS1, VS2	OUTPUT	**VOLTAGE SENSE:** Notifies the host socket of the card's VCC requirements. VS1 and VS2 are open to indicate a 5V card has been inserted.
RFU		**RESERVED FOR FUTURE USE**
N.C.		**NO INTERNAL CONNECTION TO CARD:** pin may be driven or left floating

Absolute Maximum Ratings (2)

Operating Temperature TA (ambient)	
Commercial	0°C to +60°C
Industrial	-40°C to +85°C **
Storage Temperature	
Commercial	-30°C to +80°C
Industrial	-40°C to +85°C **
Voltage on any pin relative to V_{SS}	-0.5V to V_{CC}+0.5V (1)
V_{CC} supply Voltage relative to V_{SS}	-0.5V to +7.0V

** Advanced information

Notes:
(1) During transitions, inputs may undershoot to -2.0V or overshoot to V_{CC} +2.0V for periods less than 20ns.

(2) Stress greater than those listed under "Absolute Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Characteristics (1)

Sym	Parameter	Density (Mbytes)	Notes	Typ(4)	Max	Units	Test Conditions
I_{CCR}	V_{CC} Read Current	All		40(5)	75	mA	V_{CC} = V_{CC}max tcycle = 150ns,CMOS levels
I_{CCW}	V_{CC} Program Current	All		30(6)	40(6)	mA	
I_{CCE}	V_{CC} Erase Current	All		30(6)	40(6)	mA	
I_{CCS} (CMOS)	V_{CC} Standby Current	8MB	2,3	50	200	µA	V_{CC} = V_{CC}max Control Signals = V_{CC} Reset = V_{SS}, CMOS levels
		64MB		100	400		

CMOS Test Conditions: V_{CC} = 5V ± 5%, V_{IL} = V_{SS} ± 0.2V, V_{IH} = V_{CC} ± 0.2V

Notes:
1. All currents are RMS values unless otherwise specified. ICCR, ICCW and ICCE are based on Word wide operations.
2. Control Signals: CE_1#, CE_2#, OE#, WE#, REG#.
3. ICCS is specified for lowest density card (8MB for two, 32Mb components) This represents a single pair of devices.
4. Typical: V_{CC} = 5V, T = +25°C.
5. The Icc current is typically less then 1mA/MHz per device, with with OE not active.
6. Icc active while Embedded Program or Erase algorithm is in progress. Value based on one device active.

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
I_{LI}	Input Leakage Current	1		±20	µA	V_{CC} = V_{CC}MAX Vin =V_{CC} or V_{SS}
I_{LO}	Output Leakage Current	1		±20	µA	V_{CC} = V_{CC}MAX Vout =V_{CC} or V_{SS}
V_{IL}	Input Low Voltage	1	0	0.8	V	
V_{IH}	Input High Voltage	1	0.7V_{CC}	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage	1		0.4	V	IOL = 3.2mA
V_{OH}	Output High Voltage	1	V_{CC}-0.4	V_{CC}	V	IOH = -2.0mA
V_{LKO}	V_{CC} Erase/Program Lock Voltage	1	2.0		V	

Notes:
1. Values are the same for byte and word wide modes for all card densities.
2. Exceptions: Leakage currents on CE1#, CE2#, OE#, REG# and WE# will be < 500 µA when VIN = GND due to internal pull-up resistors. Leakage currents on RST will be <150µA when VIN=V_{CC} due to internal pull-down resistor.

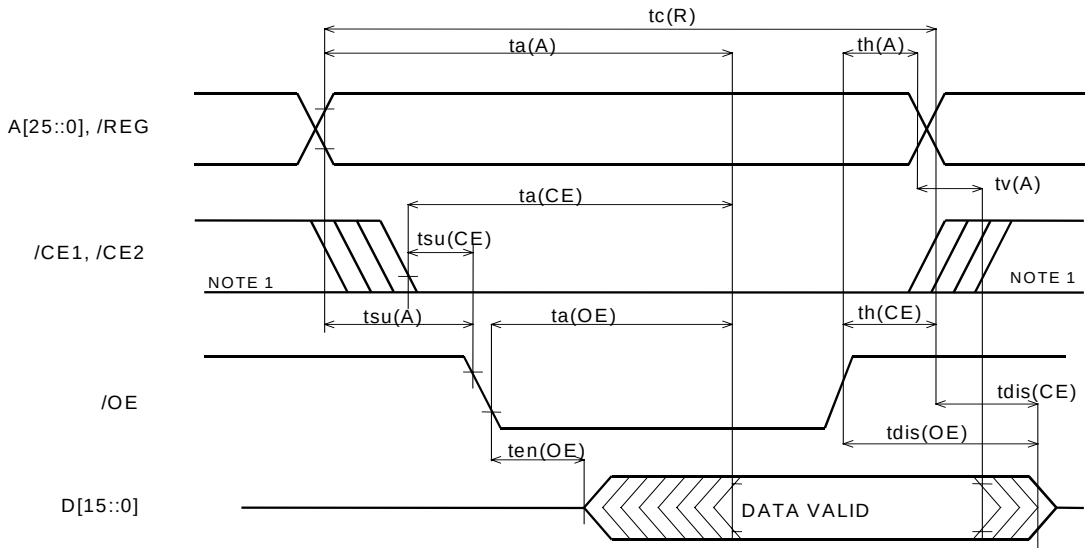
AC Characteristics

Read Timing Parameters

		150ns		
SYM (PCMCIA)	**Parameter**	**Min**	**Max**	**Unit**
t_C(R)	Read Cycle Time	150		ns
t_a(A)	Address Access Time		150	ns
t_a(CE)	Card Enable Access Time		150	ns
t_a(OE)	Output Enable Access Time		75	ns
t_{su}(A)	Address Setup Time	20		ns
t_{su}(CE)	Card Enable Setup Time	0		ns
t_h(A)	Address Hold Time	20		ns
t_h(CE)	Card Enable Hold Time	20		ns
t_v(A)	Output Hold from Address Change	0		ns
t_{dis}(CE)	Output Disable Time from CE#		75	ns
t_{dis}(OE)	Output Disable Time from OE#		75	ns
t_{en}(CE)	Output Enable Time from CE#	5		ns
t_{en}(OE)	Output Enable Time from OE#	5		ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

Read Timing Diagram



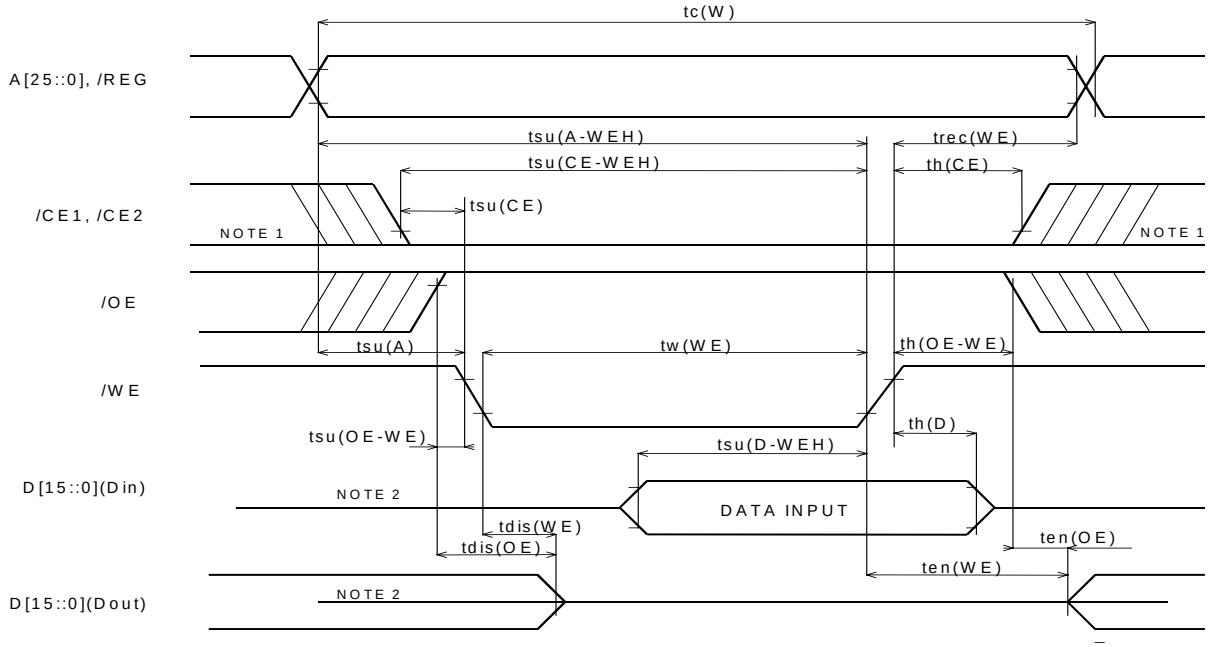
Note: Signal may be high or low in this area.

Write Timing Parameters

		150ns		
SYM (PCMCIA)	**Parameter**	**Min**	**Max**	**Unit**
$t_{C}W$	Write Cycle Time	150		ns
t_{w}(WE)	Write Pulse Width	80		ns
t_{su}(A)	Address Setup Time	20		ns
t_{su}(A-WEH)	Address Setup Time for WE#	100		ns
t_{su}(CE-WEH)	Card Enable Setup Time for WE#	100		ns
t_{su}(D-WEH)	Data Setup Time for WE#	50		ns
t_{h}(D)	Data Hold Time	20		ns
t_{rec}(WE)	Write Recover Time	20		ns
t_{dis}(WE)	Output Disable Time from WE#		75	ns
t_{dis}(OE)	Output Disable Time from OE#		75	ns
t_{en}(WE)	Output Enable Time from WE#	5		ns
t_{en}(OE)	Output Enable Time from OE#	5		ns
t_{su}(OE-WE)	Output Enable Setup from WE#	10		ns
t_{h}(OE-WE)	Output Enable Hold from WE#	10		ns
t_{su}(CE)	Card Enable Setup Time from OE#	0		ns
t_{h}(CE)	Card Enable Hold Time	20		ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

Write Timing Diagram



Notes:
1. Signal may be high or low in this area.
2. When the data I/O pins are in the output state, no signals shall be applied to the data pins (D15 - D0) by the host system.

Data Write and Erase Performance (1,3)

V_{CC} = 5V ± 5%, T_A = 0°C to + 60°C

SYM	Parameter	Notes	Min	Typ(1)	Max	Units	Test Conditions
t_{WHQV1} t_{EHQV1}	Word/Byte Program time	2,4		7	300	µs	Excludes system-level overhead
t_{WHQV2} t_{EHQV2}	Block Program Time	2		0.5	2.0	sec	
	Block Erase Time	2		1	8	sec	Excludes 00h prog. prior to erasure

Notes:
1. Typical: Nominal voltages and T_A = 25°C.
2. Excludes system overhead.
3. Valid for all speed options.
4. To maximize system performance RDY/BSY# signal should be polled.

PRODUCT MARKING

WED 7P016FLE2200C15 C995 9915

- **EDI** — Company Name
- **7P016FLE2200C15** — Part number
- **C995** — Lot code / trace number
- **9915** — Date code

Note:
Some products are currently marked with our pre-merger company name/acronym (EDI). During our transition period, some products will also be marked with our new company name/acronym (WED). Starting October 2000 all PCMCIA products will be marked only with the WED prefix.

PART NUMBERING

7 P 016 FLE22 00 C 15

Card access time

15	150ns
25	250ns

Temperature range

C	Commercial	0°C to +70°C
I	Industrial	-40°C to +85°C

Packaging option

00	Standard, type 1

Card family and version

- See Card Family and Version Info. for details (next page)

Card capacity

016	16MB

PC card

P	Standard PCMCIA
R	Ruggedized PCMCIA

Card technology

7	FLASH
8	SRAM

Ordering Information

EDI7P XXX FLE 22 SS T ZZ ⟶ Based on **Am29F032** for 5V only applications.

where

XXX:	**008**	**8MB**
	016	**16MB**
	024	**24MB**
	032	**32MB**
	040	**40MB**
	048	**48MB**
	056	**56MB**
	064	**64MB**
SS:	**00**	**WEDC Silkscreen**
	01	**Blank Housing, Type I**
	02	**Blank Housing, Type I Recessed**
T:	**C**	**Commercial**
	I	**Industrial**
ZZ:	**15**	**150ns**

Note: Options without attribute memory and with hardware write protect switch are available.

Card families:

FLE 21 - **No Attribute memory, No WP switch**
FLE 22 - **With Attribute Memory, No WP switch**
FLE 23 - **No Attribute Memory, With WP switch**
FLE 24 - **With Attribute Memory, With WP switch**

CIS Information for FLE Series Cards

CIS for FLE22, 150ns

Address	Value	Description
00H	**01H**	**CISTPL_DEVICE**
02H	**03H**	TPL_LINK
04H	**53H**	writable)
06H	**1EH**	CARD SIZE: 8MB
	3EH	16MB
	5EH	24MB
	7EH	32MB
	9EH	40MB
	BEH	48MB
	DEH	56MB
	FEH	64MB
08H	**FFH**	END OF DEVICE
0AH	**18H**	**CISTPL_JEDEC_C**
0CH	**02H**	TPL_LINK
0EH	**01H**	AMD - ID
10H	**41H**	29F032 - ID
12H	**17H**	**CISTPL_DEVICE_A**
14H	**03H**	TPL_LINK
16H	**42H**	EEPROM - 200ns
18H	**01H**	Device Size = 2KBytes
1AH	**FFH**	END OF TUPLE
1CH	**1EH**	**CISTPL_DEVICEGEO**
1EH	**06H**	TPL_LINK
20H	**02H**	DGTPL_BUS
22H	**11H**	DGTPL_EBS
24H	**01H**	DGTPL_RBS
26H	**01H**	DGTPL_WBS
28H	**01H**	DGTPL_PART
2AH	**01H**	FLASH DEVICE NON-INTERLEAVED
2CH	**20H**	**CISTPL_MANFID**
2EH	**04H**	TPL_LINK(04H)
30H	**F6H**	**EDI**TPLMID_MANF: LSB
32H	**01H**	**EDI** PLMID_MANF: MSB
34H	**00H**	*LSB: Number Not Assign.*
36H	**00H**	*MSB: Number Not Assign.*
38H	**15H**	**CISTPL_VERS1**
3AH	**47H**	TPL_LINK
3CH	**04H**	TPLLV1_MAJOR
3EH	**01H**	TPLLV1_MINOR

Address	Value	Description
40H	**45H**	E
42H	**44H**	D
44H	**49H**	I
46H	**37H**	7
48H	**50H**	P
4AH	**30H**	0
4CH	1)	x
4EH	1)	x
50H	**46H**	F
52H	**4CH**	L
54H	**45H**	E
56H	**32H**	2
58H	2)	x
5AH	**2DH**	-
5CH	**2DH**	-
5EH	**2DH**	-
60H	**31H**	1
62H	**35H**	5
64H	**20H**	SPACE
66H	**00H**	END TEXT
68H	**43H**	C
6AH	**4FH**	O
6CH	**50H**	P
6EH	**59H**	Y
70H	**52H**	R
72H	**49H**	I
74H	**47H**	G
76H	**48H**	H
78H	**54H**	T
7AH	**20H**	SPACE
7CH	**45H**	E
7EH	**4CH**	L
80H	**45E**	E
82H	**43H**	C
84H	**54H**	T
86H	**52H**	R
88H	**4FH**	O
8AH	**4EH**	N
8CH	**49H**	I
8EH	**43H**	C
90H	**20H**	SPACE
92H	**44H**	D

Address	Value	Description
94H	**45H**	E
96H	**53H**	S
98H	**49H**	I
9AH	**47H**	G
9CH	**4EH**	N
9EH	**53H**	S
A0H	**20H**	SPACE
A2H	**49H**	I
A4H	**4EH**	N
A6H	**43H**	C
A8H	**4FH**	O
AAH	**52H**	R
ACH	**50H**	P
AEH	**4FH**	O
B0H	**52H**	R
B2H	**41H**	A
B4H	**54H**	T
B6H	**45H**	E
B8H	**44H**	D
BAH	**20H**	SPACE
BCH	**00H**	END TEXT
BEH	**31H**	1
C0H	**39H**	9
C2H	**39H**	9
C4H	**39H**	9
C6H	**00H**	END TEXT
C8H	**00H**	END OF LIST

1)

Address	Value	Description
4CH	30	0
	31	1
	32	2
	33	3
	34	4
	36	6
4EH	30	0
	32	2
	34	4
	36	6
	38	8

2)

Address	Value	Description
58H	32	2
	34	4

REVISION HISTORY		
Date of revision	**Version**	**Description**
7-Feb-98	-001	Initial release
27-May-99	-002	Logo change
31-May-00	-003	Added page 9, Heading changed on all pgs
1-Aug-00	-004	Corrected Timing Errors, pgs. 6&7

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