#### **PCMCIA Flash Memory Card**

### 8 MEGABYTE through 64 MEGABYTE (AMD based)

• WHITE ELECTRONIC DESIGNS

#### **General Description**

WEDC's PCMCIA Flash memory cards offer the highest density, linear Flash solid state storage solutions for code and data storage, high performance disk emulation and execute in place (XIP) applications in mobile PC and dedicated (embedded) equipment.

Packaged in a PCMCIA type I housing, each card contains a connector, an array of Flash memories packaged in TSOP packages and card control logic. The card control logic provides the system interface and controls the internal Flash memories. Combined with file management software, such as Flash Translation Layer (FTL), WEDC Flash cards provide removable high-performance disk emulation.

The WEDC FLE series is based on AMD Flash memories. The FLE series offers byte wide and word wide operation, low power modes and Card Information Structure (CIS) for easy identification of card characteristics.

Note: Standard options include attribute memory. Cards without attribute memory are available. Cards are also available with or without a hardware write protect switch.

### Architecture Overview

#### **Features**

- Very High Density Linear Flash Card
- Supports 5V only systems
- •Based on AMD Flash Components -low standby power without entering reset mode -allows standard access from standby mode
- •Fast Read Performance - 150ns Maximum Access Time
- x8/ x16 Data Interface
- High Performance Random Writes - 7µs Typical Word Write Time
- Automated Write and Erase Algorithms - AMD Command Set
- 1,000,000 Erase Cycles per Block
- 64K word (128kB) symmetrical Block Architecture
- PC Card Standard Type I Form Factor

WEDC's FLE series is designed to support up to twenty (see Block diagram) 32Mb components, providing a wide range of density options. Cards are based on the Am29F032 (32Mb) device for 5V only applications. The device code for the Am29F032 is 41h and the manufacturer's ID is 01h. Systems should be able to recognize these codes. Cards utilizing 32Mb components provide densities ranging from 8MB to 64MB in 8MB increments.

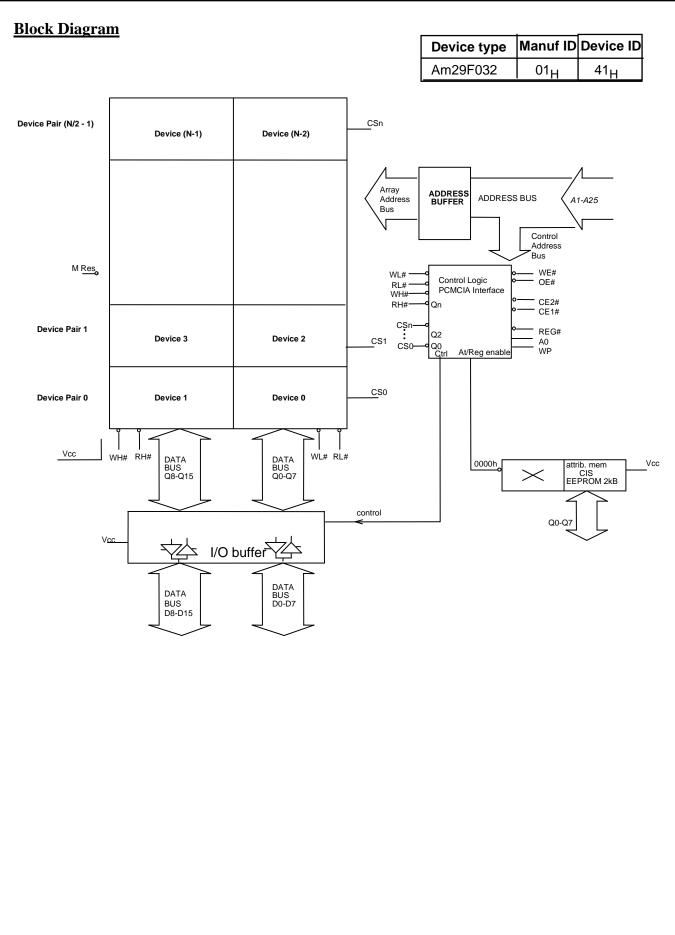
In support of the PC Card (PCMCIA) standard for word wide access, devices are paired. Therefore, the Flash array is structured in 64K word blocks. Write, read and block erase operations can be performed as either a word or byte wide operation . By multiplexing A0, CE1# and CE2#, 8-bit hosts can access all data on data lines DQ0 - DQ7. The FLE series cards conform with the PC Card Standard (formerly PCMCIA) and supported JEIDA, providing electrical and physical compatibility. The PC Card form factor offers an industry standard pinout and mechanical outline, allowing density upgrades without system design changes.

WEDC's standard cards are shipped with WEDC's silkscreen design. Cards are also available with blank housings (no silkscreen). The blank housings are available in both a recessed (for label) and flat housing. Please contact your WEDC sales representative for further information on Custom artwork.

# **PCMCIA Flash Memory Card**



## **FLE Series**



### **Pinout**

Pin	Signal name	I/O	Function	Active
1	GND		Ground	
2	DQ3	I/O	Data bit 3	
3	DQ4	I/O	Data bit 4	
4	DQ5	I/O	Data bit 5	
5	DQ6	I/O	Data bit 6	
6	DQ7	I/O	Data bit 7	
7	CE1#		Card enable 1	LOW
8	A10		Address bit 10	
9	OE#	I	Output enable	LOW
10	A11		Address bit 11	
11	A9	Ι	Address bit 9	
12	A8	I	Address bit 8	
13	A13	I	Address bit 13	
14	A14	Ι	Address bit 14	
15	WE#	I	Write Enable	LOW
16	RDY/BSY#	0	Ready/Busy	LOW
17	Vcc		Supply Voltage	
18	Vpp1		Prog. Voltage	N.C.
19	A16	_	Address bit 16	
20	A15	_	Address bit 15	
21	A12	_	Address bit 12	
22	A7	_	Address bit 7	
23	A6	_	Address bit 6	
24	A5	I	Address bit 5	
25	A4		Address bit 4	
26	A3	- 1	Address bit 3	
27	A2		Address bit 2	
28	A1	Ι	Address bit 1	
29	A0	Ι	Address bit 0	
30	DQ0	I/O	Data bit 0	
31	DQ1	I/O	Data bit 1	
32	DQ2	I/O	Data bit 2	
33	WP	0	Write Potect	HIGH
34	GND		Ground	

Pin	Signal name	I/O	Function	Active
35	GND		Ground	
36	CD1#	0	Card Detect 1	LOW
37	DQ11	I/O	Data bit 11	
38	DQ12	I/O	Data bit 12	
39	DQ13	I/O	Data bit 13	
40	DQ14	I/O	Data bit 14	
41	DQ15	I	Data bit 15	
42	CE2#	I	Card Enable 2	LOW
43	VS1	0	Voltage Sense 1	N.C.
44	RFU		Reserved	
45	RFU		Reserved	
46	A17	-	Address bit 17	
47	A18	-	Address bit 18	
48	A19	-	Address bit 19	
49	A20	1	Address bit 20	
50	A21	1	Address bit 21	
51	Vcc		Supply Voltage	
52	Vpp2		Prog. Voltage	N.C.
53	A22	Ι	Address bit 22	8MB(3)
54	A23	Ι	Address bit 23	16MB(3)
55	A24	_	Address bit 24	32MB(3)
56	A25	-	Address bit 25	64MB(3)
57	VS2	0	Voltage Sense 2	N.C.
58	RST		Card Reset	HIGH
59	Wait#	0	Extended Bus cycle	LOW (2)
60	RFU		Reserved	
61	REG#		Attrib Mem Select	
62	BVD2	0	Bat. Volt. Detect 2	(2)
63	BVD1	0	Bat. Volt. Detect 1	(2)
64	DQ8	I/O	Data bit 8	
65	DQ9	I/O	Data bit 9	
66	DQ10	0	Data bit 10	
67	CD2#	0	Card Detect 2	LOW
68	GND		Ground	

• WHITE ELECTRONIC DESIGNS

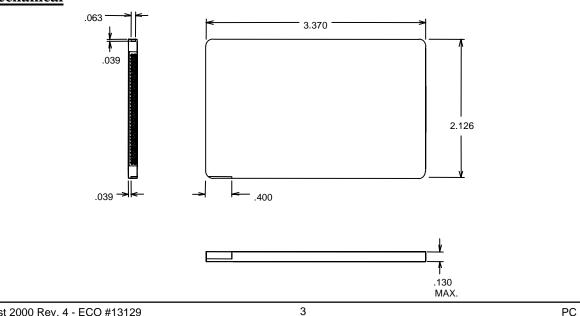
#### Notes:

1. RDY/BSY is an open drain output, external pull-up resistor is required.

2. Wait#, BVD1 and BVD2 are driven high for compatibility.

3. Shows density for which specified address bit is MSB. Higher order address bits are no connects (i.e., 16MB A23 is MSB A24, A25 are NC).

## **Mechanical**





# **Card Signal Description**

Symbol	Туре	Name and Function
A0 - A25	INPUT	ADDRESS INPUTS: A0 through A25 enable direct addressing of
		up to 64MB of memory on the card. Signal A0 is not used in word
		access mode. A25 is the most significant bit
DQ0 - DQ15	INPUT/OUTPUT	<b>DATA INPUT/OUTPUT:</b> DQ0 THROUGH DQ15 constitute the
		bi-directional databus. DQ15 is the MSB.
CE1#, CE2#	INPUT	CARD ENABLE 1 AND 2: CE1# enables even byte accesses, CE2#
		enables odd byte accesses. Multiplexing A0, CE1# and CE2# allows
		8-bit hosts to access all data on DQ0 - DQ7.
OE#	INPUT	<b>OUTPUT ENABLE:</b> Active low signal gating read data from the
		memory card.
WE#	INPUT	WRITE ENABLE: Active low signal gating write data to the
		memory card.
RDY/BSY#	OUTPUT	<b>READY/BUSY OUTPUT:</b> Indicates status of internally timed erase
		or program algorithms. A high output indicates that the card is ready
		to accept accesses. A low output indicates that one or more devices
		in the memory card are busy with internally timed erase or write
		activities.
CD1#, CD2#	OUTPUT	CARD DETECT 1 and 2: Provide card insertion detection. These
		signals are connected to ground internally on the memory card. The
		host socket interface circuitry shall supply 10K-ohm or larger pull-up
		resistors on these signal pins.
WP	OUTPUT	WRITE PROTECT: Write protect reflects the status of the Write
		Protect switch on the memory card. WP set to high = write protected,
		providing internal hardware write lockout to the Flash array.
		If card does not include optional write protect switch, this signal will
		be pulled low internally indicating write protect = "off".
VPP1, VPP2	N.C.	PROGRAM/ERASE POWER SUPPLY: Not connected for 5V
		only card.
VCC		<b>CARD POWER SUPPLY:</b> 5.0V for all internal circuitry.
GND		<b>GROUND:</b> for all internal circuitry.
REG#	INPUT	ATTRIBUTE MEMORY SELECT : provides access to Flash
		memory card registers and Card Information Structure in the
		Attribute Memory Plane.
RST	INPUT	<b>RESET:</b> Active high signal for placing card in Power-on default
		state. Reset can be used as a Power-Down signal for the memory
		array.
WAIT#	OUTPUT	WAIT: This signal is pulled high internally for compatibility. No
		wait states are generated.
BVD1, BVD2	OUTPUT	<b>BATTERY VOLTAGE DETECT:</b> These signals are pulled high to
		maintain SRAM card compatibility.
VS1, VS2	OUTPUT	VOLTAGE SENSE: Notifies the host socket of the card's VCC
		requirements. VS1 and VS2 are open to indicate a 5V card has been
		inserted.
RFU		RESERVED FOR FUTURE USE
N.C.		NO INTERNAL CONNECTION TO CARD: pin may be driven
		or left floating



### Absolute Maximum Ratings (2)

Operating Temperature TA (ambient)		(
Commercial	0°C to +60°C	t
Industrial	-40°C to +85°C **	I
Storage Temperature		(
Commercial	-30°C to +80°C	,
Industrial	-40°C to +85°C **	
Voltage on any pin relative to V <sub>SS</sub>	-0.5V to V <sub>CC</sub> +0.5V (1)	
$V_{\rm CC}$ supply Voltage relative to $V_{\rm SS}$	-0.5V to +7.0V	t

\*\* Advanced information

#### Notes:

(1) During transitions, inputs may undershoot to -2.0V or overshoot to V $_{\rm CC}$  +2.0V for periods less than 20ns.

(2) Stress greater than those listed under "Absolute Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

# **DC Characteristics** <sup>(1)</sup>

Sym	Parameter	Density (Mbytes)	Notes	Typ <sup>(4)</sup>	Max	Units	Test Conditions
I <sub>CCR</sub>	V <sub>CC</sub> Read Current	All		40(5)	75	mA	$V_{CC} = V_{CC}max$ tcycle = 150ns,CMOS levels
I <sub>CCW</sub>	V <sub>CC</sub> Program Current	All		30(6)	40(6)	mA	
I <sub>CCE</sub>	V <sub>CC</sub> Erase Current	All		30(6)	40(6)	mA	
I <sub>CCS</sub>	V <sub>CC</sub> Standby Current	8MB	2,3	50	200	μA	$V_{CC} = V_{CC}max$
(CMOS)		64MB		100	400		Control Signals = $V_{CC}$ Reset = $V_{SS}$ , CMOS levels

CMOS Test Conditions: V<sub>CC</sub> = 5V  $\pm$  5%, VIL = V<sub>SS</sub>  $\pm$  0.2V, VIH = V<sub>CC</sub>  $\pm$  0.2V

#### Notes:

- 1. All currents are RMS values unless otherwise specified. ICCR, ICCW and ICCE are based on Word wide operations.
- 2. Control Signals: CE1#, CE2#, OE#, WE#, REG#.
- 3. ICCS is specified for lowest density card (8MB for two, 32Mb components) This represents a single pair of devices.
- 4. Typical:  $V_{CC} = 5V$ , T = +25°C.

5. The lcc current is typically less then 1mA/MHz per device, with with OE not active.

6. Icc active while Embedded Program or Erase algorithm is in progress. Value based on one device active.

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
I <sub>LI</sub>	Input Leakage Current	1		±20	μΑ	$V_{CC} = V_{CC}MAX$ Vin = V <sub>CC</sub> or V <sub>SS</sub>
I <sub>LO</sub>	Output Leakage Current	1		±20	μΑ	$V_{CC} = V_{CC}MAX$ Vout = $V_{CC}$ or $V_{SS}$
V <sub>IL</sub>	Input Low Voltage	1	0	0.8	V	
V <sub>IH</sub>	Input High Voltage	1	$0.7V_{CC}$	V <sub>CC</sub> +0.5	V	
V <sub>OL</sub>	Output Low Voltage	1		0.4	V	IOL = 3.2mA
V <sub>OH</sub>	Output High Voltage	1	V <sub>CC</sub> -0.4	V <sub>CC</sub>	V	IOH = -2.0mA
V <sub>lko</sub>	V <sub>CC</sub> Erase/Program Lock Voltage	1	2.0		V	

#### Notes:

1. Values are the same for byte and word wide modes for all card densities.

 Exceptions: Leakage currents on CE1#, CE2#, OE#, REG# and WE# will be < 500 μA when VIN = GND due to internal pull-up resistors. Leakage currents on RST will be <150μA when VIN=V<sub>CC</sub> due to internal pull-down resistor.

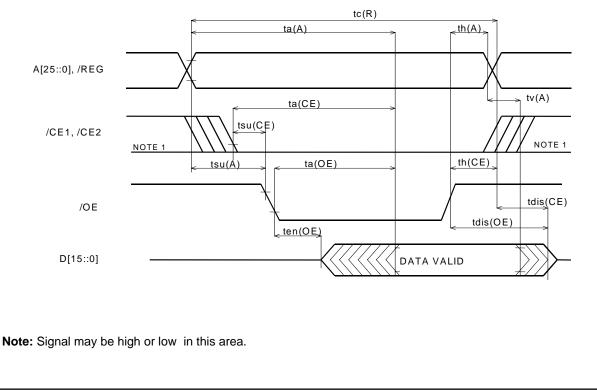
### **AC Characteristics**

#### **Read Timing Parameters**

		150ns		
SYM (PCMCIA)	Parameter	Min	Max	Unit
$t_{\rm C}(R)$	Read Cycle Time	150		ns
t <sub>a</sub> (A)	Address Access Time		150	ns
t <sub>a</sub> (CE)	Card Enable Access Time		150	ns
t <sub>a</sub> (OE)	Output Enable Access Time		75	ns
t <sub>su</sub> (A)	Address Setup Time	20		ns
t <sub>su</sub> (CE)	Card Enable Setup Time	0		ns
t <sub>h</sub> (A)	Address Hold Time	20		ns
t <sub>h</sub> (CE)	Card Enable Hold Time	20		ns
t <sub>v</sub> (A)	Output Hold from Address Change	0		ns
t <sub>dis</sub> (CE)	Output Disable Time from CE#		75	ns
t <sub>dis</sub> (OE)	Output Disable Time from OE#		75	ns
t <sub>en</sub> (CE)	Output Enable Time from CE#	5		ns
t <sub>en</sub> (OE)	Output Enable Time from OE#	5		ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

### Read Timing Diagram



Write Timing Parameters

		150ns		
SYM (PCMCIA)	Parameter	Min	Max	Unit
t <sub>c</sub> W	Write Cycle Time	150		ns
t <sub>w</sub> (WE)	Write Pulse Width	80		ns
t <sub>su</sub> (A)	Address Setup Time	20		ns
t <sub>su</sub> (A-WEH)	Address Setup Time for WE#	100		ns
t <sub>su</sub> (CE-WEH)	Card Enable Setup Time for WE#	100		ns
t <sub>su</sub> (D-WEH)	Data Setup Time for WE#	50		ns
t <sub>h</sub> (D)	Data Hold Time	20		ns
t <sub>rec</sub> (WE)	Write Recover Time	20		ns
t <sub>dis</sub> (WE)	Output Disable Time from WE#		75	ns
t <sub>dis</sub> (OE)	Output Disable Time from OE#		75	ns
t <sub>en</sub> (WE)	Output Enable Time from WE#	5		ns
t <sub>en</sub> (OE)	Output Enable Time from OE#	5		ns
t <sub>su</sub> (OE-WE)	Output Enable Setup from WE#	10		ns
t <sub>h</sub> (OE-WE)	Output Enable Hold from WE#	10		ns
t <sub>su</sub> (CE)	Card Enable Setup Time from OE#	0		ns
t <sub>h</sub> (CE)	Card Enable Hold Time	20		ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

#### tc(W) A[25::0], /REG tsu(A-WEH) trec(WE) tsu(CE-WEH) th(CE) tsu(CE) /C E 1 , /C E 2 NOTE 1 NOTE 1 /O E th (OE-WE) tsu(A) tw(WE) /W E th(D) tsu(OE-WE) tsu(D-WEH) D[15::0](Din) NOTE 2 DATA INPUT tdis(WE) ten<u>(</u>OE) ten(WE) NOTE 2 D[15::0](Dout)

#### Write Timing Diagram

#### Notes:

1. Signal may be high or low in this area.

 When the data I/O pins are in the output state, no signals shall be applied to the data pins (D15 - D0) by the host system.



### **Data Write and Erase Performance** <sup>(1,3)</sup>

 $V_{CC} = 5V \pm 5\%$ ,  $T_A = 0^{\circ}C$  to + 60°C

SYM	Parameter Note		Min	Typ <sup>(1)</sup>	Max	Units	Test Conditions	
t <sub>wHQV1</sub> t <sub>EHOV1</sub>	Word/Byte Program time	te Program time 2,4		7	, , , , , , , , , , , , , , , , , , ,		Excludes system-level overhead	
t <sub>WHQV2</sub> t <sub>EHOV2</sub>	Block Program Time	2		0.5	2.0	sec		
	Block Erase Time	2		1	8	sec	Excludes 00h prog. prior to erasure	

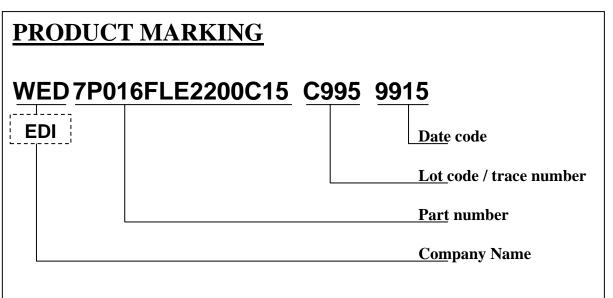
#### Notes:

1. Typical: Nominal voltages and  $T_A = 25^{\circ}C$ .

2. Excludes system overhead.

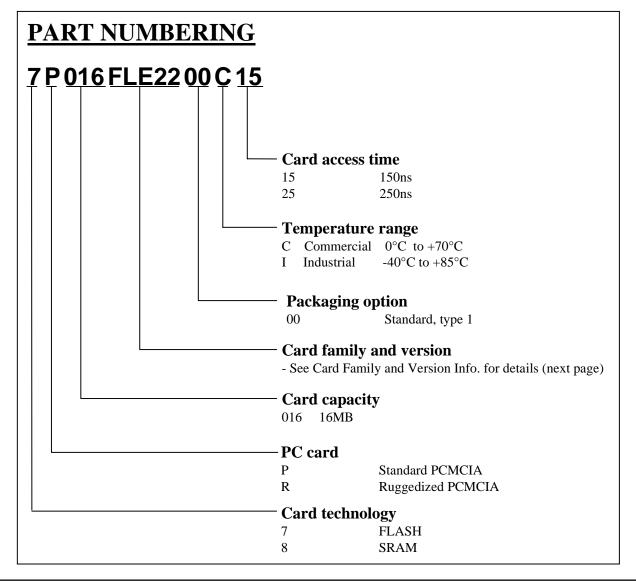
3. Valid for all speed options.

4. To maximize system performance RDY/BSY# signal should be polled.



#### Note:

Some products are currently marked with our pre-merger company name/acronym (EDI). During our transition period, some products will also be marked with our new company name/acronym (WED). Starting October 2000 all PCMCIA products will be marked only with the WED prefix.



# **PCMCIA Flash Memory Card**



# **FLE Series**

**Ordering Information** 

where

XXX:	008	8MB
	016	16MB
	024	24MB
	032	32MB
	040	40MB
	048	48MB
	056	56MB
	064	64MB
SS:	00	WEDC Silkscreen
	01	Blank Housing, Type I
	02	Blank Housing, Type I Recessed
T:	С	Commercial
	Ι	Industrial
ZZ:	15	150ns

Note: Options without attribute memory and with hardware write protect switch are available.

#### Card families:

FLE 21	- No Attribute memory, No WP switch	

- FLE 22 With Attribute Memory, No WP switch
- FLE 23 No Attribute Memory, With WP switch
- FLE 24 With Attribute Memory, With WP switch



## **CIS Information for FLE Series Cards**

# CIS for FLE22, 150ns

Address       Value       Description       Address       Value       Description       Address       Value       Description         00H       01H       CISTPL_DEVICE       40H       45H       E         04H       33H       Writable)       44H       44H       D         06H       1EH       CARD SIZ: 8MB       46H       37H       7         06H       1EH       CARD SIZ: 8MB       46H       37H       7         3EH       16MB       48H       50H       P       9CH       47H       7         9EH       40MB       42H       1)       X       AdH       47H       7         9EH       40MB       42H       1)       X       AdH       47H       8H       5         9EH       40MB       52H       4CH       L       AdH       47H       0       AdH       7H       C         0H       1H       AMD       52H       2////////////////////////////////////									
Both       Close PL_DINCE       43h       43h       E       96h       53h       S         04H       53H       writable)       44H       49H       1       98h       49h       1         06H       1EH       CARD SIZE: 8MB       48h       37H       7       9CH       4EH       N         06H       1EH       CARD SIZE: 8MB       48h       37H       7       9CH       4EH       N         06H       1EH       CARD SIZE: 8MB       48H       50H       9CH       40h       SZA         9EH       40MB       48H       50H       0       ACH       49H       1         9EH       40MB       52H       4CH       1       X       AdH       4EH       N         0BH       FFH       END OF DEVICE       58H       32H       2       ACH       49H       1         0AH       1H       AMD - ID       5CH       32H       2       ACH       5H       2H       ACH       5H       2H       ACH       4H       0         0CH       02H       TELLINK		Value	· · · · · · · · · · · · · · · · · · ·			•			•
Odf       Odf       Odf       IPL_LINK       Part       Part <t< td=""><td></td><td>01H</td><td>CISTPL_DEVICE</td><td></td><td>45H</td><td></td><td>-</td><td></td><td></td></t<>		01H	CISTPL_DEVICE		45H		-		
OHH       55H       Writable)       44H       49H       1         06H       1EH       CARD SZE: SMB       46H       37H       7         96H       1EH       CARD SZE: SMB       48H       50H       P         96H       42MB       44H       30H       0       9CH       42H       N         96H       32MB       4CH       1)       X       AOH       20H       SPACE         7EH       32MB       4CH       1)       X       AdH       4EH       N         96H       46MB       52H       4CH       L       A8H       4FH       O         08H       FFH       64MB       54H       45H       E       A8H       4FH       O         0AH       18H       CISTPL_JEDEC_C       58H       2DH       B8H       4HH       A         0CH       02H       TPL_LINK       5AH       2DH       B8H       4HH       A         12H       17H       CISTPL_DEVICE_A       60H       3HH       1       B8H       4HH       A         12H       0H	02H	03H	TPL_LINK	42H	44H	D			5
06H       1EH       CARD Size: 8MB       48H       37H       7         3EH       16MB       48H       50H       P       9CH       4EH       N         3EH       24MB       4AH       30H       0       3EH       3SH       S         9EH       32MB       4CH       1)       x       AdH       4BH       SAH         9EH       40MB       50H       4EH       1)       x       AdH       HEH       N         9EH       40MB       52H       4CH       L       AdH       4EH       N         0BH       FFH       END OF DEVICE       56H       32H       2       X       AdH       4EH       O         0AH       18H       CISTPL_JEDEC_C       58H       2)       X       AEH       4FH       O         0AH       18H       CISTPL_JEDEC_C       58H       2DH       -       BOH       52H       R         0CH       02H       TPL_LINK       62H       33H       1       AEH       4FH       O         10H       AIH       2DFU_LINK	04H	53H	writable)	44H	49H	-			G
3EH       16MB       48H       50H       P         SEH       24MB       4AH       30H       0       ADH       20H       SPCE         9EH       40MB       4CH       1)       x       ADH       20H       SPACE         9EH       40MB       4EH       1)       x       ADH       49H       1         9EH       40MB       50H       4EH       1)       x       ADH       49H       1         9EH       40MB       50H       4CH       L       ABH       43H       C         0EH       56MB       52H       4CH       L       ABH       4FH       0         0AH       18H       CISTPL_JEDECC       58H       2)       x       AEH       4FH       0         0CH       02H       TPL_LINK       5AH       2DH       -       B2H       41H       A         10H       41H       29F032 · ID       5EH       2DH       -       B2H       41H       A         12H       17H       CISTPL_DEVICE_A       60H       33H       C       C	06H	1EH	CARD SIZE: 8MB	46H	37H				
SEH       24MB       4AH       30H       0         7EH       32MB       4CH       1)       x       AQH       20H       SPACE         9EH       40MB       4EH       1)       x       AQH       49H       1         0BH       FEH       40MB       50H       46H       F       AQH       49H       1         0BH       FFH       64MB       50H       46H       F       ABH       42H       N         08H       FFH       END OF DEVICE       56H       32H       2       ACH       49H       C         0AH       18H       CISTPL_JEDEC_C       58H       32H       2       ACH       47H       O         0CH       02H       TPL_LINK       5AH       2DH       -       BBH       44H       D       B2H       41H       A         10H       41H       29F032 - ID       5EH       2DH       -       B2H       41H       A         12H       01H       CISTPL_DEVICE A       60H       00H       END TEXT       BBH       54H       1 <tr< td=""><td></td><td>3EH</td><td>16MB</td><td>48H</td><td>50H</td><td>Р</td><td></td><td></td><td></td></tr<>		3EH	16MB	48H	50H	Р			
7EH       32MB       4CH       1)       x       A2H       49H       1         9EH       40MB       50H       4EH       1)       x       A4H       4EH       N         DEH       56MB       52H       4CH       L       A8H       4FH       O         0EH       FEH       64MB       54H       45H       E       AAH       4FH       O         0BH       FFH       END OF DEVICE       56H       32H       2       ACH       52H       R         0CH       02H       TPL_LINK       5AH       2DH       -       B0H       52H       R         0CH       02H       TPL_LINK       5AH       2DH       -       B2H       41H       A         10H       AMH       TPL_LINK       62H       35H       5       BAH       42H       E       BH       4H       T         12H       17H       CISTPL_DEVICE_A       60H       3H       1       BH       4H       D         14H       03H       TPLLINK       62H       35H       5       BAH <td></td> <td>5EH</td> <td>24MB</td> <td>4AH</td> <td>30H</td> <td>0</td> <td></td> <td></td> <td></td>		5EH	24MB	4AH	30H	0			
9EH       40MB       4EH       1)       x       A4H       4EH       N         BEH       48MB       50H       46H       F       A6H       43H       4CH       43H       C         DEH       56MB       52H       4CH       L       A8H       4FH       O         08H       FFH       END OF DEVICE       56H       32H       2       ACH       50H       P         0AH       18H       CISTPL_JEDEC_C       58H       2D       X       ACH       4FH       O         0CH       02H       TPL_LINK       5AH       2DH       -       B0H       52H       R         0EH       01H       AMD - ID       5CH       2DH       -       B2H       41H       A         10H       41H       29F032 · ID       5EH       2DH       -       B4H       54H       T         12H       01H       CISTPL_DEVICE_A       60H       31H       1       B8H       44H       D         14H       01H       Derroresize = 2KBytes       66H       00H       END TEXT       B8H <td></td> <td>7EH</td> <td>32MB</td> <td>4CH</td> <td>1)</td> <td>x</td> <td></td> <td></td> <td>1</td>		7EH	32MB	4CH	1)	x			1
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		9EH	40MB	4EH	1)	х			N
DEH FEH       56MB       52H       4CH       L       A8H       4FH       O         08H       FFH       END OF DEVICE       56H       32H       2       AAH       52H       R         08H       FFH       END OF DEVICE       56H       32H       2       AAH       52H       R         00H       18H       CISTPL_JEDEC_C       58H       2)       x       AEH       4FH       O         00CH       02H       TPL_LINK       5AH       2DH       -       B0H       52H       R         01H       AMD -D       5CH       2DH       -       B4H       54H       T         12H       17H       CISTPL_DEVICE_A       60H       31H       1       B6H       45H       E         14H       03H       TPL_LINK       62H       35H       5       B8H       44H       D         16H       42H       EEPROM-200ns       64H       20H       SPACE       BCH       00H       EDTPL         18H       0H       DeviceSize 2KBytes       66H       59H       Y       C6H		BEH	48MB	50H	46H	F			
FEH       64MB       54H       45H       E       AAH       52H       R         08H       FFH       END OF DEVICE       56H       32H       2       ACH       50H       P         0AH       18H       CISTPL_JEDEC_C       58H       2)       X       ACH       50H       P         0CH       02H       TPL_LINK       5AH       2DH       -       B0H       52H       R         0EH       01H       AMD - ID       5CH       2DH       -       B2H       41H       A         10H       41H       29F032 - ID       5EH       2DH       -       B2H       41H       A         12H       01H       CISTPL_DEVICE_A       60H       31H       1       BEH       58H       44H       D         14H       03H       TPL_LINK       62H       35H       5       BAH       20H       SPACE         18H       01H       Device Size = 2KBytes       66H       00H       END TEXT       BEH       31H       1         12H       06H       TPL_LINK       62H       59H		DEH	56MB	52H	4CH	L			
08H       FFH       END OF DEVICE       56H       32H       2       ACH       50H       P         0AH       18H       CISTPL_JEDEC C       58H       2)       x       ACH       4FH       O         0CH       02H       TPL_LINK       5AH       2DH       -       B0H       52H       R         0CH       01H       AMD ID       5CH       2DH       -       B2H       41H       A         10H       41H       29F032 · ID       5EH       2DH       -       BAH       54H       T         12H       17H       CISTPL_DEVICE_A       60H       31H       1       BAH       20H       SPACE         14H       03H       TPL_LINK       62H       35H       5       BAH       20H       SPACE         18H       01H       Device Size = 2KBytes       66H       00H       END TEXT       BCH       31H       1         12H       61H       DGTPL_EBS       70H       52H       R       C4H       39H       9         22H       11H       DGTPL_RBS       72H       49H </td <td></td> <td>FEH</td> <td>64MB</td> <td>54H</td> <td>45H</td> <td>E</td> <td></td> <td></td> <td></td>		FEH	64MB	54H	45H	E			
OAH       18H       CISTPL_JEDEC_C       58H       2)       x       AEH       4FH       O         0CH       02H       TPL_LINK       5AH       2DH       -       BOH       52H       R         0EH       01H       AMD - ID       5CH       2DH       -       B2H       41H       A         10H       41H       29F032 - ID       5EH       2DH       -       B2H       41H       A         12H       17H       CISTPL_DEVICE_A       60H       31H       1       B6H       45H       E         14H       03H       TPL_LINK       62H       35H       5       BAH       20H       SPACE         18H       01H       Device Size = 2KBytes       66H       00H       END TEXT       BEH       31H       1         1CH       1EH       CISTPL_DEVICEGEO       6AH       4FH       O       CH       39H       9         2CH       02H       DGTPL_BUS       6EH       59H       Y       CH       0H       END TEXT         2H       01H       DGTPL_RAST       7CH	08H	FFH	END OF DEVICE	56H	32H	2			
OCH       O2H       TPL_LINK       5AH       2DH       -       BOH       52H       R         0EH       01H       AMD - ID       5CH       2DH       -       B2H       41H       A         10H       41H       29F032 - ID       5EH       2DH       -       B4H       54H       T         12H       17H       CISTPL_DEVICE_A       60H       31H       1       B6H       45H       E         14H       03H       TPL_LINK       62H       33H       5       B8H       44H       D       D         16H       42H       EEPROM - 200ns       64H       20H       SPACE       BAH       20H       SPACE         18H       01H       Device Size = 2KBytes       66H       00H       END TEXT       BEH       31H       1         1CH       1EH       CISTPL_DEVICEGEO       6AH       4FH       O       C2H       39H       9         20H       02H       DGTPL_BS       72H       49H       I       C4H       39H       9         24H       01H       DGTPL_PART       7	0AH	18H	CISTPL JEDEC C	58H	2)	х			0
0EH       01H       AMD - ID       5CH       2DH       -       B2H       41H       A         10H       41H       29F032 - ID       5EH       2DH       -       BdH       5H       T         12H       17H       CISTPL_DEVICE A       60H       31H       1       BdH       5H       2DH       -       BdH       45H       E         14H       03H       TPL_LINK       62H       35H       5       BdH       44H       D         16H       42H       EEPROM-200ns       64H       20H       SPACE       BCH       00H       END TEXT         18H       01H       Device Size = 2KBytes       66H       00H       END TEXT       BEH       31H       1       -         10CH       1EH       CISTPL_DEVICEGEO       6AH       4FH       O       C2H       39H       9         20H       02H       DGTPL_EBS       70H       52H       R       C6H       00H       END TEXT         24H       01H       DGTPL_EBS       72H       49H       1       Addres       30H       22	0CH			5AH	,	-			
10H       41H       29F032 · ID       5EH       2DH       -       B4H       54H       T         12H       17H       CISTPL_DEVICE_A       60H       31H       1       B6H       45H       E         14H       03H       TPL_LINK       62H       35H       5       B8H       20H       D         16H       42H       EEPROM-200ns       64H       20H       SPACE       BCH       00H       END F         18H       01H       Device Size = 2KBytes       66H       00H       END TEXT       BCH       00H       END TEXT         1AH       FFH       END OF TUPLE       68H       43H       C       C0H       39H       9         1CH       1EH       OGH       TPL_LINK       6CH       50H       P       C2H       39H       9         20H       02H       DGTPL_BUS       6EH       59H       Y       C6H       00H       END OF LIST         24H       01H       DGTPL_PART       76H       48H       H       1       Address       Value       0       0         22H			AMD - ID			-	B2H	41H	
12H       17H       CISTPL_DEVICE_A       00H       3'H       1         14H       03H       TPL_INK       62H       35H       5         18H       01H       Device Size = 2KBytes       66H       20H       SPACE       BAH       20H       SPACE         18H       01H       Device Size = 2KBytes       66H       20H       SPACE       BCH       00H       END TEXT         1AH       FFH       END OF TUPLE       68H       43H       C       COH       39H       9         1CH       1EH       CISTPL_DEVICEGEO       6AH       4FH       O       C2H       39H       9         20H       02H       DGTPL_BUS       6EH       59H       Y       C6H       00H       END TEXT         22H       11H       DGTPL_RBS       72H       49H       I       C8H       00H       END OF LIST         24H       01H       DGTPL_RBS       72H       49H       I       Address       Value       Description         22H       01H       DGTPL_MANFID       7CH       45H       E       31       1	10H	41H	29F032 - ID	5EH	2DH	-	B4H	54H	
14H       03H       1FL_LINK       62H       35H       3         16H       42H       EEPROM-200ns       64H       20H       SPACE         18H       01H       Device Size = 2KBytes       66H       00H       END TEXT         18H       01H       Device Size = 2KBytes       66H       00H       END TEXT         1AH       FFH       END OF TUPLE       68H       43H       C       COH       39H       9         1CH       1EH       06H       TPL_LINK       6CH       50H       P       C2H       39H       9         20H       02H       DGTPL_BUS       6EH       59H       Y       C6H       00H       END TEXT         22H       11H       DGTPL_RBS       72H       49H       I       C6H       00H       END TEXT         24H       01H       DGTPL_PART       76H       48H       T       Address       Value       Description         24H       01H       DGTPL_MANFID       7CH       45H       E       31       1         24H       0H       TPL_LINK(04H)       7EH	12H	17H	CISTPL DEVICE A	60H	31H	1	B6H	45H	E
16H       42H       EEPROM - 200ns       64H       20H       SPACE       BAH       20H       SPACE         18H       01H       Device Size = 2KBytes       66H       00H       END TEXT       BCH       00H       END TEXT         1AH       FFH       END OF TUPLE       68H       43H       C       COH       39H       9         1CH       1EH       CISTPL_DEVICEGEO       6AH       4FH       O       COH       39H       9         20H       02H       DGTPL_BUS       6EH       59H       Y       C6H       00H       END TEXT         22H       11H       DGTPL_BUS       6EH       59H       Y       C6H       00H       END TEXT         24H       01H       DGTPL_RBS       72H       49H       I       C8H       00H       END TEXT         28H       01H       DGTPL_PART       76H       48H       H       1       Address       Value       Description         22H       04H       TPL_LINK(04H)       7CH       45H       E       33       3         32H       01H       ED	14H	03H	TPL_LINK	62H	35H	5		44H	
18H       01H       Device Size = 2KBytes       66H       00H       END TEXT       BCH       00H       END TEXT         1AH       FFH       END OF TUPLE       68H       43H       C       BCH       39H       9         1CH       1EH       CISTPL_DEVICEGEO       6AH       4FH       O       C2H       39H       9         20H       02H       DGTPL_BUS       6EH       59H       Y       C4H       39H       9         20H       02H       DGTPL_BUS       6EH       59H       Y       C6H       00H       END TEXT         22H       11H       DGTPL_BUS       72H       49H       1       C3H       0H       END TEXT         24H       01H       DGTPL_RBS       72H       49H       1       C8H       00H       END TEXT         28H       01H       DGTPL_PART       76H       48H       T       Address       Value       Description         2CH       20H       CISTPL_MANFID       7CH       45H       T       Address       4CH       30       0         30H       F6H	16H		EEPROM - 200ns	64H		SPACE	BAH	20H	SPACE
1AH       FFH       END OF TUPLE       68H       43H       C         1CH       1EH       CISTPL_DEVICEGEO       6AH       4FH       O         1EH       06H       TPL_LINK       6CH       50H       P         20H       02H       DGTPL_BUS       6EH       59H       Y         22H       11H       DGTPL_EBS       70H       52H       R         24H       01H       DGTPL_RBS       72H       49H       1         26H       01H       DGTPL_PART       76H       48H       H         28H       01H       DGTPL_PART       76H       48H       H         2AH       01H       FLASH DEVICE       78H       54H       T         NON-INTERLEAVED       7AH       20H       SPACE       30       0         2CH       20H       CISTPL_MANFID       7CH       45H       E       33       3         32H       01H       EDI PLMID_MANF: LSB       80H       45E       E       33       3         34H       00H       LSB: Number Not Assign.       84H       54H       <	18H		Device Size = 2KBytes	66H		END TEXT		00H	END TEXT
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	1AH			68H		С			
1EH       06H       TPL_LINK       6CH       50H       P         20H       02H       DGTPL_BUS       6EH       59H       Y         22H       11H       DGTPL_EBS       70H       52H       R         24H       01H       DGTPL_RBS       72H       49H       I         26H       01H       DGTPL_PART       76H       48H       H         28H       01H       DGTPL_PART       76H       48H       H         2AH       01H       FLASH DEVICE       78H       54H       T         Address       Value       Description         4CH       30       0         2CH       20H       CISTPL_MANFID       7CH       45H       E         30H       F6H       EDITPLMID_MANF: LSB       80H       45E       E       33       3         32H       01H       EDI PLMID_MANF: LSB       80H       45H       T       4EH       30       0         34H       00H       LSB: Number Not Assign.       8H       52H       R       36       6         34H       1H			CISTPL DEVICEGEO	6AH		0			
20H       02H       DGTPL_BUS       6EH       59H       Y         22H       11H       DGTPL_EBS       70H       52H       R         24H       01H       DGTPL_RBS       72H       49H       I         26H       01H       DGTPL_RBS       72H       49H       I         26H       01H       DGTPL_PART       76H       48H       H         2AH       01H       DGTPL_PART       76H       48H       H         2AH       01H       FLASH DEVICE       78H       54H       T         Address       Value       Description         4CH       30       0         2CH       20H       CISTPL_MANFID       7CH       45H       E         30H       F6H       EDITPLMID_MANF: LSB       80H       45E       E       33       3         32H       01H       EDI PLMID_MANF: MSB       82H       43H       C       36       6         34H       00H       LSB: Number Not Assign.       86H       52H       R       36       6         34H       1H       TPL_LINK						Р			
22H       11H       DGTPL_EBS       70H       52H       R         24H       01H       DGTPL_RBS       72H       49H       I         26H       01H       DGTPL_WBS       72H       49H       I         26H       01H       DGTPL_WBS       74H       47H       G         28H       01H       DGTPL_PART       76H       48H       H         2AH       01H       DGTPL_MANFID       7CH       48H       H         2AH       01H       FLASH DEVICE       78H       54H       T         NON-INTERLEAVED       7AH       20H       SPACE       30       0         2CH       20H       CISTPL_MANFID       7CH       45H       E       31       1         2EH       04H       TPL_LINK(04H)       7EH       4CH       L       33       3         32H       01H       EDIPLMID_MANF: LSB       80H       45E       E       33       3         34H       00H       LSB: Number Not Assign.       84H       54H       T       4EH       30       0         36H						Y			
24H       01H       DGTPL_RBS       72H       49H       I         26H       01H       DGTPL_WBS       74H       47H       G         28H       01H       DGTPL_PART       76H       48H       H         2AH       01H       DGTPL_PART       76H       48H       H         2AH       01H       DGTPL_MARFID       76H       48H       H         2AH       01H       FLASH DEVICE       78H       54H       T         NON-INTERLEAVED       7AH       20H       SPACE       4CH       30       0         2CH       20H       CISTPL_MANFID       7CH       45H       E       31       1         2EH       04H       TPL_LINK(04H)       7EH       4CH       L       33       3         32H       01H       EDI PLMID_MANF: MSB       82H       43H       C       34       4         34H       00H       LSB: Number Not Assign.       84H       54H       T       4EH       30       0         36H       00H       Assign.       86H       52H       R       34									
26H       01H       DGTPL_WBS       74H       47H       G         28H       01H       DGTPL_PART       76H       48H       H       1)         2AH       01H       FLASH DEVICE       78H       54H       T       Address       Value       Description         2CH       20H       CISTPL_MANFID       7CH       45H       E       4CH       30       0         2CH       20H       CISTPL_MANFID       7CH       45H       E       31       1         2EH       04H       TPL_LINK(04H)       7EH       4CH       L       32       2         30H       F6H       EDITPLMID_MANF: LSB       80H       45E       E       33       3         32H       01H       EDI PLMID_MANF: MSB       82H       43H       C       36       6         34H       00H       LSB: Number Not Assign.       84H       54H       T       4EH       30       0         36H       00H       Assign.       86H       52H       R       32       2         38H       15H       CISTPL_VERS1       8							C8H	00H	END OF LIST
28H     01H     DGTPL_PART     76H     48H     H       2AH     01H     FLASH DEVICE     78H     54H     T       2CH     20H     CISTPL_MANFID     7CH     45H     E       2EH     04H     TPL_LINK(04H)     7EH     4CH     L     32     2       30H     F6H     EDITPLMID_MANF: LSB     80H     45E     E     33     3       32H     01H     EDI PLMID_MANF: MSB     82H     43H     C     36     6       34H     00H     LSB: Number Not Assign.     84H     54H     T     4EH     30     0       36H     00H     Assign.     86H     52H     R     32     2     34       38H     15H     CISTPL_VERS1     88H     4FH     O     34     4       36H     00H     TPL_LINK     8AH     4EH     N     36     6       38H     15H     CISTPL_VERS1     88H     4FH     O     34     4       36H     01H     TPLLV1_MAJOR     8CH     49H     1     36     6 </td <td></td> <td></td> <td></td> <td>74H</td> <td></td> <td>G</td> <td></td> <td></td> <td></td>				74H		G			
2AH       01H       FLASH DEVICE NON-INTERLEAVED       78H       54H       T       Address       Value       Description         2CH       20H       CISTPL_MANFID       7AH       20H       SPACE       4CH       30       0         2CH       20H       CISTPL_MANFID       7CH       45H       E       31       1         2EH       04H       TPL_LINK(04H)       7EH       4CH       L       32       2         30H       F6H       EDITPLMID_MANF: LSB       80H       45E       E       33       3         32H       01H       EDI PLMID_MANF: MSB       82H       43H       C       36       6         34H       00H       LSB: Number Not Assign.       84H       54H       T       4EH       30       0         36H       00H       Assign.       86H       52H       R       34       34         3AH       47H       TPL_LINK       8AH       4EH       N       36       6         3CH       04H       TPLLV1_MAJOR       8CH       49H       1       38       8       2)							1)		
NON-INTERLEAVED       7AH       20H       SPACE       4CH       30       0         2CH       20H       CISTPL_MANFID       7CH       45H       E       31       1         2EH       04H       TPL_LINK(04H)       7EH       4CH       L       32       2         30H       F6H       EDITPLMID_MANF: LSB       80H       45E       E       33       3         32H       01H       EDI PLMID_MANF: MSB       82H       43H       C       36       6         34H       00H       LSB: Number Not Assign.       84H       54H       T       4EH       30       0         36H       00H       Assign.       86H       52H       R       36       6         38H       15H       CISTPL_VERS1       88H       4FH       O       34       4         3CH       04H       TPLLV1_MAJOR       8CH       49H       1       38       8         3EH       01H       TPLLV1_MINOR       8EH       43H       C       2       2         58H       32H       90H       20H       S							Address	Value	Description
2CH     20H     CISTPL_MANFID     7CH     45H     E     31     1       2EH     04H     TPL_LINK(04H)     7EH     4CH     L     32     2       30H     F6H     EDITPLMID_MANF: LSB     80H     45E     E     33     3       32H     01H     EDI PLMID_MANF: MSB     82H     43H     C     36     6       34H     00H     LSB: Number Not Assign.     84H     54H     T     36     6       36H     00H     Assign.     86H     52H     R     32     2       38H     15H     CISTPL_VERS1     88H     4FH     O     34     4       3CH     04H     TPLLV1_MAJOR     8CH     49H     1     38     8       3CH     04H     TPLLV1_MINOR     8EH     43H     C     2)     2)       2N     90H     20H     SPACE     58H     32     2		<b>J</b> I					4CH	30	0
2EH     04H     TPL_LINK(04H)     7EH     4CH     L     32     2       30H     F6H     EDITPLMID_MANF: LSB     80H     45E     E     33     3       32H     01H     EDI PLMID_MANF: MSB     82H     43H     C     34     4       34H     00H     LSB: Number Not Assign.     84H     54H     T     36     6       36H     00H     Assign.     86H     52H     R     32     2       38H     15H     CISTPL_VERS1     88H     4FH     O     34     4       3CH     04H     TPL_LINK     8AH     4EH     N     36     6       3CH     04H     TPL_LINK     8AH     4FH     O     34     4       3CH     04H     TPLLV1_MAJOR     8CH     49H     1     38     8       3EH     01H     TPLLV1_MINOR     8EH     43H     C     2)     58H     32     2       58H     92H     44H     D     58H     32     2     38     38	2CH	20H						31	1
30H       F6H       EDITPLMID_MANF: LSB       80H       45E       E         32H       01H       EDI PLMID_MANF: MSB       82H       43H       C       34       4         34H       00H       LSB: Number Not Assign.       84H       54H       T       36       6         36H       00H       LSB: Number Not Assign.       84H       54H       T       32       2         36H       00H       Assign.       86H       52H       R       32       2         38H       15H       CISTPL_VERS1       88H       4FH       O       34       4         3CH       04H       TPLLV1_MAJOR       8CH       49H       1       38       8         3CH       01H       TPLLV1_MAJOR       8EH       43H       C       2)       38       8         3EH       01H       TPLLV1_MINOR       8EH       43H       C       2)       58H       32       2								32	2
32H     01H     EDI PLMID_MANF: MSB     82H     43H     C     34     4       34H     00H     LSB: Number Not Assign.     84H     54H     T     36     6       34H     00H     LSB: Number Not Assign.     84H     54H     T     4EH     30     0       36H     00H     Assign.     86H     52H     R     32     2       38H     15H     CISTPL_VERS1     88H     4FH     O     34     4       3AH     47H     TPL_LINK     8AH     4EH     N     36     6       3CH     04H     TPLLV1_MAJOR     8CH     49H     1     38     8       3EH     01H     TPLLV1_MINOR     8EH     43H     C     2)     58H     32     2       58H     32     2     58H     32     2     58H     32     2								33	3
34H     00H     LSB: Number Not Assign.     84H     54H     T     36     6       34H     00H     LSB: Number Not Assign.     84H     54H     T     4EH     30     0       36H     00H     Assign.     86H     52H     R     32     2       38H     15H     CISTPL_VERS1     88H     4FH     O     34     4       3AH     47H     TPL_LINK     8AH     4EH     N     36     6       3CH     04H     TPLLV1_MAJOR     8CH     49H     I     38     8       3EH     01H     TPLLV1_MINOR     8EH     43H     C     2)     58H     32     2       58H     32     2     58H     32     2     38     38     32     2								34	4
34H     00H     LSB: Number Not Assign.     84H     54H     T     4EH     30     0       36H     00H     Assign.     86H     52H     R     32     2       38H     15H     CISTPL_VERS1     88H     4FH     O     32     2       38H     15H     CISTPL_VERS1     88H     4EH     N     34     4       3CH     04H     TPL_LINK     8AH     4EH     N     36     6       3CH     04H     TPLLV1_MAJOR     8CH     49H     I     36     6       3EH     01H     TPLLV1_MINOR     8EH     43H     C     2)     2	5211			5211				36	6
MSB: Number Not     MSB: Number Not     4EH     30     0       36H     00H     Assign.     86H     52H     R     32     2       38H     15H     CISTPL_VERS1     88H     4FH     O     34     4       3AH     47H     TPL_LINK     8AH     4EH     N     36     6       3CH     04H     TPLLV1_MAJOR     8CH     49H     I     38     8       3EH     01H     TPLLV1_MINOR     8EH     43H     C     2)     58H     32     2	34H	00H	LSB: Number Not Assign.	84H	54H	т			
36H     00H     Assign.     86H     52H     R     32     2       38H     15H     CISTPL_VERS1     88H     4FH     O     34     4       3AH     47H     TPL_LINK     8AH     4EH     N     36     6       3CH     04H     TPLLV1_MAJOR     8CH     49H     I     38     8       3EH     01H     TPLLV1_MINOR     8EH     43H     C     2)     2         90H     20H     SPACE     58H     32     2			<b>.</b>				4EH	30	0
38H       15H       CISTPL_VERS1       88H       4FH       O       34       4         3AH       47H       TPL_LINK       8AH       4EH       N       36       6         3CH       04H       TPLLV1_MAJOR       8CH       49H       I       38       8         3EH       01H       TPLLV1_MINOR       8EH       43H       C       2)       2	36H	00H	Assign.	86H	52H	R			
3AH     47H     TPL_LINK     8AH     4EH     N     36     6       3CH     04H     TPLLV1_MAJOR     8CH     49H     I     38     8       3EH     01H     TPLLV1_MINOR     8EH     43H     C     2)     2)     2	38H	15H	CISTPL_VERS1	88H	4FH	0			
3CH       04H       TPLLV1_MAJOR       8CH       49H       I       38       8         3EH       01H       TPLLV1_MINOR       8EH       43H       C       2)       2       2         Image: State of the sta	3AH	47H	TPL_LINK	8AH	4EH	N			
3EH       01H       TPLLV1_MINOR       8EH       43H       C       2)       2)         90H       20H       SPACE       58H       32       2	3CH	04H	TPLLV1_MAJOR	8CH	49H	I			
90H 20H SPACE 58H 32 2	3EH		TPLLV1_MINOR	8EH		С	2)	30	O
92H <b>44H</b> D 58H 32 2				90H	20H	SPACE	,		0
							58H		
						J		34	4



REVISION HISTORY		
Date of revision	Version	Description
7-Feb-98	-001	Initial release
27-May-99	-002	Logo change
31-May-00	-003	Added page 9, Heading changed on all pgs
1-Aug-00	-004	Corrected Timing Errors, pgs. 6&7

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