EB04

FEATURES

- COMPATIBLE WITH PWM FREQUENCIES UP TO 50KHZ
- 10.8V TO 50V MOTOR SUPPLY
- 5A CONTINUOUS OUTPUT CURRENT
- HCMOS COMPATIBLE SCHMITT TRIGGER LOGIC INPUTS
- SEPARATE SOURCE OUTPUTS FOR NEGATIVE RAIL CURRENT SENSE
- SLEEP MODE
- SINGLE SUPPLY FOR GATE DRIVE AND LOGIC
- BUILT-IN DELAY ELIMINATES SHOOT THROUGH DUE TO FETS CROSSFIRING

APPLICATIONS

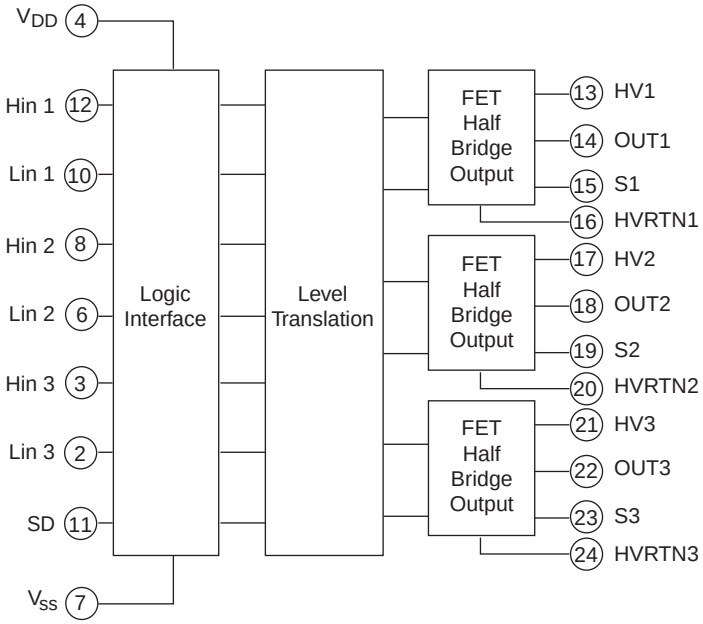
HIGH POWER CIRCUITS FOR DIGITAL CONTROL OF:

- THREE AXIS MOTION USING BRUSH TYPE MOTORS
- THREE PHASE BRUSHLESS DC MOTOR DRIVE
- THREE PHASE AC MOTOR DRIVE
- THREE PHASE HIGH POWER MICROSTEPPING STEP MOTORS

DESCRIPTION

The EB04 consists of three independent FET half bridges with drivers. The drivers may be interfaced with CMOS or HCMOS level logic.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

MOTOR VOLTAGE SUPPLY, HV	50V
OUTPUT CURRENT, peak	10A
OUTPUT CURRENT, continuous[1]	5A
LOGIC SUPPLY VOLTAGE, Vdd	-0.5V TO 7V
POWER DISSIPATION, internal[1]	40W
LOGIC INPUT VOLTAGE	-0.3V to V_{dd} + 0.3V
THERMAL RESISTANCE TO CASE[3]	5°C/Watt
TEMPERATURE, pin solder, 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE RANGE, storage	–55 to +150°C
OPERATING TEMPERATURE, case	–25 to +85°C
GROUND DIFFERENTIAL | V_{ss}–HVRTN |	1V

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[6]	MIN	TYP	MAX	UNITS
POSITIVE OUTPUT VOLTAGE	I_{OUT}=5A; V_{dd}=5V HV=50V, Fpwm=50kHz, L=100 µH	48.2		51.6[4]	Volts
NEGATIVE OUTPUT VOLTAGE	"	-1.6[4]		1.1	Volts
POSITIVE EDGE DELAY (upper FET)			170		nS
NEGATIVE EDGE DELAY (upper FET)			1'10		nS
POSITIVE EDGE DELAY (upper FET)			320		nS
NEGATIVE EDGE DELAY (lower FET)			46		nS
RISE TIME (upper FET turn-on)	LOAD =4mH in series with 10 ohms		810		nS
FALL TIME (upper FET turn-off)	LOAD =4mH in series with 10 ohms		86		nS
RISE TIME (lower FET turn-off)	LOAD =4mH in series with 10 ohms		29		nS
FALL TIME (lower FET turn-on)	LOAD =4mH in series with 10 ohms		794		nS
REVERSE RECOVERY TIME (upper FET body diode)	LOAD =4mH in series with 10 ohms		47		nS
REVERSE RECOVERY TIME (lower FET body diode)	LOAD =4mH in series with 10 ohms		86		nS
R_{DS} (on) Upper FET	25°C Base Temp		0.16	0.25	ohms
R_{DS} (on) Upper FET	85°C Base Temp		0.23	0.31	ohms
R_{DS} (on) Lower FET	25°C Base Temp		0.082	0.126	ohms
R_{DS} (on) Lower FET	85°C Base Temp		0.156	0.162	ohms
PWM FREQUENCY	Set by external circuitry			50	kHz
INPUT IMPEDANCE	Set by internal resistors		50		k-ohm

INPUT AND OUTPUT SIGNALS

PIN	SYMBOL	FUNCTION	PIN	SYMBOL	FUNCTION
1	N.C.	Gate supply 3	13	HV1	High Voltage supply 1
2	Lin3	Low drive logic in 3	14	OUT1	Section 1 output
3	Hin3	High drive logic in 3	15	S1	Section 1 source
4	V_{dd}	Logic supply	16	HVRTN1	Section 1 return
5	N.C.	Gate supply 2	17	HV2	High voltage supply 2
6	Lin2	Low drive logic in 2	18	OUT 2	Section 2 output
7	V_{ss}	Signal ground	19	S2	Section 2 source
8	Hin2	High drive logic in 2	20	HVRTN2	Section 2 return
9	N.C.	Gate supply 1	21	HV3	High voltage supply 3
10	Lin1	Low drive logic in 1	22	OUT 3	Section 3 output
11	SD	Shut down logic in	23	S3	Section 3 source
12	Hin1	High drive logic in 1	24	HVRTN 3	Section 3 return

NOTES:
1. Over Entire Environmental Range.
2. Long term operation at the maximum junction temperature will result in reduced product life. Lower internal temperature by reducing internal dissipation or using better heatsinking to achieve high MTTF.
3. Each FET.
4. Assumes turning off inductive load.
5. Logic input to output when driving non-inductive load.
6. Unless otherwise noted: TC=25°C; I_{out} = 5A; V_{dd} = 5V; HV=50V; F_{PWM} =50kHz; L_{Load} = 100µH

INPUT

A logic level input independently controls each FET in the half bridge. A logic level high turns on the FET and low turns it off. A common shut down input turns off all FETs when high.

All inputs are Schmitt triggers with the upper threshold at 2/3 V_{dd} and the lower threshold at 1/3 V_{dd}. This comfortably interfaces with CMOS or HCMOS provided that the Vdd for the logic family and the EB04 are the same.

TTL families may be used if a pull-up to Vcc is added to the TTL gates driving the EB04, and Vdd for the EB04 is the same supply as V_{cc} for the TTL family.

An open signal connector pulls the shut down input high and all other inputs low, insuring that all outputs are off. However, input impedance is 50k on all inputs; therefore if one input is open circuited a high radiated noise level could spuriously turn on a FET.

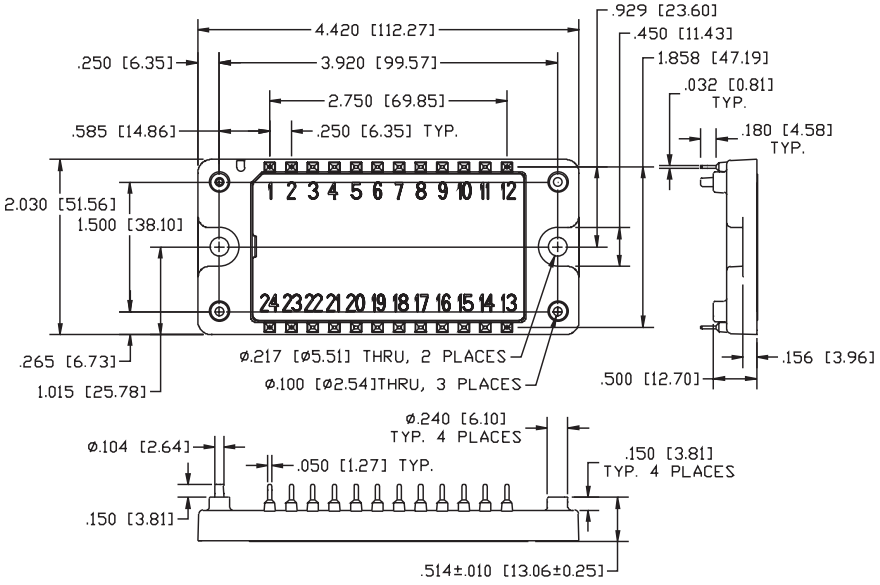
OUTPUT

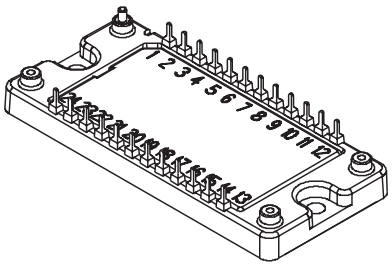
Each output section consists of a switching mode FET half bridge. Separate HV supply, source, and HV return lines are provided for each section.

The FETs are conservatively rated to carry 5A. At 5A the saturation voltage is 1.9V maximum.

Each FET has an intrinsic diode connected in anti-parallel. When switching an inductive load this diode will conduct, and the drop at 5A will be 1.9V maximum.

DIP9 PACKAGE





WEIGHT: 69 g or 2.4 oz
DIMENSIONS ARE IN INCHES
ALTERNATE UNITS ARE [MM]

POWER SUPPLY REQUIREMENTS

SUPPLY	VOLTAGE	MAX CURRENT
HV1	10.8V to 50V	5A, continuous, 10A peak
HV2	10.8V to 50V	5A, continuous, 10A peak
HV3	10.8V to 50V	5A, continuous, 10A peak
V_{dd}	4.75 – 5.25	105 mA

HV1, HV2, and HV3 may be used independently, or may be one supply. The V_{dd} supply must be compatible with the input logic. If a high voltage logic such as CMOS is used it may be tied with the V_{cc} supplies. HCMOS requires a 5V±10% supply

SPECIAL CONSIDERATIONS

GENERAL

The EB04 is designed to give the user maximum flexibility in a digital or DSP based motion control system. Thermal, overvoltage, overcurrent, and crossfire protection circuits are part of the user's design.

Users should read Application Note 1, "General Operating Considerations;" and Application Note 30, "PWM Basics" for much useful information in applying this part. These Application Notes are in the "Power Integrated Circuits Data Book" and on line at www.apexmicrotech.com.

GROUNDING AND BYPASSING

As in any high power PWM system, grounding and bypassing are one of the keys to success. The EB04 is capable of generating 250W pulses with 30 n-second rise and fall times. If improperly grounded or bypassed this can cause horrible conducted and radiated EMI.

In order to reduce conducted EMI, the EB04 provides a separate power ground, named HVRTN, for each high voltage supply. These grounds are not directly coupled. This isolation helps minimize high current ground loops. Apex recommends back to back high current diodes between logic and power grounds; this will maintain isolation but keep offset at a safe level. All grounds should tie together at one common point in the system.

In order to reduce radiated EMI, Apex recommends a 50 µF or larger capacitor between HV and HVRTN. This capacitor should be a switching power grade electrolytic capacitor with ESR rated at 20 kHz. This capacitor should be placed physically as close to the EB04 as possible.

However, such a capacitor will typically have a few hundred milli-ohms or so ESR. Therefore, each section must also be bypassed with a low ESR 1µF or larger ceramic capacitor.

In order to minimize radiated noise it is necessary to minimize the area of the loop containing high frequency current. (The size of the antenna.) Therefore the 1µF ceramic capacitors should bypass each HV to its return right at the pins the EB04.

SHOOT THROUGH PROTECTION

Power FETs have a relatively short turn on delay, and a longer turn off delay. Therefore, turn on delay has been built in, and turn on signals may be applied simultaneoulsy with the turn off input to the other FET in that half bridge.

PROTECTION CIRCUITS

The EB04 does not include protection circuits.

However, there is a shut down input which will turn off all FETs when at logic "1". This input may be used with user designed temperature sensing and current sensing circuits to shut down the FETs in the event of a detected unsafe condition. This is recommended since the FETs may be turned off this way even if the normal input logic or DSP programming is faulty.

HEATSINK

The heatsink for the EB04 should be sized for the application. When driving a 3-phase motor at 50V, 5 amps with a 50 kHz PWM frequency, the EB04 should be provided with sufficient heatsink to dissipate 25 Watts.

Determining the power dissipated internally involves a complex set of calculations dependent on load, switching frequency and duty cycle. Worse case switching losses occur when driving an inductive load at maximum current and maintaining a duty cycle large enough to keep the load current moving in one direction only.

Switching Losses in this case:

1. Mostly occurs during the "ON" transition of the upper FET of the "sourcing" half-bridge and the "ON" transition of the lower FET of the "sinking" half-bridge, and is proportional to frequency.
2. The switching time for the other two transistors is a function of the "Reverse Recovery Time" of the respective body diodes and is relatively short.

Conductive Losses are a function of:

1. The "ON" Duty Cycle and $I^2R_{DS}(on)$ losses of the upper "sourcing" FET and the $I^2R_{DS}(on)$ losses of the lower "sinking" FET.
2. The "OFF" Duty Cycle and IE ($I_{avg} \times V_{SD}$) losses of the body diodes of the other two FETs in the half-bridges.

APPLICATION REFERENCES:

For additional technical information please refer to the following Application Notes:

AN 01: General Operating Considerations

AN 40: Using the Easy Bridge as a Brushless DC Motor Driver