EB02

FEATURES

- COMPATIBLE WITH PWM FREQUENCIES UP TO 50KHZ
- 10V TO 100 V MOTOR SUPPLY
- 10A CONTINUOUS OUTPUT CURRENT
- HCMOS COMPATIBLE SCHMITT TRIGGER LOGIC INPUTS
- SEPARATE SOURCE OUTPUTS FOR NEGATIVE RAIL CURRENT SENSE
- SLEEP MODE
- WIDE RANGE FOR GATE DRIVE AND LOGIC SUPPLIES

APPLICATIONS

HIGH POWER CIRCUITS FOR DIGITAL CONTROL OF:

- THREE AXIS MOTION USING BRUSH TYPE MOTORS
- THREE PHASE BRUSHLESS DC MOTOR DRIVE
- THREE PHASE AC MOTOR DRIVE
- THREE PHASE STEP MOTOR DRIVE

DESCRIPTION

The EB02 consists of three independent FET half bridges with drivers. The drivers may be interfaced with CMOS or HCMOS level logic.

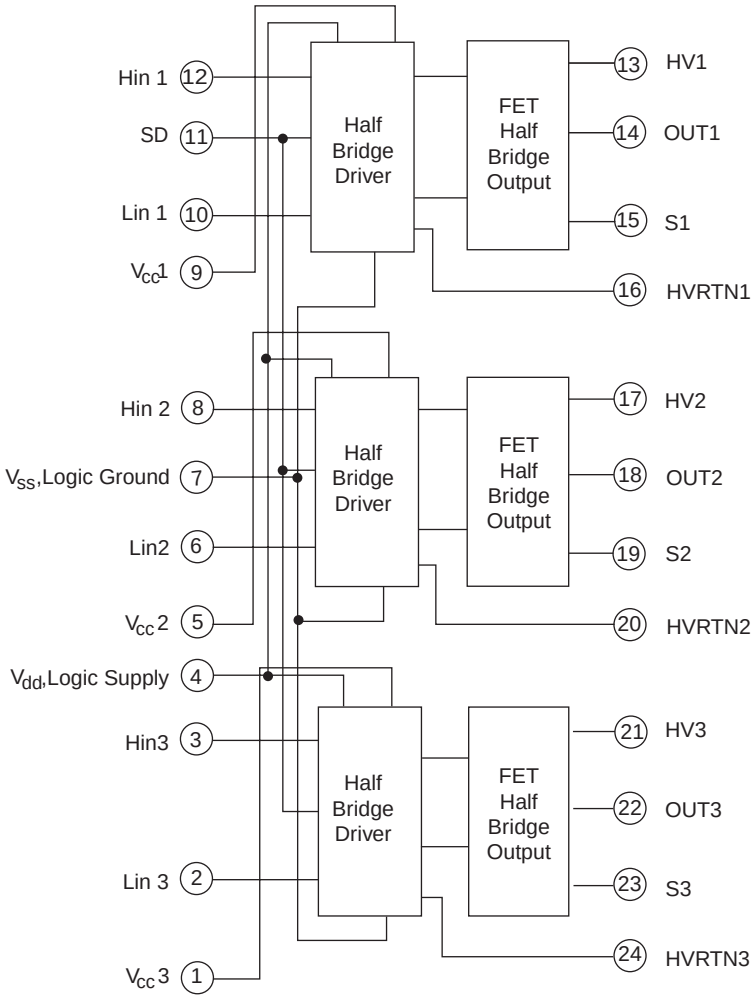


FIGURE 1. BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

MOTOR VOLTAGE SUPPLY, HV	100V
OUTPUT CURRENT, peak	20A
OUTPUT CURRENT, continuous[1]	10A
GATE SUPPLY VOLTAGE, Vcc	20V
LOGIC SUPPLY VOLTAGE, Vdd	20V
POWER DISSIPATION, internal[1]	51 Watts
LOGIC INPUT VOLTAGE	-0.3V to V_{dd} + 0.3V
THERMAL RESISTANCE TO CASE[3]	2.1°C/Watt
TEMPERATURE, pin solder, 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE RANGE, storage	–55 to +150°C
OPERATING TEMPERATURE, case	–25 to +85°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POSITIVE OUTPUT VOLTAGE	I_{OUT}=10A; V_{cc}=10.8V, V_{dd}=5V; HV=100V, Fpwm=50kHz, L=100 µH	99.2		101.5	Volts
NEGATIVE OUTPUT VOLTAGE	"	-1.5		.8	Volts
POSITIVE EDGE DELAY	"		260		n-second
RISETIME	"		50		n-second
NEGATIVE EDGE DELAY	"		310		n-second
FALLTIME	"		5 0		n-second
PWM FREQUENCY	Set by external circuitry			50	kHz
INPUT IMPEDANCE	Set by internal resistors		50		k-ohm

INPUT AND OUTPUT SIGNALS

PIN	SYMBOL	FUNCTION	PIN	SYMBOL	FUNCTION
1	V_{cc}3	Gate supply 3	13	HV1	High Voltage supply 1
2	Lin3	Low drive logic in 3	14	OUT1	Section 1 output
3	Hin3	High drive logic in 3	15	S1	Section 1 source
4	V_{dd}	Logic supply	16	HVRTN1	Section 1 return
5	V_{cc}2	Gate supply 2	17	HV2	High voltage supply 2
6	Lin2	Low drive logic in 2	18	OUT 2	Section 2 output
7	V_{ss}	Signal ground	19	S2	Section 2 source
8	Hin2	High drive logic in 2	20	HVRTN2	Section 2 return
9	V_{cc}1	Gate supply 1	21	HV3	High voltage supply 3
10	Lin1	Low drive logic in 1	22	OUT 3	Section 3 output
11	SD	Shut down logic in	23	S3	Section 3 source
12	Hin1	High drive logic in 1	24	HVRTN 3	Section 3 return

NOTES: 1. Over full operating temperature range.
2. Long term operation at the maximum junction temperature will result in reduced product life. Lower internal temperature by reducing internal dissipation or using better heatsinking to achieve high MTTF.
3. Each FET.

INPUT

A logic level input independently controls each FET in the half bridge. A logic level high turns on the FET and low turns it off. A common shut down input turns off all FETs when high.

All inputs are Schmitt triggers with the upper threshold at 2/3 V_{dd} and the lower threshold at 1/3 V_{dd}. This comfortably interfaces with CMOS or HCMOS provided that the Vdd for the logic family and the EB02 are the same.

TTL families may be used if a pull-up to Vcc is added to the TTL gates driving the EB02, and Vdd for the EB02 is the same supply as V_{cc} for the TTL family.

An open signal connector pulls the shut down input high and all other inputs low, insuring that all outputs are off.

However, input impedance is 50k on all inputs; therefore, if one input is open circuited a high radiated noise level could spuriously turn on a FET.

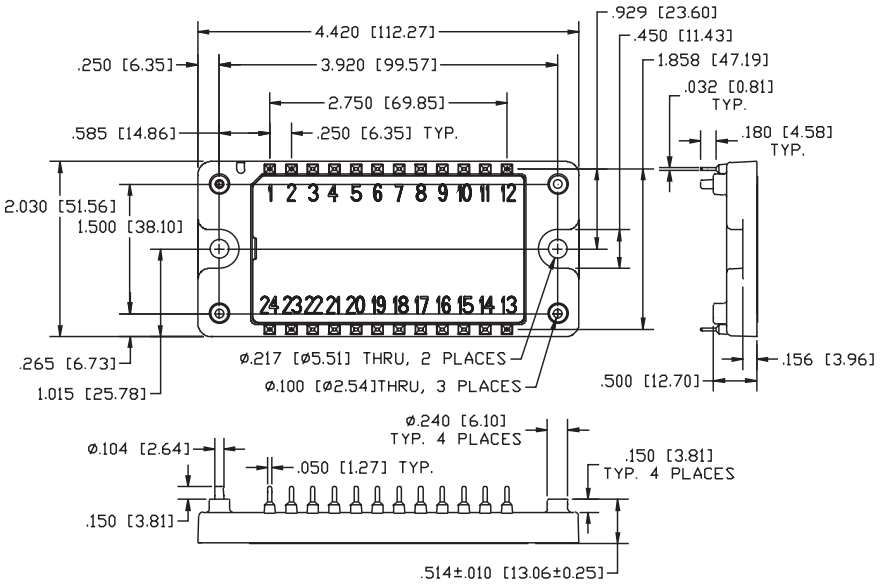
OUTPUT

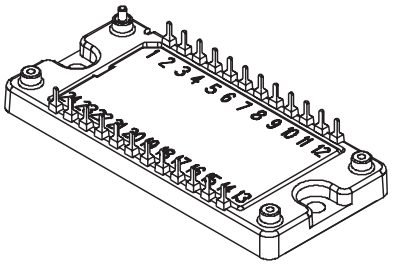
Each output section consists of a switching mode FET half bridge. Separate HV supply, emitter, and HV return lines are provided for each section.

The FETs are conservatively rated to carry 10A. At 10A the saturation voltage is 1.5 V maximum, over the full environmental range.

Each FET has an intrinsic diode connected in anti-parallel. When switching an inductive load this diode will conduct, and the drop at 10A will be 1.5V maximum, over the full environmental range.

PACKAGE SPECIFICATIONS
DIP9 PACKAGE





WEIGHT: 69 g or 2.4 oz
DIMENSIONS ARE IN INCHES
ALTERNATE UNITS ARE [MM]

POWER SUPPLY REQUIREMENTS

SUPPLY	VOLTAGE	MAX CURRENT
HV1	10V to 100V	10A, continuous, 20A peak
HV2	10V to 100V	10A, continuous, 20A peak
HV3	10V to 100V	10A, continuous, 20A peak
$V_{cc}1$	10V to 20V	10mA
$V_{cc}2$	10V to 20V	10mA
$V_{cc}3$	10V to 20V	10mA
V_{dd}	4.5 to 20V	10mA

HV1, HV2, and HV3 may be used independently, or may be one supply. Also $V_{cc}1$, $V_{cc}2$, and $V_{cc}3$ may be used independently or tied together. The V_{dd} supply must be compatible with the input logic. If a high voltage logic such as CMOS is used it may be tied with the V_{cc} supplies. HCMOS requires a 5V±10% supply

SPECIAL CONSIDERATIONS

GENERAL

The EB02 is designed to give the user maximum flexibility in a digital or DSP based motion control system. Thermal, overvoltage, overcurrent, and crossfire protection circuits are part of the user's design.

Users should read Application Note 1, "General Operating Considerations;" and Application Note 30, "PWM Basics" for much useful information in applying this part. These Application Notes are in the "Power Integrated Circuits Data Book" and on line at www.apexmicrotech.com.

GROUNDING AND BYPASSING

As in any high power PWM system, grounding and bypassing are some of the keys to success. The EB02 is capable of generating 2 kW pulses with 40 n-second rise and fall times. If improperly grounded or bypassed this can cause horrible conducted and radiated EMI.

In order to reduce conducted EMI, the EB02 provides a separate power ground, named HVRTN, for each high voltage supply. These grounds are electrically isolated from the logic ground and each other. This isolation eliminates high current ground loops. However, more than 5V offset between the grounds will destroy the EB02. Apex recommends back to back high current diodes between logic and power grounds; this will maintain isolation but keep offset at a safe level. All grounds should tie together at one common point in the system.

In order to reduce radiated EMI, Apex recommends a 100 µF or larger capacitor between HV and HVRTN. This capacitor should be a switching power grade capacitor with ESR rated at 20kHz. This capacitor should be placed physically as close to the EB02 as possible.

However, such a capacitor will typically have a few hundred milli-ohms or so ESR. Therefore, each section must also be bypassed with a low ESR 1µF or larger ceramic capacitor.

In order to minimize radiated noise, it is necessary to minimize the area of the loop containing high frequency current. (The size of the antenna.) Therefore, the 1µF ceramic capacitors should bypass each HV to its return at the pins of the EB02.

SHOOT THROUGH PROTECTION

Power FETs have a relatively short turn on delay, and a long turn off delay. Therefore, if the turn on input to an FET in a half bridge circuit is applied simultaneously with the turn off input to the other FET in that half bridge, there will be a time when both FETs are simultaneously on. This "shoot through condition" will short the power rails through the FETs, causing excessive power dissipation and very high EMI.

To avoid the shoot through condition the turn on of one FET must be delayed long enough for the other FET in the same half bridge to have completely turned off.

A delay of at least 0.5 µ-seconds is required for the EB02. This delay is required for both the Hin and Lin inputs.

PROTECTION CIRCUITS

The EB02 does not include protection circuits.

However, there is a shut down input which will turn off all FETs when at logic "1". This input may be used with user designed temperature sensing and current sensing circuits to shut down the FETs in the event of a detected unsafe condition. This is recommended since the FETs may be turned off this way even if the normal input logic or DSP programming is faulty.

START UP CONSIDERATIONS

The lower rail FET in the half bridge must be turned on for at least 2 µ-seconds to charge the bootstrap capacitor before the top rail FET can be turned on. This must be done no more than 330 µ-seconds prior to turning on the top rail FET. However, a grounded load will give the same purpose as turning on the lower rail FET. However a grounded load will give the same purpose as turning on the lower rail FET. Therefore a grounded load may be operated without this consideration.

An internal floating supply is used to enhance the operation of the bootstrap bias circuit. This allows the top rail FETs to be held on indefinitely once turned on.

HEATSINK

The EB02 should be provided with sufficient heatsink to dissipate 51 watts when operating at 100V, 10A, 50kHz and 3 sections simultaneously providing maximum current.

The dissipation is composed of conduction losses ($I_{out}xV_{sat}$) up to 16 watt per half bridge and switching losses of about 1 watt per half bridge. The conduction losses are proportional to I_{out}; switching losses are proportional to HV supply voltage, load capacitance, and switching frequency.