National Semiconductor

May 2004

LM2459
Monolithic Single Channel 15 MHz DTV CRT Driver

General Description

The LM2459 is a single channel high voltage CRT driver circuit designed for use in DTV applications. The IC contains a high input impedance, wide band amplifier which directly drives the cathode of a CRT. The amplifier has its gain internally set to –51 and can drive CRT capacitive loads as well as resistive loads present in other applications, limited only by the package's power dissipation.

The IC is packaged in a staggered 7-lead TO-220 molded plastic power package designed specifically to meet high voltage spacing requirements. See Thermal Considerations section.

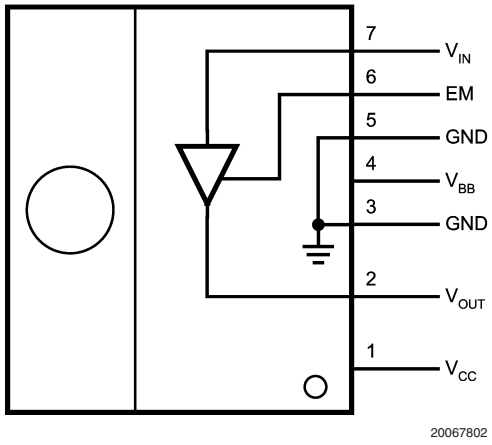
Features

- 15MHz bandwith at $130V_{PP}$ output swing
- 0V to 4V input range
- Greater than $130V_{PP}$ output swing capability
- Stable with 0–20 pF capacitive loads and inductive peaking networks
- Transient response improvement option via pin 6 (EM)

Applications

- AC coupled DTV applications using the 480p format as well as standard NTSC and PAL formats.

Connection Diagram



Note: Tab is at GND

Top View
Order Number LM2459TE

FIGURE 1. Simplified Connection and Pinout Diagram

Schematic Diagram

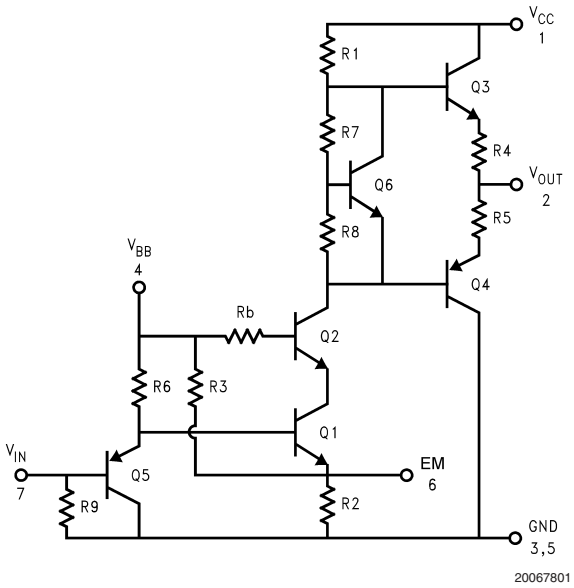


FIGURE 2. Simplified Schematic Diagram

Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	+200V
Bias Voltage (V_{BB})	+15V
Input Voltage (V_{IN})	-0.5V to V_{BB} +0.5V
Storage Temperature Range (T_{STG})	−65˚C to +150˚C
Lead Temperature	
(Soldering, <10 sec.)	300˚C
ESD Tolerance,	
Human Body Model	2kV
Machine Model	200V
Junction Temperature	150˚C
θ_{JC} (typ)	4.2˚C/W

Operating Ranges (Note 2)

V_{CC}	+130V to +180V
V_{BB}	+7V to +13V
V_{IN}	+0V to +4V
V_{OUT}	+25V to +178V
Case Temperature	Refer to *Figure 11*

Do not operate the part without a heat sink.

Electrical Characteristics (See *Figure 3* for Test Circuit)

Unless otherwise noted: V_{CC} = +180V, V_{BB} = +8V, C_L = 10pF, T_C = 30˚C, Pin 6 floating.
DC Tests: $V_{IN} = 2.5V_{DC}$
AC Tests: Output = $130V_{PP}$ (35V - 165V) at 1MHz

Symbol	Parameter	Conditions	LM2459			Units
			Min	Typical	Max	
I_{CC}	Supply Current	No AC Input Signal, No Output Load		6	12	mA
I_{BB}	Bias Current			4	7	mA
$V_{OUT, 1}$	DC Output Voltage	No AC Input Signal, $V_{IN} = 2.5V_{DC}$	99	104	109	V_{DC}
$V_{OUT, 2}$	DC Output Voltage	No AC Input Signal, $V_{IN} = 1.2V_{DC}$	165	170	175	V_{DC}
A_V	DC Voltage Gain	No AC Input Signal	-48	−51	-54	
LE	Linearity Error	(Note 4), No AC Input Signal		5		%
t_R	Rise Time	(Note 5), 10% to 90%		26		ns
t_F	Fall Time	(Note 5), 90% to 10%		30		ns
OS	Overshoot	(Note 5)		5		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

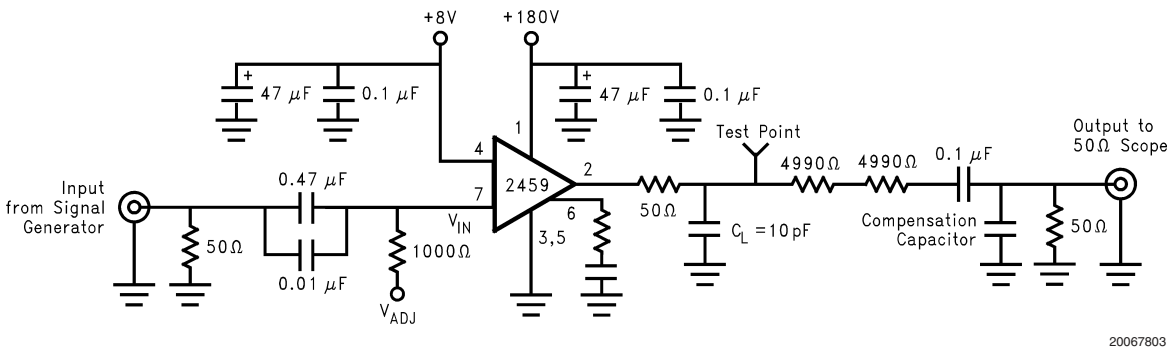
Note 2: Operating ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may change when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: Linearity Error is the variation in DC gain from V_{IN} = 1.1V to V_{IN} = 3.8V.

Note 5: Input from signal generator: t_r, t_f < 1 ns.

AC Test Circuit



Note: 10pF load includes parasitic capacitance.

FIGURE 3. Test Circuit

Figure 3 shows a typical test circuit for evaluation of the LM2459. This circuit is designed to allow testing of the LM2459 in a 50Ω environment without the use of an expensive FET probe. The two 4990Ω resistors form a 400:1 divider with the 50Ω resistor and the oscilloscope. A test point is included for easy use of an oscilloscope probe.The compensation capacitor is used to compensate the network to achieve a flat frequency response.

Typical Performance Characteristics (V_{CC} = +180V_{DC}, V_{BB} = +8V_{DC}, C_L = 10pF, V_{OUT} = 130V_{PP} (35V – 165V), Test Circuit - *Figure 3*, Pin 6 floating, unless otherwise specified)

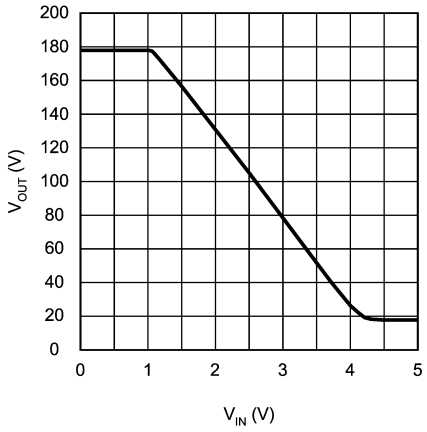


FIGURE 4. V_{OUT} vs V_{IN}

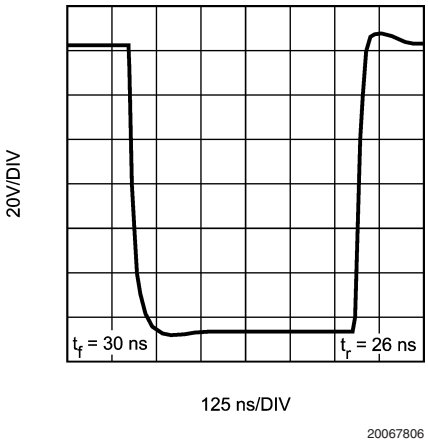


FIGURE 5. LM2459 Pulse Response

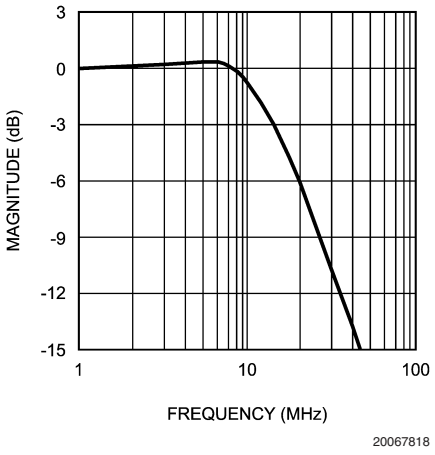


FIGURE 6. Bandwidth

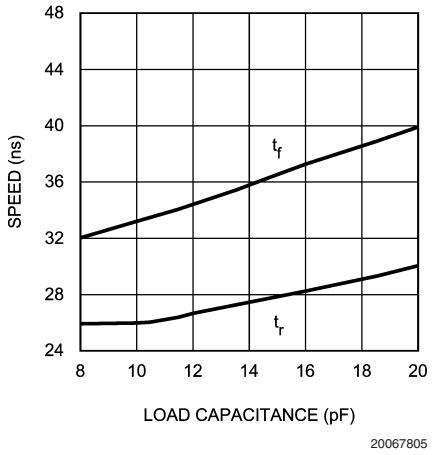


FIGURE 7. Speed vs Load Capacitance

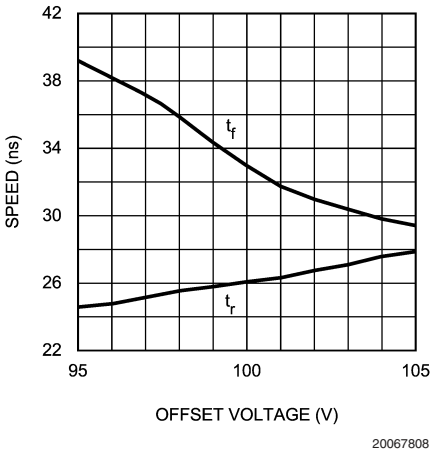


FIGURE 8. Speed vs Offset

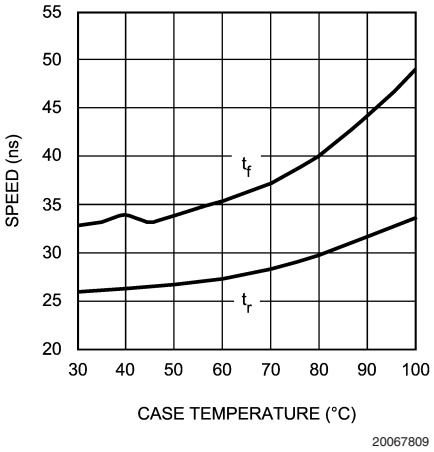


FIGURE 9. Speed vs Case Temperature

Typical Performance Characteristics (V_{CC} = +180V_{DC}, V_{BB} = +8V_{DC}, C_L = 10pF, V_{OUT} = 130V_{PP} (35V – 165V), Test Circuit - *Figure 3*, Pin 6 floating, unless otherwise specified) (Continued)

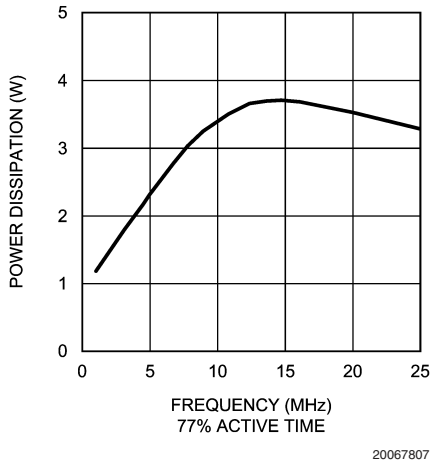


FIGURE 10. Power Dissipation vs Frequency

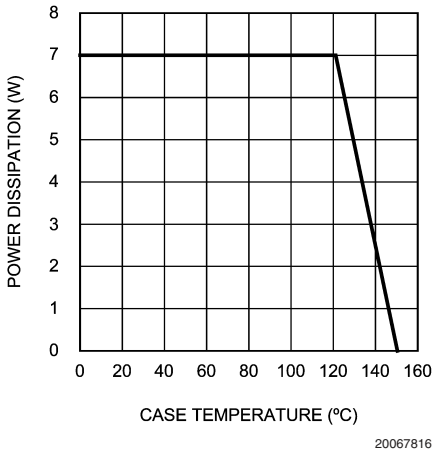


FIGURE 11. Power Derating Curve

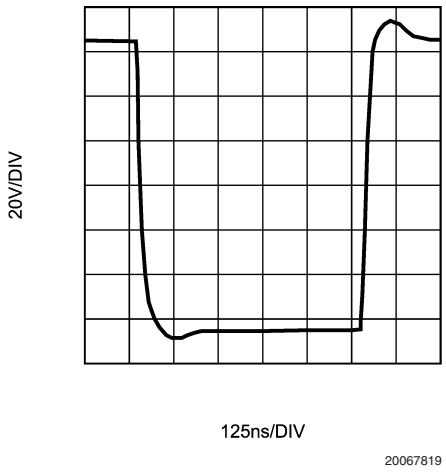


FIGURE 12. Cathode Pulse Response

Typical Performance Characteristics (V_{CC} = +180V_{DC}, V_{BB} = +8V_{DC}, C_L = 10pF, V_{OUT} = 130V_{PP} (35V – 165V), Test Circuit - *Figure 3*, Pin 6 floating, unless otherwise specified) (Continued)

TABLE 1. Power Dissipation for Various Video Patterns

Power Dissipation (W)		
Pattern	Format	
	480i	480p
Raster	0.5	0.5
Full White Field	1.2	1.2
White Box, 75% Screen Size	0.9	0.9
Gray Bars	1.0	1.0
Color Bars 75% Amplitude	0.8	0.8
Color Bars 100% Amplitude	0.9	0.9
SMPTE Color Bars	0.8	0.8
SMPTE 133	1.0	1.1
Cross Hatch 16x12	0.7	0.7
Resolution Chart	1.1	1.2
Multiburst	1.4	1.9
White Text on Black Background	1.5	2.2
Windows Pattern	0.9	1.2
Windows Pattern	0.9	1.2
Windows Pattern	1.4	1.7
Vertical Lines 5 On 5 Off	1.3	1.7
Vertical Lines 4 On 4 Off	1.3	1.8
Vertical Lines 3 On 3 Off	1.5	2.2
Vertical Lines 2 On 2 Off	1.8	2.8
Vertical Lines 1 On 1 Off	2.8	3.8

Note: Input from signal generator: t_r, t_f < 2 ns.

Theory of Operation

The LM2459 is a high voltage monolithic single channel CRT driver suitable for HDTV applications. The LM2459 operates with 180V and 8V power supplies. The part is housed in a staggered 7-lead TO-220 molded plastic power package.

The circuit diagram of the LM2459 is shown in *Figure 2*. The PNP emitter follower, Q5, provides input buffering. Q1 and Q2 form a fixed gain cascode amplifier with resistors R1 and R2 setting the gain at –51. Emitter followers Q3 and Q4 isolate the high output impedance of the cascode stage from the capacitance of the CRT cathode which decreases the sensitivity of the device to load capacitance. Q6 provides biasing to the output emitter follower stage to reduce crossover distortion at low signal levels.

Figure 3 shows a typical test circuit for evaluation of the LM2459. This circuit is designed to allow testing of the LM2459 in a 50Ω environment without the use of an expensive FET probe. In this test circuit, the two 4.99kΩ resistors form a 400:1 wideband, low capacitance probe when connected to a 50Ω coaxial cable and a 50Ω load (such as a 50Ω oscilloscope input). The input signal from the generator is ac coupled to the base of Q5.

Application Hints

INTRODUCTION

National Semiconductor (NSC) is committed to provide application information that assists our customers in obtaining the best performance possible from our products. The following information is provided in order to support this commitment. The reader should be aware that the optimization of performance was done using a specific printed circuit board designed at NSC. Variations in performance can be realized due to physical changes in the printed circuit board and the application. Therefore, the designer should know that component value changes may be required in order to optimize performance in a given application. The values shown in this document can be used as a starting point for evaluation purposes. When working with high bandwidth circuits, good layout practices are also critical to achieving maximum performance.

IMPORTANT INFORMATION

The LM2459 performance is targeted for the HDTV market. The application circuits shown in this document to optimize performance and to protect against damage from CRT arcover are designed specifically for the LM2459. If another member of the LM245X family is used, please refer to its datasheet.

POWER SUPPLY BYPASS

Since the LM2459 is a wide bandwidth amplifier, proper power supply bypassing is critical for optimum performance. Improper power supply bypassing can result in large overshoot, ringing or oscillation. 0.1µF capacitors should be connected from the supply pins, V_{CC} and V_{BB}, to ground, as close to the LM2459 as is practical. Additionally, a 22µF or larger electrolytic capacitor should be connected from both supply pins to ground reasonably close to the LM2459.

Application Hints (Continued)

ARC PROTECTION

During normal CRT operation, internal arcing may occasionally occur. Spark gaps, in the range of 300V, connected from the CRT cathodes to CRT ground will limit the maximum voltage, but to a value that is much higher than allowable on the LM2459. This fast, high voltage, high energy pulse can damage the LM2459 output stage. The application circuit shown in *Figure 13* is designed to help clamp the voltage at the output of the LM2459 to a safe level. The clamp diodes, D1 and D2, should have a fast transient response, high peak current rating, low series impedance and low shunt capacitance. 1SS83 or equivalent diodes are recommended. D1 and D2 should have short, low impedance connections to V_{CC} and ground respectively. The cathode of D1 should be located very close to a separately decoupled bypass capacitor (C3 in *Figure 13*). The ground connection of D2 and the decoupling capacitor should be very close to the LM2459 ground. This will significantly reduce the high frequency voltage transients that the LM2459 would be subjected to during an arcover condition. Resistor R2 limits the arcover current that is seen by the diodes while R1 limits the current into the LM2459 as well as the voltage stress at the outputs of the device. R2 should be a ½W solid carbon type resistor. R1 can be a ¼W metal or carbon film type resistor. Having large value resistors for R1 and R2 would be desirable, but this has the effect of increasing rise and fall times. Inductor L1 is critical to reduce the initial high frequency voltage levels that the LM2459 would be subjected to. The inductor will not only help protect the device but it will also help minimize rise and fall times as well as minimize EMI. For proper arc protection, it is important to not omit any of the arc protection components shown in *Figure 13*.

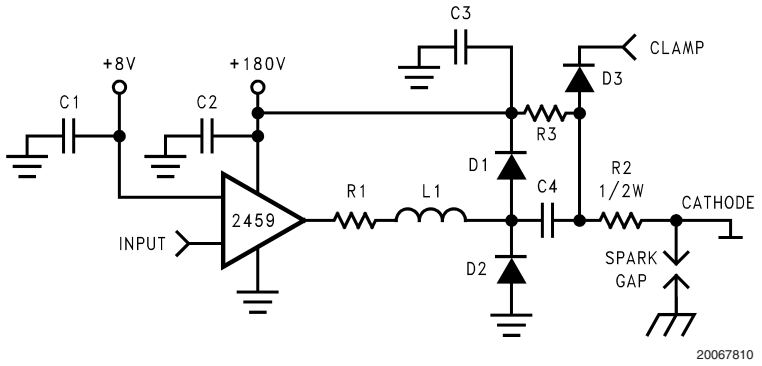


FIGURE 13. Recommended Application Circuit

EFFECT OF LOAD CAPACITANCE

Figure 7 shows the effect of increased load capacitance on the speed of the device. This demonstrates the importance of knowing the load capacitance in the application.

EFFECT OF OFFSET

Figure 8 shows the variation in rise and fall times when the output offset of the device is varied from 95 to 105V_{DC}. The rise time shows a variation of less than 7% relative to the center data point (100V_{DC}). The fall time shows a variation of 18% relative to the center data point.

THERMAL CONSIDERATIONS

Figure 9 shows the performance of the LM2459 in the test circuit shown in *Figure 3* as a function of case temperature. The figure shows that the rise and fall times of the LM2459 increase by approximately 18% and 29%, respectively, as the case temperature increases from 50˚C to 90˚C. This corresponds to a speed degradation of 5% and 7% for every 10˚C rise in case temperature.

Figure 10 shows the maximum power dissipation of the LM2459 vs. frequency when the device is driving a 10pF load with a 130V_{PP} alternating one pixel on, one pixel off signal. The graph assumes a 77% active time (device operating at the specified frequency), which is typical in a TV application. The other 23% of the time the device is assumed to be sitting at the black level (165V in this case). Table 1 also shows the typical power dissipation of the LM2459 for various video patterns in the 480i and 480p video formats.

Figure 10, *Figure 11*, and *Table 1* give the designer the information needed to determine the heatsink requirement for the LM2459. For example, if an HDTV application uses the 480p format and "Vertical Lines 1 On 1 Off" is assumed to be the worst-case pattern to be displayed, then the power dissipated will be 3.8W (from *Table 1*). *Figure 11* shows that the maximum allowed case temperature is 134˚C when 3.8W is dissipated. If the maximum expected ambient temperature is 70˚C, then a maximum heatsink thermal resistance can be calculated:

$$R_{TH} = \frac{134°C - 70°C}{3.8W} = 16.8°C/W$$

This example assumes a capacitive load of 10pF and no resistive load. The designer should note that if the load capacitance is increased, then the AC component of the total power dissipation will also increase.

Note: An LM126X preamplifier, with rise and fall times of about 2 ns, was used to drive the LM2459 for these power measurements. Using a preamplifier with rise and fall times slower than the LM126X will cause the LM2459 to dissipate less power than shown in *Table 1*.

OPTIMIZING TRANSIENT RESPONSE

Referring to *Figure 13*, there are three components (R1, R2 and L1) that can be adjusted to optimize the transient response of the application circuit. Increasing the values of R1 and R2 will slow the circuit down while decreasing overshoot. Increasing the value of L1 will speed up the circuit as

Application Hints (Continued)

well as increase overshoot. It is very important to use inductors with very high self-resonant frequencies, preferably above 300 MHz. Ferrite core inductors from J.W. Miller Magnetics (part # 78FR_ _k) were used for optimizing the performance of the device in the NSC application board. The values shown in *Figure 14* can be used as a good starting point for the evaluation of the LM2459. Using a variable resistor for R1 will simplify finding the value needed for optimum performance in a given application. Once the optimum value is determined, the variable resistor can be replaced with a fixed value.

Figure 12 shows the typical cathode pulse response with an output swing of $110V_{PP}$ using a LM1269 preamplifier.

The transient response can also be improved by adding a capacitor from pin 6 to the ground plane used by the LM2459. A small capacitor, such as a 22pF ceramic, will notably improve the fall time and only increase the overshoots and settling times slightly. Note that increasing the capacitance beyond 22pF will only improve the fall time marginally, but will increase the settling times significantly. This option allows for better matching between the rise and fall time.

PC BOARD LAYOUT CONSIDERATIONS

For optimum performance, an adequate ground plane, isolation between channels, good supply bypassing and minimizing unwanted feedback are necessary. Also, the length of the signal traces from the preamplifier to the LM2459 and from the LM2459 to the CRT cathode should be as short as possible. The following references are recommended:

Ott, Henry W., "Noise Reduction Techniques in Electronic Systems", John Wiley & Sons, New York, 1976.

"Video Amplifier Design for Computer Monitors", National Semiconductor Application Note 1013.

Pease, Robert A., "Troubleshooting Analog Circuits", Butterworth-Heinemann, 1991.

Because of its high small signal bandwidth, the part may oscillate in a TV if feedback occurs around the video channel through the chassis wiring. To prevent this, leads to the video amplifier input circuit should be shielded, and input circuit wiring should be spaced as far as possible from output circuit wiring.

TYPICAL APPLICATION

A typical application of the LM2459 is shown in the schematic for the NSC demonstration board in *Figure 14*. Used in conjunction with an LM126X preamplifier, a complete video channel from input to CRT cathode can be achieved. Performance is ideal for DTV applications. The NSC demonstration board can be used to evaluate the LM2459 in a TV.

NSC DEMONSTRATION BOARD

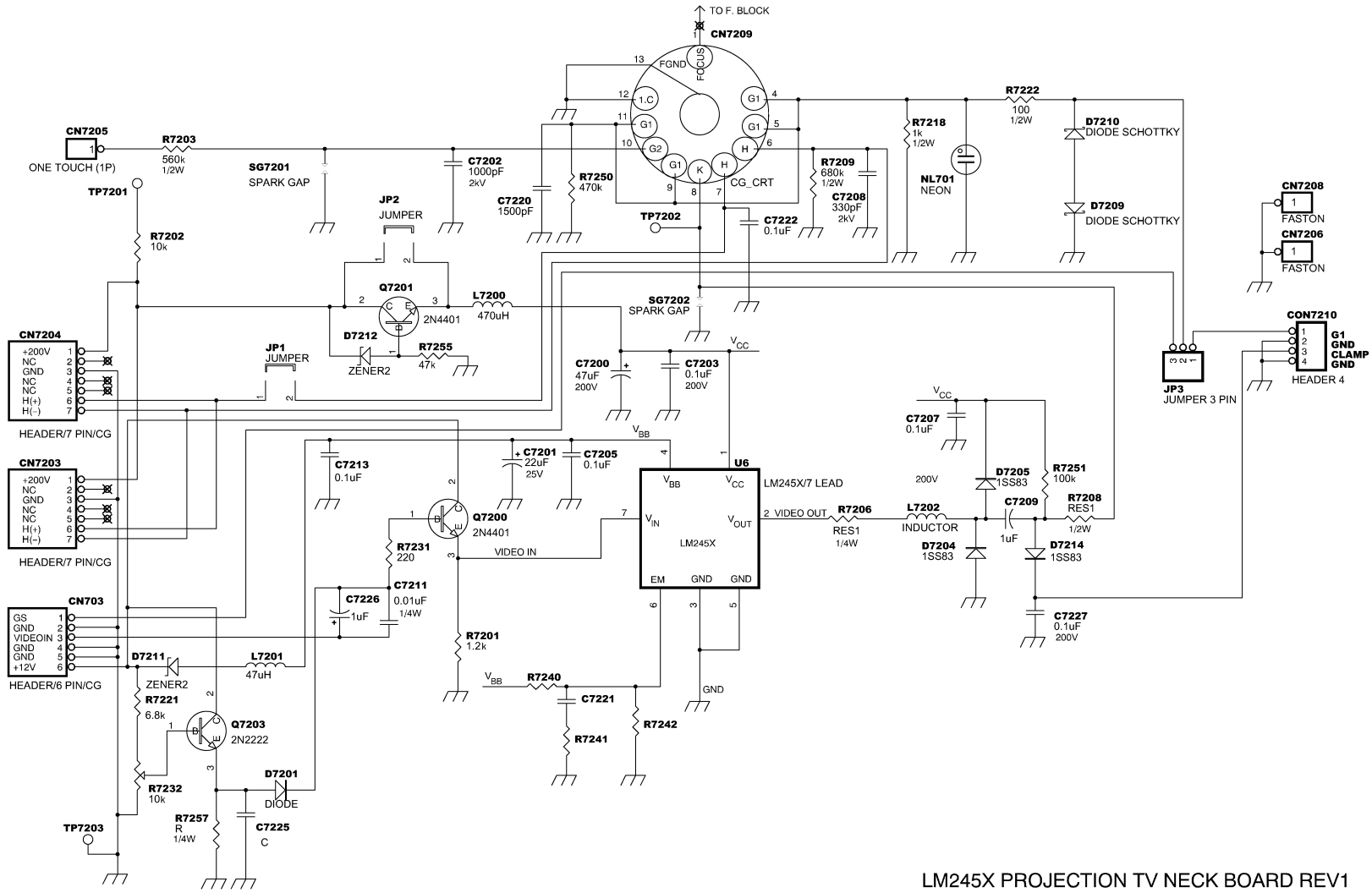
Figure 15 shows the routing and component placement on the NSC LM2459 demonstration board. This board provides a good example of a layout that can be used as a guide for future layouts. Note the location of the following components:

- C7203 — V_{CC} bypass capacitor, located very close to pin 1 and ground pins
- C7205 — V_{BB} bypass capacitor, located close to pin 4 and ground
- C7207 — V_{CC} bypass capacitor, near LM2459 and V_{CC} clamp diodes. Very important for arc protection.

The routing of the LM2459 output to the CRT is very critical to achieving optimum performance. *Figure 16* shows the routing and component placement from pin 2 (V_{OUT}) of the LM2459 to the cathode. Note that the components are placed so that they almost line up from the output pin of the LM2459 to the cathode pin of the CRT connector. This is done to minimize the length of the video path between these two components. Note also that D7204, D7205, R7251 and D7214 are placed to minimize the size of the video nodes that they are attached to. This minimizes parasitic capacitance in the video path and also enhances the effectiveness of the protection diodes. The anode of protection diode D7204 is connected directly to a section of the the ground plane that has a short and direct path to the LM2459 ground pins. The cathode of D7205 is connected to V_{CC} very close to decoupling capacitor C7207 (see *Figure 16*) which is connected to the same section of the ground plane as D7204. The diode placement and routing is very important for minimizing the voltage stress on the LM2459 during an arcover event. Lastly, notice that SG7202 is placed very close to the cathode and is tied directly to CRT ground.

This demonstration board uses medium-sized PCB holes to accommodate socket pins, which function to allow for multiple insertions of the LM2459 in a convenient manner. To benefit from the enhanced LM2459 package with thin leads, the device should be secured in small PCB holes to optimize the metal-to-metal spacing between the leads.

Application Hints (Continued)



LM245X PROJECTION TV NECK BOARD REV1

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FIGURE 14. LM2459 Demonstration Board Schematic

Application Hints (Continued)

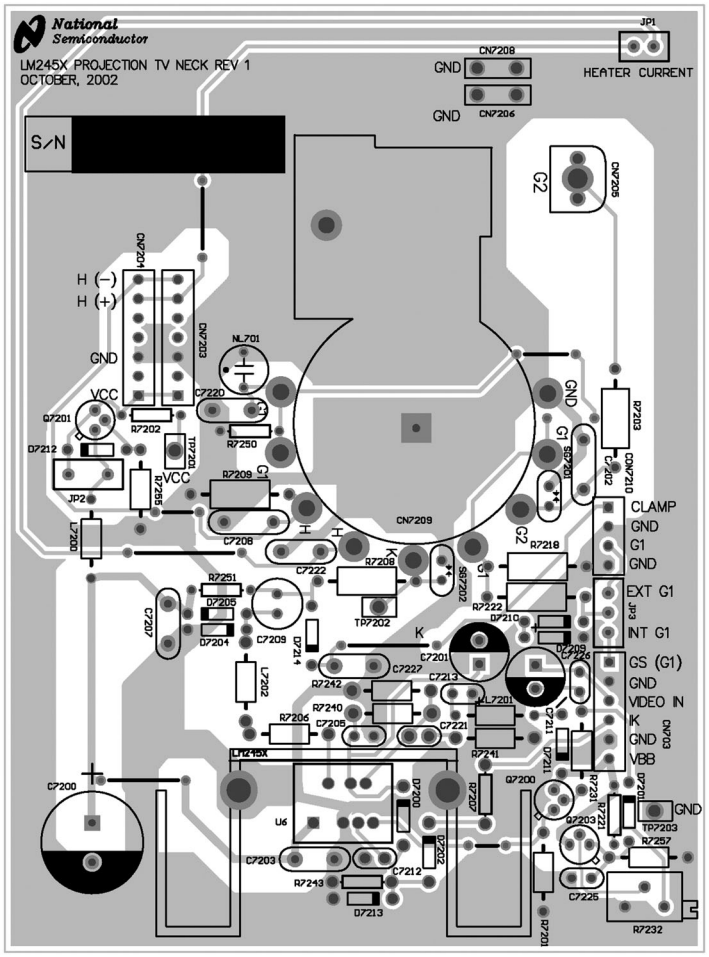

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FIGURE 15. LM2459 Demonstration Board Layout

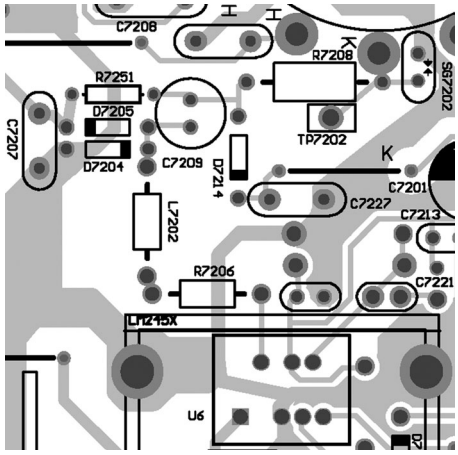

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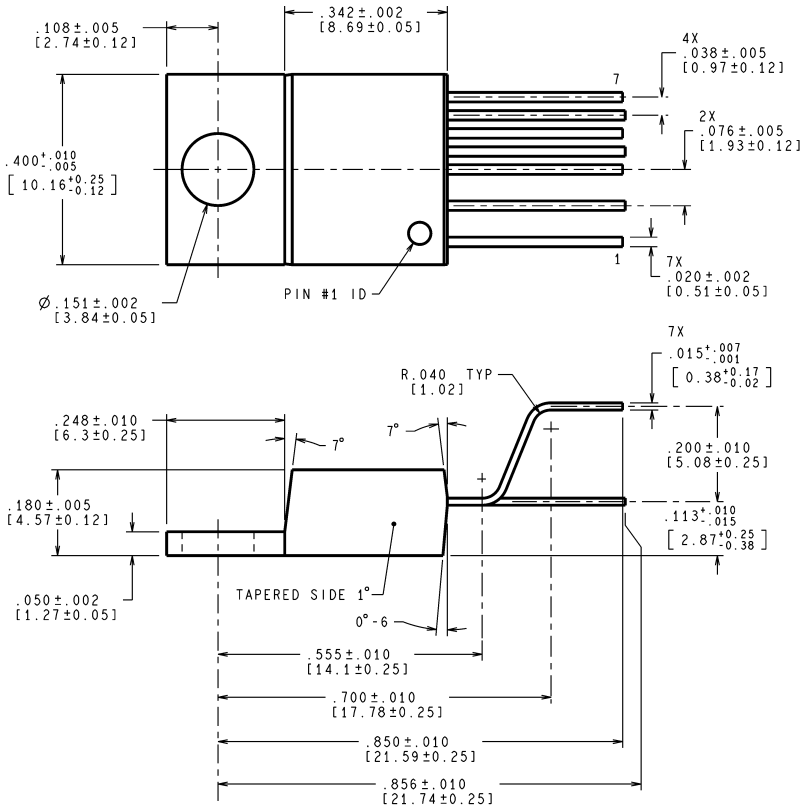
FIGURE 16. Trace Routing and Component Placement from LM2459 Output to Cathode

Physical Dimensions inches (millimeters)

unless otherwise noted



CONTROLING DIMENSION IS INCH
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TE07A (Rev A)

NS Package Number TE07A
Order Number LM2459TE

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