1 GSPS Quadrature Digital Upconverter w/18-Bit IQ Data Path and 14-Bit DAC

PRELIMINARY TECHNICAL DATA

AD9957

FEATURES

1GSPS internal clock speed (up to 400MHz analog out)
Integrated 1GSPS 14-bit DAC
250 MHz I/Q data throughput rate
Phase noise ≤ –123 dBc/Hz (400 MHz carrier)
Excellent dynamic performance >80 dB narrowband SFDR
8 Programmable Profiles for shift keying
SIN(X)/(X) Correction (Inverse SINC filter)
Reference Clock Multiplier
Internal oscillator for a single crystal operation
Software and hardware controlled power-down
Integrated RAM
Phase modulation capability
Multichip synchronization
Easy interface to Blackfin™ SPORT
Interpolation factors from 4x to 252x
Test tone circuitry
Interpolation DAC Mode
Gain control DAC
Internal divider allows references up to 2 GHz
1.8V & 3.3V Power Supplies
100 Lead TQFP package

APPLICATIONS

HFC Data, Telephony & Video Modems
Wireless Base Station Transmission
Broadband Communications Transmissions
Internet Telephony

GENERAL DESCRIPTION

The AD9957 functions as a universal I/Q modulator and agile upconverter for communications systems where cost, size, power consumption and dynamic performance are critical. The AD9957 integrates a high speed Direct Digital Synthesizer (DDS), a high performance, high speed 14-bit digital to analog converter (DAC), clock multiplier circuitry, digital filters and other DSP functions onto a single chip. It provides for base band up-conversion for data transmission in a wired or wireless communications system.

The AD9957 is the third offering in a family of a quadrature digital upconverters (QDUCs), which includes the AD9857 and AD9856. It offers performance gains in operating speed, power consumption and spectral performance. Unlike its predecessors, it also supports a 16-bit serial input mode for I/Q base band data. The device can alternatively be programmed to operate as a single-tone sinusoidal source or as an interpolating DAC.

The Reference Clock input circuitry includes a crystal oscillator, a high speed divide-by-two input, and a low noise PLL for multiplication of the reference clock frequency.

The user interface to the control functions includes a serial port easily configured to interface to the SPORT of the Blackfin DSP and profile pins which enable fast and easy shift keying of any signal parameter (phase, frequency, and amplitude).

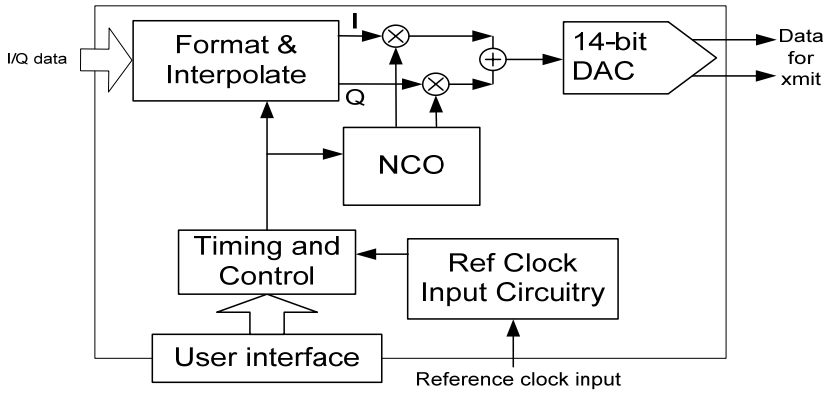

Figure 1: Basic Block Diagram

Rev. PrF

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TABLE OF CONTENTS

REVISION HISTORY

Revision PrA (5/25/05): Initial Version of Preliminary Datasheet

Revision PrB (9/30/05): Register map, pinout, pin description added

Revision PrC (12/06/05): Register map completed, pinout updated.

Revision PrD (2/27/06) Further progress

Revision PrE (3/31/06) Incorporated Marketing review comments

ELECTRICAL SPECIFICATIONS

Table 1. Unless otherwise noted, AVDD, DVDD = 1.8V ± 5%, DAC_VDD, DVDD_I/O = 3.3 V ± 5%, R_{SET} = 10kΩ, External Reference Clock Frequency = 25 MHz. 40x REFLCK multiplier engaged.

Parameter	Min	Typ	Max	Unit
REF CLOCK INPUT CHARACTERISTICS				
Frequency Range				
REFCLK Multiplier Disabled, Divider Disabled	1		1000	MHz
REFCLK Multiplier Disabled, Divider Enabled			2000	MHz
REFCLK Multiplier Enabled at 8×	52.5		125	MHz
REFCLK Multiplier Enabled at 64×	6.5		35	MHz
REFCLK Multiplier Enabled at 127×	3.3		7.9	MHz
XTAL frequency on REFCLK inputs	20		30	MHz
Input Capacitance		3		pF
Input Impedance		1.5		kΩ
Duty Cycle		50		%
Duty Cycle with REFCLK Multiplier Enabled	35		65	%
REFCLK Input Voltage Swing	100		1000	mV pk-pk
REFCLK Input Power[1]	–15	0	+3	dBm
DAC OUTPUT CHARACTERISTICS				
Full Scale Output Current	10	20	30	mA
Gain Error	–10		+10	%FS
Output Offset			0.6	µA
Differential Nonlinearity		1		LSB
Integral Nonlinearity		2		LSB
Output Capacitance		5		pF
Residual Phase Noise @ 1 kHz Offset, 400 MHz A_{OUT}				
REFCLK Multiplier Disabled		–123		dBc/Hz
REFCLK Multiplier Enabled @ 127×		TBD		dBc/Hz
REFCLK Multiplier Enabled @ 64×		–105		dBc/Hz
REFCLK Multiplier Enabled @ 8×		–115		dBc/Hz
AC Voltage Compliance Range	-0.5V		0.5V	V
SPURIOUS-FREE DYNAMIC RANGE (SFDR)				
fout = 50 MHz		TBD		dBc
fout = 104 MHz		TBD		dBc
fout = 209 MHz		TBD		dBc
fout = 315 Mhz		TBD		dBc
fout = 403 MHz		TBD		dBc
TWO TONE INTERMODULATION DISTORTION (IMD)				
fout = fout + 1.25 MHz				
fout = 50 MHz		TBD		dBc
fout = 104 MHz		TBD		dBc
fout = 209 MHz		TBD		dBc
fout = 315 Mhz		TBD		dBc
fout = 403 MHz		TBD		dBc
NOISE SPECTRAL DENSITY (NSD) Single Tone				
fout = 50 MHz		TBD		dBm / Hz
fout = 104 MHz		TBD		dBm / Hz
fout = 209 MHz		TBD		dBm / Hz
fout = 315 Mhz		TBD		dBm / Hz
fout = 403 MHz		TBD		dBm / Hz

Parameter	Min	Typ	Max	Unit
NOISE SPECTRAL DENSITY (NSD) Continued				
Eight Tone, 500KHz Tone Spacing				
fout = 50 MHz		TBD		dBm / Hz
fout = 104 MHz		TBD		dBm / Hz
fout = 209 MHz		TBD		dBm / Hz
fout = 315 Mhz		TBD		dBm / Hz
fout = 403 MHz		TBD		dBm / Hz
MODULATOR CHARACTERISTICS (260MHz A_{OUT}				
Input Data: 10MS/s, QPSK, 4x Oversampled				
I/Q Offset	55	65		dB
Error Vector Magnitude		0.4	1	%
Input Data: 10MS/s GMSK 4x Oversampled				
I/Q Offset	TBD	TBD		dB
Error Vector Magnitude		TBD	TBD	%
Input Data: 10MS/s 256-QAM 4x Oversampled				
I/Q Offset	TBD	TBD		dB
Error Vector Magnitude		TBD	TBD	%
Adjacent Channel Leakage Ratio (ACLR)				
WCDMA with 3.84MHz BW, 5MHz Channel Spacing				
fDAC=1GSPS, fOUT=200MHz		79		dB
fDAC=1GSPS, fOUT=400MHz		74		dB
TIMING CHARACTERISTICS				
Parallel Data Bus				
Maximum Frequency		250		MS/s
Minimum TxEnable Pulse Width Low		2		ns
Minimum TxEnable Pulse Width High		2		ns
Minimum Data Setup Time (TxEnable to PDClk)		4		ns
Minium Data Hold Time (PDClk rising edge to data change)		0		ns
Serial Control Bus				
Maximum Frequency		25		Mbps
Minimum Clock Pulse Width Low	7			ns
Minimum Clock Pulse Width High	7			ns
Maximum Clock Rise/Fall Time		2		ns
Minimum Data Setup Time DVDD_I/O = 3.3 V	3			ns
Minimum Data Hold Time	0			ns
Maximum Data Valid Time		25		ns
Wake-Up Time[2]				
Minimum Reset Pulse Width High	5			SYSCLK Cycles3
I/O UPDATE, PS0, PS1 to SYNCCLK Setup Time DVDD_I/O = 3.3 V	4			ns
I/O UPDATE, PS0, PS1 to SYNCCLK Hold Time	0			ns
Latency				
I/O UPDATE to Frequency Change Propagation Delay	24			SYSCLK Cycles
I/O UPDATE to Phase Offset Change Propagation Delay	24			SYSCLK Cycles
I/O UPDATE to Amplitude Change Propagation Delay	16			SYSCLK Cycles
CMOS LOGIC INPUTS				
Logic 1 Voltage	2.2			V
Logic 0 Voltage			0.8	V
Logic 1 Current		3	12	µA
Logic 0 Current			12	µA
Input Capacitance		2		pF

Parameter	Min	Typ	Max	Unit
CMOS LOGIC OUTPUTS (1 mA Load)				
Logic 1 Voltage	2.8			V
Logic 0 Voltage			0.4	V
XTAL OUTPUT BUFFER SPECS				
Logic 1 Voltage	1.6			V
Logic 0 Voltage			TBD	V
Output Current			TBD	mA
POWER CONSUMPTION				
DVDD_I/O(3.3V) current consumption (QDUC mode)				mA
DVDD(1.8V) current consumption (QDUC mode)				mA
AVDD(3.3V) current consumption (QDUC mode)				mA
AVDD(1.8V) current consumption (QDUC mode)				mA
Single Tone Mode		500		mW
Continuous Modulation 255x Interpolation		TBD	1000	mW
Continuous Modulation 4x Interpolation		TBD	TBD	mW
Burst Modulation (25%) 255x Interpolation		TBD	TBD	mW
Burst Modulation (25%) 4x Interpolation		TBD	TBD	mW
Full-Sleep Mode		TBD	TBD	mW
Inverse Sinc Filter Power Consumption		150	TBD	mW

1 To achieve the best possible phase noise, the largest amplitude clock possible should be used. Reducing the clock input amplitude will reduce the phase noise performance of the device.

2 Wake-up time refers to the recovery from analog power-down modes.

3 SYSCLK cycle refers to the actual clock frequency used on-chip by the DDS. If the reference clock multiplier is used to multiply the external reference clock frequency, the SYSCLK frequency is the external frequency multiplied by the reference clock multiplication factor. If the reference clock multiplier and divider are not used, the SYSCLK frequency is the same as the external reference clock frequency.

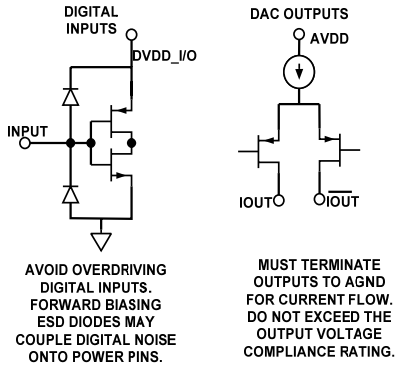


Figure 2 Equivalent Input/Output (I/O) Circuits

ABSOLUTE MAXIMUM RATINGS

Table 2.

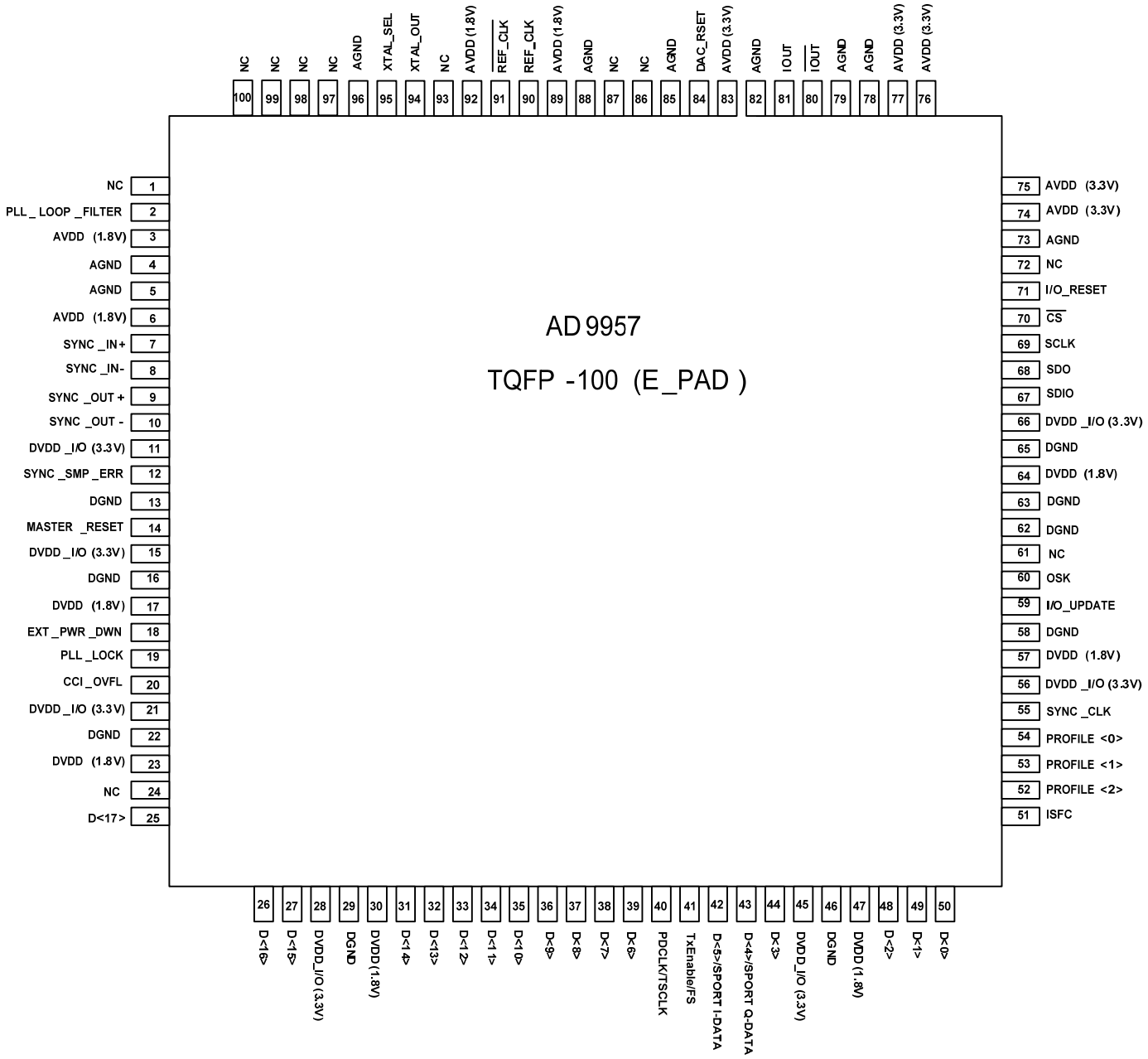
Parameter	Rating
Maximum Junction Temperature	150°C
AVDD(1.8V), DVDD(1.8V) supplies	2 V
AVDD(3.3V), DVDD_I/O(3.3V) supplies	4V
Digital Input Voltage)	–0.7 V to +4V
Digital Output Current	5 mA
Storage Temperature	–65°C to +150°C
Operating Temperature	–40°C to +85°C
Lead Temperature (10 sec Soldering)	300°C
θ_{JA}	38°C/W
θ_{JC}	15°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Caution

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN DESCRIPTION

Pin #	Mnemonic	I/O	Description
1, 24, 61, 72, 86, 87, 93, 97-100	NC		Not Connected. Allow device pin to float.
2	PLL_LOOP_FILTER	I	PLL loop filter compensation pin.
3, 6, 89, 92	AVDD (1.8V)	I	Analog Core VDD: 1.8V Analog Supply.
74-77, 83	AVDD (3.3V)	I	Analog DAC VDD: 3.3V Analog Supply.
17, 23, 30, 47, 57, 64	DVDD (1.8V)	I	Digital Core VDD: 1.8V Digital Supply.
11, 15, 21, 28, 45, 56, 66	DVDD_I/O (3.3V)	I	Digital Input/Output VDD: 3.3V Digital Supply.
4, 5, 73, 78, 79, 82, 85, 88, 96	AGND	I	Analog Ground.
13, 16,22, 29,46,58,62,63 65	DGND	I	Digital Ground.
7	SYNC_IN+	I	Digital input (rising edge active). Synchronization signal from external master to synchronize internal sub-clocks.
8	SYNC_IN-	I	Digital input (rising edge active). Synchronization signal from external master to synchronize internal sub-clocks.
9	SYNC_OUT+	O	Digitaloutput (rising edge active). Synchronization signal from internal device sub-clocks to synchronize external slave devices.
10	SYNC_OUT-	O	Digitaloutput (rising edge active). Synchronization signal from internal device sub-clocks to synchronize external slave devices.
12	SYNC_SMP_ERR	O	Digital output (active high). Sync sample error: A high on this pin indicates that the AD9957 did not receive a valid sync signal on SYNC_I+/SYNC_I-.
14	MASTER _RESET	I	Digital Input (active high). Master reset: clears all memory elements and sets registers to default values.
18	EXT_PWR_DWN	I	Digital input (active high). External Power Down: A high level on this pin initates the currently programmed power down mode. Please see the Power Down Modes section of this document for further details. If unused, tie to ground.
19	PLL_LOCK	O	Digital output (active high). PLL_Lock: A high indicates the clock multiplier PLL has acquired lock to the reference clock input.
20	CCI_OVFL	O	Digital output (active high). CCI Overflow: A high indicates a CCI filter overflow. This pin will remain high until the CCI overflow condition is cleared.
25-27, 31-39, 42-44, 48-50	D<17:0>	I	Parallel data input bus (active high). These pins provide the interleaved 18 bit digital I & Q vectors for the modulator to upconvert.
42	SPORT I-DATA	I	In Blackfin interface mode, this pin serves as the I-data serial input.
43	SPORT Q-DATA	I	In Blackfin interface mode, this pin serves as the Q-data serial input.
40	PDCLK/TSCLK	O	Digital output (clock) Parallel Data Clock see Signal Processing section for details
41	TxENABLE	I	Digital input (active high). Transmit enable: see Signal Processing section for details
41	FS	I	In Blackfin interface mode, this pin serves as the FS Input, to receive the RFS OUTPUT signal from the ADSP BF533
51	ISFC	I	Digital input (active high). Input Scaling Function Control: Control for the RAM amplitude scaling function. When this function is engaged, a high sweeps the amplitude from the beginning RAM address to the end. A low sweeps the amplitude from the end RAM address to the beginning.
52-54	PROFILE <2:0>	I	Digital inputs (active high). Profile select pins: used to select one of eight phase/frequency profiles for the DDS core (single-tone or carrier tone). Changing the state of one of these pins will transfer the current contents of all I/O buffers to the corresponding registers. State changes should be setup to the IO_SYNC_CLK pin.
55	SYNC_CLK	O	Digital output (clock). Outputs System clock/4. The I/O_UPDATE and PROFILE<2:0> pins should be setup to the rising edge of this signal.

59	I/O_UPDATE	I	Digital input (active high). Input/Output update: A high on this pin transfers the contents of the I/O buffers to the corresponding internal registers.
60	OSK	I	Digital input (active high). Output shaped keying: When the OSK features (manual or automatic), this device controls the OSK function. In manual mode, it toggles the multiplier between 0 (low) and the programmed amplitude scale factor (high). In automatic mode, a low sweeps the amplitude down to zero, a high sweeps the amplitude up to the amplitude scale factor.
67	SDIO	I/O	Digital input/output (active high). Serial data input/output: this pin can be either uni-directional or bidirectional (default), depending on configuration settings. In bidirectional serial port mode, this pin acts as the serial data input and output. In unidirectional, it is an input only.
68	SDO	O	Digital output (active high). Serial Data output: this pinis only active in unidirectional serial data mode. In this mode, it functions as the output. In bidirectional mode, this pin is not operational and should be left floating.
69	SCLK	O	Digital clock (rising edge on write, falling edge on read). Serial data clock: this pin provides the serial data clock for the control data path. Write operations to the AD9957 use the rising edge. Readback operations from the AD9957 use the falling edge.
70	$\overline{CS}$	I	Digital input (active low) Chip Select: Bringing this pin low enables the AD9957 to detect serial clock rising/falling edges. Bringing this pin high will cause the AD9957 to ignore input on the serial data pins.
71	I/O_RESET	I	Digital input (active high) I/O Reset: Rather than resetting the entire device during a failed communication cycle, when brought high this pin will reset the state machine of the serial port controller and clear any I/O buffers that have been written since the last I/O Update. When unused, tie this pin to ground to avoid accidental resets.
80	$\overline{IOUT}$	O	Analog output (current mode): Open source DAC complementary output source. Connect through 50Ω to AGND.
81	IOUT	O	Analog output (current mode): Open source DAC output source. Connect through 50Ω to AGND.
84	DAC_RSET	O	Analog reference pin: programs the DAC output full scale reference current. Attach a 10KΩ resistor to AGND.
90	REF_CLK	I	Analog input(active high): Reference CLK input. Can be driven by either an external oscillator or a simple crystal when the internal oscillator is engaged.
91	REF_$\overline{CLK}$	I	Analog input(active high): Reference CLK input
94	XTAL_OUT	O	Analog output (active high). Crystal Output: Provides the output of the internal oscillator's response to a crystal.
95	XTAL_SEL	O	Crystal Select: selects the reference clock input mode when using the on-chip PLL. Pulling this pin low allows the user to provide a reference clock input to the PLL from an external source. Pulling this pin high enables the on-chip XTAL buffer and allows the user to drive the reference input clock with a crystal

MODES OF OPERATION

The AD9957 has three basic operating modes:

- Quadrature modulation mode (default)
- Interpolating DAC mode
- Single-tone mode

The active mode is selected via the QDUC Operating mode bits (CFR1 <25:24>). The Inverse SINC filter is available in all three modes.

QUADRATURE MODULATION MODE

A block diagram of the AD9957 operating in the quadrature modulation mode is shown in Figure 3. In quadrature modulation mode, both I and Q data paths are active and the parallel data clock (PDCLK) serves to synchronize the input of I/Q data to the AD9957. One 18-bit I word and one 18-bit Q word together comprise one internal *sample*. Each sample propagates along the internal data pathway in parallel fashion.

The DDS core provides a quadrature (sine and cosine) local oscillator signal to the quadrature modulator, where the I and Q data are multiplied by the respective phase of the carrier and summed together, producing a quadrature-modulated data stream. This data stream is routed through Inverse SINC filter (optionally) and the output scaling multiplier and then applied to the 14-bit DAC which produces the quadrature-modulated analog output signal. Note: The profile and I/O_UPDATE pins are also synchronous to the PDCLK.

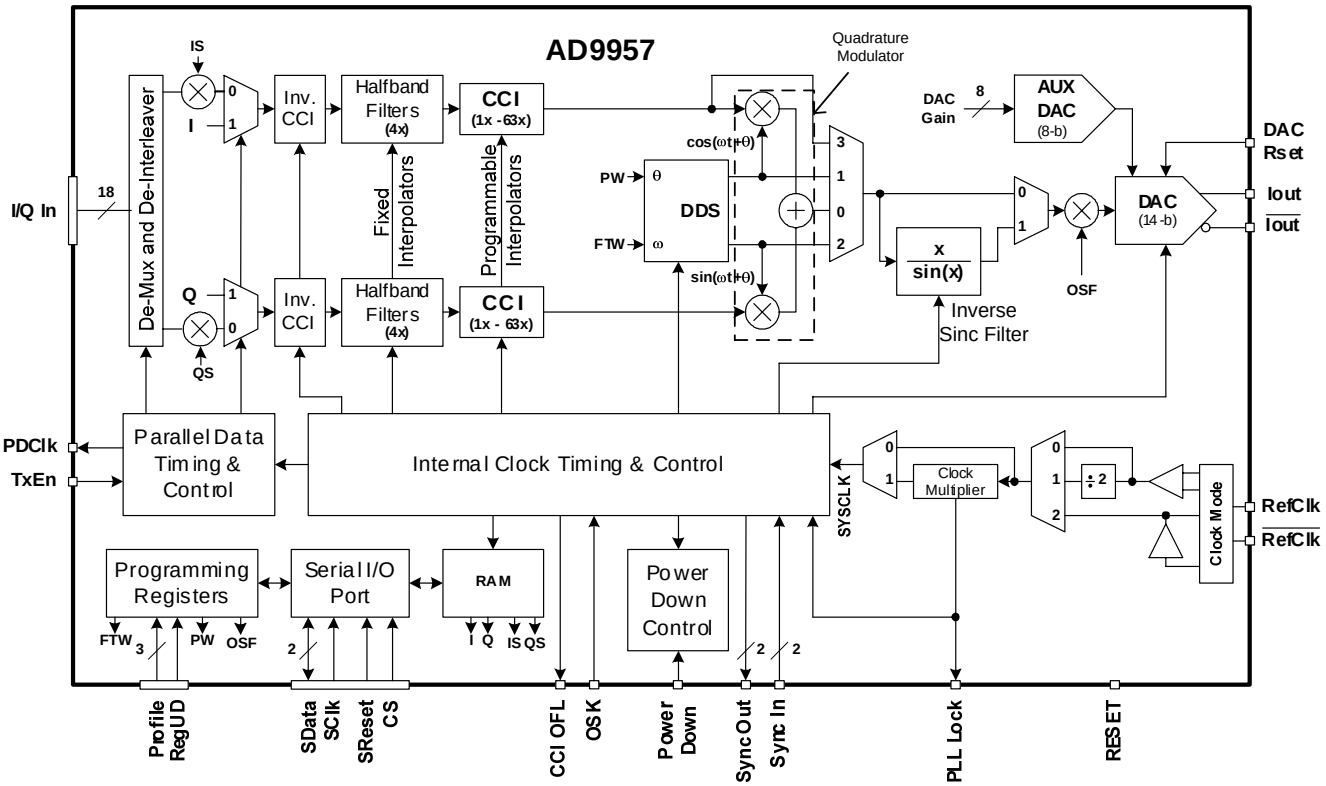


Figure 3: Quadrature Modulation Mode

BLACKFIN INTERFACE MODE

A subset of the quadrature modulation mode is the BlackFin Interface (**BFI**) mode, which is shown in Figure 4. In this mode a separate I and Q serial bit stream is applied to the base band data port. The serial input provides for 16-bit I and Q words (unlike parallel operation, which uses 18-bit words). The BlackFin Interface mode includes an additional pair of half band filters in both the I and Q signal paths, increasing the interpolation of the base band data by 4x relative to the normal quadrature modulation mode.

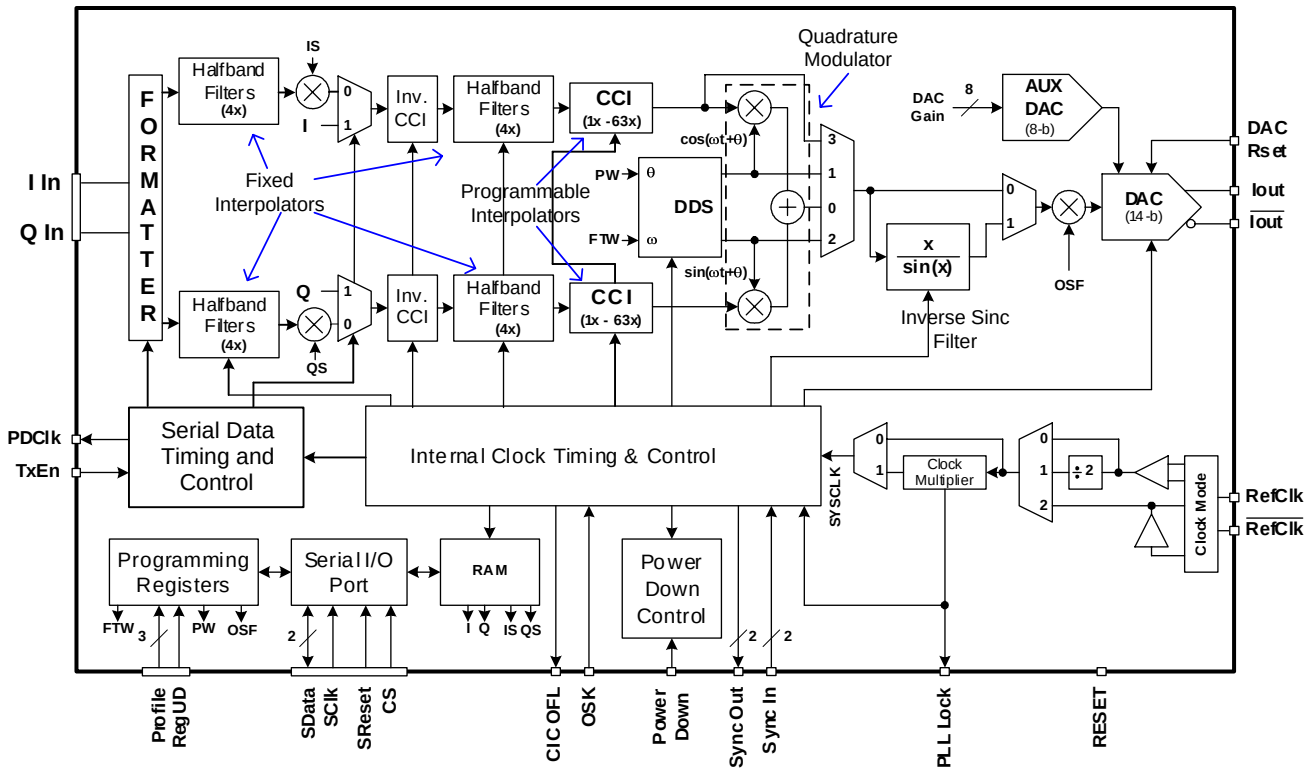


Figure 4: Quadrature Modulation Mode -- BlackFin Interface

SIGNAL PROCESSING (QDUC & BFI MODES)

To better understand the operation of the AD9957 it is helpful to follow the signal path in quadrature modulation mode from the parallel data port to the output of the DAC, examining the function of each block (refer to Figure 4).

All timing within the AD9957 is provided by the internal system clock (SYSCLK) signal, which is generated from the timing source provided to the REFCLK pins.

PDCLK Pin

The timing of input data supplied to the AD9957 is easily facilitated with the PDCLK output pin, which serves as a data clock timing source. In QDUC mode, PDCLK controls the timing of the 18-bit parallel input port. In BFI mode, PDCLK controls the timing of the dual serial input port. The PDCLK is provided as a continuous clock (i.e., always active). However, even though the PDCLK output is active by default, it can be disabled via the *Enable PDCLK* bit in the register map.

In QDUC mode, the AD9957 expects alternating I and Q data words at the parallel port (see Figure 5). Each rising edge of PDCLK captures one 16-bit word; that is, two PDCLK cycles per I/Q pair.. In BFI mode, the AD9957 expects two serial bit streams each segmented into 16-bit words with each rising edge of PDCLK indicating a new bit. In either case, the output clock rate is f_{DATA} as explained in the *Input Data Assembler* section.

TxEnable Pin

The rising edge of the TxENABLE signal is used to synchronize the device. While TxENABLE is in the Logic 0 state, the device ignores the data applied to the parallel port allowing the internal data path to be flushed by forcing zeros down the I and Q data pathways. On the rising edge of TxENABLE, the device is ready for the first I word. The first I word is latched into the device coincident with the rising edge of PDCLK. The next rising edge of PDCLK latches in a Q word, etc., until TxENABLE is set to a Logic 0 state by the user.

It is important that the user ensure an even number of PDCLK intervals are observed during any given TxENABLE period. The device must capture *both* an I and a Q sample before the data is processed along the signal chain.

In BFI mode, operation of the TxENABLE pin is similar except that instead of the rising edge marking the first "I word", it marks the first I (and Q) bit in a serial frame.

It is important that the user ensure a multiple of 16 PDCLK cycles are observed during any given TxENABLE period. The device must capture a full 16-bit I and Q sample before the data is processed along the signal chain.

The timing relationship between TxENABLE, PDCLK, and

DATA is shown in Figure 5 and Figure 6.

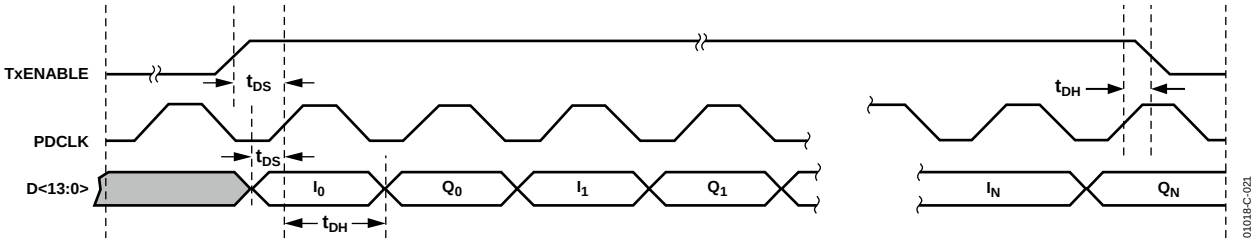


Figure 5. 18-Bit Parallel Port Timing Diagram—Quadrature Modulation Mode

Table 3. Parallel Data Bus Timing

Symbol	Definition	Minimum
t_{DS}	**Data Setup Time**	**4 ns**
t_{DH}	**Data Hold Time**	**0 ns**

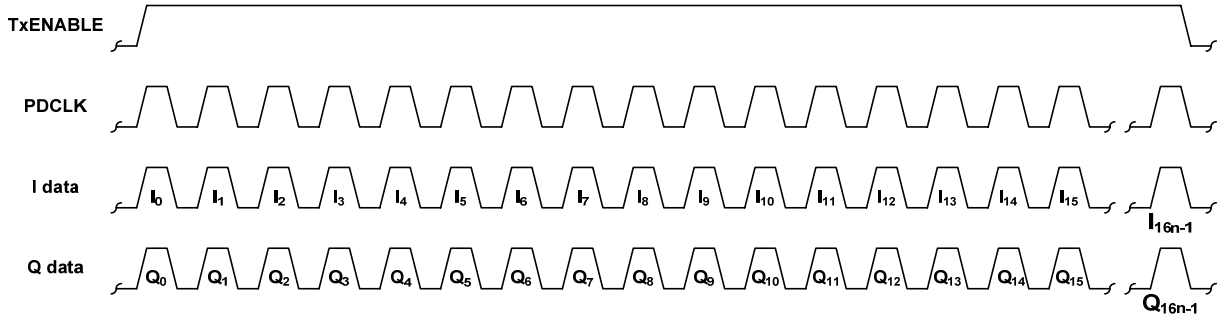


Figure 6: Dual Serial I/Q Bitstream Timing Diagram – BFI mode

Table 4: Serial Data Bus Timing

Symbol	Definition	Minimum
t_{DS}	**Data Setup Time**	**TBD**
t_{DH}	**Data Hold Time**	**TBD**

Input Data Assembler

The input to the AD9957 is an 18-bit parallel data port in quadrature modulation mode (or a dual serial data port in the BFI mode). It is assumed that two consecutive 18-bit words represent the real (I) and imaginary (Q) parts of a complex number that has the form I+jQ. The 18-bit words are supplied to the input of the AD9957 at a rate of:

$$f_{DATA} = \frac{f_{SYSCLK}}{2R} \quad \text{(QDUC mode)}$$

Where f_{SYSCLK} is the sample rate of the DAC and R is the interpolation factor of the programmable interpolation filter.

When device is programmed to operate in BFI mode, the 18-bit parallel input is converted to a dual serial input. That is, one pin is assigned as the serial input for the "I" words and one pin is assigned as the serial input for the "Q" words. The other 16 pins are not used in the BFI mode. Furthermore, each I and Q word has 16-bit resolution (as compared with 18-bit resolution in the non-BFI mode). In BFI mode, f_{DATA} is the bit rate of the I and Q data streams and is given by:

$$f_{DATA} = \frac{f_{SYSCLK}}{R} \quad \text{(BFI mode)}$$

Encoding and pulse shaping of symbols must be implemented before the data is presented to the input of the AD9957. Data

delivered to the input of the AD9957 may be formatted as either twos-complement or unsigned binary (see the *Data Format* bit in the register map). Furthermore, in BFI mode, the order of the bit sequence can be set to either "MSB First" or "LSB First" (via the *BlackFin Bit Order* bit in the register map).

Inverse CCI Filter

The inverse CCI (cascaded comb integrator) filter precompensates the data to offset the slight attenuation gradient imposed by the CCI filter (see the Programmable (2× to 63×) CCI Interpolating filter section). Data entering the first half-band filter occupies a maximum band width of one-half f_{IQ} as defined by Nyquist (where f_{IQ} is the sample rate at the input of the first half-band filter). This is shown graphically in Figure 7.

If the CCI filter is employed, the inband attenuation gradient could pose a problem for those applications requiring an extremely flat pass band. For example, if the spectrum of the data as supplied to the AD9957 occupies a significant portion of the one-half f_{DATA} region, the higher frequencies of the data spectrum receives slightly more attenuation than the lower frequencies (the worst-case overall droop from f=0 to $\frac{1}{2}f_{DATA}$ is < 0.8 dB). The Inverse CCI filter has a response characteristic that is the inverse of the CCI filter response over the $\frac{1}{2}f_{IQ}$ region.

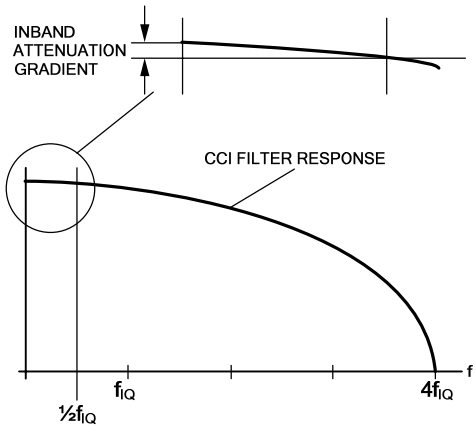


Figure 7. CCI Filter Response

The product of the two responses yields in an extremely flat pass band (±0.05 dB over the base band Nyquist band width), thereby eliminating the inband attenuation gradient introduced by the CCI filter. The cost is a slight attenuation of the input signal of approximately 0.5 dB for a CCI interpolation rate of 2 and 0.8 dB for interpolation rates of 3 to 63.

The Inverse CCI filter can be bypassed using the appropriate bit in the register map. Even if it is enabled, it is automatically bypassed if the CCI interpolation rate is 1×. When the Inverse CCI filter is bypassed, power to the stage is turned off to reduce power consumption.

Fixed interpolator (4x)

This block is a fixed 4× rate interpolator. It is implemented as a cascade of two half-band filters. Together, the two half-band filters provide a factor of four increase in the sampling rate, while preserving the spectrum of the base band signal applied at the input. Both half-band filters are linear phase filters, so that virtually no phase distortion is introduced within the pass band of the filters. Their combined insertion loss is 0.01 dB, thus preserving the relative amplitude of the input signal.

The half-band filters are designed so that their composite performance yields a usable pass band of 40% of the input sample rate (0.2 on the frequency scale below). Within that pass band, the ripple does not exceed 0.002 dB. The stop band extends from 60% to 200% of the input sample rate (0.3 to 1.0 on the frequency scale) and offers a minimum of 85 dB attenuation. Figure 8 and Figure 9 show the composite response of the two half-band filters.

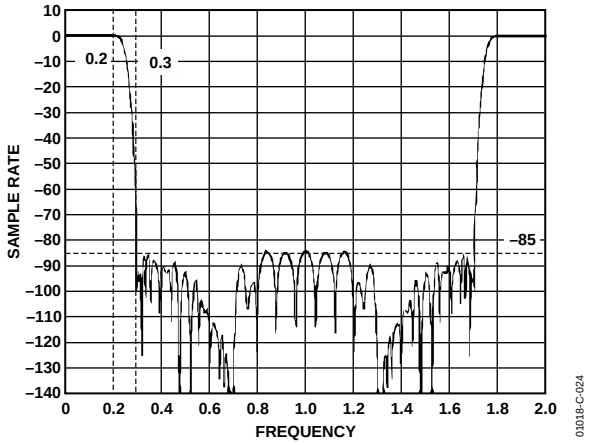


Figure 8. Half-Band 1 and 2 Frequency Response; Frequency Relative to HB1 Output Sample Rate

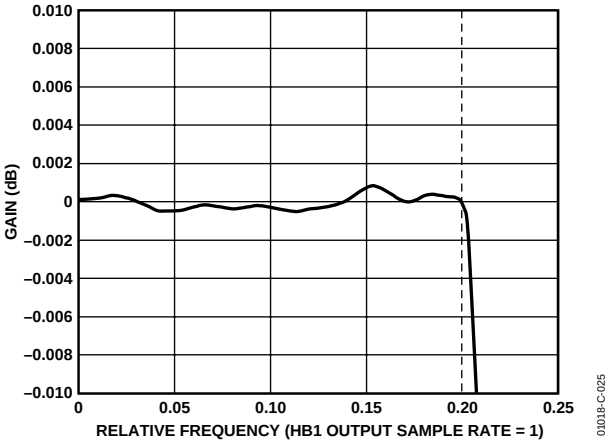


Figure 9. Combined Half-Band 1 and 2 Pass Band Detail; Frequency Relative to HB1 Output Sample Rate

Knowledge of the frequency response of the half-band filters is essential to understanding their impact on the spectral properties of the input signal. This is especially true when using the quadrature modulator to upconvert a base band signal containing complex data symbols that have been pulse shaped.

To better understand this concept, consider that a complex symbol is represented by a real (I) and imaginary (Q) component. Thus, two digital words are required to represent a single complex sample of the form: I+jQ. The sample rate associated with a sequence of complex symbols will be referred to as f_{SYMBOL}. If pulse shaping is applied to the symbols, then the sample rate must necessarily be increased by some integer factor, M (a consequence of the pulse shaping process). This new sample rate with be referred to as f_{IQ}, and is related to the symbol rate by:

$$f_{IQ} = Mf_{SYMBOL}$$

Thus, f_{IQ} is the rate at which complex samples must be supplied to the input of the first half-band filter in both the "I" and "Q" signal paths. *NOTE: This rate is not to be confused with the rate at which parallel data is supplied to the AD9957(f_{DATA}), which is equal to $2f_{IQ}$.*

Typically, pulse shaping is applied to the base band symbols via a filter having a raised cosine response. In such cases, an excess band width factor (α) is used to modify the band width of the data where $0 \le \alpha \le 1$. A value of 0 causes the data band width to correspond to $\frac{1}{2}f_{SYMBOL}$, while a value of 1 causes the data band width to be extended to f_{SYMBOL}. Figure 10 illustrates the relationship between α, the band width of the raised cosine response, and the response of the first half-band filter.

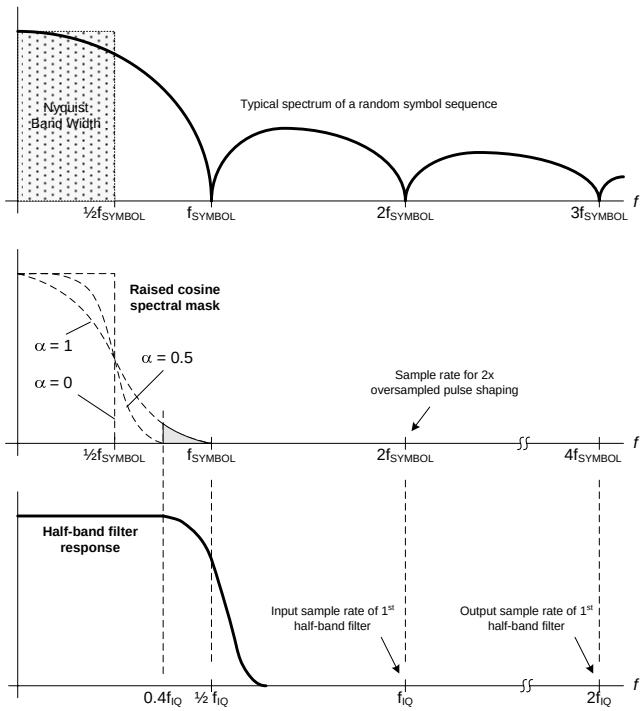


Figure 10. Effect of the Excess Band width Factor (α)

The responses in Figure 10 are shown for the specific case of M=2 (the interpolation factor for the pulse shaping operation). In cases for which M>2, the location of the f_{IQ} point on the half-band response portion of the diagram shifts to the right, as it must remain aligned with the corresponding Mf_{SYMBOL} point on the frequency axis of the raised cosine spectral diagram. However, if f_{IQ} shifts to the right, so does the half-band response, proportionally.

The result is that the raised cosine spectral mask always lies within the flat portion (DC to $0.4f_{IQ}$) of the pass band response of the first half-band filter, regardless of the choice of α so long as M>2. Therefore, for M>2, the first half-band filter has absolutely no negative impact on the spectrum of the base band signal when raised cosine pulse shaping is employed. However, for the case of M=2, a problem can arise. This is highlighted by the shaded area in the tail of the α=1 trace on the raised cosine spectral mask diagram. Notice that this portion of the raised cosine spectral mask extends beyond the flat portion of the half-band response and will cause unwanted amplitude and phase distortion as the signal passes through the first half-band filter. To avoid this, simply ensure that $\alpha \le 0.6$ when M=2.

Programmable Interpolating Filter

The Programmable Interpolator is implemented as a CCI filter with a low-pass frequency characteristic. It is programmable by a 6-bit control word, giving a range of 2× to 63× interpolation.

The Programmable Interpolator is bypassed when programmed for an interpolation factor of 1. When bypassed, power to the stage is removed and the Inverse CCI filter (see above) is also bypassed, because its compensation is not needed in this case.

The output of the Programmable Interpolator is the data from the 4× interpolator further upsampled by the CCI filter, according to the rate chosen by the user. This results in the input data being upsampled by a factor of 8× to 252× in steps of 4.

The transfer function of the CCI interpolating filter is

$$H(f) = \left(\sum_{k=0}^{R-1} e^{-j(2\pi fk)} \right)^5 \quad (1)$$

where *R* is the programmed interpolation factor, and *f* is the frequency relative to SYSCLK.

Quadrature Modulator

The digital quadrature modulator stage shifts the frequency of the *base band* spectrum of the incoming data stream up to the desired carrier frequency (this process is known as *up-conversion*).

At this point the base band data, which was delivered to the device at an I/Q sample rate of f_{IQ}, has been upsampled to a rate equal to the frequency of SYSCLK, making the data sampling rate equal to the sampling rate of the carrier signal.

The frequency of the carrier signal is controlled numerically by a Direct Digital Synthesizer (DDS). The DDS generates the desired carrier frequency from the internal reference clock (SYSCLK) very precisely. The carrier is applied to the I and Q multipliers in quadrature fashion (90° phase offset) and summed, yielding a data stream that represents the *quadrature modulated carrier*.

The modulation is done digitally avoiding the phase offset, gain imbalance and crosstalk issues commonly associated with analog modulators. Note that the modulated "signal" is a number stream sampled at the rate of SYSCLK, the same rate at which the DAC is clocked.

The orientation of the modulated signal with respect to the carrier is controlled by a spectral invert bit. This bit resides in each of the four profile registers. By default, the time domain output of the quadrature modulator takes the form:

$$I(t) \times \cos(\omega t) - Q(t) \times \sin(\omega t) \quad (2)$$

When the spectral invert bit asserted, it becomes:

$$I(t) \times \cos(\omega t) + Q(t) \times \sin(\omega t) \quad (3)$$

DDS Core

The Direct Digital Synthesizer (DDS) block generates the sine and cosine carrier reference signals that digitally modulate the I/Q data. The DDS output is tuned using registers accessed via the serial programming port. This allows for both precise tuning of the carrier frequency and the ability to change frequency instantaneously.

The equation relating output frequency (f_{OUT}) of the AD9957 digital modulator to the frequency tuning word (FTW) and the system clock (f_{SYSCLK}) is

$$f_{OUT} = \left(\frac{FTW}{2^{32}} \right) f_{SYSCLK} \quad (4)$$

where FTW is a decimal number from 0 to 2,147,483,647 ($2^{31}-1$).

Solving for FTW yields:

$$FTW = round\left(2^{32} \left(\frac{f_{OUT}}{f_{SYSCLK}} \right) \right) \quad (5)$$

The *round()* function means to round the result to the nearest integer. For example, for f_{OUT} = 41 MHz and f_{SYSCLK} = 122.88 MHz, then FTW = 1,433,053,867 (556AAAAB hex).

Inverse SINC Filter

The sampled carrier data stream is the input to the digital-to-analog converter (DAC) integrated onto the AD9957. The DAC output spectrum is shaped by the characteristic sin(x)/x (or SINC) envelope, due to the intrinsic zero-order hold effect associated with DAC-generated signals. The SINC envelope is well known and can be compensated for. This envelope restoration function is provided by the Inverse SINC filter that precedes the DAC. By default, the filter is bypassed. It is enabled via a bit in the register map. The inverse SINC function is implemented as an FIR filter. It's response characteristic is the exact inverse of the SINC response. The Inverse SINC filter predistorts the data prior to its arrival at the DAC. The correction is only accurate for output frequencies up to approximately 40% of SYSCLK. *NOTE: The inverse SINC filter exhibits ~3.5dB of insersion loss.*

Output Scale Factor (OSF)

Output amplitude is controlled using an 8-bit digital multiplier. The 8-bit multiplier value is called the Output Scale Factor (OSF) and is programmed via the appropriate control registers. It is available for each of the eight profiles. The LSB weight is 2^{-7}, which yields a multiplier range of 0 to 1.9921875 ($2-2^{-7}$). The gain extends to nearly a factor of 2 to provide a means to overcome the intrinsic loss through the modulator when operating in the quadrature modulation mode. *NOTE: Programming the 8-bit multiplier to unity gain (80h) bypasses the stage and reduces power consumption.*

14-Bit DAC

The AD9957 incorporates an integrated 14-bit current-output DAC. The output current is delivered as a balanced signal using

two outputs. The use of balanced outputs reduces the amount of common-mode noise at the DAC output, increasing signal-to-noise ratio. An external resistor (R_{SET}) connected between the DAC_R_{SET} pin and the DAC ground (AGND_DAC) establishes a reference current. The full-scale output current of the DAC (I_{OUT}) is produced as a scaled version of the reference current (see the Auxiliary DAC section that follows).

Proper attention should be paid to the load termination to keep the output voltage within the specified compliance range, as voltages developed beyond this range will cause excessive distortion and might even damage the DAC output circuitry.

Auxiliary DAC

The full scale output current of the main DAC (I_{OUT}) is controlled by an 8-bit auxiliary DAC. An 8-bit code word stored in the appropriate register map location sets I_{OUT} according to the following equation:

$$I_{OUT} = \frac{86.4}{R_{SET}}\left(1+\frac{CODE}{96}\right) \quad (6)$$

Where R_{SET} is the value of the R_{SET} resistor (in ohms) and CODE is the 8-bit value supplied to the auxiliary DAC (default is 127). For example, with R_{SET}=10,000 and CODE=127, then I_{OUT}=20.07mA.

INTERPOLATING DAC MODE

A block diagram of the AD9957 operating in the interpolating DAC mode is shown in Figure 11; grayed out items are inactive. In this mode, the Q data path, DDS and modulator are all disabled; only the I data path is active.

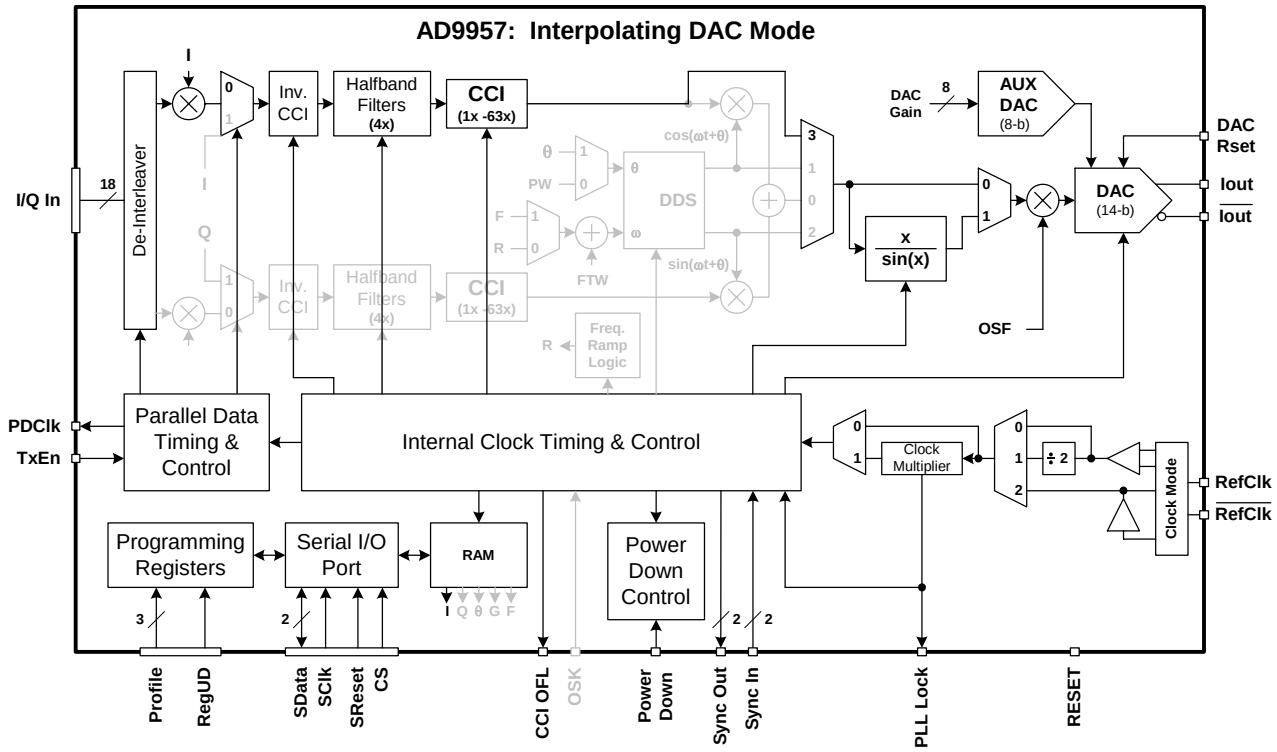


Figure 11: Interpolating DAC Mode

As in the quadrature modulation mode, the PDCLK pin functions as a clock which serves to synchronize the input of data to the AD9957. The PDCLK rate is given below. Note that it operates at a rate that is half of that for the quadrature modulation mode.

$$f_{DATA} = \frac{f_{SYSCLK}}{4R} \quad \text{(Interpolating DAC mode)}$$

Because no modulation takes place, the spectrum of the data supplied at the parallel port remains at base band. However, a sample rate conversion takes place based on the programmed interpolation rate. The interpolation hardware processes the signal, by effectively performing an over-sample with zero-stuffing operation. However, the original input spectrum remains intact and the images that would otherwise occur from the sample rate conversion process are suppressed by the interpolation signal chain.

The PDCLK pin is an output and serves as a data clock timing source. The output clock rate is f_{DATA} as explained in the *Input Data Assembler* section. Each PDCLK rising edge latches a data word into the I data path.

The timing relationship between TxENABLE, PDCLK, and DATA is shown in Figure 12.

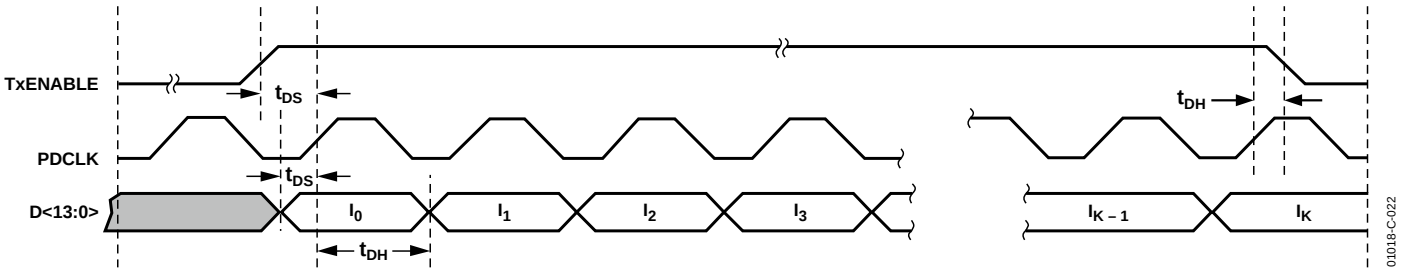


Figure 12. 18-Bit Parallel Port Timing Diagram—Interpolating DAC Mode

SINGLE-TONE MODE

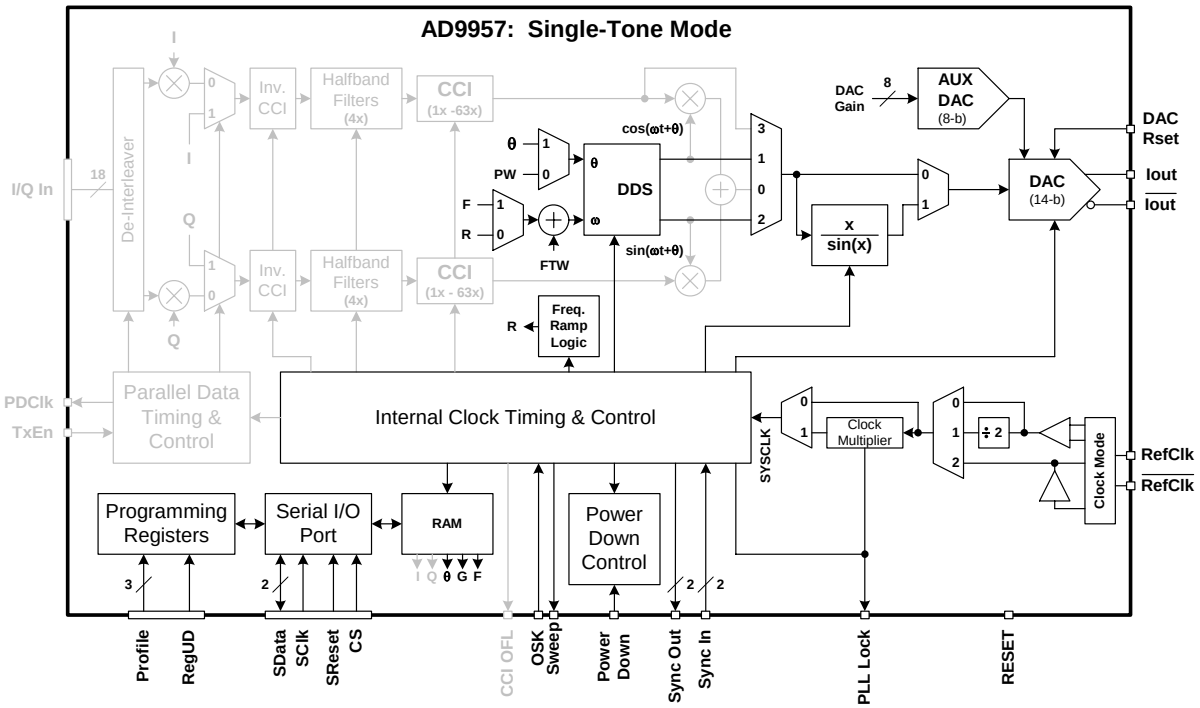


Figure 13: Single-Tone Mode

A block diagram of the AD9957 operating in the single-tone mode is shown in Figure 13; grayed out items are inactive. In this mode, both I and Q data paths are disabled from the 18-bit parallel data port up to and including the modulator. The internal DDS core produces a signal whose frequency depends on the programmed tuning word. The user may select either the cosine (default) or sine output of the DDS. The sinusoid at the DDS output can be scaled via a 14-bit amplitude scale factor (ASF) and optionally routed through the Inverse SINC filter.

Amplitude Scale Factor (ASF)

Output amplitude is controlled by a 14-bit digital multiplier called the Amplitude Scale Factor (ASF), which is programmed via the appropriate control registers. It is available for each of the eight profiles. The LSB weight is 2^{-14}, which yields a multiplier range of 0 to 1.99993896484375 ($1-2^{-14}$).

In addition to the ability to generate single tone signals in this mode, the AD9957 can also provide 2-, 4-, or 8-level modulation of frequency, phase, or amplitude by means of the eight available profile registers and the Profile<0:2> pins.

I/O_UPDATE Pin

In the single-tone mode, the I/O_UPDATE pin serves as a signal update strobe. Frequency, phase and amplitude control words for the DDS are programmed via the serial port (see the Control Register description). The serial port is an asynchronous interface; the I/O_UPDATE pin allows for synchronization of the AD9957 output with external circuitry when new frequency, phase, or amplitude values are programmed into the on-chip profile registers. A rising edge initiates transfer of the

programmed data for the selected profile (see the Profile section), thus resuming the frequency synthesis process with the new values. *NOTE: The transfer of programmed data from the programming registers to the internal hardware is also accomplished by switching between profiles.*

REFCLK INPUT

The AD9957 supports a few methods for generating the internal system clock. An on-chip oscillator circuit is available for initiating a low frequency reference signal by connecting a crystal to the clock input pins. The system clock may also be generated using the internal, PLL-based reference clock multiplier, allowing the part to operate with a low frequency clock source while still providing a high update rate for the DDS and DAC. Using the clock multiplier can impact the output phase noise characteristics - for best phase noise performance, a clean, stable clock with a high slew is required. A clock of frequency higher than the maximum allowable clock rate can be used if the REFCLK input divide by 2 is enabled using the REFCLK input divider enable bit CFR3<15>.

REFCLK PLL

Enabling the PLL (via the PLL Enable Bit, CFR3<8>) allows multiplication of the reference clock frequency. The multiplication factor in the clock multiplier is set by bits CFR3 <7:1> with values ranging from 8 to 10 and 12 to 127 (decimal). Programming CFR3<7:1> for values less than 8 or 11 is not valid and will cause unpredictable device performance. The system clock rate with the clock multiplier enabled is equal to the reference clock rate times the multiplication factor. When using the clock multiplier, the correct VCO and charge pump current must be selected. The VCO range is selected by programming the VCO SEL bits, CFR3 <26:24>.. The charge pump current is programmed through the ICP bits, CFR3<21:19>. See the register map for Tables showing the available settings

Whenever the PLL clock multiplier is enabled or the multiplication value changed, the PLL must reacquire lock. Once lock is achieved, the LOCK_DETECT signal will be output on pin 19. While the PLL is out of lock, transmission in the QDUC is gated off.

REFCLK PLL WITH CRYSTAL

The on-chip oscillator for crystal operation is enabled using XTAL_SEL (pin 95). The XTAL_SEL pin is an analog input, operating on 1.8V logic. With the on-chip oscillator enabled, connecting an external crystal across the REF_CLK and REF_CLKB inputs produces a low frequency reference clock. The range of frequencies supported is listed in the specification table.

A buffer outputs a regenerated REFCLK/crystal oscillator signal on the XTAL_OUT pin (pin 94). Harmonic interference effects may be mitigated using DRV slew rate control bits CFR3<31:30>.

Table 5 summarizes the clock mode options. See the Register Table/Map section for more detail.

XTAL_SEL Pin (95)	CFR1<7:1> PLL, Bits = M	PLL Enabled (CFR3<15>	System Clock ($f_{SYS\,CLK}$)	Min/Max Freq. Range (MHz)
High = 1.8 V logic	12 ≤ M ≤ 127, or 8 ≤ M ≤ 10	Yes CFR3<15>=1	$f_{SYS\,CLK} = f_{OSC} \times M$	$500 < f_{SYSCLK} < 1000$
High = 1.8 V logic	M < 8, M=11, or M > 127	No	$f_{SYS\,CLK} = F_{OSC}$	$20 < f_{SYSCLK} < 30$
Low	12 ≤ M ≤ 127 or 8 ≤ M ≤ 10	Yes CFR3<15> = 1	$f_{SYS\,CLK} = F_{REF\,CLK} \times M$	$500 < f_{SYSCLK} < 1000$
Low	M < 8, M=11, or M > 127	No	$f_{SYS\,CLK} = F_{REF\,CLK}$	$0 < f_{SYS\,CLK} < 1000$

Table 5 Clock Mode Options

REFCLK: EXTERNAL INTERFACE

The reference clock input circuitry has two modes of operation. The first mode configures it as an input buffer. In this mode, the reference clock must be ac-coupled to the input due to internal dc biasing. This mode supports either differential or single-ended configurations. If single-ended mode is desired, CLKB (Pin 91) should be decoupled to AVDD or AGND via a 0.1 µF capacitor. The next three figures exemplify common reference clock configurations for the AD9957.

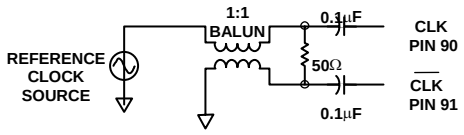


Figure 14

The reference clock inputs can also support an LVPECL or PECL driver as the reference clock source.

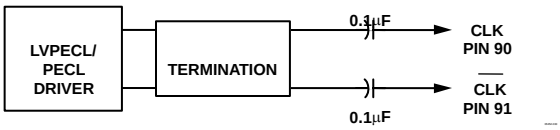


Figure 15

For external crystal operation, both clock inputs must be dc-coupled via the crystal leads and bypassed. Figure 16 shows the configuration for using a crystal.

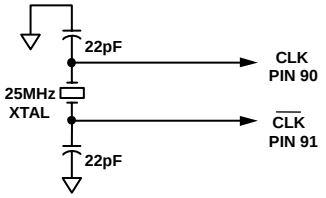


Figure 16

SERIAL PROGRAMMING

CONTROL INTERFACE—SERIAL I/O

The AD9957 serial port is a flexible, synchronous serial communications port allowing easy interface to many industry standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola 6905/11 SPI and Intel 8051 SSR protocols.

The interface allows read/write access to all registers that configure the AD9957. MSB first or LSB first transfer formats are supported. In addition, the AD9957's serial interface port can be configured as a single pin I/O (SDIO), which allows a two-wire interface or two unidirectional pins for in/out (SDIO/SDO), which enables a three wire interface. Two optional pins (IORESET and CSB) enable greater flexibility for system design-in of the AD9957.

With the AD9957, the Instruction Byte specifies read/write operation and register address. Serial operations on the AD9957 occur only at the register level, not the byte level due to the lack of byte address space in the Instruction Byte.

For the AD9957, the serial port controller recognizes the register address in the Instruction Byte and expects that all bytes of that register will be accessed, otherwise, the serial port controller will be out of sequence for the next write routine. However, one way to write less bytes than required is to use the IORESET feature. The IORESET function can be used to abort an IO operation and reset the pointer in the serial port controller. After an IORESET, the next byte will be the instruction byte. Every byte that is written prior to the IORESET is preserved. Partial bytes are not preserved.

GENERAL OPERATION OF THE SERIAL INTERFACE

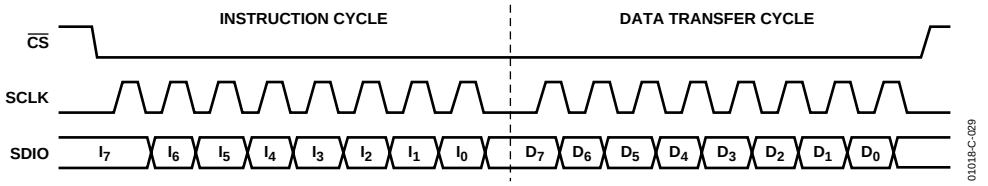
There are two phases to a communication cycle with the AD9957. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9957, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9957 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write and the serial address of the register being accessed

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9957. The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9957 and the system controller. The number of bytes transferred during Phase 2 of the communication cycle is a function of the register being accessed. For example, when accessing the Control Function Register #2, which is four bytes wide, Phase 2 requires that four bytes be transferred. If accessing the Amplitude Scale Factor Register, which is two bytes wide, Phase 2 requires that two bytes be transferred. After transferring all data bytes per the instruction, the communication cycle is completed.

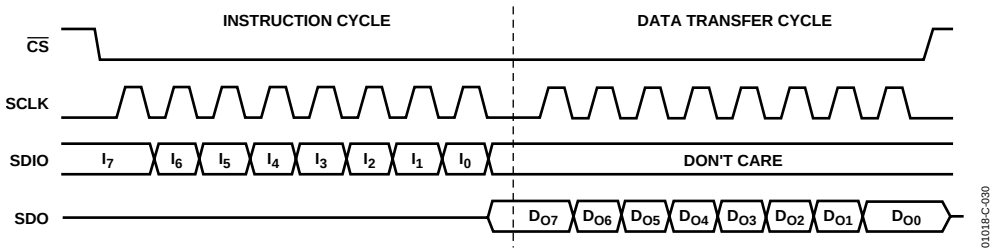
At the completion of any communication cycle, the AD9957 serial port controller expects the next 8 rising SCLK edges to be the instruction byte of the next communication cycle.

All data input to the AD9957 is registered on the rising edge of SCLK. All data is driven out of the AD9957 on the falling edge of SCLK.

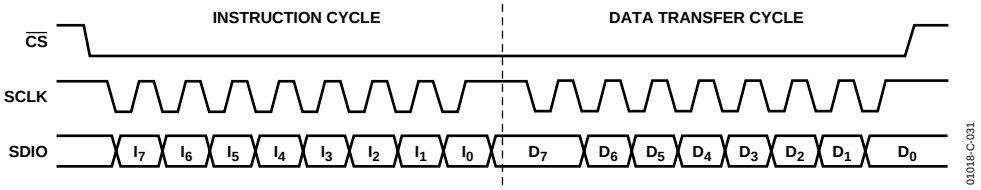
The Figures below are useful in understanding the general operation of the AD9957 Serial Port.



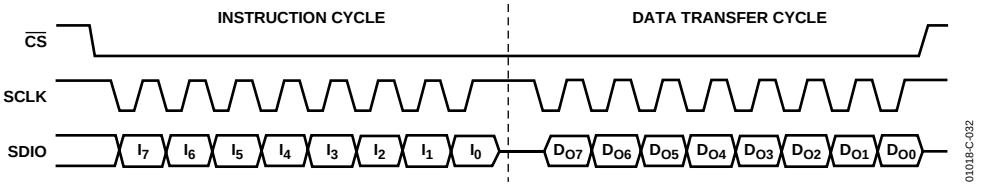
Serial Port Writing Timing—Clock Stall Low



3-Wire Serial Port Read Timing—Clock Stall Low



Serial Port Write Timing—Clock Stall High



2-Wire Serial Port Read Timing—Clock Stall High

INSTRUCTION BYTE

The instruction byte contains the following information as shown in the table below:

Instruction Byte Information

MSB	D6	D5	D4	D3	D2	D1	LSB
R/Wb	x	x	A4	A3	A2	A1	A0

R/-Wb—Bit 7 of the instruction byte determines whether a read or write data transfer will occur after the instruction byte write. Logic high indicates read operation. Logic zero indicates a write operation.

X, X—Bits 6 and 5 of the instruction byte are don't care.

A4, A3, A2, A1, A0—Bits 4, 3, 2, 1, 0 of the instruction byte determine which register is accessed during the data transfer portion of the communications cycle.

SERIAL INTERFACE PORT PIN DESCRIPTION

SCLK — Serial Clock. The serial clock pin is used to synchronize data to and from the AD9957/10 and to run the internal state machines. SCLK maximum frequency is 10 MHz.

CSB — Chip Select Bar. Active low input that allows more than one device on the same serial communications line. The SDO and SDIO pins will go to a high impedance state when this input is high. If driven high during any communications cycle, that cycle is suspended until CS is reactivated low. Chip Select can be tied low in systems that maintain control of SCLK.

SDIO — Serial Data I/O. Data is always written into the AD9957/10 on this pin. However, this pin can be used as a bi-directional data line. Bit 7 of register address 0h controls the configuration of this pin. The default is logic zero, which configures the SDIO pin as bi-directional.

SDO — Serial Data Out. Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9957/10 operates in a single bi-directional I/O mode, this pin does not output data and is set to a high impedance state.

IORESET — Synchronizes the I/O port state machines without affecting the addressable registers contents. An active high input on the IORESET pin causes the current communication cycle to abort. After IORESET returns low (Logic 0) another communication cycle may begin, starting with the instruction byte write.

MSB/LSB TRANSFERS

The AD9957/10 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by the Control Function Register #1 <0> bit. The default value of Control Function Register #1 <0> bit is low (MSB first). When Control Function Register #1 <0> bit is set high, the AD9957/10 serial port is in LSB first format. The instruction byte must be written in the format indicated by Control Function Register #1 <0> bit. That is, if the AD9957/10 is in LSB first mode, the instruction byte must be written from least significant bit to most significant bit.

For MSB first operation, the serial port controller will generate the most significant byte (of the specified register) address first followed by the next lesser significant byte addresses until the IO op-

eration is complete. All data written to (read from) the AD9957/10 must be (will be) in MSB first order. If the LSB mode is active, the serial port controller will generate the least significant byte address first followed by the next greater significant byte addresses until the IO operation is complete. All data written to (read from) the AD9957/10 must be (will be) in LSB first order.

RAM IO VIA SERIAL PORT

Accessing the RAM via the serial port is identical to any other serial IO operation except that the number of bytes transferred is determined by the address space between the beginning address and the final address as specified in the current RAM Segment Control Word (RSCW). The final address describes the most significant word address for all IO transfers and the beginning address specifies the least significant address.

RAM IO supports MSB/LSB first operation. When in MSB first mode, the first data byte will be for the most significant byte of the memory address described by the final address with the remaining three bytes making up the lesser significant bytes of that address. The remaining bytes come in most significant to least significant, destined for RAM addresses generated in descending order until the final four bytes are written into the address specified as the beginning address. When in LSB first mode, the first data byte will be for the least significant byte of the memory (specified by the beginning address) with the remaining three bytes making up the greater significant bytes of that address. The remaining bytes come in least significant to most significant, destined for RAM addresses generated in ascending order until the final four bytes are written into the memory address described by the final address. Of course, the bit order for all bytes is least significant to most significant first when in the LSB first bit is set. When the LSB first bit is cleared (default) the bit order for all bytes is most significant to least significant.

RAM CONTROL MODES

BASEBAND INPUT SCALING WITH RAM

In QDUC and DAC interpolation modes, the baseband data may be scaled via the 18x16 bit multiplier(s)(IS,QS), whose multiplicand is driven by the RAM. This function offers the customer a means of performing an arbitrary amplitude ramp up/down of the baseband data. The ramp profile is generated at the input sample rate and interpolated up to the DAC sample rate through the baseband signal chain in the same manner as the I/Q data, significantly reducing power dissipation.

In this configuration, the 32-bit RAM words are partitioned into two 16-bit words. The data being used as a scale factor for the I/Q words supplied by the user to the 18-bit parallel port. The RAM words are accessed at the IQ sample rate (output rate of the data assembler logic).

The scale factor, driven from the RAM, is an unsigned value. All zeros multiplies the baseband data by 0 (decimal) and FFFFh multiplies the baseband data by nearly 1.0 (0.FFFF equates to .99985).

Invoke the input Data Scaling Mode using the RAM enable bit and the RAM QDUC Evaluation bit, while in QDUC or interpolating DAC mode. The Input Scale Factor Control (ISFC) pin is used to start and stop the RAM controller. Two 48-bit registers are dedicated for controlling the RAM segmentation and ramp rates. See the QDUC RAM Segment #0 (QRSR0) and the QDUC RAM Segment #1 (QRSR1) registers in the register map.

I AND Q INPUT DATA FROM RAM

In the QDUC mode, the RAM can be configured to supply IQ data. The RAM is partitioned as two 16-bit words. The two words are routed to the baseband data pathway.

One word is routed to the "I" channel and the other word is routed to the "Q" channel. This will allow the user to easily generate a customized modulation waveform composed of up to 1024 I/Q samples without the need for external support circuitry to supply data to the parallel input port. This feature is an attempt to simplify the user's design/debug process when the device is incorporated into a new product design.

Synchronizing Multiple AD9957s Devices

The AD9957 product includes circuitry that enables multiple AD9957 products to be automatically synchronized to one another. Multiple devices are considered synchronized when the state of the clock generation state machines are identical for all parts. Multiple part synchronization can be achieved by a simple connection of LVDS outputs on the master device to the LVDS inputs of the slave device(s). Devices are configured as master and slaves through programming bits, accessible via the serial port.

Pipeline Matching of the FTW, Phase Offset, and Output Scaling

The AD9957 offers a feature that enables the simultaneous application of changes in frequency, phase and amplitude to be applied in a manner that allows these parameters to be synchronized to the specific pipe delays of the preceding logic blocks. This feature is controllable via the serial port and is activated by writing the Match Pipe Delays Active bit to a logic one.

Output Shaped On-Off Keying modes

Auto and Manual shaped On-Off keying modes are supported. AUTO mode generates a linear scale factor at a rate determined by the Amplitude Ramp Rate Register (ARR), controlled by an external pin (OSK). MANUAL mode allows the user to directly control the output amplitude by writing the scale factor value into the Amplitude Scale Factor Register (ASFR).

REGISTER MAP AND DESCRIPTIONS

REGISTER MAP

Register Name (Serial Address)	Bit Range	Bit 7 (MSB)	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value OR Profile
Control Function Register 1 **CFR1** (00h)	<31:24>	RAM Enable	OPEN		RAM QDUC Evaluation	OPEN		QDUC Operating Mode		00h
	<23:16>	Manual OSK External Control	Inverse Sinc Filter Enable	Clear CCI	Internal Profile Control				Enable Sine Output	00h
	<15:8>	OPEN		Auto-Clear Phase Accum	OPEN	Clear Phase Accum	Load ARR @ I/O update	Output Shaped Keying Enable	Auto Output Shaped Keying	00h
	<7:0>	Digital Power Down	DAC Power Down	Clock Input Power Down	Aux DAC Power Down	External Power Down Mode	Auto Power Down Enable	SDIO Input Only	LSB First	00h
Control Function Register 2 (CFR2) (01h)	<31:24>	BlackFin Interface Mode Active	BlackFin Bit Order	Black Fin Early Frame Sync Enable			OPEN			00h
	<23:16>	Internal IO Update Active	Enable IO Update Clock			OPEN			Read Effective FTW	40h
	<15:8>	IO Update Rate Control		PDCLK Rate Control	Data Format	Enable PDCLK	PDCLK Clock Invert	TxEnable Invert	Q First Data Pairing	08h
	<7:0>	Matched Latency Enable	Data Assembler Hold Last Value	Sync Sample Error Mask	OPEN		FM Gain			20h
Control Function Register 3 (CFR3) (02h)	<31:24>	DRV0<1:0>			OPEN			VCO SEL <2:0>		1Fh
	<23:16>	OPEN			ICP<2:0>			OPEN		3Fh
	<15:8>	REFCLK Input Divider Disable			OPEN				PLL Enable	40h
	<7:0>				N:<6:0>				OPEN	00h
Auxilliary DAC Control Register (03h)	<31:24>	OPEN								00h
	<23:16>	OPEN								00h
	<15:8>	OPEN								00h
	<7:0>	FSC<7:0>								FFh

Register Name (Serial Address)	Bit Range (Internal Address)	Bit 7 (MSB)	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value OR Profile
IO Update Rate Register (04h)	<31:24>	IO Update Rate <31:24>								FFh
	<23:16>	IO Update Rate <23:16>								FFh
	<15:8>	IO Update Rate <15:8>								FFh
	<7:0>	IO Update Rate <7:0>								FFh
QDUC RAM Segment Register #0 (05h)	<47:40>	RAM Segment 0 Address Ramp Rate <15:8>								ISFC0
	<39:32>	RAM Segment 0 Address Ramp Rate <7:0>								ISFC0
	<31:24>	RAM Segment 0 Final Address <9:2>								ISFC0
	<23:16>	RAM Segment 0 Final Address <1:0>			OPEN					ISFC0
	<15:8>	RAM Segment 0 Beginning Address <9:2>								ISFC0
	<7:0>	RAM Segment 0 Beginning Address <1:0>			OPEN		RAM Segment 0 Mode Control <2:0>			ISFC0
QDUC RAM Segment Register #1 (06h)	<47:40>	RAM Segment 1 Address Ramp Rate <15:8>								ISFC1
	<39:32>	RAM Segment 1 Address Ramp Rate <7:0>								ISFC1
	<31:24>	RAM Segment 1 Final Address <9:2>								ISFC1
	<23:16>	RAM Segment 1 Final Address <1:0>			OPEN					ISFC1
	<15:8>	RAM Segment 1 Beginning Address <9:2>								ISFC1
	<7:0>	RAM Segment 1 Beginning Address <1:0>			OPEN		RAM Segment 1 Mode Control <2:0>			ISFC1
FTW Register (07h)	<31:24>	Frequency Tuning Word <31:24>								00h
	<23:16>	Frequency Tuning Word <23:16>								00h
	<15:8>	Frequency Tuning Word <15:8>								00h
	<7:0>	Frequency Tuning Word <7:0>								00h
POW Register (08h)	<15:8>	Phase Offset Word <15:8>								00h
	<7:0>	Phase Offset Word <7:0>								00h
ASF Register (09h)	<31:24>	Amplitude Ramp Rate <15:8>								00h
	<23:16>	Amplitude Ramp Rate <7:0>								00h
	<15:8>	Amplitude Scale Factor <13:6>								00h
	<7:0>	Amplitude Scale Factor <5:0>						Amplitude Ramp Rate Speed Control <1:0>		00h

Register Name (Serial Address)	Bit Range (Internal Address)	Bit 7 (MSB)	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
Multi-Chip Sync Register (0Ah)	<31:24>	Sync Window Delay <3:0>				Sync Enable	Sync Driver Enable	Sync Polarity	Internal Sync Loop Enable	00h
	<23:16>	System Clock Offset<5:0>						OPEN		00h
	<15:8>	Output Sync Pulse Delay <4:0>						OPEN		00h
	<7:0>	Input Sync Pulse Delay <4:0>						OPEN		00h
	<23:16>	Falling Sweep Ramp Rate Word <7:0>								00h
	<15:8>	Rising Sweep Ramp Rate Word <15:8>								00h
	<7:0>	Rising Sweep Ramp Rate Word <7:0>								00h
QDUC Profile 0 Register (0Eh)	<63:56>	CCI Interpolation Rate						Spectral Invert	Inverse CCI Bypass	000
	<55:48>	Output Scale Factor #0								000
	<47:40>	Phase Offset Word #0 <15:8>								000
	<39:32>	Phase Offset Word #0 <7:0>								000
	<31:24>	Frequency Tuning Word #0 <31:24>								000
	<23:16>	Frequency Tuning Word #0 <23:16>								000
	<15:8>	Frequency Tuning Word #0 <15:8>								000
	<7:0>	Frequency Tuning Word #0 <7:0>								000
QDUC Profile 1 Register (0Fh)	<63:56>	CCI Interpolation Rate						Spectral Invert	Inverse CCI Bypass	001
	<55:48>	Output Scale Factor #1								001
	<47:40>	Phase Offset Word # 1 <15:8>								001
	<39:32>	Phase Offset Word #1 <7:0>								001
	<31:24>	Frequency Tuning Word #1 <31:24>								001
	<23:16>	Frequency Tuning Word #1 <23:16>								001
	<15:8>	Frequency Tuning Word #1 <15:8>								001
	<7:0>	Frequency Tuning Word #1 <7:0>								001

Register Name (Serial Address)	Bit Range (Internal Address)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Profile Pins (PS2 ->PS0)
QDUC Profile 2 Register (10h)	<63:56>	CCI Interpolation Rate						Spectral Invert	Inverse CCI Bypass	010
	<55:48>	Output Scale Factor #2								010
	<47:40>	Phase Offset Word #2 <15:8>								010
	<39:32>	Phase Offset Word #2 <7:0>								010
	<31:24>	Frequency Tuning Word #2 <31:24>								010
	<23:16>	Frequency Tuning Word #2 <23:16>								010
	<15:8>	Frequency Tuning Word #2 <15:8>								010
	<7:0>	Frequency Tuning Word #2 <7:0>								010
QDUC Profile 3 Register (11h)	<63:56>	CCI Interpolation Rate						Spectral Invert	Inverse CCI Bypass	011
	<55:48>	Output Scale Factor #3								011
	<47:40>	Phase Offset Word # 3 <15:8>								011
	<39:32>	Phase Offset Word #3 <7:0>								011
	<31:24>	Frequency Tuning Word #3 <31:24>								011
	<23:16>	Frequency Tuning Word #3 <23:16>								011
	<15:8>	Frequency Tuning Word #3 <15:8>								011
	<7:0>	Frequency Tuning Word #3 <7:0>								011
QDUC Profile 4 Register (12h)	<63:56>	CCI Interpolation Rate						Spectral Invert	Inverse CCI Bypass	100
	<55:48>	Output Scale Factor #4								100
	<47:40>	Phase Offset Word #4 <15:8>								100
	<39:32>	Phase Offset Word #4 <7:0>								100
	<31:24>	Frequency Tuning Word #4 <31:24>								100
	<23:16>	Frequency Tuning Word #4 <23:16>								100
	<15:8>	Frequency Tuning Word #4 <15:8>								100
	<7:0>	Frequency Tuning Word #4 <7:0>								100

Register Name (Serial Address)	Bit Range (Internal Address)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Profile Pins (PS2 ->PS0)
QDUC Profile 5 Register (13h)	<63:56>	CCI Interpolation Rate						Spectral Invert	Inverse CCI Bypass	101
	<55:48>	Output Scale Factor #5								101
	<47:40>	Phase Offset Word # 5 <15:8>								101
	<39:32>	Phase Offset Word #5 <7:0>								101
	<31:24>	Frequency Tuning Word #5 <31:24>								101
	<23:16>	Frequency Tuning Word #5 <23:16>								101
	<15:8>	Frequency Tuning Word #5 <15:8>								101
	<7:0>	Frequency Tuning Word #5 <7:0>								101
QDUC Profile 6 Register (14h)	<63:56>	CCI Interpolation Rate						Spectral Invert	Inverse CCI Bypass	110
	<55:48>	Output Scale Factor #6								110
	<47:40>	Phase Offset Word #6 <15:8>								110
	<39:32>	Phase Offset Word #6 <7:0>								110
	<31:24>	Frequency Tuning Word #6 <31:24>								110
	<23:16>	Frequency Tuning Word #6 <23:16>								110
	<15:8>	Frequency Tuning Word #6 <15:8>								110
	<7:0>	Frequency Tuning Word #6 <7:0>								110
QDUC Profile 7 Register (15h)	<63:56>	CCI Interpolation Rate						Spectral Invert	Inverse CCI Bypass	111
	<55:48>	Output Scale Factor #7								111
	<47:40>	Phase Offset Word # 7 <15:8>								111
	<39:32>	Phase Offset Word #7 <7:0>								111
	<31:24>	Frequency Tuning Word #7 <31:24>								111
	<23:16>	Frequency Tuning Word #7 <23:16>								111
	<15:8>	Frequency Tuning Word #7 <15:8>								111
	<7:0>	Frequency Tuning Word #7 <7:0>								111

Register Name (Serial Address)	Bit Range (Internal Address)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Profile Pins (PS2 ->PS0)
RAM (16h)	<31:0>	RAM [1023:0] <31:0>								***
QDUC Single Tone Profile 0 Register (0Eh)	<63:56>	OPEN			Amplitude Scale Factor #0 <13:8>					000
	<55:48>	Amplitude Scale Factor #0 <7:0>								000
	<47:40>	Phase Offset Word #0 <15:8>								000
	<39:32>	Phase Offset Word #0 <7:0>								000
	<31:24>	Frequency Tuning Word #0 <31:24>								000
	<23:16>	Frequency Tuning Word #0 <23:16>								000
	<15:8>	Frequency Tuning Word #0 <15:8>								000
	<7:0>	Frequency Tuning Word #0 <7:0>								000
QDUC Single Tone Profile 1 Register (0Fh)	<63:56>	OPEN			Amplitude Scale Factor #1 <13:8>					001
	<55:48>	Amplitude Scale Factor #1 <7:0>								001
	<47:40>	Phase Offset Word #1 <15:8>								001
	<39:32>	Phase Offset Word #1 <7:0>								001
	<31:24>	Frequency Tuning Word #1 <31:24>								001
	<23:16>	Frequency Tuning Word #1 <23:16>								001
	<15:8>	Frequency Tuning Word #1 <15:8>								001
	<7:0>	Frequency Tuning Word #1 <7:0>								001
QDUC Single Tone Profile 2 Register (10h)	<63:56>	OPEN			Amplitude Scale Factor #2 <13:8>					010
	<55:48>	Amplitude Scale Factor #2 <7:0>								010
	<47:40>	Phase Offset Word #2 <15:8>								010
	<39:32>	Phase Offset Word #2 <7:0>								010
	<31:24>	Frequency Tuning Word #2 <31:24>								010
	<23:16>	Frequency Tuning Word #2 <23:16>								010
	<15:8>	Frequency Tuning Word #2 <15:8>								010
	<7:0>	Frequency Tuning Word #2 <7:0>								010

Register Name (Serial Address)	Bit Range (Internal Address)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Profile Pins (PS2 ->PS0)
QDUC Single Tone Profile 3 Register (11h)	<63:56>	OPEN			Amplitude Scale Factor #3 <13:8>					011
	<55:48>	Amplitude Scale Factor #3 <7:0>								011
	<47:40>	Phase Offset Word #3 <15:8>								011
	<39:32>	Phase Offset Word #3 <7:0>								011
	<31:24>	Frequency Tuning Word #3 <31:24>								011
	<23:16>	Frequency Tuning Word #3 <23:16>								011
	<15:8>	Frequency Tuning Word #3 <15:8>								011
	<7:0>	Frequency Tuning Word #3 <7:0>								011
QDUC Single Tone Profile 4 Register (12h)	<63:56>	OPEN			Amplitude Scale Factor #4 <13:8>					100
	<55:48>	Amplitude Scale Factor #4 <7:0>								100
	<47:40>	Phase Offset Word #4 <15:8>								100
	<39:32>	Phase Offset Word #4 <7:0>								100
	<31:24>	Frequency Tuning Word #4 <31:24>								100
	<23:16>	Frequency Tuning Word #4 <23:16>								100
	<15:8>	Frequency Tuning Word #4 <15:8>								100
	<7:0>	Frequency Tuning Word #4 <7:0>								100
QDUC Single Tone Profile 5 Register (13h)	<63:56>	OPEN			Amplitude Scale Factor #5 <13:8>					101
	<55:48>	Amplitude Scale Factor #5 <7:0>								101
	<47:40>	Phase Offset Word #5 <15:8>								101
	<39:32>	Phase Offset Word #5 <7:0>								101
	<31:24>	Frequency Tuning Word #5 <31:24>								101
	<23:16>	Frequency Tuning Word #5 <23:16>								101
	<15:8>	Frequency Tuning Word #5 <15:8>								101
	<7:0>	Frequency Tuning Word #5 <7:0>								101

Register Name (Serial Address)	Bit Range (Internal Address)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Profile Pins (PS2 ->PS0)
QDUC Single Tone Profile 6 Register (14h)	<63:56>	OPEN			Amplitude Scale Factor #6 <13:8>					110
	<55:48>	Amplitude Scale Factor #6 <7:0>								110
	<47:40>	Phase Offset Word #6 <15:8>								110
	<39:32>	Phase Offset Word #6 <7:0>								110
	<31:24>	Frequency Tuning Word #6 <31:24>								110
	<23:16>	Frequency Tuning Word #6 <23:16>								110
	<15:8>	Frequency Tuning Word #6 <15:8>								110
	<7:0>	Frequency Tuning Word #6 <7:0>								110
QDUC Single Tone Profile 7 Register (15h)	<63:56>	OPEN			Amplitude Scale Factor #7 <13:8>					111
	<55:48>	Amplitude Scale Factor #7 <7:0>								111
	<47:40>	Phase Offset Word #7 <15:8>								111
	<39:32>	Phase Offset Word #7 <7:0>								111
	<31:24>	Frequency Tuning Word #7 <31:24>								111
	<23:16>	Frequency Tuning Word #7 <23:16>								111
	<15:8>	Frequency Tuning Word #7 <15:8>								111
	<7:0>	Frequency Tuning Word #7 <7:0>								111

REGISTER DESCRIPTIONS

Control Function Register #1 (CFR1)

The CFR1 is comprised of four bytes located in address 00h.

CFR1<31>: **RAM Enable bit**.

When **CFR1<31>**= 0 *(default),* disables the RAM putting it in the lowest power state (unless being written to via the serial port).

When **CFR1<31>** = 1, enables the RAM.

CFR1<30:29>: **OPEN**. Always leave these bits clear.

CFR1<28>: **RAM QDUC Evaluation Enable bi**t.

When **CFR1<28>** = 0 *(default)*, The RAM QDUC evaluation mode of the device is inactive.

When **CFR1<28>** = 1, The RAM QDUC evaluation mode is activated, if the RAM Enable bit is set. When in the RAM QDUC Evaluation mode the input data port is disengaged form the signal processing path and the RAM drives the I and Q data at the IQ sample rate.

CFR1<27:26>: **OPEN**. Always leave these bits clear.

CFR1<25:24>: **QDUC Operating Mode bits**.

The CFR1<25:24> bits set the mode of operation:

CFR1<25:24>	Mode of Operation
00 (*default*)	Quadrature Modulation
01	Single Tone
1x	Interpolating DAC

CFR1<23>: **Manual OSK External Control**.

Note, this bit is ignored unless manual OSK mode is selected using CFR1<9:8>.

When **CFR1<23>** = 0 *(default)*, the manual OSK mode does not require the use of the OSK input pin to operate.

When **CFR1<23>** = 1, the manual OSK mode uses the OSK input pin. See pin description.

CFR1<22>: **Inverse Sinc Enable bit**.

When **CFR1<22>** = 0 *(default)*, the inverse sinc filter is inactive - the local clock is stopped to save power. The input data is passed directly to the output of the filter.

When **CFR1<22>** = 1, the inverse sinc filter is enabled and operational.

CFR1<21>: **Clear CCI bit**.

When **CFR1<21>** = 0 *(default)*, the CCI filter operates normally.

When **CFR1<21>** = 1, The CCI filter is asynchronously cleared.

CFR1<20:17>: **Internal Profile Control bits**.

These bits cause the Profile Bits to be ignored and put the device into an automatic "profile loop sequence" that allows the user to implement a frequency/phase composite sweep that runs without external inputs.

CFR1<16>: **Sine Enable bit**.

When CFR1<16> = 0 *(default)*, the angle-to-amplitude conversion logic outputs a COSINE function.

When CFR1<16> = 1, the angle-to-amplitude conversion logic outputs a SINE function.

CFR1<15:14>: **OPEN**. Always leave these bits clear.

CFR1<13>: Auto Clear Phase Accumulator

When CFR1<13> = 0 *(default)*, *)*, the accumulation function is not interrupted.

When CFR1<13> = 1, this bit automatically and synchronously clears (loads zeros into) the phase accumulator for one cycle upon receipt of the I/O UPDATE sequence indicator.

CFR1<12>: OPEN. Always leave this bit clear.

CFR1<11>: Clear Phase Accumulator

When CFR1<11> = 0 *(default)*, the phase accumulator functions as normal.

When CFR1<11> = 1, the phase accumulator memory element is asynchronously cleared.

CFR1<10>: **Load Amplitude Rate Register @ IOUpdate**

When CFR1<10> = 0 *(default)*, the amplitude ramp rate timer is loaded only upon timeout (timer ==1); it is not loaded due to an I/O UPDATE input signal (or change in profile).

When CFR1<10> = 1, the amplitude ramp rate timer is loaded upon timeout (timer ==1) or at the time of an I/O UPDATE input signal (or change in profile).

CFR1<9>: **Output Shaped Keying Enable**

CFR1<9> = 0 (*default*), disables Shaped On-Off Keying. The clocks to this function are stopped for power savings.

CFR1<9> = 1, enables Shaped On-Off Keying. CFR1<8> sets the mode of operation.

CFR1<8>: Automatic Output Shaped Keying Enable

If CFR1<9> is clear, this bit is ignored.

CFR1<8> = 0 enables MANUAL Shaped On-Off Keying.

CFR1<8> = 1 enables AUTO Shaped On-Off Keying.

CFR1<7>: Digital Power Down

CFR1<7> = 0 (*default*), enables the digital circuitry.

CFR1<7> = 1, disables the digital circuitry, putting it in its' lowest power dissipation state.

CFR1<6>: DAC Power Down

CFR1<6> = 0 (*default*), enables the DAC Circuitry.

CFR1<6> = 1, disables the DAC Circuitry, putting it in a low power dissipation state.

CFR1<5>: Clock Input Power Down

CFR1<5> = 0 (*default*), enables the Clock Input Circuitry.

CFR1<5> = 1, disables the Clock Input Circuitry putting it in a low power dissipation state.

CFR1<4>: Open

CFR1<3>: External Power Down Mode

When CFR1<3> = 0 *(default)* the external power down mode selected is "fast recovery power down". In this mode, when the EXTPWRDWN input pin is high, the digital logic and the DAC digital logic are powered down. The DAC bias circuitry, comparator, PLL, oscillator, and clock input circuitry is NOT powered down.

When CFR1<3> = 1, the external power down mode selected is "full power down". In this mode, when the EXTPWRDWN input pin is high, all functions are powered down including the DAC and PLL, which take a significant amount of time to power up.

CFR1<2>: Automatic Power Down

CFR1<2> = 0 (*default*), disables automatic power down.

When CFR1<2> = 1 when TX ENABLE is de-asserted for a sufficiently long period of time the device automatically switches into its low power mode.

CFR1<1>: SDIO Input Only

CFR1<1> = 0 (*default*), configures the SDIO pin for bi-directional operation (2-wire serial programming mode).

CFR1<1> = 1, configures the serial data I/O pin (SDIO) as an input only pin (3-wire serial programming mode).

CFR1<0>: LSB First

CFR1<0> = 0 (*default*), sets MSB first format.

CFR1<0> = 1, sets LSB first format.

Control Function Register #2 (CFR2)

CFR2<31>: BlackFin Interface Mode Active bit.

When **CFR2<31>**= 0 *(default),* the parallel input data port operates as described in the data assembler section of this document.

When **CFR2<31>** = 1, the AD9957 data port is configured for direct connection to the BlackFin SPORT interface. See the **BlackFin Interface** section of this document for details.

CFR2<30>: BlackFin Bit Order bit.

This bit is ignored if the AD9957 is not operating in the BlackFin Interface Mode (see CFR2<31>).

CFR2<30>= 0 *(default)* sets MSB first format.

CFR2<30> = 1 sets LSB first format.

CFR2<29>: BlackFin Early Frame Sync Enable bit.

This bit is ignored if the AD9957 is not operating in the BlackFin Interface Mode (see CFR2<31>).

When **CFR2<29>**= 0 *(default)*, the frame sync signal is expected by the AD9957 to be co-incident with the first data bit transmitted. ('Late frame sync operation' in the Blackfin documentation).

When **CFR2<29>** = 1, the frame sync signal is expected by the AD9957 to be one cycle preceding the first data bit transmitted. ('Early frame sync operation' in the Blackfin documentation). Also, for continuous data transmission, the early frame sync bit will be co-incident with the last bit of the previous word transmitted.

CFR2<28:25>: Open. Leave these bits clear

CFR2<24>: Single Tone Profile Enable bit.

When **CFR2<24>**= 0 *(default)*, direct modulation of

amplitude via the profile registers is not possible.

When **CFR2<24>** = 1, direct modulation of amplitude via the profile registers is possible, depending upon other chip configurations.

CFR2<23>: **Internal IO Update Active bit**.

When **CFR2<23>**= 0 *(default)*, the IO Update feature is controlled externally through the I/O_UPDATE pin, which is configured as an input..

When **CFR2<23>** = 1, the IO Update feature is controlled internally via a down counter. The I/O_UPDATE pin, is configured as an output to signal the user to when IO updates have occurred.

CFR2<22>: **Enable IO SYNC CLK bit**.

CFR2<22>= 1 *(default)*, activates the IOSYNCCLK pin.

When **CFR2<22>** = 0, the IOSYNCCLK pin is pulled low.

CFR2<21:17>: **OPEN**. Always leave these bits clear.

CFR2<16>: **Read Effective FTW bit**

When **CFR2<16>**= 0 *(default,* a serial IO read instruction reads hex address 07h (FTW register), the serial port reads back the register at hex address 07h.

When **CFR2<16>** = 1, a serial IO read instruction reads hex address 07h (FTW register), the serial port reads back the active FTW.

CFR2<15:14>: **IO Update Rate Control bits**.

These bits are ignored if Internal IO Update is not activated using bit CFR2<23>

The CFR2<15:14> bits set the clock rate for the IO Update down counter. The table below indicates the clock rate divisor

CFR2<15:14>	IO SYNC CLK Divisor
00	1
01	2
10	4
11	8

CFR2<13>: **PDCLK Rate Control bit**.

When **CFR2<13>**= 0 *(default),* the rate out of the PDCLK pin is equal to the input data rate.

When **CFR2<13>** = 1, the rate out of the PDCLK pin is equal to one half the input data rate. This provides insight into the phase of the signal processing clock, relative to the input data rate. See the **Data Assembler** section of the functional description for details.

CFR2<12>: **Data Format bit**.

When **CFR2<12>**= 0 *(default)*, data received is treated as 'twos complement'.

When **CFR2<12>** = 1, data received is treated as 'offset binary'. The MSB of the data word is inverted before being sent to the signal processing logic.

CFR2<11>: **Enable PDCLK bit**

CFR2<11> = 0 pulls the PDCLK pin low.

CFR2<11>= 1 *(default)* activates PDCLK pin.

CFR2<10>: **PDCLK Invert bit**

When **CFR2<10>**= 0 *(default)*, the PDCLK pin is in phase with the clock that samples the data into the part.

When **CFR2<10>** = 1, the PDCLK pin is in inverted from the clock that samples the data into the part.

CFR2<9>: **TxEnable Invert bit**

When **CFR2<9>**= 0 *(default)*, a logic 1 on the TxEnable pin indicates I data and a logic 0 on the TxEnable pin indicates Q data, if the user is employing a continuous timing style on the TxEnable pin. For burst timing style, if the TxEnable Invert bit is cleared, a logic 1 on the TxEnable pin enables the AD9957 to transmit data and a logic zero indicates no further data is to be transmitted.

When **CFR2<9>** = 1, a logic 1 on the TxEnable pin indicates Q data and a logic 0 on the TxEnable pin indicates I data, if the user is employing a continuous timing style on the TxEnable pin. For burst timing style, if the TxEnable Invert bit is set, a logic 0 on the TxEnable pin enables the AD9957 to transmit data and a logic one indicates no further data is to be transmitted.

CFR2<8>: **Q First Data Pairing bit**

When **CFR2<8>**= 0 *(default)*, I data precedes Q data in the assembly of the I/Q data pair that is processing in the QDUC signal chain.

When **CFR2<8>** = 1, Q data precedes I data in the assembly of the I/Q data pair that is processing in the QDUC signal chain.

CFR2<7>: **Matched Latency bit**.

When **CFR2<7>**= 0 *(default)*, the Frequency Tuning Word, Phase Offset and Amplitude Scalar pipe delays are minimized. The output will reflect amplitude changes before it reflects phase changes, and phase changes before it reflects frequency changes.

When **CFR2<7>** = 1, the Frequency Tuning Word, Phase Offset and Amplitude Scalar pipe delays are implemented such that the simultaneous application of changes in frequency, phase and amplitude are reflected on the output simultaneously too.

CFR2<6>: **Data Assembler Holds Last Value bit**

When **CFR2<6>**= 0 *(default)*, the data port drives logic zeros onto the signal processing data path when transmission is disabled.

When **CFR2<6>** = 1, the data port holds the last data word registered when transmission is disabled.

CFR2<5>: **Sync Sample Error Mask bit**

CFR2<5>= 0 disables the SYNC_SMP_ERR pin.

CFR2<5> = 1 *(default)* enables the SYNC_SMP_ERR pin.

CFR2<3:0>: **FM Gain bits**.

When operating the device in single tone mode and FM modulation is selected via the Data Port Destination bits, if the Single Tone Data Port Enable bit is set, these bits are used to select one of 16 possible 16-bit ranges relative to the 32-bit DDS tuning word.

Control Function Register #3 (CFR3)

CFR3<31:30>: DRV0 (XTAL_OUT) control bits.

These bits set the drive strength of the buffered reference clock output on pin 93.

00 = OFF *(default)*
01 = Low drive strength
10 = Mid drive strength
11 = High drive strength

CFR3<29:27>: **Open**. Leave these bits clear.

CFR3<26:24>: **VCO Selection Bits.**

As per the table below, these bits set the VCO for the appropriate range.

Bits	Min	Max
000	420MHz	485MHz
001	485MHz	560MHz
010	560MHz	655MHz
011	655MHz	830MHz
100	830MHz	920MHz
101	920MHz	1000MHz
11x	PLL WILL NOT FUNCTION	

CFR3<21:19>: Charge Pump Current Bits

As per the table below, these bits set the charge pump output current.

CFR3<21:19>	Charge Pump Current (µA)
000	200
001	225
010	250
011	275
100	300
101	325
110	350
111	375

Table 6 Charge Pump Output Current Settings

CFR3<18:16>: **OPEN**. Leave these bits clear

CFR3<15>: REFCLK Input Divider Disable bit.

When **CFR3<15>** = 0 The AD9957 REFCLK input divider is bypassed. The internal sysclk fed to the device (or the clock multiplier) equals the REFCLK rate

When **CFR3<15>** = 1 (default) The AD9957 REFCLK input divider is enabled (to ÷2). The internal sysclk fed to the device (or the clock multiplier) is equal to ½ the REFCLK rate.

CFR3<14>: **OPEN**

This bit is used strictly for testing, leave SET.

CFR3<13:9>: **OPEN**

These bits are used for testing; leave CLEAR.

CFR3<8>: **PLL Enable bit.**

When **CFR3<8>**= 0 *(default)*. The AD9957 reference clock rate equals the DAC clock sampling rate. The PLL is bypassed and the clock multiplier is powered down.

When **CFR3<8>** = 1, The AD9957 reference clock rate times the PLL Multiplier bit (integer equivalent) equals the DAC clock sampling rate.

CFR3<7:1>: **REFCLK Multiplier bits.**

These bits make up the 8-bit word that is the multiplication factor used by the PLL Clock Multiplier circuitry. The decimal equivalent of the binary value of these bits is the multiplication factor. Only certain values are valid (See Ta-

ble 4). If the PLL is enabled (CFR3<8>), a valid value must be programmed here for proper PLL operation. If the PLL is disabled, these bits are ignored.

CFR3<0>: REFCLK input doubler active bit

When **CFR3<0>**= 0 *(default)* the reference clock is fed directly to the PFD.

When **CFR3<0>** = 1, the reference clock is doubled in frequency prior to being fed to the PFD.

Auxilliary DAC Control Register

These 8 bits control the auxiliary DAC that modulates the full scale current of the Tx DAC. For a default DAC_Rset value of 10K, these bits modulate the DAC output full scale current between 8.66mA and 31.66mA, with each LSB representing approximately 90µA of resolution.

IO Update Rate Register

This register sets the interval for the down counter which divides the system clock down to an internal I/O update interval period. When the internal I/O Update mode is disabled, this register is ignored. Each LSB represents one SYNC_CLK cycle, so the interval for an internal I/O update rate varies between 1 and 2^32(4,294,967,296) sync_clock cycles, where a sync_clock cycle is ¼ of a system clock cycle.

QDUC RAM Segment Registers (QRSR0, QRSR1)

These registers program the behavior of the internal RAM controller for when the RAM is configured to drive QDUC data or drive the input scalars. QRSR0 feeds data to the I-channel and QRSR1 feeds data to the Q-channel. These registers serve no function when the AD9957 is programmed to be in single-tone mode.

QRSRX<47:32> RAM Segment Address Ramp Rate

This 16 bit word controls the period between QDUC RAM segment steps. Each LSB in this word weights the delay by 1 SYNC_CLK cycle (which is ¼ the system clock rate).

QRSRX<31:22> RAM Segment Final Address

This 10 bit word specifies the final address location in the RAM where the data profile is stored.

QRSRX<21:16> OPEN

QRSRX<15:6> RAM Segment Beginning Address

This 10 bit word specifies the beginning address location in the RAM where the data profile is stored.

QRSRX<5:3> OPEN

QSRX<2:0> RAM Segment Mode Control

This 3 bit word specifies the behavior the RAM controller follows when stepping through the Segment according to the following table. Note, the behavior indicated refers to the RAM address itself, not necessarily the data stored and sent to the QDUC.

QSRX<2:0>	RAM Mode
000	Direct Switch (Beginning Address only)
001	Ramp Up
010	Bidirectional Ramp (ramp up, ramp down)
011	Continuous Bidirectional (ramp up, ramp down, ramp up, etc)
100	Continous recirculate (Ramp up from beginning to final address, then immediately return to beginning address and repeat).
101, 110, 111	Not Used

Frequency Tuning Word Register (FTW)

This register sets the frequency tuning word of the DDS core, which is either the output frequency (single tone mode) or the carrier frequency (modulator mode). When the Phase/Frequency/Amplitude Profiles are enabled, this register serves no function.

Phase Offset Word Register (POW)

This register controls the phase offset of the DDS core in either the output frequency (single tone mode) or the carrier frequency (modulator mode). When the Phase/Frequency/Amplitude Profiles are enabled, this register serves no function.

Amplitude Scale Factor (ASF)

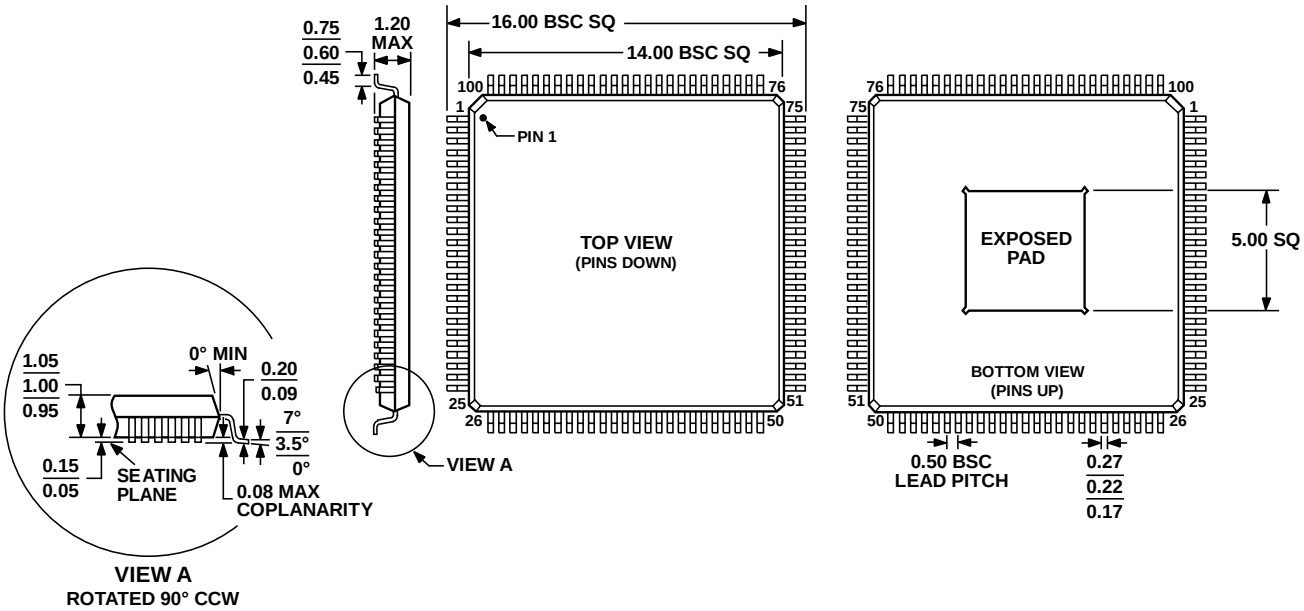
This register controls the digital multiplier (amplitude scale factor) inside the DDS core itself. It does not affect the digital multiplier immediately prior to the DAC . In automatic OSK mode, this controls the ramp rate and final value of the amplitude ramping function. In manual OSK mode, only the Amplitude Scale Factor is used, the Amplitude Ramp Rate is 'don't care'. When the Phase /Frequency /Amplitude Profiles are enabled, this register serves no function.

QDUC Profile X Register (QDUC-PXR)/ Single Tone Profile X Register (ST-PXR)

There are 8 special purpose registers which reside at addresses h'0E to h'15. These registers can take on one of three roles: they can either be QDUC Profile Registers, RAM Profile Registers or Single Tone Profile Registers.

First and foremost, the part will use these registers as QDUC Profile registers if the part is in quadrature modulator mode CFR1<25:24> = 00.

OUTLINE DIMENSIONS



PR06384-0-9/06(PrF)

COMPLIANT TO JEDEC STANDARDS MS-026-AED-HD

NOTES
1. CENTER FIGURES ARE TYPICAL UNLESS OTHERWISE NOTED.
2. THE AD9957 HAS A CONDUCTIVE HEAT SLUG TO HELP DISSIPATE HEAT AND ENSURE RELIABLE OPERATION OF THE DEVICE OVER THE FULL INDUSTRIAL TEMPERATURE RANGE. THE SLUG IS EXPOSED ON THE BOTTOM OF THE PACKAGE AND ELECTRICALLY CONNECTED TO V_{EE}. IT IS RECOMMENDED THAT NO PCB SIGNAL TRACES OR VIAS BE LOCATED UNDER THE PACKAGE THAT COULD COME IN CONTACT WITH THE CONDUCTIVE SLUG. ATTACHING THE SLUG TO A V_{EE} PLANE WILL REDUCE THE JUNCTION TEMPERATURE OF THE DEVICE WHICH MAY BE BENEFICIAL IN HIGH TEMPERATURE ENVIRONMENTS.

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ORDERING GUIDE

Model	Temperature Range	Package Description	Package Outline
AD9957BSVZ	–40°C to +105°C	48-Lead Thin Plastic Quad Flat Package, Exposed Pad (TQFP_EP)	
AD9957BSVZ-REEL13	–40°C to +105°C	48-Lead Thin Plastic Quad Flat Package, Exposed Pad (TQFP_EP), 1000 Device, 13-Inch Reel	
AD9957/PCBZ		Evaluation Board	