

### FEATURES

#### Analog Interface

- 140 MSPS Maximum Conversion Rate
- Programmable Analog Bandwidth
- 0.5 V to 1.0 V Analog Input Range
- 500 ps p-p PLL Clock Jitter at 140 MSPS
- 3.3 V Power Supply
- Full Sync Processing
- Midscale Clamping
- 4:2:2 Output Format Mode

#### Digital Interface

- DVI 1.0 Compatible Interface
- 112 MHz Operation
- High Skew Tolerance of 1 Full Input Clock
- Sync Detect for "Hot Plugging"
- Supports High Bandwidth Digital Content Protection

### APPLICATIONS

- RGB Graphics Processing
- LCD Monitors and Projectors
- Plasma Display Panels
- Scan Converter
- Microdisplays
- Digital TV

### GENERAL DESCRIPTION

The AD9882 offers designers the flexibility of an analog interface and Digital Visual Interface (DVI) receiver integrated on a single chip. Also included is support for High bandwidth Digital Content Protection (HDCP).

#### Analog Interface

The AD9882 is a complete 8-bit 140 MSPS monolithic analog interface optimized for capturing RGB graphics signals from personal computers and workstations. Its 140 MSPS encode rate capability and full power analog bandwidth of 300 MHz supports resolutions up to SXGA (1280 × 1024 at 75 Hz).

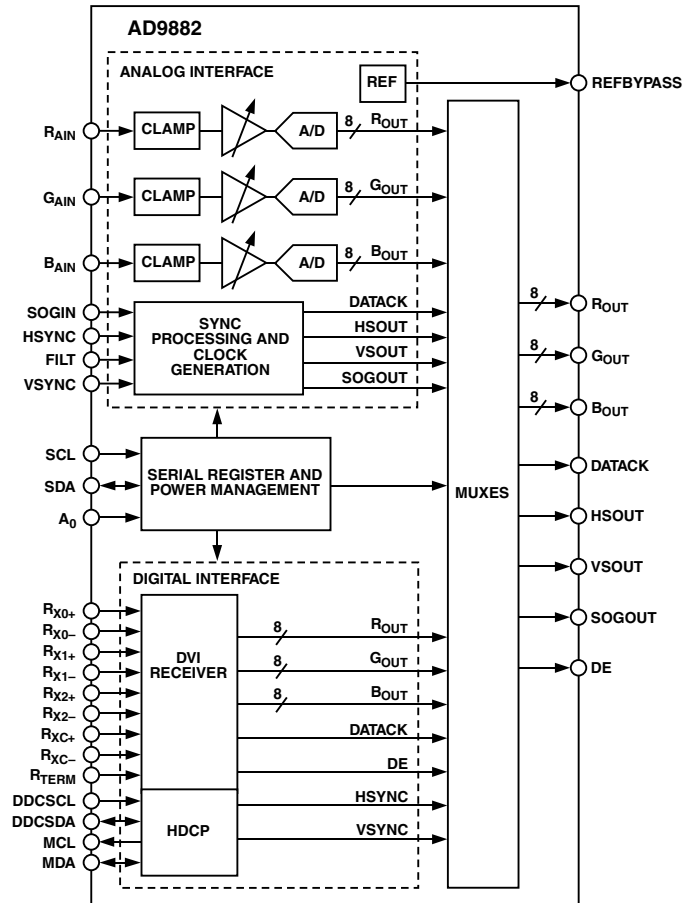
The analog interface includes a 140 MHz triple ADC with internal 1.25 V reference, a Phase Locked Loop (PLL), and programmable gain, offset, and clamp control. The user provides only a 3.3 V power supply, analog input, and Hsync. Three-state CMOS outputs may be powered from 2.2 V to 3.3 V.

The AD9882's on-chip PLL generates a pixel clock from Hsync. Pixel clock output frequencies range from 12 MHz to 140 MHz. PLL clock jitter is typically 500 ps p-p at 140 MSPS. The AD9882 also offers full sync processing for composite sync and Sync-on-Green (SOG) applications.

#### REV. A

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### FUNCTIONAL BLOCK DIAGRAM



#### Digital Interface

The AD9882 contains a DVI 1.0 compatible receiver and supports display resolutions up to SXGA (1280 × 1024 at 60 Hz). The receiver features an intra-pair skew tolerance of up to one full clock cycle.

With the inclusion of HDCP, displays may now receive encrypted video content. The AD9882 allows for authentication of a video receiver, decryption of encoded data at the receiver, and renewability of that authentication during transmission as specified by the HDCP v1.0 protocol.

Fabricated in an advanced CMOS process, the AD9882 is provided in a space-saving 100-lead LQFP surface-mount plastic package and is specified over the 0°C to 70°C temperature range.

# AD9882—SPECIFICATIONS

## ANALOG INTERFACE

### ELECTRICAL CHARACTERISTICS ( $V_D = 3.3\text{ V}$ , $V_{DD} = 3.3\text{ V}$ , ADC Clock = Maximum Conversion Rate, unless otherwise noted.)

Parameter	Temp	Test Level	AD9882KST-100			AD9882KST-140			Unit
			Min	Typ	Max	Min	Typ	Max	
RESOLUTION			8			8			Bits
DC ACCURACY									
Differential Nonlinearity	25°C	I	±0.5			±0.5			LSB
	Full	VI	+1.25/−1.0			+1.35/−1.0			LSB
Integral Nonlinearity	25°C	I	±0.5			±0.5			LSB
	Full	VI	±1.85			±2.0			LSB
	Full	VI	±2.0			±2.3			LSB
No Missing Codes	Full	VI	Guaranteed			Guaranteed			
ANALOG INPUT									
Input Voltage Range									
Minimum	Full	VI	0.5			0.5			V p-p
Maximum	Full	VI	1.0			1.0			V p-p
Gain Tempco	25°C	V	100			100			ppm/°C
Input Bias Current	Full	IV	1			1			µA
Input Full-Scale Matching	Full	VI	1.5			1.5			% FS
Offset Adjustment Range	Full	VI	46	49	56	46	49	56	% FS
REFERENCE OUTPUT									
Output Voltage	Full	VI	1.20	1.25	1.32	1.20	1.25	1.32	V
Temperature Coefficient	Full	V	±50			±50			ppm/°C
SWITCHING PERFORMANCE <sup>1</sup>									
Maximum Conversion Rate	Full	VI	100			140			MSPS
Minimum Conversion Rate	Full	IV	10			10			MSPS
Data to Clock Skew	Full	IV	−0.5			−0.5			ns
Serial Port Timing									
$t_{BUFF}$	Full	VI	4.7			4.7			µs
$t_{STAH}$	Full	VI	4.0			4.0			µs
$t_{DHO}$	Full	VI	0			0			µs
$t_{DAL}$	Full	VI	4.7			4.7			µs
$t_{DAH}$	Full	VI	4.0			4.0			µs
$t_{DSU}$	Full	VI	250			250			ns
$t_{STASU}$	Full	VI	4.7			4.7			µs
$t_{STOSU}$	Full	VI	4.0			4.0			µs
Hsync Input Frequency	Full	IV	15			110			kHz
Maximum PLL Clock Rate	Full	VI	100			140			MHz
Minimum PLL Clock Rate	Full	IV	12			12			MHz
PLL Jitter	25°C	IV	500			500			ps p-p
	Full	IV	700 <sup>2</sup>			700 <sup>2</sup>			ps p-p
	Full	IV	1000 <sup>2</sup>			1000 <sup>2</sup>			ps p-p
Sampling Phase Tempco	Full	IV	15			15			ps/°C
DIGITAL INPUTS									
Input Voltage, High ( $V_{IH}$ )	Full	VI	2.6			2.6			V
Input Voltage, Low ( $V_{IL}$ )	Full	VI	0.8			0.8			V
Input Current, High ( $I_{IH}$ )	Full	IV	−1.0			−1.0			µA
Input Current, Low ( $I_{IL}$ )	Full	IV	+1.0			+1.0			µA
Input Capacitance	25°C	V	3			3			pF
DIGITAL OUTPUTS <sup>1</sup>									
Output Voltage, High ( $V_{OH}$ )	Full	IV	$V_{DD} - 0.1$			$V_{DD} - 0.1$			V
Output Voltage, Low ( $V_{OL}$ )	Full	IV	0.4			0.4			V
Duty Cycle, DATAACK	Full	IV	45	50	55	45	50	55	%
Output Coding			Binary			Binary			

Parameter	Temp	Test Level	AD9882KST-100			AD9882KST-140			Unit
			Min	Typ	Max	Min	Typ	Max	
<b>POWER SUPPLY<sup>1</sup></b>									
V <sub>D</sub> Supply Voltage	Full	IV	3.15	3.3	3.45	3.15	3.3	3.45	V
V <sub>DD</sub> Supply Voltage	Full	IV	2.2	3.3	3.6	2.20	3.3	3.6	V
PV <sub>D</sub> Supply Voltage	Full	IV	3.15	3.3	3.45	3.15	3.3	3.45	V
I <sub>D</sub> Supply Current (V <sub>D</sub> )	25°C	V		162			181		mA
I <sub>DD</sub> Supply Current (V <sub>DD</sub> ) <sup>3</sup>	25°C	V		47			63		mA
IPV <sub>D</sub> Supply Current (PV <sub>D</sub> )	25°C	V		19			21		mA
Total Supply Current	Full	VI		228	237		265	274	mA
Power-Down Supply Current	Full	VI		30	35		30	35	mA
<b>DYNAMIC PERFORMANCE</b>									
Analog Bandwidth, Full Power	25°C	V		300			300		MHz
Signal-to-Noise Ratio (SNR) f <sub>IN</sub> = 2.3 MHz	25°C	V		44			43		dB
Crosstalk	Full	V		55			55		dBc
<b>THERMAL CHARACTERISTICS</b>									
θ <sub>JA</sub> Junction-to-Ambient <sup>4</sup>		V		43			43		°C/W

## NOTES

<sup>1</sup>Drive Strength = 11.<sup>2</sup>VCO Range = 10, Charge Pump Current = 110, PLL Divider = 1693.<sup>3</sup>DATAACK Load = 15 pF, Data Load = 5 pF.<sup>4</sup>Simulated typical performance with package mounted to a four-layer board.

Specifications subject to change without notice.

# AD9882

## DIGITAL INTERFACE

### ELECTRICAL CHARACTERISTICS ( $V_D = 3.3\text{ V}$ , $V_{DD} = 3.3\text{ V}$ , Clock = Maximum, unless otherwise noted.)

Parameter	Conditions	Temp	Test Level	AD9882KST			Unit
				Min	Typ	Max	
RESOLUTION					8		Bits
DC DIGITAL I/O Specifications							
High Level Input Voltage ( $V_{IH}$ )		Full	VI	2.6			V
Low Level Input Voltage ( $V_{IL}$ )		Full	VI			0.8	V
High Level Output Voltage ( $V_{OH}$ )		Full	IV	2.4			V
Low Level Output Voltage ( $V_{OL}$ )		Full	IV			0.4	V
Output Leakage Current ( $I_{OL}$ )	High Impedance	Full	IV	-10		+10	$\mu\text{A}$
DC SPECIFICATIONS							
Output High Drive ( $I_{OHD}$ )( $V_{OUT} = V_{OH}$ )	Output Drive = High	Full	V		11		mA
	Output Drive = Med	Full	V		8		mA
	Output Drive = Low	Full	V		5		mA
Output Low Drive ( $I_{OLD}$ )( $V_{OUT} = V_{OL}$ )	Output Drive = High	Full	V		-7		mA
	Output Drive = Med	Full	V		-6		mA
	Output Drive = Low	Full	V		-5		mA
DATAACK High Drive ( $V_{OHC}$ )( $V_{OUT} = V_{OH}$ )	Output Drive = High	Full	V		28		mA
	Output Drive = Med	Full	V		14		mA
	Output Drive = Low	Full	V		7		mA
DATAACK Low Drive ( $V_{OLC}$ )( $V_{OUT} = V_{OL}$ )	Output Drive = High	Full	V		-15		mA
	Output Drive = Med	Full	V		-9		mA
	Output Drive = Low	Full	V		-7		mA
Differential Input Voltage Single-Ended Amplitude		Full	IV	75		800	mV
POWER SUPPLY							
$V_D$ Supply Voltage		Full	IV	3.15	3.3	3.45	V
$V_{DD}$ Supply Voltage		Full	IV	2.2	3.3	3.6	V
$PV_D$ Supply Voltage		Full	IV	3.15	3.3	3.45	V
$I_D$ Supply Current (Typical Pattern) <sup>1</sup>		25°C	V		269		mA
$I_{DD}$ Supply Current (Typical Pattern) <sup>1,2</sup>		25°C	V		32		mA
$IPV_D$ Supply Current (Typical Pattern) <sup>1</sup>		25°C	V		54		mA
Total Supply Current with HDCP (Typical Pattern) <sup>1,2</sup>		Full	IV		355	367	mA
$I_D$ Supply Current (Worst-Case Pattern) <sup>3</sup>		25°C	V		276		mA
$I_{DD}$ Supply Current (Worst-Case Pattern) <sup>2,3</sup>		25°C	V		127		mA
$IPV_D$ Supply Current (Worst-Case Pattern) <sup>3</sup>		25°C	V		54		mA
Total Supply Current with HDCP (Worst-Case Pattern) <sup>2,3</sup>		Full	IV		457	468	mA
Power-Down Supply Current ( $I_{PD}$ )		Full	VI		30	35	mA

Parameter	Conditions	Temp	Test Level	AD9882KST			Unit
				Min	Typ	Max	
<b>AC SPECIFICATIONS</b>							
Intra-Pair (+ to -) Differential Input Skew ( $T_{DPS}$ )		Full	IV			360	ps
Channel-to-Channel Differential Input Skew ( $T_{CCS}$ )		Full	IV			1	Clock Period
Low-to-High Transition Time for Data ( $D_{LHT}$ )	Output Drive = High, $C_L = 10$ pF	Full	IV			2.2	ns
	Output Drive = Med, $C_L = 7$ pF	Full	IV			2.5	ns
	Output Drive = Low, $C_L = 5$ pF	Full	IV			3.2	ns
Low-to-High Transition Time for DATAACK ( $D_{LHT}$ )	Output Drive = High, $C_L = 10$ pF	Full	IV			1.0	ns
	Output Drive = Med, $C_L = 7$ pF	Full	IV			1.6	ns
	Output Drive = Low, $C_L = 5$ pF	Full	IV			2.1	ns
High-to-Low Transition Time for Data ( $D_{HLT}$ )	Output Drive = High, $C_L = 10$ pF	Full	IV			2.2	ns
	Output Drive = Med, $C_L = 7$ pF	Full	IV			1.9	ns
	Output Drive = Low, $C_L = 5$ pF	Full	IV			1.7	ns
High-to-Low Transition Time for DATAACK ( $D_{HLT}$ )	Output Drive = High, $C_L = 10$ pF	Full	IV			1.0	ns
	Output Drive = Med, $C_L = 7$ pF	Full	IV			1.0	ns
	Output Drive = Low, $C_L = 5$ pF	Full	IV			1.4	ns
Data-to-Clock Skew <sup>4</sup>		Full	IV	-0.5		+2.0	ns
Duty Cycle, DATAACK <sup>4</sup>		Full	IV	40	46	50	%
DATAACK Frequency ( $F_{CIP}$ )		Full	VI	25		112	MHz

## NOTES

<sup>1</sup>The typical pattern contains a grayscale area, Output Drive = High.

<sup>2</sup>DATAACK Load = 10 pF, Data Load = 10 pF.

<sup>3</sup>The worst-case pattern contains a black and white checkerboard pattern, Output Drive = High.

<sup>4</sup>DRIVE STRENGTH = 11

Specifications subject to change without notice.

# AD9882

## ABSOLUTE MAXIMUM RATINGS\*

V <sub>D</sub>	3.6 V
V <sub>DD</sub>	3.6 V
Analog Inputs	V <sub>D</sub> to 0.0 V
VREF	V <sub>D</sub> to 0.0 V
Digital Inputs	5 V to 0.0 V
Digital Output Current	20 mA
Operating Temperature	-25°C to +85°C
Storage Temperature	-65°C to +150°C
Maximum Junction Temperature	175°C
Maximum Case Temperature	150°C

\*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## ORDERING GUIDE

Model	Temperature Range	Package Option
AD9882KST-100	0°C to 70°C	ST-100
AD9882KST-140	0°C to 70°C	ST-100
AD9882/PCB	25°C	Evaluation Board

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9882 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## EXPLANATION OF TEST LEVELS

### Test Level

- I. 100% production tested.
- II. 100% production tested at 25°C and sample tested at specified temperatures.
- III. Sample tested only.
- IV. Parameter is guaranteed by design and characterization testing.
- V. Parameter is a typical value only.
- VI. 100% production tested at 25°C; guaranteed by design and characterization testing.



## PIN CONFIGURATION

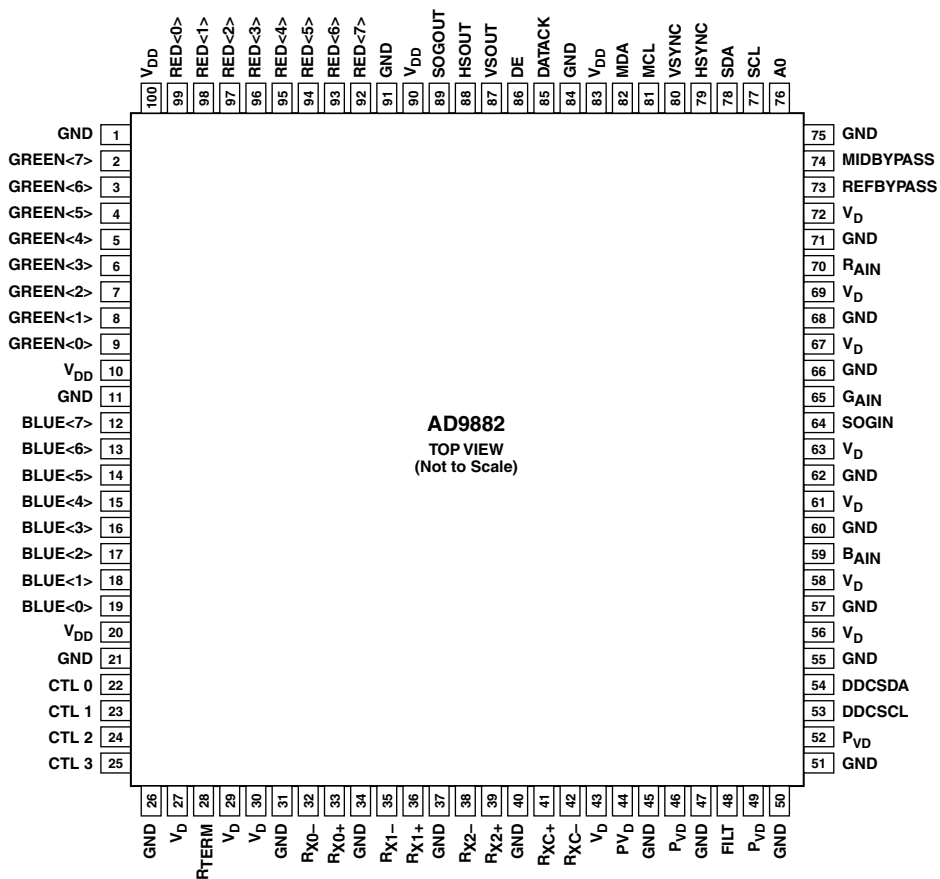


Table I. Complete Pinout List

Pin Type	Mnemonic	Function	Value	Pin Number	Interface
Analog Video Inputs	R <sub>AIN</sub>	Analog Input for Converter R	0.0 V to 1.0 V	70	Analog
	G <sub>AIN</sub>	Analog Input for Converter G	0.0 V to 1.0 V	65	Analog
	B <sub>AIN</sub>	Analog Input for Converter B	0.0 V to 1.0 V	59	Analog
External Sync/Clock	HSYNC	Horizontal Sync Input	3.3 V CMOS	79	Analog
	VSYNC	Vertical Sync Input	3.3 V CMOS	80	Analog
	SOGIN	Input for Sync-on-Green	0.0 V to 1.0 V	64	Analog
Sync Outputs	HSOUT	HSYNC Output Clock (Phase-Aligned with DATAACK)	3.3 V CMOS	88	Both
	VSOUT	VSYNC Output Clock	3.3 V CMOS	87	Both
	SOGOUT	Sync-on-Green Slicer Output	3.3 V CMOS	89	Analog
References	REFBYPASS	Internal Reference Bypass	1.25 V	73	Analog
	MIDBYPASS	Internal Midscale Voltage Bypass		74	Analog
PLL Filter	FILT	Connection for External Filter Components for Internal PLL		48	Analog
Power Supply	V <sub>D</sub>	Analog Power Supply	3.15 V to 3.45 V		Both
	V <sub>DD</sub>	Output Power Supply	2.2 V to 3.6 V		Both
	PV <sub>D</sub>	PLL Power Supply	3.15 V to 3.45 V		Both
	GND	Ground	0 V		Both
Serial Port Control	SDA	Serial Port Data I/O	3.3 V CMOS	78	Both
	SCL	Serial Port Data Clock (100 kHz Max)	3.3 V CMOS	77	Both
	A0	Serial Port Address Input	3.3 V CMOS	76	Both
Data Outputs	Red [7:0]	Outputs of Converter “Red”, Bit 7 is the MSB	3.3 V CMOS	92–99	Both
	Green [7:0]	Outputs of Converter “Green”, Bit 7 is the MSB	3.3 V CMOS	2–9	Both
	Blue [7:0]	Outputs of Converter “Blue”, Bit 7 is the MSB	3.3 V CMOS	12–19	Both
Data Clock Output	DATAACK	Data Output Clock for the Analog and Digital Interface	3.3 V CMOS	85	Both
Digital Video Data Inputs	R <sub>X0+</sub>	Digital Input Channel 0 True		33	Digital
	R <sub>X0-</sub>	Digital Input Channel 0 Complement		32	Digital
	R <sub>X1+</sub>	Digital Input Channel 1 True		36	Digital
	R <sub>X1-</sub>	Digital Input Channel 1 Complement		35	Digital
	R <sub>X2+</sub>	Digital Input Channel 2 True		39	Digital
	R <sub>X2-</sub>	Digital Input Channel 2 Complement		38	Digital
Digital Video Clock Inputs	R <sub>XC+</sub>	Digital Data Clock True		41	Digital
	R <sub>XC-</sub>	Digital Data Clock Complement		42	Digital
Data Enable	DE	Data Enable	3.3 V CMOS	86	Digital
Control Bits	CTL [0:3]	Decoded Control Bits	3.3 V CMOS	22–25	Digital
R <sub>TERM</sub>	R <sub>TERM</sub>	Sets Internal Termination Resistance		28	Digital
HDCP	DDCSCL	HDCP Slave Serial Port Data Clock	3.3 V CMOS	53	Digital
	DDCSDA	HDCP Slave Serial Port Data I/O	3.3 V CMOS	54	Digital
	MCL	HDCP Master Serial Port Data Clock	3.3 V CMOS	81	Digital
	MDA	HDCP Master Serial Port Data I/O	3.3 V CMOS	82	Digital



### PIN DESCRIPTIONS OF SHARED PINS BETWEEN ANALOG AND DIGITAL INTERFACES

**HSOUT**      **Horizontal Sync Output**  
A reconstructed and phase-aligned version of the video Hsync. The polarity of this output can be controlled via a serial bus bit. In analog interface mode, the placement and duration are variable. In digital interface mode, the placement and duration are set by the graphics transmitter.

**VSOUT**      **Vertical Sync Output**  
The separated Vsync from a composite signal or a direct pass-through of the Vsync input. The polarity of this output can be controlled via a serial bus bit. The placement and duration in all modes is set by the graphics transmitter.

### SERIAL PORT (2-WIRE)

**SDA**      **Serial Port Data I/O**

**SCL**      **Serial Port Data Clock**

**A0**      **Serial Port Address Input**

For a full description of the 2-wire serial register, refer to the Control Port section on 2-Wire Serial Control.

### DATA OUTPUTS

**RED**      **Data Output, RED Channel**

**GREEN**      **Data Output, GREEN Channel**

**BLUE**      **Data Output, BLUE Channel**

The main data outputs. Bit 7 is the MSB. These outputs are shared between the two interfaces and behave according to which interface is active. Refer to the sections on the two interfaces for more information on how these outputs behave.

**DATAACK**      **Data Output Clock**

Just like the data outputs, the data clock output is shared between the two interfaces. It behaves differently depending on which interface is active. Refer to the sections on the two interfaces to determine how this pin behaves.

**Table II. Analog Interface Pin List**

Pin Type	Mnemonic	Function	Value	Pin Number
Analog Video Inputs	R <sub>AIN</sub>	Analog Input for Converter R	0.0 V to 1.0 V	70
	G <sub>AIN</sub>	Analog Input for Converter G	0.0 V to 1.0 V	65
	B <sub>AIN</sub>	Analog Input for Converter B	0.0 V to 1.0 V	59
External Sync/Clock	HSYNC	Horizontal SYNC Input	3.3 V CMOS	79
	VSYNC	Vertical SYNC Input	3.3 V CMOS	80
	SOGIN	Sync-on-Green Input	0.0 V to 1.0 V	64
Sync Outputs	HSOUT	Hsync Output (Phase-Aligned with DATAACK)	3.3 V CMOS	88
	VSOUT	Vsync Output	3.3 V CMOS	87
	SOGOUT	Composite SYNC	3.3 V CMOS	89
Voltage Reference Clamp Voltages	REFBYPASS	Internal Reference Bypass	1.25 V	73
	MIDBYPASS	Internal Midscale Voltage Bypass		74
PLL Filter	FILT	Connection for External Filter Components for Internal PLL		48
Power Supply	V <sub>D</sub>	Main Power Supply	3.15 V to 3.45 V	
	PV <sub>D</sub>	PLL Power Supply (Nominally 3.3 V)	3.15 V to 3.45 V	
	V <sub>DD</sub>	Output Power Supply	2.2 V to 3.6 V	
	GND	Ground	0 V	

# AD9882

## PIN FUNCTION DETAIL (ANALOG INTERFACE)

### INPUTS

**R<sub>AIN</sub>** Analog Input for RED Channel

**G<sub>AIN</sub>** Analog Input for GREEN Channel

**B<sub>AIN</sub>** Analog Input for BLUE Channel

High impedance inputs that accept the RED, GREEN, and BLUE channel graphics signals, respectively. For RGB, the three channels are identical and can be used for any colors, but colors are assigned for convenient reference.

For proper 4:2:2 formatting in a YPbPr application, the Y must be connected to the G<sub>AIN</sub> input, the Pb must be connected to the B<sub>AIN</sub> input, and the Pr must be connected to the R<sub>AIN</sub> input.

They accommodate input signals ranging from 0.5 V to 1.0 V full scale. Signals should be ac-coupled to these pins to support clamp operation.

**HSYNC** Horizontal Sync Input

This input receives a logic signal that establishes the horizontal timing reference and provides the frequency reference for pixel clock generation.

The logic sense of this pin is controlled by Serial Register Bit 10H, Bit 6 (Hsync Polarity). Only the leading edge of Hsync is active; the trailing edge is ignored. When Hsync Polarity = 0, the falling edge of Hsync is used. When Hsync Polarity = 1, the rising edge is active.

The input includes a Schmitt trigger for noise immunity, with a nominal input threshold of 1.5 V.

Electrostatic Discharge (ESD) protection diodes will conduct heavily if this pin is driven more than 0.5 V above the maximum tolerance voltage (3.3 V), or more than 0.5 V below ground.

**VSYNC** Vertical Sync Input

This is the input for vertical sync.

**SOGIN** Sync-on-Green Input

This input is provided to assist with processing signals with embedded sync, typically on the GREEN channel. The pin is connected to a high speed comparator with an internally generated threshold, which is set by the value of register 0FH, Bits 7–3.

When connected to an ac-coupled graphics signal with embedded sync, it will produce a noninverting digital output on SOGOUT.

When not used, this input should be left unconnected. For more details on this function and how it should be configured, refer to the Sync-on-Green section.

**SOGOUT**

**Sync-on-Green Slicer Output**

This pin can be programmed to produce either the output from the Sync-on-Green slicer comparator or an unprocessed but delayed version of the Hsync input. See the Sync Processing Block Diagram, Figure 18, to view how this pin is connected.

Note: The output from this pin is the composite SYNC without additional processing from the AD9882.

**FILT**

**External Filter Connection**

For proper operation, the pixel clock generator PLL requires an external filter. Connect the filter shown in Figure 6 to this pin. For optimal performance, minimize noise and parasitics on this node.

**REFBYPASS** Internal Reference BYPASS

Bypass for the internal 1.25 V band gap reference. It should be connected to ground through a 0.1  $\mu$ F capacitor.

The absolute accuracy of this reference is  $\pm 4\%$ , and the temperature coefficient is  $\pm 50$  ppm, which is adequate for most AD9882 applications. If higher accuracy is required, an external reference may be employed instead.

**MIDBYPASS** Midscale Voltage Reference BYPASS

Bypass for the internal midscale voltage reference. It should be connected to ground through a 0.1  $\mu$ F capacitor. The exact voltage varies with the gain setting of the RED channel.

**HSOUT**

**Horizontal Sync Output**

A reconstructed and phase-aligned version of the Hsync input. The duration of Hsync can only be programmed on the analog interface, not the digital.

**DATAACK**

**Data Output Clock**

The data clock output signal is used to clock the output data and HSOUT into external logic.

It is produced by the internal clock generator and is synchronous with the internal pixel sampling clock.

When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The Data, DATAACK, and HSOUT outputs are all moved so the timing relationship among the signals is maintained.

**VSOUT**

**Vertical Sync Output**

The separated Vsync from a composite signal or a direct pass-through of the Vsync input. The polarity of this output can be controlled via Register 10H, Bit 2. The placement and duration in all modes is set by the graphics transmitter.

**RED**            **Data Output, RED Channel**  
**GREEN**       **Data Output, GREEN Channel**  
**BLUE**         **Data Output, BLUE Channel**

These are the main data outputs. Bit 7 is the MSB.

The delay from pixel sampling time to output is fixed. When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The DATAACK and HSOUT outputs are also moved, so the timing relationship among the signals is maintained.

Please refer to the timing diagrams for more information.

**POWER SUPPLY**

**V<sub>D</sub>**            **Main Power Supply**

These pins supply power to the main elements of the circuit. They should be as quiet as possible.

**V<sub>DD</sub>**           **Digital Output Power Supply**

A large number of output pins (up to 25) switching at high speed (up to 140 MHz) generates a lot of power supply transients. These supply pins are identified separately from the V<sub>D</sub> pins so special care can be taken to minimize output noise transferred into the sensitive analog circuitry.

If the AD9882 is interfacing with lower voltage logic, V<sub>DD</sub> may be connected to a lower supply voltage (as low as 2.2 V) for compatibility.

**PV<sub>D</sub>**           **Clock Generator Power Supply**

The most sensitive portion of the AD9882 is the clock generation circuitry. These pins provide power to the clock PLL and help the user design for optimal performance. The designer should provide noise-free power to these pins.

**GND**           **Ground**

The ground return for all circuitry on chip. It is recommended that the AD9882 be assembled on a single solid ground plane, with careful attention to ground current paths.

**Table III. Interface Selection Controls**

AIO (0FH Bit 2)	Analog Interface Detect	Digital Interface Detect	AIS (0FH Bit 1)	Active Interface	Description
1	X	X	0	Analog	Force the analog interface active.
			1	Digital	Force the digital interface active.
0	0	0	X	None	Neither interface was detected. Both interfaces are powered down.
			X	Digital	The digital interface was detected. Power down the analog interface.
			X	Analog	The analog interface was detected. Power down the digital interface.
			0	Analog	Both interfaces were detected. The analog interface gets priority.
1	Digital	Both interfaces were detected. The digital interface gets priority.			

Table IV. Power-Down Modes, 4:2:2 and 4:4:4 Format Descriptions

Mode	Power-Down <sup>1</sup>	Analog Interface Detect <sup>2</sup>	Digital Interface Detect <sup>3</sup>	Active Interface Override	Active Interface Select	4:2:2 Formatting	Data Sheet Signals Powered On
Soft Power-Down (Seek Mode)	1	0	0	0	X	X	Serial bus, digital interface clock detect, analog interface clock detect, SOG
Digital Interface On	1	0	1	0	X	X	Serial bus; digital interface and analog interface activity detect; SOG, band gap reference; red, green, and blue outputs
Analog Interface On 4:4:4 Format	1	1	0	0	X	0	Serial bus; analog interface and digital interface clock detect; SOG, band gap reference; red, green, and blue outputs
Analog Interface On 4:2:2 Format	1	1	0	0	X	1	Serial bus; analog interface and digital interface clock detect; SOG, band gap reference; red and green outputs only
Serial Bus Arbitrated Interface	1	1	1	1	0	0	Same as Analog Interface on 4:4:4 Mode
Serial Bus Arbitrated Interface	1	1	1	1	0	1	Same as Analog Interface on 4:2:2 Mode
Serial Bus Arbitrated Interface	1	1	1	1	1	X	Same as Digital Interface Mode
Override to Analog Interface	1	1	X	1	0	0	Same as Analog Interface 4:4:4 Mode
Override to Analog Interface	1	1	X	1	0	1	Same as Analog Interface 4:2:2 Mode
Override to Digital Interface	1	X	1	1	1	X	Same as Digital Interface Mode
Absolute Power-Down	0	X	X	X	X	X	Serial Bus

## NOTES

<sup>1</sup>Power-down is controlled via Bit 1 in Serial Bus Register 14H.

<sup>2</sup>Analog Interface Detect is determined by OR-ing Bits 7, 6, and 5 in Serial Bus Register 15H.

<sup>3</sup>Digital Interface Detect is determined by Bit 4 in Serial Bus Register 15H.

## THEORY OF OPERATION (INTERFACE DETECTION)

### Active Interface Detection and Selection

The AD9882 includes circuitry to detect whether an interface is active or not. See Table III.

For detecting the *analog* interface, the circuitry monitors the presence of Hsync, Vsync, and Sync-on-Green. The result of the detection circuitry can be read from the 2-wire serial interface bus at Address 15H, Bits 7, 5, and 6, respectively. If one of these sync signals disappears, the maximum time it takes for the circuitry to detect it is 100 ms.

For detecting the *digital* interface, there are two stages of detection. The first stage searches for the presence of the digital interface clock. The circuitry for detecting the digital interface clock is active even when the digital interface is powered down. The result of this detection stage can be read from the 2-wire serial interface bus at Address 15H, Bit 4. If the clock disappears, the maximum time it takes for the circuitry to detect it is 100 ms. Once a digital interface clock is detected, the digital interface is powered up and the second stage of detection begins. During the second stage, the circuitry searches for 32 consecutive DEs. Once 32 DEs are found, the detection process is complete.

There is an override for the automatic interface selection. It is the AIO (Active Interface Override) bit, Register 0FH, Bit 2. When the AIO bit is set to logic "0," the automatic circuitry will be used. When the AIO bit is set to logic "1," the AIS (Active Interface Select) bit (Register 0FH, Bit 1) will be used to determine the active interface rather than the automatic circuitry.

### Power Management

The AD9882 is a dual interface device with shared outputs. Only one interface can be used at a time. For this reason, the chip automatically powers down the unused interface. When the analog interface is being used, most of the digital interface circuitry is powered down, and vice versa. This helps to minimize the AD9882 total power dissipation. In addition, if neither interface has activity on it, then the chip powers down both interfaces. The AD9882 uses the activity detect circuits, the active interface bits in Serial Register 15H, the active interface override bits in Register 0FH, Bits 2 and 1, and the power-down bit in Register 14H, Bit 1, to determine the correct power state. In a given power mode, not all circuitry in the inactive interface is powered down completely. When the digital interface is active, the band gap reference Hsync, Vsync, and SOG detect circuitry remain powered up. When the analog interface is active, the digital interface clock detect circuit is not powered down. Table IV summarizes how the AD9882 determines what power mode to be in and what circuitry is powered on/off in each of these modes. The power-down command has priority, then the active interface override, and then the automatic circuitry.

## THEORY OF OPERATION AND DESIGN GUIDE (ANALOG INTERFACE)

### General Description

The AD9882 is a fully integrated solution for capturing analog RGB signals and digitizing them for display on flat panel monitors or projectors. The device is ideal for implementing a computer interface for HDTV monitors or as the front end to high performance video scan converters.

Implemented in a high performance CMOS process, the interface can capture signals with pixel rates of up to 140 MHz.

The AD9882 includes all necessary input buffering, signal dc restoration (clamping), offset and gain (brightness and contrast) adjustment, pixel clock generation, sampling phase control, and output data formatting. All controls are programmable via a 2-wire serial interface. Full integration of these sensitive analog functions makes the system design straightforward and less sensitive to the physical and electrical environment.

With a typical power dissipation of only 875 mW and an operating temperature range of 0°C to 70°C, the device requires no special environmental considerations.

### Input Signal Handling

The AD9882 has three high impedance analog input pins for the RED, GREEN, and BLUE channels. They will accommodate signals ranging from 0.5 V to 1.0 V p-p.

Signals are typically brought onto the interface board via a DVI-I connector, a 15-pin D connector, or BNC connectors. The AD9882 should be located as close as practical to the input connector. Signals should be routed via matched-impedance traces (normally 75  $\Omega$ ) to the IC input pins.

At that point, the signal should be resistively terminated (75  $\Omega$  to the signal ground return) and capacitively coupled to the AD9882 inputs through 47 nF capacitors. These capacitors form part of the dc restoration circuit. See Figure 1.

In an ideal world of perfectly matched impedances, the best performance can be obtained with the widest possible signal bandwidth. The wide bandwidth inputs of the AD9882 (300 MHz) can track the input signal continuously as it moves from one pixel level to the next and digitize the pixel during a long, flat pixel time. In many systems, however, there are mismatches, reflections, and noise, which can result in excessive ringing and distortion of the input waveform. This makes it more difficult to establish a sampling phase that provides good image quality. It has been shown that a small inductor in series with the input is effective in rolling off the input bandwidth slightly and providing a high quality signal over a wider range of conditions. Using a Fair-Rite #2508051217Z0 High Speed Signal Chip Bead inductor in the circuit of Figure 1 gives good results in most applications.

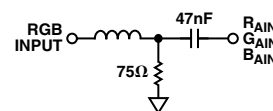


Figure 1. Analog Input Interface Circuit

# AD9882

## Hsync, Vsync Inputs

The AD9882 receives a horizontal sync signal and uses it to generate the pixel clock and clamp timing. This can be either a sync signal directly from the graphics source or a preprocessed TTL or CMOS level signal.

The Hsync input includes a Schmitt trigger buffer and is capable of handling signals with long rise times, with superior noise immunity. In typical PC based graphic systems, the sync signals are simply TTL level drivers feeding unshielded wires in the monitor cable. As such, no termination is required.

## Serial Control Port

The serial control port is designed for 3.3 V logic. If there are 5 V drivers on the bus, these pins should be protected with 150  $\Omega$  series resistors placed between the pull-up resistors and the input pins.

## Output Signal Handling

The digital outputs are designed and specified to operate from a 3.3 V power supply ( $V_{DD}$ ). They can also work with a  $V_{DD}$  as low as 2.5 V for compatibility with other 2.5 V logic.

## Clamping

### RGB Clamping

To properly digitize the incoming signal, the dc offset of the input must be adjusted to fit the range of the on-board A/D converters.

Most graphics systems produce RGB signals with black at ground and white at approximately 0.75 V. However, if sync signals are embedded in the graphics, the sync tip is often at ground and black is at 300 mV; white will be approximately 1.0 V. Some common RGB line amplifier boxes use emitter-follower buffers to split signals and increase drive capability. This introduces a 700 mV dc offset to the signal, which is removed by clamping for proper capture by the AD9882.

The key to clamping is to identify a portion (time) of the signal when the graphic system is known to be producing black. Originating from CRT displays, the electron beam is “blanked” by sending a black level during horizontal retrace to prevent disturbing the image. Most graphics systems maintain this format of sending a black level between active video lines.

An offset is then introduced, which results in the A/D converters producing a black output (code 00H) when the known black input is present. The offset then remains in place when other signal levels are processed, and the entire signal is shifted to eliminate offset errors.

In systems with embedded sync, a blacker-than-black signal (Hsync) is produced briefly to signal the CRT that it is time to begin a retrace. For obvious reasons, it is important to avoid clamping on the tip of Hsync. Fortunately, there is virtually always a period following Hsync called the back porch, in which a good black reference is provided. This is the time when clamping should be done.

The clamp timing is established by the AD9882 internal clamp timing generator. The Clamp Placement Register (05H) is programmed with the number of pixel times that should pass after the trailing edge of Hsync before clamping starts. A second register (Clamp Duration, 06H) sets the duration of the clamp.

These are both 8-bit values, providing considerable flexibility in clamp generation. The clamp timing is referenced to the trailing edge of Hsync since the back porch (black reference) always follows Hsync. A good starting point for establishing clamping is to set the clamp placement to 08H (providing eight pixel periods for the graphics signal to stabilize after sync) and set the clamp duration to 14H (giving the clamp 20 pixel periods to re-establish the black reference).

The value of the external input coupling capacitor affects the performance of the clamp. If the value is too small, there can be an amplitude change during a horizontal line time (between clamping intervals). If the capacitor is too large, then it will take excessively long for the clamp to recover from a large change in incoming signal offset. The recommended value (47 nF) results in recovery from a step error of 100 mV to within one-half LSB in 10 lines using a clamp duration of 20 pixel periods on a 75 Hz SXGA signal.

### YUV Clamping

YUV signals are slightly different from RGB signals in that the dc reference level (black level in RGB signals) will be at the midpoint of the U and V video. For these signals, it can be necessary to clamp to the midscale range of the A/D converter range (80H) rather than the bottom of the A/D converter range (00H).

Clamping to midscale rather than ground can be accomplished by setting the clamp select bits in the serial bus register. Each of the three converters has its own selection bit so that they can be clamped to either midscale or ground independently. These bits are located in Register 11H and are Bits 4–6. The midscale reference voltage that each A/D converter clamps to is provided on the MIDBYPASS pin (Pin 74). This pin should be bypassed to ground with a 0.1  $\mu$ F capacitor (even if midscale clamping is not required).

### Gain and Offset Control

The AD9882 can accommodate input signals with inputs ranging from 0.5 V to 1.0 V full scale. The full-scale range is set in three 8-bit registers (RED Gain, GREEN Gain, and BLUE Gain).

A code of 0 establishes a minimum input range of 0.5 V; 255 corresponds with the maximum range of 1.0 V. Note that INCREASING the gain setting results in an image with LESS contrast.

The offset control shifts the entire input range, resulting in a change in image brightness. Three 7-bit registers (RED Offset, GREEN Offset, BLUE Offset) provide independent settings for each channel.

The offset controls provide a  $\pm 63$  LSB adjustment range. This range is connected with the full-scale range, so if the input range is doubled (from 0.5 V to 1.0 V), the offset step size is also doubled (from 2 mV per step to 4 mV per step).

Figure 2 illustrates the interaction of gain and offset controls. The magnitude of an LSB in offset adjustment is proportional to the full-scale range, so changing the full-scale range also changes the offset. The change is minimal if the offset setting is near midscale. When changing the offset, the full-scale *range* is not affected, but the full-scale *level* is shifted by the same amount as the zero-scale level.



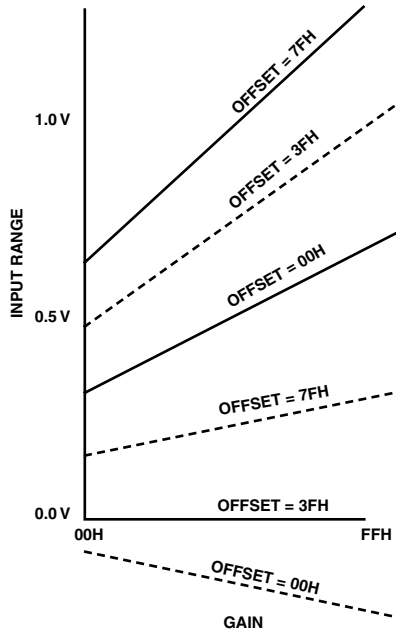


Figure 2. Gain and Offset Control

**Sync-on-Green (SOG)**

The Sync-on-Green input operates in two steps. First, it sets a baseline clamp level off of the incoming video signal with a negative peak detector. Second, it sets the Sync trigger level (nominally 150 mV above the negative peak). The exact trigger level is variable and can be programmed via Register 0FH, Bits 7-3. The Sync-on-Green input must be ac-coupled to the green analog input through its own capacitor as shown in Figure 3. The value of the capacitor must be 1 nF ±20%. If Sync-on-Green is not used, this connection is not required and SOGIN should be left unconnected. (Note: The Sync-on-Green signal is always negative polarity.) Please refer to the Sync Processing section for further information.

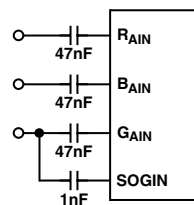


Figure 3. Typical Clamp Configuration

**Clock Generation**

A Phase Locked Loop (PLL) is employed to generate the pixel clock. The Hsync input provides a reference frequency for the PLL. A Voltage Controlled Oscillator (VCO) generates a much higher pixel clock frequency. This pixel clock is divided by the PLL divide value (Registers 01H and 02H) and phase compared with the Hsync input. Any error is used to shift the VCO frequency and maintain lock between the two signals.

The stability of this clock is a very important element in providing the clearest and most stable image. During each pixel time, there is a period during which the signal is slewing from the old pixel amplitude and settling at its new value. Then there is a time when the input voltage is stable, before the signal must slew to a new value (Figure 4). The ratio of the slewing time to the stable time is a function of the bandwidth of the graphics DAC and the bandwidth of the transmission system (cable and termination). It is also a function of the overall pixel rate. Clearly, if the dynamic characteristics of the system remain fixed, then the slewing and settling time is likewise fixed. This time must be subtracted from the total pixel period, leaving the stable period. At higher pixel frequencies, the total cycle time is shorter, and the stable pixel time becomes shorter as well.

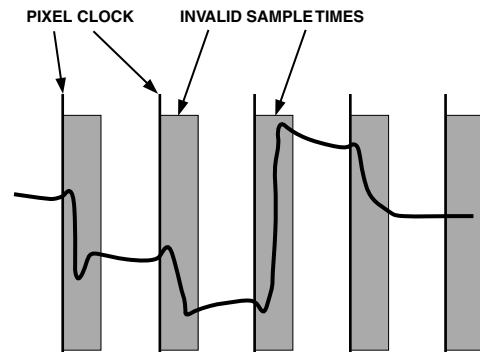


Figure 4. Pixel Sampling Times

Any jitter in the clock reduces the precision with which the sampling time can be determined and must also be subtracted from the stable pixel time.

Considerable care has been taken in the design of the AD9882's clock generation circuit to minimize jitter. As indicated in Figure 5, the clock jitter of the AD9882 is less than 6% of the total pixel time in all operating modes, making the reduction in the valid sampling time due to jitter negligible.

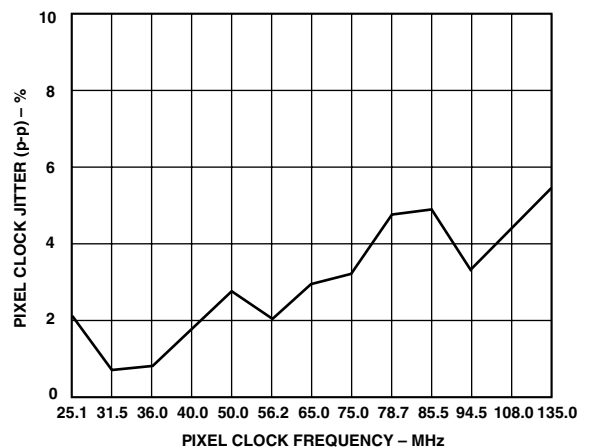


Figure 5. Pixel Clock Jitter vs. Frequency

# AD9882

The PLL characteristics are determined by the loop filter design, the PLL charge pump current, and the VCO range setting. The loop filter design is illustrated in Figure 6. Recommended settings of VCO range and charge pump current for VESA standard display modes are listed in Table VII.

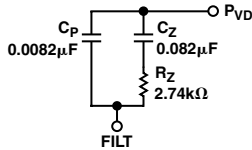


Figure 6. PLL Loop Filter Detail

Four programmable registers are provided to optimize the performance of the PLL. These registers are:

1. The 12-bit Divisor Register (Registers 01H and 02H). The input Hsync frequencies range from 15 kHz to 110 kHz. The PLL multiplies the frequency of the Hsync signal, producing pixel clock frequencies in the range of 12 MHz to 140 MHz. The Divisor Register controls the exact multiplication factor. This register may be set to any value between 221 and 4095. (The divide ratio that is actually used is the programmed divide ratio plus one.)
2. The 2-bit VCO Range Register (Register 03H, Bits 6 and 7). To improve the noise performance of the AD9882, the VCO operating frequency range is divided into three overlapping regions. The VCO Range register sets this operating range. The frequency ranges for the lowest and highest regions are shown in Table V.

Table V. VCO Frequency Ranges

PV1	PV0	Pixel Clock Range (MHz)
0	0	12–41
0	1	41–82
1	0	82–140

3. The 3-bit Charge Pump Current Register (Register 03H, Bits 3–5). This register allows the current that drives the low-pass loop filter to be varied. The possible current values are listed in Table VI.

Table VI. Charge Pump Current/Control Bits

Ip2	Ip1	Ip0	Current (µA)
0	0	0	50
0	0	1	100
0	1	0	150
0	1	1	250
1	0	0	350
1	0	1	500
1	1	0	750
1	1	1	1500

4. The 5-bit Phase Adjust Register (Register 04H, Bits 3–7). The phase of the generated sampling clock may be shifted to locate an optimum sampling point within a clock cycle. The Phase Adjust Register provides 32 phase-shift steps of 11.25° each. The Hsync signal with an identical phase shift is available through the HSOUT pin.

Table VII. Recommended VCO Range and Charge Pump Current Settings for Standard Display Formats

Standard	Refresh Resolution	Horizontal Rate (Hz)	Frequency (kHz)	Pixel Rate (MHz)	VCORNGE	CURRENT
VGA	640 × 480	60	31.5	25.175	00	101
		72	37.7	31.500	00	101
		75	37.5	31.500	00	101
		85	43.3	36.000	00	110
SVGA	800 × 600	56	35.1	36.000	00	101
		60	37.9	40.000	00	110
		72	48.1	50.000	01	101
		75	46.9	49.500	01	101
		85	53.7	56.250	01	101
XGA	1024 × 768	60	48.4	65.000	01	101
		70	56.5	75.000	01	110
		75	60.0	78.750	01	110
		80	64.0	85.500	10	101
		85	68.3	94.500	10	101
SXGA	1280 × 1024	60	64.0	108.000	10	101
		75	80.0	135.000	11	110



The COAST function allows the PLL to continue to run at the same frequency, in the absence of the incoming Hsync signal or during disturbances in Hsync (such as equalization pulses). This may be used during the vertical sync period, or any other time that the Hsync signal is unavailable. Also, the polarity of the Hsync signal may be set through the Hsync Polarity Bit (Register 10H, Bit 6). If not using automatic polarity detection, the Hsync polarity bit should be set to match the polarity of the Hsync input signal.

#### TIMING (ANALOG INTERFACE)

The following timing diagrams show the operation of the AD9882.

The Output Data Clock signal is created so that its rising edge always occurs between data transitions and can be used to latch the output data externally.

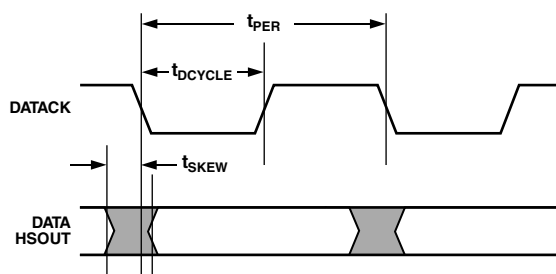


Figure 7. Output Timing

#### Hsync Timing

Horizontal Sync (Hsync) is processed in the AD9882 to eliminate ambiguity in the timing of the leading edge with respect to the phase-delayed pixel clock and data.

The Hsync input is used as a reference to generate the pixel sampling clock. The sampling phase can be adjusted, with respect to Hsync, through a full 360° in 32 steps via the Phase Adjust

Register (Register 04H) to optimize the pixel sampling time. Display systems use Hsync to align memory and display write cycles, so it is important to have a stable timing relationship between Hsync output (HSOUT) and data clock (DATAACK).

Three things happen to Horizontal Sync in the AD9882. First, the polarity of Hsync input is determined and will thus have a known output polarity. The known output polarity can be programmed either active high or active low (Register 10H, Bit 5). Second, HSOUT is aligned with DATAACK and data outputs. Third, the duration of HSOUT (in pixel clocks) is set via Register 07H. HSOUT is the sync signal that should be used to drive the rest of the display system.

#### Coast Timing

In most computer systems, the Hsync signal is provided continuously on a dedicated wire. In these systems, the COAST function is unnecessary and should be disabled using Register 11H, Bits 1–3.

In some systems, however, Hsync is disturbed during the Vertical Sync period (Vsync). In other cases, Hsync pulses disappear. In other systems, such as those that employ Composite Sync (Csync) signals or embedded Sync-on-Green (SOG), Hsync includes equalization pulses or other distortions during Vsync. To avoid upsetting the clock generator during Vsync, it is important to ignore these distortions. If the pixel clock PLL sees extraneous pulses, it will attempt to lock to this new frequency and will have changed frequency by the end of the Vsync period. It will then take a few lines of correct Hsync timing to recover at the beginning of a new frame, resulting in a “tearing” of the image at the top of the display.

The COAST function is provided to eliminate this problem. It is an internally generated signal, created by the sync processing engine that disables the PLL input and allows the clock to free-run at its then-current frequency. The PLL can free-run for several lines without significant frequency drift.

# AD9882

## TIMING DIAGRAMS

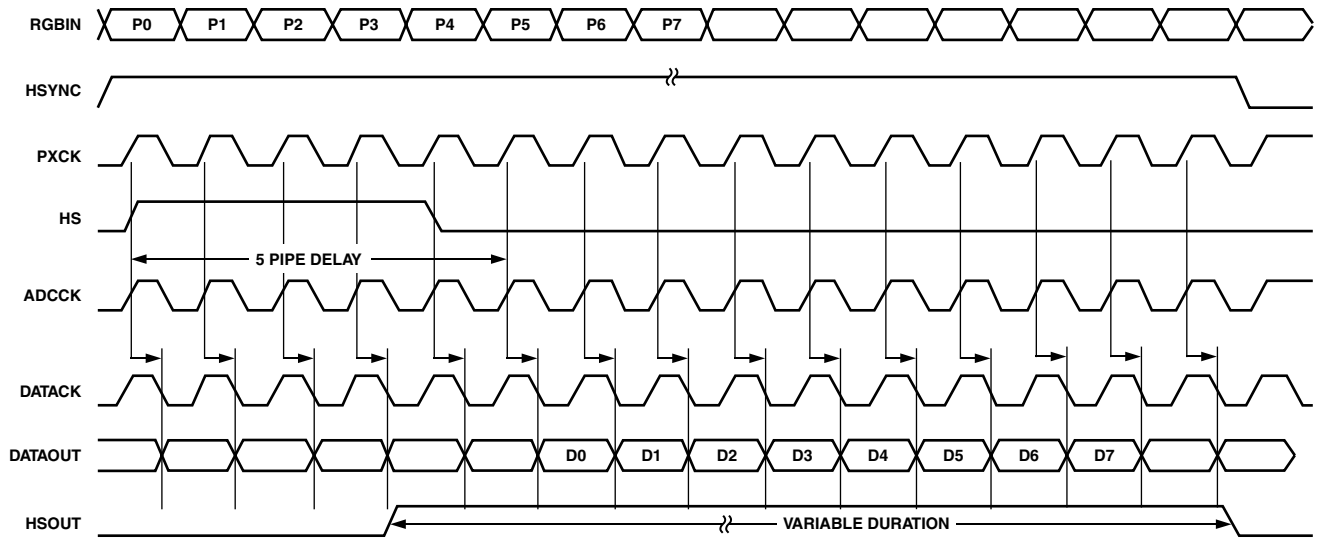


Figure 8. 4:4:4 Mode (for RGB and YPbPr)

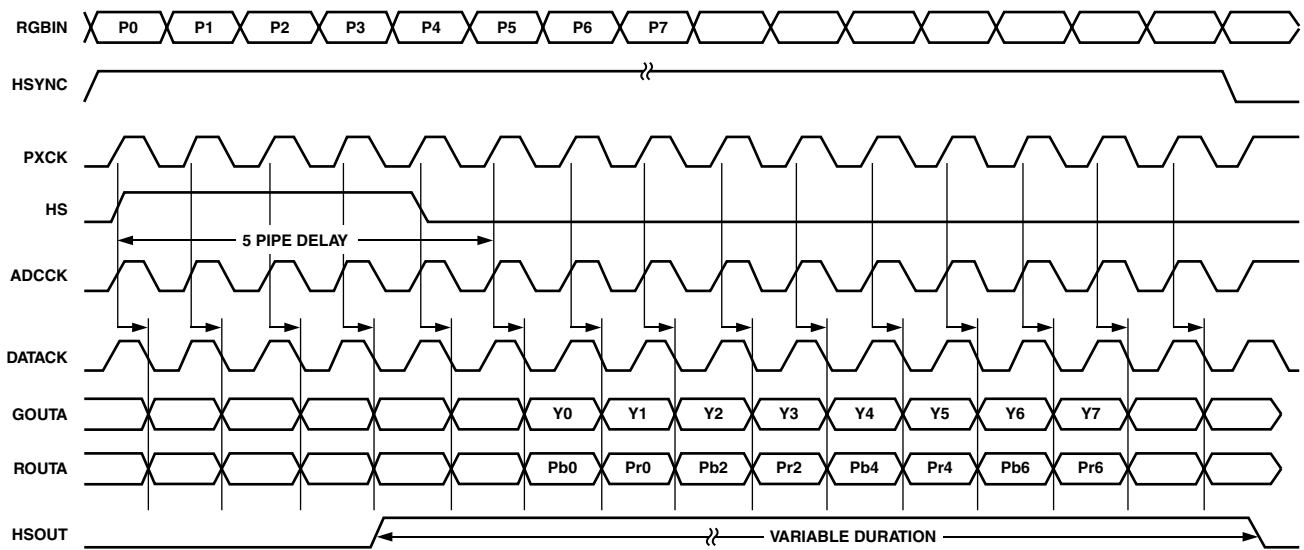


Figure 9. 4:2:2 Mode (for YPbPr Only)

Table VIII. Digital Interface Pin List

Pin Type	Mnemonic	Function	Value	Pin Number
Digital Video Data Inputs	R <sub>X0+</sub>	Digital Input Channel 0 True		33
	R <sub>X0-</sub>	Digital Input Channel 0 Complement		32
	R <sub>X1+</sub>	Digital Input Channel 1 True		36
	R <sub>X1-</sub>	Digital Input Channel 1 Complement		35
	R <sub>X2+</sub>	Digital Input Channel 2 True		39
	R <sub>X2-</sub>	Digital Input Channel 2 Complement		38
Digital Video Clock Inputs	R <sub>XC+</sub>	Digital Data Clock True		41
	R <sub>XC-</sub>	Digital Data Clock Complement		42
Termination Control	R <sub>TERM</sub>	Control Pin for Setting the Internal Termination Resistance		28
Outputs	DE	Data Enable	3.3 V CMOS	86
	HSOUT	Hsync Output	3.3 V CMOS	88
	VSOUT	Vsync Output	3.3 V CMOS	87
	CTL0, CTL1, CTL2, CTL3	Decoded Control Bit Outputs	3.3 V CMOS	22–25
HDCP	DDCSCL	HDCP Slave Serial Port Data Clock	3.3 V CMOS	53
	DDCSDA	HDCP Slave Serial Port Data I/O	3.3 V CMOS	54
	MCL	HDCP Master Serial Port Data Clock	3.3 V CMOS	81
	MDA	HDCP Master Serial Port Data I/O	3.3 V CMOS	82
Power Supply	V <sub>D</sub>	Main Power Supply	3.15 V to 3.45 V	
	PV <sub>D</sub>	PLL Power Supply	3.15 V to 3.45 V	
	V <sub>DD</sub>	Output Power Supply	2.2 V to 3.6 V	
	GND	Ground Supply	0 V	

**DIGITAL INTERFACE PIN DESCRIPTIONS****DIGITAL DATA INPUTS**

R <sub>X0+</sub>	Positive Differential Input Data (Channel 0)
R <sub>X0-</sub>	Negative Differential Input Data (Channel 0)
R <sub>X1+</sub>	Positive Differential Input Data (Channel 1)
R <sub>X1-</sub>	Negative Differential Input Data (Channel 1)
R <sub>X2+</sub>	Positive Differential Input Data (Channel 2)
R <sub>X2-</sub>	Negative Differential Input Data (Channel 2)

These six pins receive three pairs of differential, low voltage swing input pixel data from a DVI transmitter.

**DIGITAL CLOCK INPUTS**

R <sub>XC+</sub>	Positive Differential Input Clock
R <sub>XC-</sub>	Negative Differential Input Clock

These two pins receive the differential, low voltage swing input pixel clock from a DVI transmitter.

**TERMINATION CONTROL**

R <sub>TERM</sub>	<b>Internal Termination Set Pin</b> This pin is used to set the termination resistance for all of the digital interface high speed inputs. To set, place a resistor of value equal to 10× the desired input termination resistance between this pin (Pin 28) and ground supply. Typically, the value of this resistor should be 500 Ω.
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**OUTPUTS**

<b>DE</b>	<b>Data Enable Output</b> This pin outputs the state of data enable (DE). The AD9882 decodes DE from the incoming stream of data. The DE signal will be HIGH during active video and will be LOW while there is no active video.
<b>DDCSCL</b>	<b>HDCP Slave Serial Port Data Clock</b> For use in communicating with the HDCP enabled DVI transmitter.
<b>DDCSDA</b>	<b>HDCP Slave Serial Port I/O</b> For use in communicating with the HDCP enabled DVI transmitter.
<b>MCL</b>	<b>HDCP Master Serial Port Data Clock</b> Connects to the EEPROM for reading the encrypted HDCP keys.
<b>MDA</b>	<b>HDCP Master Serial Port Data I/O</b> Connects to the EEPROM for reading the encrypted HDCP keys.
<b>CTL</b>	<b>Digital Control Outputs</b> These pins output the control signals for the Red and Green channels. CTL0 and CTL1 correspond to the Red channel's input, while CTL2 and CTL3 correspond to the Green channel's input.

# AD9882

## POWER SUPPLY

<b>V<sub>D</sub></b>	<b>Main Power Supply</b> It should be as quiet as possible.
<b>PV<sub>D</sub></b>	<b>PLL Power Supply</b> It should be as quiet as possible.
<b>V<sub>DD</sub></b>	<b>Outputs Power Supply</b> The power for the data and clock outputs. It can run at 3.3 V or 2.5 V.
<b>GND</b>	<b>Ground</b> The ground return for all circuitry on the device. It is recommended that the application circuit board have a single, solid ground plane.

## THEORY OF OPERATION (DIGITAL INTERFACE)

### Capturing of the Encoded Data

The first step in recovering the encoded data is to capture the raw data. To accomplish this, the AD9882 employs a high speed phase locked loop (PLL) to generate clocks capable of oversampling the data at the correct frequency. The data capture circuitry continuously monitors the incoming data during horizontal and vertical blanking times (when DE is low) and selects the best sampling phase for each data channel independently. The phase information is stored and used until the next blanking period (one video line).

### Data Frames

The digital interface data is captured in groups of 10 bits each, which are called data frames. During the active data period, each frame is made up of the nine encoded video data bits and one dc balancing bit. The data capture block receives this data serially but outputs each frame in parallel 10-bit words.

### Special Characters

During periods of horizontal or vertical blanking time (when DE is low), the digital transmitter will transmit special characters. The AD9882 will receive these characters and use them to set the video frame boundaries and the phase recovery loop for each channel. There are four special characters that can be received. They are used to identify the top, bottom, left side, and right side of each video frame. The data receiver can differentiate these special characters from active data because the special characters have a different number of transitions per data frame.

### Channel Resynchronization

The purpose of the channel resynchronization block is to resynchronize the three data channels to a single internal data clock. Coming into this block, all three data channels can be on different phases of the 3× oversampling PLL clock (0°, 120°, and 240°). This block can resynchronize the channels from a worst-case skew of one full input period (8.93 ns at 112 MHz).

## Data Decoder

The data decoder receives frames of data and sync signals from the data capture block (in 10-bit parallel words) and decodes them into groups of eight RGB bits, two control bits, and a data enable bit (DE).

## HDCP

The AD9882 contains all the circuitry necessary for decryption of a high bandwidth digital content protection encoded DVI video stream. A typical HDCP implementation is shown in Figure 10. Several features of the AD9882 make this possible and add functionality to ease the implementation of HDCP.

The basic components of HDCP are included in the AD9882. A slave serial bus connects to the DDC clock and DDC data pins on the DVI connector to allow the HDCP enabled DVI transmitter to coordinate the HDCP algorithm with the AD9882. A second serial port (MDA/MCL) allows the AD9882 to read the HDCP keys and key selection vector (KSV) stored in an external serial EEPROM. When transmitting encrypted video, the DVI transmitter enables HDCP through the DDC port. The AD9882 then decodes the DVI stream using information provided by the transmitter, HDCP keys, and KSV.

The AD9882 allows the MDA and MCL pins to be three-stated using the MDA/MCL three-state bit (Register 1B, Bit 7) in the configuration registers. The three-state feature allows the EEPROM to be programmed in-circuit. The MDA/MCL port must be three-stated before attempting to program the EEPROM using an external master. The keys will be stored in an I<sup>2</sup>C compatible 3.3 V serial EEPROM of at least 512 bytes in size. The EEPROM should have a device address of A0H.

Proprietary software licensed from Analog Devices encrypts the keys and creates properly formatted EEPROM images for use in a production environment. Encrypting the keys helps maintain the confidentiality of the HDCP keys as required by the HDCP v1.0 specification. The AD9882 includes hardware for decrypting the keys in the external EEPROM.

ADI will provide a royalty free license for the proprietary software needed by customers to encrypt the keys between the AD9882 and the EEPROM only after customers provide evidence of a completed HDCP Adopter's license agreement and sign ADI's software license agreement. The Adopter's license agreement is maintained by Digital Content Protection, LLC, and can be downloaded from [www.digital-cp.com](http://www.digital-cp.com). To obtain ADI's software license agreement, contact the Display Electronics Product Line directly by sending an email to [flatpanel\\_apps@analog.com](mailto:flatpanel_apps@analog.com).

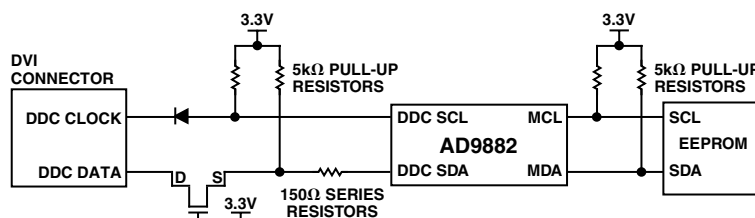


Figure 10. HDCP Implementation Using the AD9882

GENERAL TIMING DIAGRAMS (DIGITAL INTERFACE)

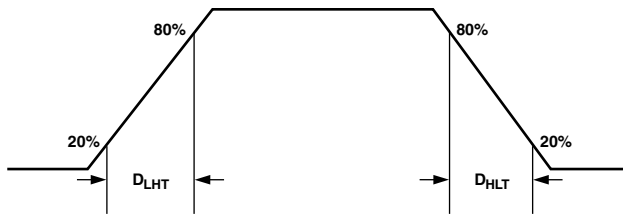


Figure 11. Digital Output Rise and Fall Times

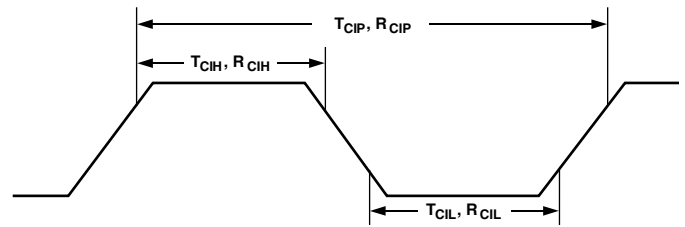


Figure 12. Clock Cycle/High/Low Times

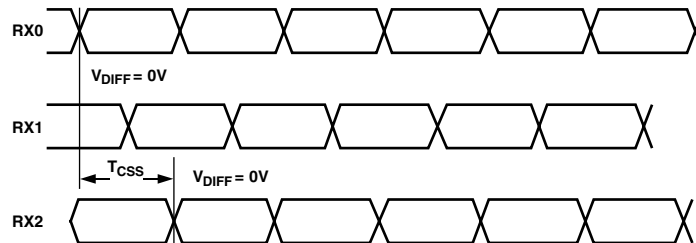


Figure 13. Channel-to-Channel Skew Timing

TIMING MODE DIAGRAMS (DIGITAL INTERFACE)

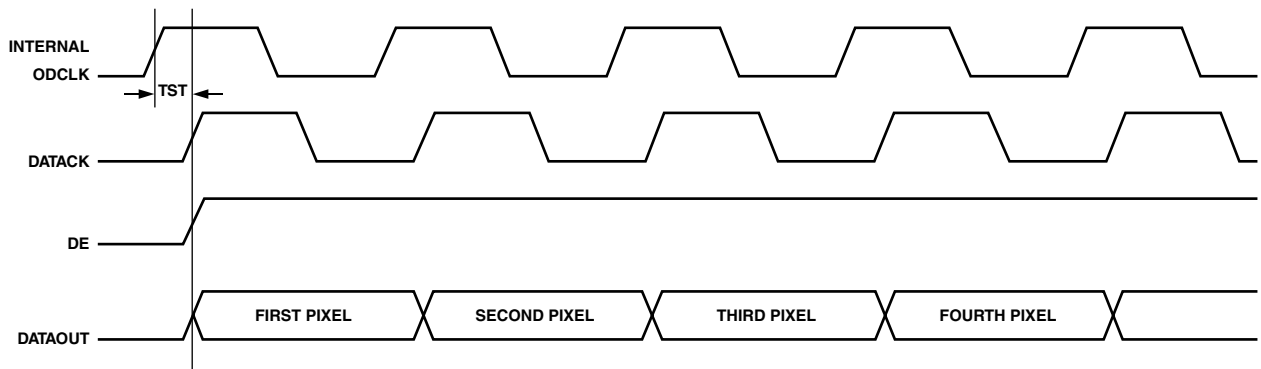


Figure 14. DVI CLK Invert = 1 (Register 14, Bit 4)

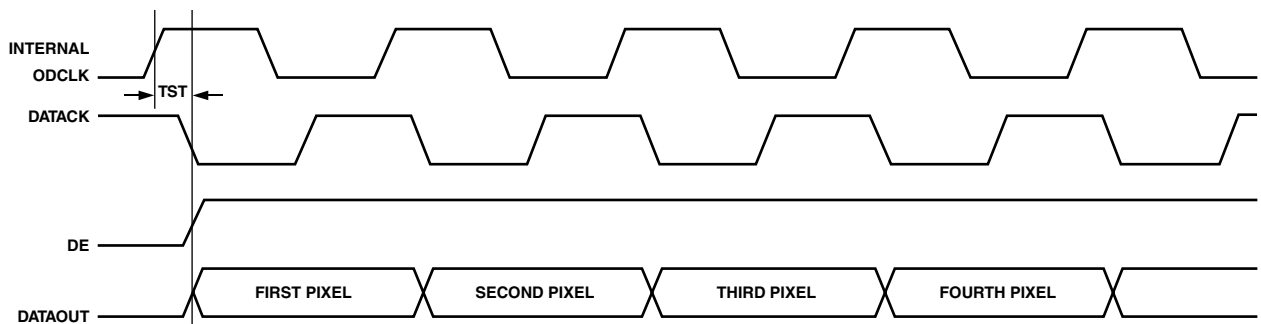


Figure 15. DVI CLK Invert = 0 (Register 14, Bit 4)

# AD9882

## 2-WIRE SERIAL REGISTER MAP

The AD9882 is initialized and controlled by a set of registers that determines the operating modes. An external controller is employed to write and read the Control Registers through the 2-wire serial interface port.

**Table IX. Control Register Map**

Hex Address	Read and Write or Read Only	Bit	Default Value	Register Name	Function
00	RO	7–0		Chip Revisions	An 8-bit register that represents the silicon level. Revision 0 = 0000 0000
01	R/W	7–0	0110 1001	PLL Div MSB	This register is for Bits [11:4] of the PLL divider. Larger values mean the PLL operates at a faster rate. This register should be loaded first whenever a change is needed. (This will give the PLL more time to lock.) <sup>1</sup>
02	R/W	7–4	1101 ****	PLL Div LSB	Bits [3:0] LSBs of the PLL divider word. Links to PLL MSB to make a 12-bit register. <sup>1</sup>
03	R/W	7–6 5–3	01** **** **00 1***	VCO Range Charge Pump	Selects VCO frequency range. Varies the current that drives the PLL loop filter.
04	R/W	7–3	1000 0***	Phase Adjust	ADC clock phase adjustment. Larger values mean more delay (1 LSB = T/32).
05	R/W	7–0	0000 1000	Clamp Placement	Places the clamp signal an integer number of clock periods after the trailing edge of Hsync.
06	R/W	7–0	0001 0100	Clamp Duration	Number of clock periods that the clamp signal is actively clamping.
07	R/W	7–0	0010 0000	Hsync Output Pulsewidth	Sets the number of pixel clocks that HSOUT will remain active.
08	R/W	7–0	1000 0000	Red Gain	Controls the ADC input range (contrast) of the red channel. Larger values give less contrast.
09	R/W	7–0	1000 0000	Green Gain	Controls the ADC input range (contrast) of the green channel. Larger values give less contrast.
0A	R/W	7–0	1000 0000	Blue Gain	Controls the ADC input range (contrast) of the blue channel. Larger values give less contrast.
0B	R/W	7–1	1000 000*	Red Offset	Controls the dc offset (brightness) of the red channel. Larger values decrease brightness.
0C	R/W	7–1	1000 000*	Green Offset	Controls the dc offset (brightness) of the green channel. Larger values decrease brightness.
0D	R/W	7–1	1000 000*	Blue Offset	Controls the dc offset (brightness) of the blue channel. Larger values decrease brightness.
0E	R/W	7–0	0010 0000	Sync Separator Threshold	Sets how many pixel clocks to count before toggling high or low. This should be set to some number greater than the maximum Hsync or equalization pulsewidth.
0F	R/W	7–3 2 1	0111 1*** **** *0** **** **0*	Sync-On-Green Threshold Active Interface Override Active Interface Select	Sets the voltage level of the Sync-on-Green slicer's comparator. 0 = No override 1 = User overrides, interface set by 0FH, Bit 1 0 = Analog interface active 1 = Digital interface active This interface is selected only if Register 0FH, Bit 2 is set to 1, or if both interfaces are active.

NOTE

<sup>1</sup>The AD9882 only updates the PLL divide ratio when the LSBs are written to Register 02H.

Table IX. Control Register Map (continued)

Hex Address	Read and Write or Read Only	Bit	Default Value	Register Name	Function
10	R/W	7	0*** ****	Hsync Polarity Override	0 = Polarity determined by chip 1 = Polarity set by 10H, Bit 6
		6	*1** ****	Input Hsync Polarity	0 = Active low polarity 1 = Active high polarity
		5	**0* ****	Output Hsync Polarity	0 = Active high sync signal 1 = Active low sync signal
		4	***0 ****	Active Hsync Override	0 = No override 1 = User overrides, analog Hsync set by 10H, Bit 3
		3	**** 0***	Active Hsync Select	0 = Analog Hsync from the Hsync input pin 1 = Analog Hsync from SOG This bit is used if Register 10H, Bit 4 is set to 1 or if both syncs are active.
		2	**** *0**	Output Vsync Polarity	0 = Invert 1 = Not inverted
		1	**** **0*	Active Vsync Override	0 = No override 1 = User overrides, analog Vsync set by 10H, Bit 0
		0	**** ***0	Active Vsync Select	0 = Analog Vsync from the Vsync input pin 1 = Analog Vsync from sync separator
11	R/W	7	0*** ****	Clamp Function	0 = Clamping with internal clamp 1 = Clamping disabled
		6	*0** ****	Red Clamp Select	0 = Clamp to ground 1 = Clamp to midscale for red channel
		5	**0* ****	Green Clamp Select	0 = Clamp to ground 1 = Clamp to midscale for green channel
		4	***0 ****	Blue Clamp Select	0 = Clamp to ground 1 = Clamp to midscale for blue channel
		3	**** 1***	Coast Select	0 = Disabled coast 1 = Coasting with internally generated coast signal
		2	**** *0**	Coast Polarity Override	0 = Coast polarity determined by the chip 1 = Coast polarity set by 11H, Bit 1
		1	**** **1*	Input Coast Polarity	This bit must be set to 1 to disable coast. 0 = Active low coast signal 1 = Active high coast signal This bit must be set to 1 to disable coast.
12	R/W	7-0	0000 0000	Pre-Coast	Number of Hsync periods that coast goes active prior to Vsync.
13	R/W	7-0	0000 0000	Post-Coast	Number of Hsync periods before coast goes inactive following Vsync.
14	R/W	7-6	11** ****	Output Drive Select	Selects among high, medium, and low output drive strength.
		5	**1* ****	Programmable Bandwidth	0 = Low bandwidth of 10 MHz 1 = High bandwidth of 300 MHz
		4	***0 ****	DVI Clock Invert	0 = DVI data clock output not inverted 1 = DVI data clock output inverted For digital interface only.
		3	**** 0***	DVI PDO Three-State	0 = Normal outputs 1 = High impedance outputs
		2	**** *0**	HDCP Address	Address Bit 0 = 0 for HDCP Slave Port Address Bit 1 = 1 for HDCP Slave Port
1	**** **1*	Power-Down	0 = Full chip power-down		

Table IX. Control Register Map (continued)

Hex Address	Read and Write or Read Only	Bit	Default Value	Register Name	Function
14	R/W	0	**** **0	Enable 4:2:2	0 = 4:4:4 mode 1 = 4:2:2 mode
15	RO	7		Analog Hsync Active	0 = Hsync not detected 1 = Hsync detected
		6		Analog SOG Active	0 = Sync signal not detected on green channel 1 = Sync signal detected on green channel
		5		Analog Vsync Active	0 = Vsync not detected 1 = Vsync detected
		4		DVI Active	0 = Digital interface clock not detected 1 = Digital interface clock detected
		3		Active Interface	0 = Analog interface active 1 = DVI interface active
16	RO	7		Active Hsync	0 = Hsync from the Hsync input pin 1 = Hsync from the SOG input
		6		Hsync Polarity Detected	0 = Active low polarity detected 1 = Active high polarity detected
		5		Active Vsync	0 = Vsync from the Vsync input pin 1 = Vsync from SOG
		4		Vsync Polarity Detected	0 = Active high polarity detected 1 = Active low polarity detected
		3		Coast Polarity Detected	0 = Active low polarity detected 1 = Active high polarity detected
		2		HDCP Keys Detected	This function works only with internal coast. 0 = Not detected 1 = Detected
17	R/W	7-0	0000 0000	Test Register	Must be set to 1000 0000 for proper operation.
18	R/W	7-0	0000 000X	Test Register	Must be set to 1100 000x for proper operation.
19	R/W	7-0	0000 010X	Test Register	Must be set to 0111 110x for proper operation.
1A	R/W	7-0	0011 1111	Test Register	Must be set to default for proper operation.
1B	R/W	7	1*** **	MDA and MCL	0 = MDA and MCL three-stated 1 = MDA and MCL not three-stated
		6-0	*111 0000	Test Register	Must be set to *110 0111 for proper operation.
1C	R/W	7-0	0000 1111	Test Register	Must be set to default for proper operation.
1D	RO	7-0		Test Register	Reserved for future use.
1E	RO	7-0		Test Register	Reserved for future use.



**2-WIRE SERIAL CONTROL REGISTER DETAIL****CHIP IDENTIFICATION****00 7-0 Chip Revision**

An 8-bit register that represents the silicon revision. Revision 0 = 0000 0000.

**PLL DIVIDER CONTROL****01 7-0 PLL Divide Ratio MSBs**

The eight most significant bits of the 12-bit PLL divide ratio PLLDIV. (The operational divide ratio is PLLDIV + 1.)

The PLL derives a pixel clock from the incoming Hsync signal. The pixel clock frequency is then divided by an integer value, such that the output is phase-locked to Hsync. This PLLDIV value determines the number of pixel times (pixels plus horizontal blanking overhead) per line. This is typically 20% to 30% more than the number of active pixels in the display.

The 12-bit value of the PLL divider supports divide ratios from 221 to 4095. The higher the value loaded in this register, the higher the resulting clock frequency with respect to a fixed Hsync frequency.

VESA has established some standard timing specifications that will assist in determining the value for PLLDIV as a function of the horizontal and vertical display resolution and frame rate (Table VII). However, many computer systems do not conform precisely to the recommendations, and these numbers should be used only as a guide. The display system manufacturer should provide automatic or manual means for optimizing PLLDIV. An incorrectly set PLLDIV will usually produce one or more vertical noise bars on the display. The greater the error, the greater the number of bars produced.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 69H, PLLDIVL = DxH).

The AD9882 updates the full divide ratio only when the LSBs are changed. Writing to this register by itself will not trigger an update.

**02 7-4 PLL Divide Ratio LSBs**

The four least significant bits of the 12-bit PLL divide ratio PLLDIV. The operational divide ratio is PLLDIV + 1.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 69H, PLLDIVL = DxH).

The AD9882 updates the full divide ratio only when this register is written.

**03 7-6 VCO Range Select**

Two bits that establish the operating range of the clock generator.

VCORNGE must be set to correspond with the desired operating frequency (incoming pixel rate).

The PLL VCO gives the best jitter performance while operating at high frequencies. For this reason, in order to output low pixel rates and still get good jitter performance, the PLL VCO actually operates at a higher frequency but then divides down the clock rate afterward. Table X shows the pixel rates for each VCO range setting. The PLL output divisor is automatically selected with the VCO range setting.

**Table X. VCO Ranges**

VCORNGE	Pixel Rate Range
00	12-41
01	41-82
10	82-140

The power-up default value is VCORNGE = 01.

**03 5-3 CURRENT Charge Pump Current**

Three bits that establish the current driving the loop filter in the clock generator.

**Table XI. Charge Pump Currents**

Charge Pump	Current ( $\mu$ A)
000	50
001	100
010	150
011	250
100	350
101	500
110	750
111	1500

CHARGE PUMP must be set to correspond with the desired operating frequency (incoming pixel rate). See Table XI for the charge pump current for each register setting.

The power-up default value is CURRENT = 001.

**04 7-3 Phase Adjust**

A 5-bit value that adjusts the sampling phase in 32 steps across one pixel time. Each step represents an 11.25° shift in sampling phase.

The power-up default Phase adjust value is 10H.

**CLAMP TIMING****05 7-0 Clamp Placement**

An 8-bit register that sets the position of the internally generated clamp.

When CLAMP FUNCTION (Register 11H, Bit 7) = 0, a clamp signal is generated internally at a position established by the clamp placement and for a duration set by the clamp duration. Clamping is started (Clamp Placement) an integral number of pixel periods after the trailing edge of Hsync. The clamp placement may be programmed to any value between 1 and 255.

The clamp should be placed during a time that the input signal presents a stable black-level reference, usually the back porch period between Hsync and the image.

When CLAMP FUNCTION = 1, this register is ignored.

**06 7-0 Clamp Duration**

An 8-bit register that sets the duration of the internally generated clamp.

For the best results, the clamp duration should be set to include the majority of the black reference signal time that follows the Hsync signal trailing edge. Insufficient clamping time can produce brightness changes at the top of the screen and a slow recovery from large changes in the Average Picture Level (APL) or brightness.

When CLAMP FUNCTION = 1, this register is ignored.

# AD9882

## HSYNC OUTPUT PULSEWIDTH

### 07 7-0 Hsync Output Pulsewidth

An 8-bit register that sets the duration of the Hsync output pulse.

The leading edge of the Hsync output is triggered by the internally generated, phase adjusted PLL feedback clock. The AD9882 then counts a number of pixel clocks equal to the value in this register minus one. This triggers the trailing edge of the Hsync output, which is also phase adjusted.

## INPUT GAIN

### 08 7-0 REDGAIN RED Gain

An 8-bit word that sets the gain of the RED channel. The AD9882 can accommodate input signals with a full-scale range of between 0.5 V and 1.0 V p-p. Setting REDGAIN to 255 corresponds to an input range of 1.0 V. A REDGAIN of 0 establishes an input range of 0.5 V. Note that INCREASING REDGAIN results in the picture having LESS CONTRAST (the input signal uses fewer of the available converter codes). See Figure 2.

### 09 7-0 GREENGAIN GREEN Gain

An 8-bit word that sets the gain of the GREEN channel. See REDGAIN (08).

### 0A 7-0 BLUEGAIN BLUE Gain

An 8-bit word that sets the gain of the BLUE channel. See REDGAIN (08).

## INPUT OFFSET

### 0B 7-1 RED Channel Offset Adjust

A 7-bit offset binary word that sets the dc offset of the RED channel. One LSB of offset adjustment equals approximately one LSB change in the ADC offset. Therefore, the absolute magnitude of the offset adjustment scales as the gain of the channel is changed. A nominal setting of 64 results in the channel nominally clamping the back porch (during the clamping interval) to code 00. An offset setting of 127 results in the channel clamping to code 63 of the ADC. An offset setting of 0 clamps to code -64 (off the bottom of the range). Increasing the value of RED offset DECREASES the brightness of the channel.

### 0C 7-1 GREEN Channel Offset Adjust

A 7-bit offset binary word that sets the dc offset of the GREEN channel. See REDOFST (0B).

### 0D 7-1 BLUE Channel Offset Adjust

A 7-bit offset binary word that sets the dc offset of the BLUE channel. See REDOFST (0B).

### 0E 7-0 Sync Separator Threshold

This register is used to set the responsiveness of the sync separator. It sets how many internal 5 MHz clock periods the sync separator must count to before toggling high or low. It works like a low-pass filter to ignore Hsync pulses in order to extract the Vsync signal. This register should be set to some number greater than the maximum Hsync pulsewidth. Note: the sync separator threshold uses an internal dedicated clock with a frequency of approximately 5 MHz.

The default for this register is 20H.

### 0F 7-3 Sync-on-Green Slicer Threshold

This register allows the comparator threshold of the Sync-on-Green slicer to be adjusted. This register adjusts it in steps of 10 mV, with the minimum setting equaling 10 mV and the maximum setting equaling 330 mV.

The default setting is 15 decimal and corresponds to a threshold value of 170 mV.

### 0F 2 AIO Active Interface Override

This bit is used to override the automatic interface selection (Bit 3 in Register 15H). To override, set this bit to logic 1. When overriding, the active interface is set via Bit 1 in this register.

Table XII. Active Interface Override Settings

AIO	Result
0	Autodetermine the active interface.
1	Override, Bit 1 determines the active interface.

The default for this register is 0.

### 0F 1 AIS Active Interface Select

This bit is used under two conditions. It is used to select the active interface when the override bit is set (Register 0FH, Bit 2). Alternatively, it is used to determine the active interface when not overriding but both interfaces are detected.

Table XIII. Active Interface Select Settings

AIS	Result
0	Analog interface
1	Digital interface

The default for this register is 0.

### 10 7 Hsync Input Polarity Override

This register is used to override the internal circuitry that determines the polarity of the Hsync signal going into the PLL.

Table XIV. Hsync Input Polarity Override Settings

Override Bit	Result
0	Hsync polarity determined by chip.
1	Hsync polarity determined by Register 10H, Bit 6.

The default for Hsync polarity override is 0. (Polarity determined by chip.)

### 10 6 HSPOL Hsync Input Polarity

A bit that must be set to indicate the polarity of the Hsync signal that is applied to the PLL Hsync input.

Table XV. Hsync Input Polarity Settings

HSPOL	Function
0	Active LOW
1	Active HIGH

Active LOW means the leading edge of the Hsync pulse is negative-going. All timing is based on the leading edge of Hsync, which is the FALLING edge. The rising edge has no effect.

Active HIGH means the leading edge of the Hsync pulse is positive-going. This means that timing will be based on the leading edge of Hsync, which is now the RISING edge.

The device will operate if this bit is set incorrectly, but the internally generated clamp position, as established by Clamp Placement (Register 05H), will not be placed as expected, which may generate clamping errors.

The power-up default value is HSPOL = 1.

#### 10 5 Hsync Output Polarity

One bit that determines the polarity of the Hsync output and the SOG output. Table XVI shows the effect of this option. SYNC indicates the logic state of the sync pulse.

**Table XVI. Hsync Output Polarity Settings**

Setting	SYNC
0	Logic 1 (positive polarity)
1	Logic 0 (negative polarity)

The default setting for this register is 0.

#### 10 4 Active Hsync Override

This bit is used to override the automatic Hsync selection. To override, set this bit to logic 1. When overriding, the active Hsync is set via Bit 3 in this register.

**Table XVII. Active Hsync Override Settings**

Override	Result
0	Autodetermine the active Hsync.
1	Override. Bit 3 determines the active Hsync.

The default for this register is 0.

#### 10 3 Active Hsync Select

This bit is used under two conditions. It is used to select the active Hsync when the override bit is set (Bit 4). Alternately, it is used to determine the active Hsync when not overriding, but both Hsyncs are detected.

**Table XVIII. Active Hsync Select Settings**

Select	Result
0	Hsync input
1	Sync-on-Green input

The default for this register is 0.

#### 10 2 Vsync Output Polarity

One bit that determines the polarity of the Vsync output. Table XIX shows the effect of this option. SYNC indicates the logic state of the sync pulse.

**Table XIX. Vsync Output Polarity Settings**

Setting	SYNC
1	Not invert
0	Invert

The default setting for this register is 0.

#### 10 1 Active Vsync Override

This bit is used to override the automatic Vsync selection. To override, set this bit to logic 1. When overriding, the active interface is set via Bit 0 in this register.

**Table XX. Active Vsync Override Settings**

Override	Result
0	Autodetermine the active Vsync
1	Override. Bit 0 determines the active Vsync.

The default for this register is 0.

#### 10 0 Active Vsync Select

This bit is used to select the active Vsync when the override bit is set (Bit 1).

**Table XXI. Active Vsync Select Settings**

Select	Result
0	Vsync input
1	Sync separator output

The default for this register is 0.

#### 11 7 Clamp Function

A bit that enables/disables clamping.

**Table XXII. Clamp Input Signal Source Settings**

Clamp Function	Function
0	Internally generated clamp enabled
1	Clamping disabled

A 0 enables the clamp timing circuitry controlled by clamp placement and clamp duration. The clamp position and duration is counted from the trailing edge of Hsync.

A 1 disables clamping. The three channels are clamped when the CLAMP signal is active.

Power-up default value is CLAMP FUNCTION = 0.

#### 11 6 RED Clamp Select

A bit that determines whether the RED channel is clamped to ground or to midscale. For RGB video, all three channels are referenced to ground. For YPbPr, the Y channel is referenced to ground, but the PbPr channels are referenced to midscale. Clamping to midscale actually clamps to Pin 74.

**Table XXIII. RED Clamp Select Settings**

Clamp	Function
0	Clamp to ground
1	Clamp to midscale (Pin 74)

The default setting for this register is 0.

# AD9882

## 11 5 GREEN Clamp Select

A bit that determines whether the GREEN channel is clamped to ground or to midscale.

**Table XXIV. GREEN Clamp Select Settings**

Clamp	Function
0	Clamp to ground
1	Clamp to midscale (Pin 74)

The default setting for this register is 0.

## 11 4 BLUE Clamp Select

A bit that determines whether the BLUE channel is clamped to ground or to midscale.

**Table XXV. BLUE Clamp Select Settings**

Clamp	Function
0	Clamp to ground
1	Clamp to midscale (Pin 74)

The default setting for this register is 0.

## 11 3 Coast Select

This bit is used to enable or disable the coast signal. If coast is enabled, the additional decision of using the Vsync input pin or the output from the sync separator needs to be made (Register 10H, Bits 1, 0). To disable coast, the user must set Register 11H, Bit 2 to 1 and 11H, Bit 1 to 1.

**Table XXVI. Coast Enable Settings**

Select	Result
0	Coast disabled
1	Internally generated coast signal

The default for this register is 1.

## 11 2 Coast Input Polarity Override

This register is used to override the internal circuitry that determines the polarity of the coast signal going into the PLL. When disabling coast, Register 11, Bit 2 must be set to 1 and Register 11H, Bit 1 must be set to 1. This register only works when Coast is disabled. It does not work with internal Coast.

**Table XXVII. Coast Input Polarity Override Settings**

Override Bit	Result
0	Coast polarity determined by chip
1	Coast polarity determined by user

The default for coast polarity override is 0.

## 11 1 Coast Input Polarity

A bit to indicate the polarity of the coast signal that is applied to the PLL coast input.

This register can only be used when coast is disabled and Register 11H, Bit 2 is set to 1.

**Table XXVIII. Coast Input Polarity Settings**

CSTPOL	Function
0	Active LOW
1	Active HIGH

The power-up default value is CSTPOL = 1.

## 12 7-0 Pre-Coast

This register allows the coast signal to be applied prior to the Vsync signal. This is necessary in cases where pre-equalization pulses are present. This register defines the number of edges that will be filtered before Vsync on a composite sync.

The default is 0.

## 13 7-0 Post-Coast

This register allows the coast signal to be applied following the Vsync signal. This is necessary in cases where post-equalization pulses are present. The step size for this control is one Hsync period. This register defines the number of edges that will be filtered after Vsync on a composite sync.

The default is 0.

## 14 7-6 Output Drive

The two bits select the drive strength for the high speed digital outputs (all data output and clock output pins). Higher drive strength results in faster rise/fall times, and in general makes it easier to capture data. Lower drive strength results in slower rise/fall times and helps reduce EMI and digitally generated power supply noise.

**Table XXIX. Output Drive Strength Settings**

Bit 7	Bit 6	Result
1	X	High drive strength
0	1	Medium drive strength
0	0	Low drive strength

The default for this register is 11, high drive strength. (This option works on both the analog and digital interfaces.)

## 14 5 Programmable Analog Bandwidth

Bits that select the analog bandwidth.

**Table XXX. Analog Bandwidth Control**

Bit 5	Analog Bandwidth
0	10 MHz
1	300 MHz

## 14 4 Clk Inv Data Output Clock Invert

A control bit for the inversion of the output data clock (Pin 85). This function works only for the digital interface. When not inverted, data is output on the falling edge of the data clock. See the timing diagrams, Figures 14 and 15, to see how this affects timing.

**Table XXXI. Clock Output Invert Settings**

Clk Inv	Function
0	Not inverted
1	Inverted

The default for this register is 0 (not inverted).

**14 3 PDO Power-Down Outputs**

A bit that can put the outputs in a high impedance mode. This applies to the 24 data output pins, HSOUT, VSOUT, and DE Pins.

**Table XXXII. Power-Down Output Settings**

PDO	Function
0	Normal operation
1	Three-state

The default for this register is 0. (This option works on both the analog and digital interfaces.)

**14 2 HDCP Address**

This bit is used to set the HDCP Slave Port address.

**Table XXXIII. HDCP Address Settings**

Address Bit	Result
0	0 for HDCP Slave Port
1	1 for HDCP Slave Port

The default for this register is 0.

**14 1 PWRDN**

This bit is used to control chip power-down. See the section on power management for details about which blocks are actually powered down.

**Table XXXIV. Power-Down Settings**

Select	Result
0	Power-down
1	Normal operation

The default for this register is 1.

**14 0 4:2:2 Output Mode Select**

A bit that configures the output data in 4:2:2 mode. This mode can be used to reduce the number of data lines used from 24 to 16 for applications using YPbPr graphics signals. A timing diagram for this mode is shown in Figure 9. Recommended input and output configurations are shown in Table XXXVI. In 4:2:2 mode, the RED and BLUE channels can be interchanged to help satisfy board layout or timing requirements, but the GREEN channel must be configured for Y.

**Table XXXV. 4:2:2 Output Mode Select**

Select	Output Mode
0	4:4:4
1	4:2:2

**Table XXXVI. 4:2:2 Input/Output Configuration**

Channel	Input Connection	Output Format
RED	Pr	Pb/Pr
GREEN	Y	Y
BLUE	Pr	High impedance

**15 7 Hsync Detect**

This bit is used to indicate when activity is detected on the Hsync input pin (Pin 79). If Hsync is held high or low, activity will not be detected.

**Table XXXVII. Hsync Detection Results**

Detect	Function
0	No activity detected
1	Activity detected

The Sync Processing Block Diagram, Figure 18, shows where this function is implemented.

**15 6 Sync-on-Green Detect**

This bit is used to indicate when sync activity is detected on the Sync-on-Green input pin (Pin 64).

**Table XXXVIII. Sync-on-Green Detection Results**

Detect	Function
0	No activity detected
1	Activity detected

The Sync Processing Block Diagram, Figure 18, shows where this function is implemented.

Note: If no Sync signal is presented on the GREEN video input, normal video may still trigger activity.

**15 5 Vsync Detect**

This bit is used to indicate when activity is detected on the Vsync input pin (Pin 80). If Vsync is held high or low, activity will not be detected.

**Table XXXIX. Vsync Detection Results**

Detect	Function
0	No activity detected
1	Activity detected

The Sync Processing Block Diagram, Figure 18, shows where this function is implemented.

**15 4 Digital Interface Clock Detect**

This bit is used to indicate when activity is detected on the digital interface clock input.

**Table XL. Digital Interface Clock Detection Results**

Detect	Function
0	No activity detected
1	Activity detected

The Sync Processing Block Diagram, Figure 18, shows where this function is implemented.



## 15 3 Active Interface

This bit is used to indicate which interface should be active, analog or digital. It checks for activity on the analog interface and for activity on the digital interface, then determines which should be active according to Table XLII. Specifically, analog interface detection is determined by OR-ing Bits 7, 6, and 5 in this register. Digital interface detection is determined by Bit 4 in this register. If both interfaces are detected, the user can determine which has priority via Bit 1 in Register 0FH. The user can override this function via Bit 2 in Register 0FH. If the override bit is set to logic 1, then this bit will be forced to the same state as Bit 1 in Register 0FH.

**Table XLII. Active Interface Results**

Bits 7, 6, or 5 (Analog Detection)	Bit 4 (Digital Detection)	Override	AI
0	0	0	Soft Power-Down (Seek Mode)
0	1	0	1
1	0	0	0
1	1	0	Bit 1 in 0FH
X	X	1	Bit 1 in 0FH

AI = 0 means analog interface  
 AI = 1 means digital interface  
 The override bit is in Register 0FH, Bit 2.

## 16 7 AHS Active Hsync

This bit indicates which Hsync input source is being used by the PLL (Hsync input or Sync-on-Green). Bits 6 and 7 in Register 15H determine which source is used. If both Hsync and SOG are detected, the user can determine which has priority via Bit 3 in Register 10H. The user can override this function via Bit 4 in Register 10H. If the override bit is set to logic 1, then this bit will be forced to the same state as Bit 3 in Register 10H.

**Table XLIII. Active Hsync Results**

Hsync Detect Register 15H Bit 7	SOG Detect Register 15H Bit 6	Override Register 10H Bit 4	AHS Register 16H Bit 7
0	0	0	Bit 3 in 10H
0	1	0	1
1	0	0	0
1	1	0	Bit 3 in 10H
X	X	1	Bit 3 in 10H

AHS = 0 means use the Hsync pin input for Hsync  
 AHS = 1 means use the SOG pin input for Hsync  
 The override bit is in Register 10H, Bit 4.

## 16 6 Detected Hsync Input Polarity Status

This bit reports the status of the Hsync input polarity detection circuit. It can be used to determine the polarity of the Hsync input. The detection circuit's location is shown in the Sync Processing Block Diagram, Figure 18.

**Table XLIV. Detected Hsync Input Polarity Status**

Hsync Polarity Status	Result
0	Hsync polarity is negative/active low.
1	Hsync polarity is positive/active high.

## 16 5 AVS Active Vsync

This bit indicates which Vsync source is being used for the analog interface: the Vsync input or output from the sync separator. If the override bit (10H, Bit 1) is set to logic 1, then this bit will be forced to the same state as Bit 0 in Register 10H.

**Table XLV. Active Vsync Results**

Vsync Detect Register 16H Bit 5	Override Register 10H Bit 1	AVS
0	0	0
1	0	1
X	1	Bit 0 in 10H

AVS = 0 means Vsync input  
 AVS = 1 means Sync separator  
 The override bit is in Register 10H, Bit 1.

## 16 4 Detected Vsync Output Polarity Status

This bit reports the status of the Vsync output polarity detection circuit. It can be used to determine the polarity of the Vsync output. The detection circuit's location is shown in the Sync Processing Block Diagram, Figure 18.

**Table XLVI. Detected Vsync Input Polarity Status**

Vsync Polarity Status	Result
0	Vsync polarity is active high.
1	Vsync polarity is active low.

## 16 3 Detected Coast Polarity Status

This bit reports the status of the coast input polarity detection circuit. The detection circuit's location is shown in the Sync Processing Block Diagram, Figure 18. This bit only applies to the internal Coast and does not apply when Coast is disabled.

**Table XLVII. Detected Coast Input Polarity Status**

Hsync Polarity Status	Result
0	Coast polarity is negative/active low.
1	Coast polarity is positive/active high.

## 16 2 Key Read Verification

This bit reports wherever HDCP keys are detected.

**Table XLVIII. Key Read Verification**

Detect	Function
0	Not detected
1	Detected

## 1B 7 MDA and MCL Three-State

The MDA and MCL three-state feature allows the EEPROM to be programmed in-circuit. The MDA/MCL port must be three-stated before attempting to program the EEPROM using an external master. The keys will be stored in an I<sup>2</sup>C compatible 3.3 V serial EEPROM of at least 512 bytes. The EEPROM should have a device address of A0H.

## 2-WIRE SERIAL CONTROL PORT

A 2-wire serial control interface is provided. Two AD9882 devices may be connected to the 2-wire serial interface, with each device having a unique address.

The 2-wire serial interface comprises a clock (SCL) and a bidirectional data (SDA) pin. The analog flat panel interface acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled HIGH by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL is LOW. If SDA changes state while SCL is HIGH, the serial interface interprets that action as a start or stop sequence.

There are five components to serial bus operation:

- Start signal
- Slave address byte
- Base register address byte
- Data byte to read or write
- Stop signal

When the serial interface is inactive (SCL and SDA are HIGH), communications are initiated by sending a start signal. The start signal is a HIGH-to-LOW transition on SDA while SCL is HIGH. This signal alerts all slaved devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal comprise a 7-bit slave address (the first seven bits) and a single  $R/\overline{W}$  bit (the eighth bit). The  $R/\overline{W}$  bit indicates the direction of data transfer: read from (1) or write to (0) the slave device. If the transmitted slave address matches the address of the device (set by the state of the SA input pin in Table XLVIII), the AD9882 acknowledges by bringing SDA LOW on the ninth SCL pulse. If the addresses do not match, the AD9882 does not acknowledge.

**Table XLVIII. Serial Port Addresses**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
A6 (MSB)	A5	A4	A3	A2	A1	A0 (LSB)
1	0	0	1	1	0	0
1	0	0	1	1	0	1

## Data Transfer via Serial Interface

For each byte of data read or written, the MSB is the first bit of the sequence.

If the AD9882 does not acknowledge the master device during a write sequence, the SDA remains HIGH so the master can generate a stop signal. If the master device does not acknowledge the AD9882 during a read sequence, the AD9882 interprets this as “end of data.” The SDA remains HIGH so the master can generate a stop signal.

Writing data to specific control registers of the AD9882 requires that the 8-bit address of the control register of interest be written after the slave address has been established. This control register address is the base address for subsequent write operations. The base address autoincrements by one for each byte of data written after the data byte intended for the base address. If there are more bytes transferred than there are available addresses, the address will not increment and will remain at its maximum value of 1Eh. Any base address higher than 1Eh will not produce an acknowledge signal.

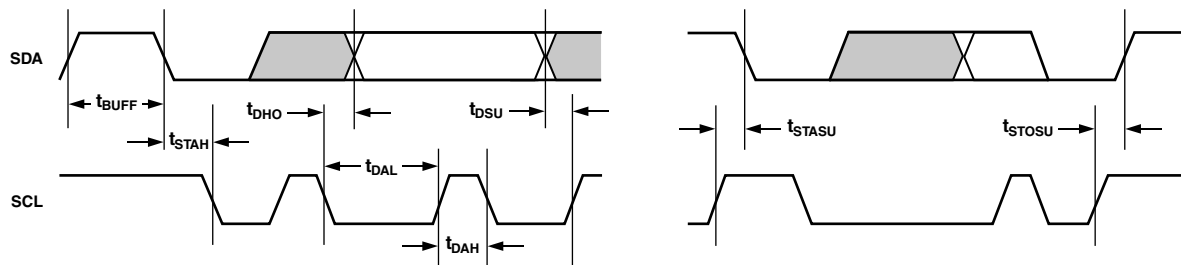
Data are read from the control registers of the AD9882 in a similar manner. Reading requires two data transfer operations:

The base address must be written with the  $R/\overline{W}$  bit of the slave address byte LOW to set up a sequential read operation.

Reading (the  $R/\overline{W}$  bit of the slave address byte HIGH) begins at the previously established base address. The address of the read register autoincrements after each byte is transferred.

To terminate a read/write sequence to the AD9882, a stop signal must be sent. A stop signal comprises a LOW-to-HIGH transition of SDA while SCL is HIGH. The timing for the read/write is shown in Figure 16, and a typical byte transfer is shown in Figure 17.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.



*Figure 16. Serial Port Read/Write Timing*

# AD9882

## Serial Interface Read/Write Examples

Write to one control register

- Start signal
- Slave address byte ( $R/\overline{W}$  bit = LOW)
- Base address byte
- Data byte to base address
- Stop signal

Write to four consecutive control registers

- Start signal
- Slave address byte ( $R/\overline{W}$  bit = LOW)
- Base address byte
- Data byte to base address
- Data byte to (base address + 1)
- Data byte to (base address + 2)
- Data byte to (base address + 3)
- Stop signal

Read from one control register

- Start signal
- Slave address byte ( $R/\overline{W}$  bit = LOW)
- Base address byte
- Start signal
- Slave address byte ( $R/\overline{W}$  bit = HIGH)
- Data byte from base address
- Stop signal

Read from four consecutive control registers

- Start signal
- Slave address byte ( $R/\overline{W}$  bit = LOW)
- Base address byte
- Start signal
- Slave address byte ( $R/\overline{W}$  bit = HIGH)
- Data byte from base address
- Data byte from (base address + 1)
- Data byte from (base address + 2)
- Data byte from (base address + 3)
- Stop signal

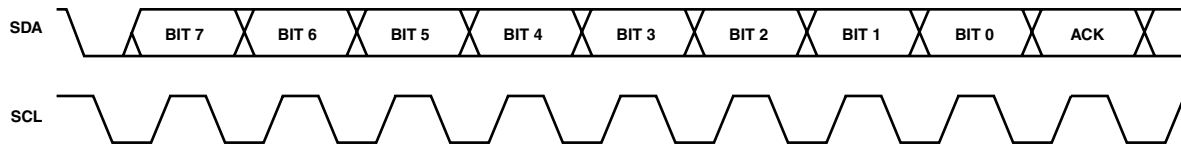


Figure 17. Serial Interface, Typical Byte Transfer



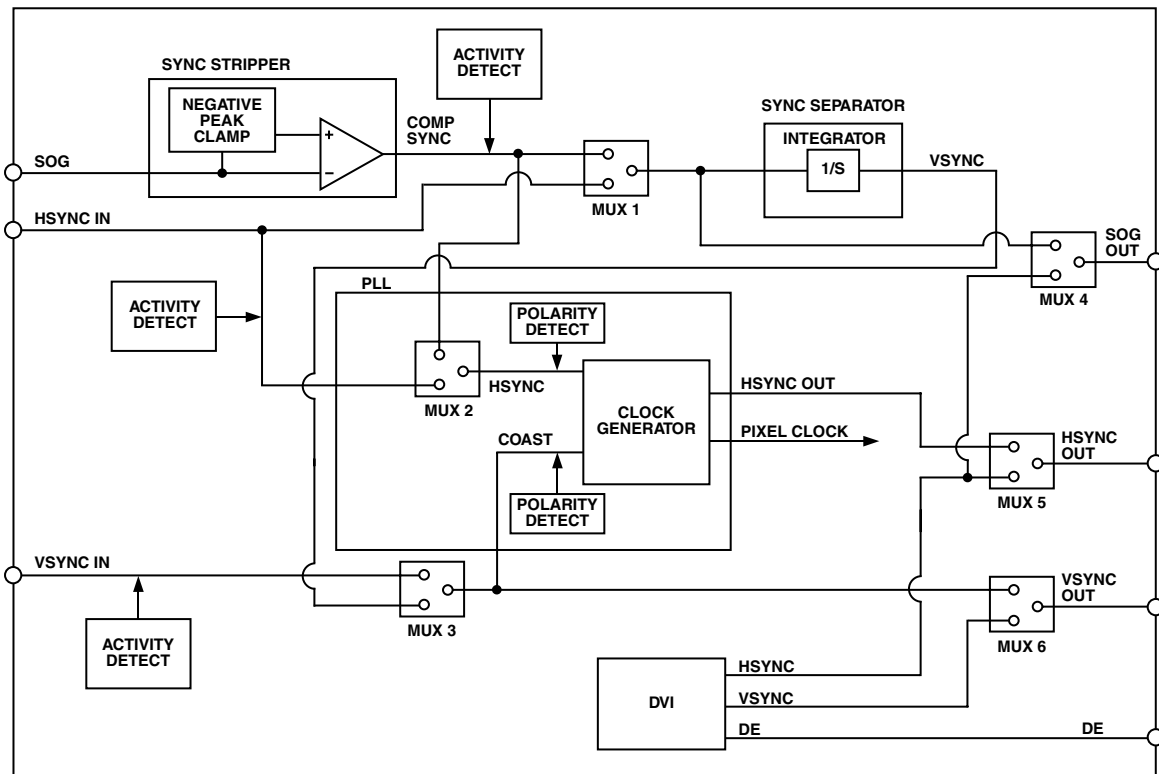


Figure 18. Sync Processing Block Diagram

Table XLIX. Control of the Sync Block Muxes via the Serial Register

Mux Number(s)	Serial Bus Control Bit	Control Bit State	Result
1 and 2	10H: Bit 3	0	Pass Hsync
		1	Pass Sync-on-Green
3	10H: Bit 0	0	Pass Vsync
		1	Pass Sync Separator Signal
4, 5, and 6	0FH: Bit 1	0	Pass Analog Interface Signals
		1	Pass Digital Interface Signals

# AD9882

## THEORY OF OPERATION

### Sync Stripper

This section is devoted to the basic operation of the sync processing engine. (Refer to Figure 18.)

The purpose of the sync stripper is to extract the sync signal from the green graphics channel. A sync signal is not present on all graphics systems; only those with Sync-on-Green. The sync signal is extracted from the GREEN channel in a two-step process. First, the SOG input is clamped to its negative peak (typically 0.3 V below the black level). Next, the signal goes to a comparator with a variable trigger level, nominally 0.15 V above the clamped level. The output signal is typically a composite sync signal containing both Hsync and Vsync.

### Sync Separator

A sync separator extracts the Vsync signal from a composite sync signal. It does this through a low-pass filter-like or integrator-like operation. It works on the idea that the Vsync signal stays active for a much longer time than the Hsync signal. So, it rejects any signal shorter than a threshold value, which is somewhere between an Hsync pulsewidth and a Vsync pulsewidth.

The sync separator on the AD9882 is simply an 8-bit digital counter with a 5 MHz clock. It works independently of the polarity of the composite sync signal. (Polarities are determined elsewhere on the chip.) The basic idea is that the counter counts up when Hsync pulses are present. But since Hsync pulses are relatively short in width, the counter only reaches a value of N before the pulse ends. It then starts counting down, eventually reaching 0 before the next Hsync pulse arrives. The specific value of N will vary for different video modes, but will always be less than 255. For example, with a 1  $\mu$ s width Hsync, the counter will only reach 5 (1  $\mu$ s/200 ns = 5). Now, when Vsync is present on the composite sync the counter will also count up. However, since the Vsync signal is much longer, it will count to a higher number M. For most video modes, M will be at least 255. So, Vsync can be detected on the composite sync signal by detecting when the counter counts to higher than N. The specific count that triggers detection (T) can be programmed through the serial register (0EH).

Once Vsync has been detected, a similar process detects when it goes inactive. At detection, the counter first resets to 0, then starts counting up when Vsync goes away. In a way similar to the previous case, it will detect the absence of Vsync when the counter reaches the threshold count (T). In this way, it will reject noise and/or serration pulses. Once Vsync is determined to be absent, the counter resets to 0 and begins the cycle again.

## PCB LAYOUT RECOMMENDATIONS

The AD9882 is a high precision, high speed analog device. In order to derive the maximum performance out of the part, it is important to have a well laid out board. The following is a guide for designing a board using the AD9882.

### Analog Interface Inputs

Using the following layout techniques on the graphics inputs is extremely important.

Minimize the trace length running into the graphics inputs. This is accomplished by placing the AD9882 as close as possible to the graphics VGA connector. Long input trace lengths are undesirable because they will pick up more noise from the board and other external sources.

Place the 75  $\Omega$  termination resistors (see Figure 1) as close to the AD9882 chip as possible. Any additional trace length between the termination resistors and the input of the AD9882 increases the magnitude of reflections, which will corrupt the graphics signal.

Use 75  $\Omega$  matched impedance traces. Trace impedances other than 75  $\Omega$  will also increase the chance of reflections.

The AD9882 has a very high input bandwidth (300 MHz). While this is desirable for acquiring a high resolution PC graphics signal with fast edges, it means that it will also capture any high frequency noise present. Therefore, it is important to reduce the amount of noise that gets coupled to the inputs. Avoid running any digital traces near the analog inputs.

Due to the high bandwidth of the AD9882, sometimes low-pass filtering the analog inputs can help to reduce noise. (For many applications, filtering is unnecessary.) Experiments have shown that placing a series ferrite bead prior to the 75  $\Omega$  termination resistor is helpful in filtering out excess noise. Specifically, the part used was the #2508051217Z0 from Fair-Rite, but different applications may work best with different bead values. Alternatively, placing a 100  $\Omega$  to 120  $\Omega$  resistor between the 75  $\Omega$  termination resistor and the input coupling capacitor can also be beneficial.

### Digital Interface Inputs

Many of the same techniques that are recommended for the analog interface inputs should also be used for the digital interface inputs. It is important to minimize trace lengths, then make the input trace impedances match the input termination (typically 50  $\Omega$ ). Each differential input pair ( $R_{X0+}$ ,  $R_{X0-}$ ,  $R_{XC+}$ ,  $R_{XC-}$ , and so on) should be routed together using 50  $\Omega$  strip line routing techniques and should be kept as short as possible. No other components, e.g., no clamping diodes, should be placed on these inputs. Every effort should be made to route these signals on a single layer (component layer) with no vias.

### Power Supply Bypassing

Bypassing each power supply pin with a 0.1  $\mu$ F capacitor is recommended. The exception is the case in which two or more supply pins are adjacent to each other. For these groupings of powers/grounds, it is necessary to have one bypass capacitor. The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power pin. Also, avoid placing the capacitor on the side of the PC board opposite the AD9882, as that interposes resistive vias in the path.

The bypass capacitors should be physically located between the power plane and the power pin. Current should flow from the power plane  $\rightarrow$  capacitor  $\rightarrow$  power pin. Do not make the power connection between the capacitor and the power pin. Placing a via underneath the capacitor pads, down to the power plane, is generally the best approach.

It is particularly important to maintain low noise and good stability of  $PV_D$  (the clock generator supply). Abrupt changes in  $PV_D$  can result in similarly abrupt changes in sampling clock phase and frequency. This can be avoided by careful attention to regulation, filtering, and bypassing. It is highly desirable to provide separate regulated supplies for each of the analog circuitry groups ( $V_D$  and  $PV_D$ ).

Some graphic controllers use levels of power when active (during active picture time) that are substantially different from those used when they are idle (during horizontal and vertical sync periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can in turn produce changes in the regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least  $PV_{DD}$ , from a different, cleaner, power source (for example, from a 12 V supply).

Using a single ground plane for the entire board is also recommended. Experience has repeatedly shown that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller than one common ground plane, and long ground loops can result.

In some cases, using separate ground planes is unavoidable. For those cases where they must be used, it is recommended that at least a single ground plane be placed under the AD9882. The location of the split should be at the receiver of the digital outputs. For this case, it is even more important to place components wisely because the current loops will be much longer (current takes the path of least resistance). The following is an example of a current loop: power plane → AD9882 → digital output trace → digital data receiver → digital ground plane → analog ground plane.

#### **PLL**

Place the PLL loop filter components as close to the **FILT** pin as possible.

Do not place any digital or other high frequency traces near these components.

Use the values suggested in the data sheet with 10% or smaller tolerances.

#### **Outputs (Data and Clocks)**

Try to minimize the trace length that the digital outputs have to drive. Longer traces have higher capacitance and require more current, which causes more internal digital noise.

Shorter traces reduce the possibility of reflections.

Adding a series resistor with a value of 22  $\Omega$  to 100  $\Omega$  can suppress reflections, reduce EMI, and reduce the current spikes inside of the AD9882. However, if 50  $\Omega$  traces are used on the PCB, the data output should not need these resistors.

A 22  $\Omega$  resistor on the **DATAACK** output should provide good impedance matching that will reduce reflections. If EMI or current spiking is a concern, use a lower drive strength setting by adjusting register 14H. If series resistors are used, place them as close to the AD9882 pins as possible (but avoid adding vias or extra length to the output trace in order to get the resistors closer).

If possible, limit the capacitance that each of the digital outputs drives to less than 10 pF. This can be accomplished easily by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance will increase the current transients inside the AD9882, creating more digital noise on its power supplies.

#### **Digital Inputs**

The digital inputs on the AD9882 were designed to work with 3.3 V signals, but are tolerant of 5.0 V signals. No extra components need to be added if 5.0 V logic is used.

Any noise that gets onto the **Hsync** input trace will add jitter to the system. Therefore, minimize the trace length and do not run any digital or other high frequency traces near it.

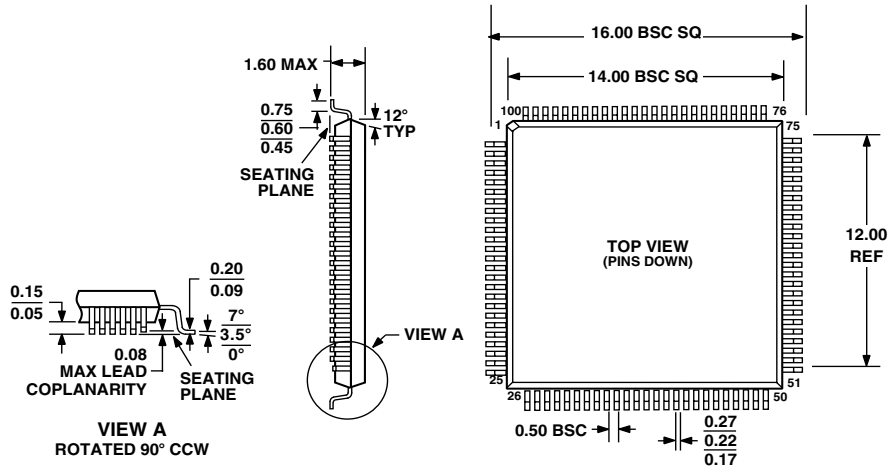
#### **Voltage Reference**

Bypass with a 0.1  $\mu\text{F}$  capacitor. Place as close to the AD9882 pin as possible. Make the ground connection as short as possible.

OUTLINE DIMENSIONS

100-Lead Quad Flatpack [LQFP]  
(ST-100)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026BED  
THE ACTUAL POSITION OF EACH LEAD IS WITHIN 0.08 OF ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION

Revision History

Location	Page
1/03—Data Sheet changed from REV. 0 to REV. A.	
Edits to PIN CONFIGURATION headings	7
Edits to Table IX	22