IECQ-CECC **QC 88000-C004**

COMPONENT **ISSUE 1**

SPECIFICATION **March 2007**

Component Specification
For
Ceramic Hermetically Sealed
High Speed Logic Gate
High CMR Transistor Optocouplers

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FOREWORD

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The object of the System is to facilitate international trade by the harmonization of the specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognised Mark, or Certificate of Conformity. The components produced or services provided under the system are thereby acceptable in all member countries without further testing.

This Component Specification is based upon the requirements of IEC Publication QC 001002-2, and has been prepared by:

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and published under the authority of:

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AMENDMENT RECORD

No previous issue.

REQUIREMENTS

The requirements for IECQ-CECC Component Specifications as detailed in QC 001002-2 Amendment 1 clause 5.4 are satisfied by the following data sheet.

It should note that IECQ-CECC are not responsible for manufacturers declarations made in data sheets which fall outside the limits of approved detailed in IECQ-CECC certificates.

This Component Specification is intended for use with applicable IECQ-CECC Assessment Specifications. Eg: QC 88000-A001

ISOCOM® LTD

Ceramic Hermetically Sealed High Speed Logic Gate High CMR Transistor Optocouplers

- 6N134
- CD650
- CD651
- CH350
- CS600
- CSM169
- CSM1600
- MC600

Features

- Release to IECQ-CECC
- Hermetically Sealed
- High Density Packaging
- 1500V DC withstand Test Voltage
- Low Input Requirements
- High Current Transfer Ratio

Applications

- Military, high reliability system
- Medical instruments
- Mos, Cmos Applications
- Logic Interfacing
- Data Transmission
- Transportation

Description

These devices are single, dual and quad, hermetically sealed optocouplers. The products are capable of operation and storage over the full military and space temperature range. Each channel is composed of a light emitting diode, optically coupled to an integrated high gain photon detector. The high gain output features an open collector output providing both lower saturation voltage and higher signalling speed. Package styles for these devices include 8 pin, 16 pin, 16 pin flat pack, leadless 6 pin and hybrid 5 pin, with surface mount, butt cut and gull wing options available.

The same electrical die, assembly processes and materials are used for each channel of each device shown below. Therefore absolute maximum ratings, recommended operating conditions, electrical specifications and performance characteristics are identical for all units. Any exceptions, due to packaging variations and limitations, are as noted.

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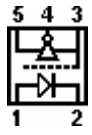
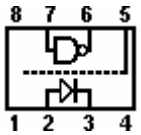
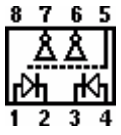
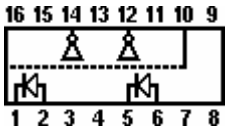
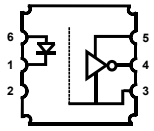
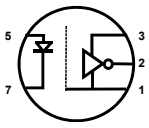
Selection Guide Package Styles and Configuration Options

Package	16 pin DIP	8 pin DIP	6 pin DIP	16 pin Flat Pack	6 Pad LCCC	6 pin Metal Can TO-5
Lead Style						
Channels	2	1/2	1	4	1	1
Common Channel Wiring						
Isocom Part Numbers and Options						
Commercial	6N134	CS600 CD650/651	CH350	CSM169	CSM1600	MC600
Defense Level	6N134/L2	CS600/L2 CD650/651/L2	CH350/L2	CSM169/L2	CSM1600/L	MC600/L2
Space Level	6N134/L2S	CS600/L2S CD650/651/L2S	CH350/L2S	CSM169/L2S	CSM1600/L2	MC600/L2S
Standard Gold Plate Finish	Gold Plate	Gold Plate	Gold Plate	Gold Plate	Gold Plate	Gold Plate
Solder Dipped	Option 20	Option 20	Option 20			
Butt Cut/Gold Plate	Option 10	Option 10	Option 10			
Gull Wing/Soldered	Option 30	Option 30	Option 30			
Crew Cut/Gold Plate	Option 60	Option 60	Option 60			

Functional Diagrams

CH350	CS600	CD650/651	6N134	CSM169	CSM1600
1 Channel	1 Channel	2 Channel	2 Channel	4 Channel	1 Channel
					

MC600
1 Channel


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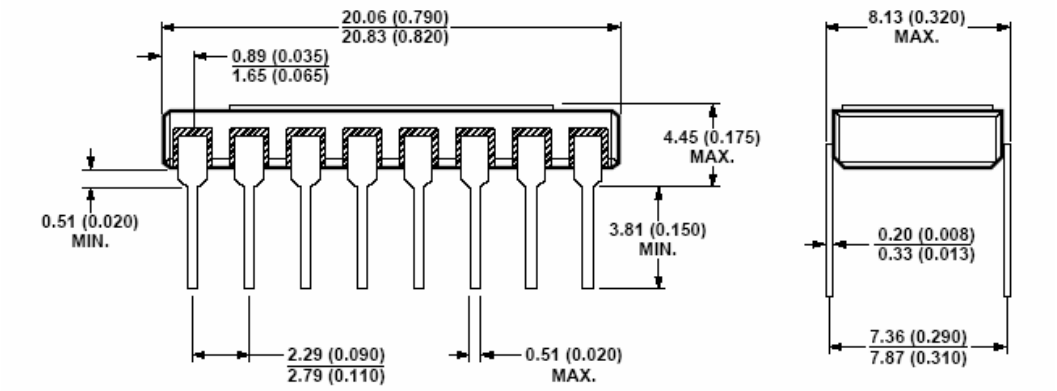
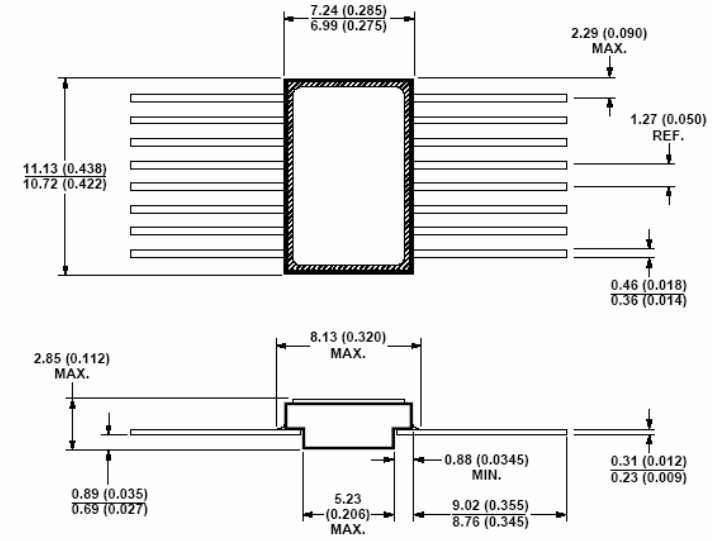
Outline Drawings

16 pin DIP, 4 Channel

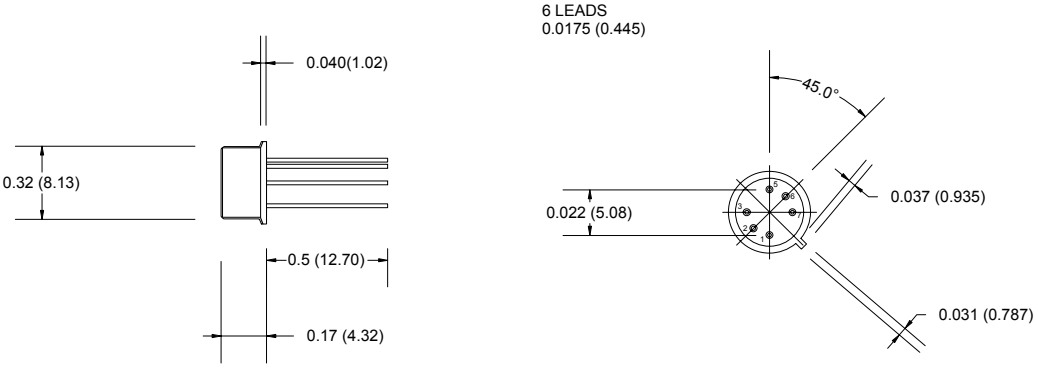


16 pin Flat Pack, 4 Channel



NOTE: DIMENSIONS IN MILLIMETERS

6 pin TO-5, 1 Channel



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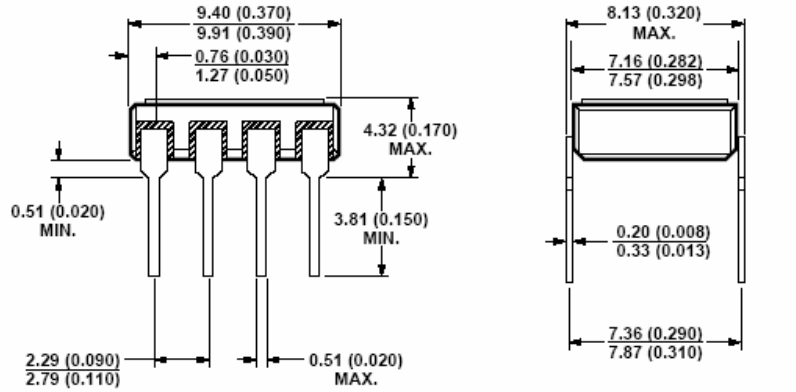
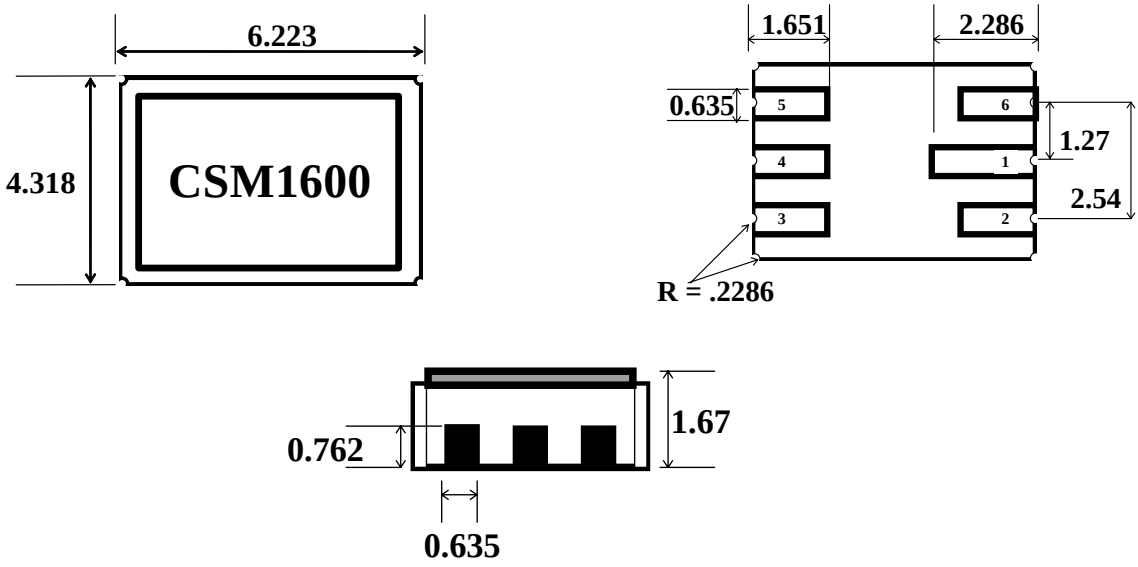
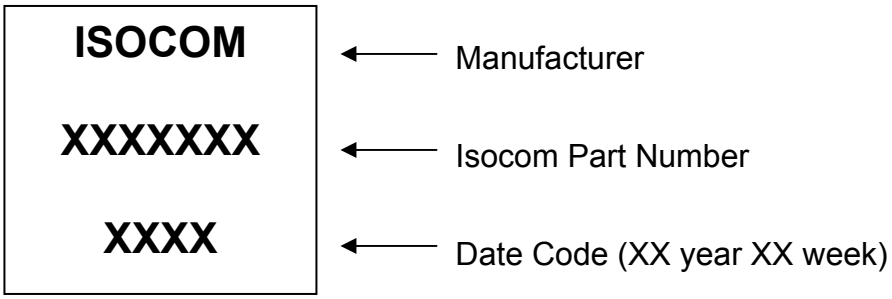
8 pin DIP 1 and 2 Channel



6 Terminal LCC Surface Mount, 1 Channel



Device Marking



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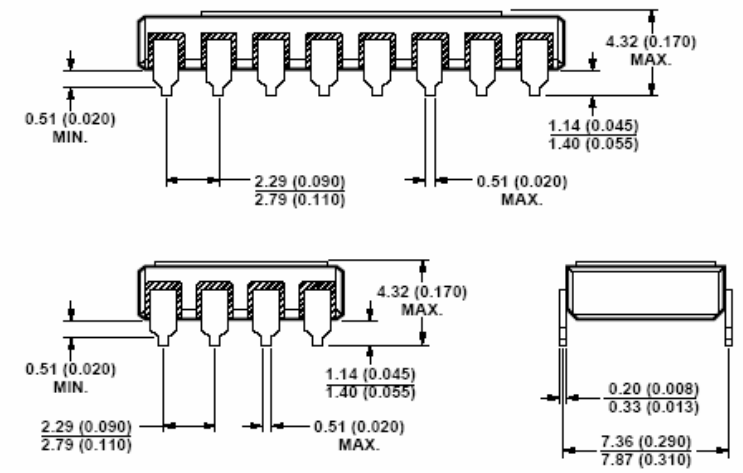
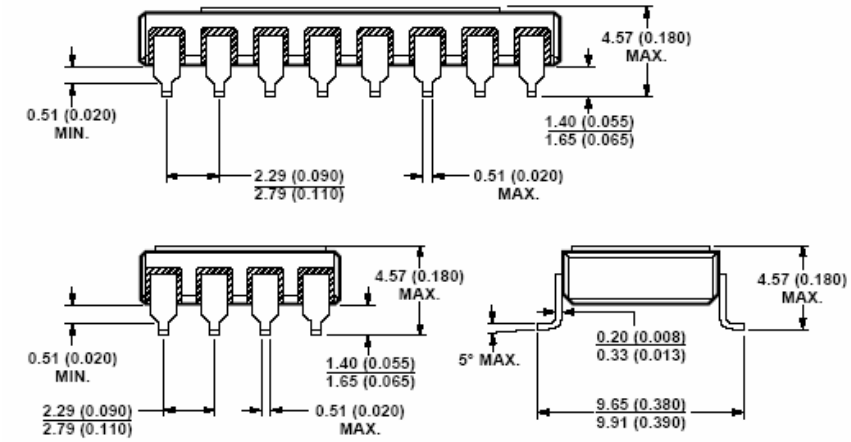
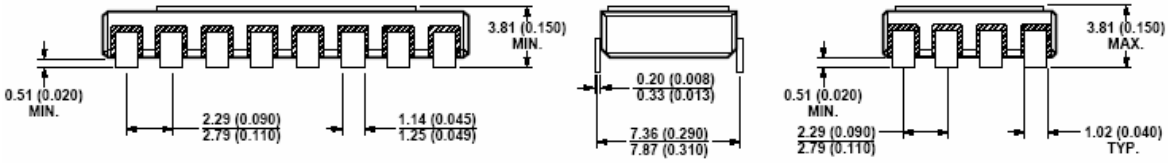
Hermetic Optocoupler Options

Option	Description
10	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial hi-rel product in 8 and 16 pin DIP 
20	
30	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product in 8 and 16 pin DIP. 
60	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial hi-rel product in 8 and 16 pin DIP 

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Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C
Lead Soldering Temperature	260C for 10S, 1.6mm below seating plane where appropriate

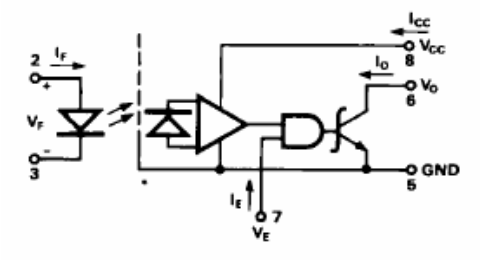
Input Diode

Peak Forward Current	40mA	I_F (≤ 1 mS duration)
Average Forward Current	20mA	I_F
Reverse Voltage	5V	V_R
Power Dissipation	35mW	

Output Detector

Supply Voltage	7V	V_{CC} (1minute maximum)
Current	25mA	I_O
Collector Power Dissipation	40mW	
Voltage	7V	V_O (See note 1)

Single Channel Schematic



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Electrical Characteristics

T_{A} = -55°C to +125°C U.O.S.
All typical values at V_{CC} = 5V, T_A = 25°C (each channel where appropriate).

Parameter	Symbol	Test Conditions	Device	Min	Type	Max	Units
High Level Output Current (See note 1)	I_{OH}	I_F = 250µA, V_O = V_{CC} = 5.5V		-	20	250	µA
Lower Level Output Voltage (See notes 1 & 9)	V_{OL}	I_F = 10mA, V_{CC} = 5.5V, I_{OL}(sinking) = 10mA		-	0.4	0.6	V
		I_F = 5mA, V_{CC} = 5.5V, I_{OL}(sinking) = 13mA	CD650				
High Level Supply Current	I_{CCH}	V_{CC} = 5.5V, I_{F1} = I_{F2} = 0		-	15	30	mA
Low Level Supply Current	I_{CCL}	V_{CC} = 5.5V, I_{F1} = I_{F2} = 10mA	Cs600	-	15	19	mA
			Cd650 Cd651		20	38	
		V_{CC} = 5.5V, I_{F1} = I_{F2} = 13mA	Ch350			36	
		V_{CC} = 5.5V, I_{F1} = I_{F2} = 20mA	6N134			36	
Input-Output Insulation Leakage Current (See notes 2 & 10)	I_{I-O}	RH = 45%, T_A = 25°C, t = 5S V_{IO} = 1500Vdc		-	-	1.0	µA
Input Forward Voltage (See note 1)	V_F	I_F = 10mA, T_A = 25°C		-	1.5	1.9	V
		I_F = 20mA		-	-	1.9	
Input Reverse Breakdown Voltage (See note 1)	B_{VR}	I_R = 10µA, T_A = 25°C		5	-	-	V
Propagation Delay Time to High Output Level See notes 1 & 5)	t_{PLH}	R_L = 510Ω, I_F = 13mA, T_A = 25°C, C_L = 50pF	6N134	-	-	100	nS
		R_L = 510Ω, I_F = 13mA, T_A = 25°C, C_L = 15pF	6N134 CD651	-	60	90	
			CH350			200	
		R_L = 350Ω, I_F = 7.5mA, T_A = 25°C, C_L = 15pF	Cs600			75	
Propagation Delay Time to Low Output Level (See notes 1 & 6)	t_{PHL}	R_L = 510Ω, I_F = 13mA, T_A = 25°C, C_L = 50pF	6N134	-	-	100	nS
		R_L = 510Ω, I_F = 13mA, T_A = 25°C, C_L = 15pF	6N134 CD651	-	55	90	
		R_L = 510Ω, I_F = 13mA, T_A = 25°C, C_L = 15pF	CH350			200	
		R_L = 350Ω, I_F = 7.5mA, T_A = 25°C, C_L = 15pF	CS600 CD650			100	
Current Transfer Ratio (See note 1)	CTR	I_F = 10mA, V_O = 0.6V, V_{CC} = 5.5V		100	-	-	%
		I_F = 5mA, V_O = 0.6V, V_{CC} = 5.5V	CS600 CD650	100	300		

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Typical Characteristics

T_A = 25°C, V_{CC} = 5V each channel where appropriate

Parameter	Symbol	Test Conditions	Notes	Min	Type	Max	Units
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	I_F = 20mA	1	-	-1.9	-	mV/°C
Resistance	R_{I-O}	V_{10} = 500V	3	-	10^{12}	-	Ω
Capacitance	C_{I-O}	f = 1MHz	3	-	1.9	-	pF
Input Capacitance	C_{IN}	f = 1MHz, V_F = 0	1	-	60	-	pF
Input-Input Leakage Current	I_{I-I}	45% Relative Humidity V_{II} = 500Vdc, t = 5S	4	-	0.5	-	nA
Resistance	R_{I-I}	V_{II} = 500Vdc	4	-	10^{12}	-	Ω
Capacitance	C_{I-I}	f = 1MHz	4	-	0.6	-	pF
Output Rise (10-90%)	tr	R_L = 510Ω, C_L = 15pF, I_F = 13mA	1	-	35	-	nS
Output Fall Time (90-10%)	tf	R_L = 510Ω, C_L = 15pF, I_F = 13mA	1	-	35	-	nS
Common Mode Transient Immunity at Logic High Output Level	CM_H	V_O (min) = 2V, V_{CM} = 10V (peak) R_L = 510Ω, I_F = 0mA	1 & 7	-	1000	-	V/µS
Common Mode Transient Immunity at Logic Low Output Level	CM_L	V_O(max) = 0.8V, V_{CM} = 10V (peak) R_L = 510Ω, I_F = 10mA	1 & 8	-	-1000	-	V/µS

Notes: (Apply typically to 16 pin package)

1. Each channel, where appropriate.
2. Measured between pins 1 through 4 shorted together, and pins 9 through 16 shorted together.
3. Measured between pins 1 and 2, or 5 and 6 shorted together, and pins 9 through 16 shorted together.
4. Measured between pins 1 and 2 shorted together, and pins 5 and 6 shorted together.
5. The t_{PLH} propagation delay is measured from the 6.5mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
6. The t_{PHL} propagation delay is measured from the 6.5mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
7. CM_H is the maximum tolerable common mode transient to assure that the output will remain in a high logic state (i.e., V_O > 2.0V).
8. CM_L is the maximum tolerable common mode transient to assure that the output will remain in the logic low state (i.e., V_O < 2.0V).
9. It is essential that a bypass capacitor (0.1 to 0.1µF, ceramic) be connected from pin 10 to pin 15. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20mm.
10. This is a momentary withstand test, not an operating condition.

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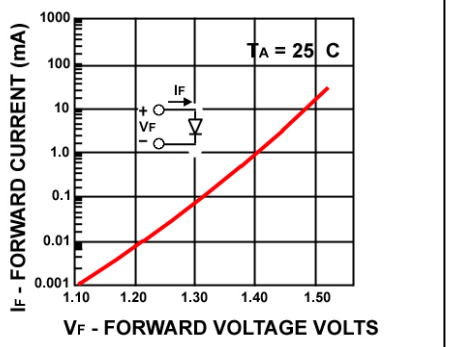
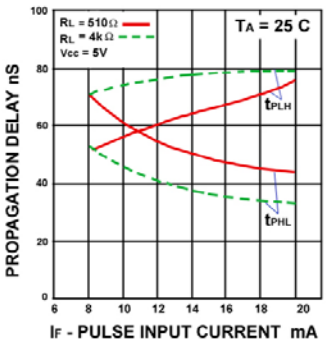
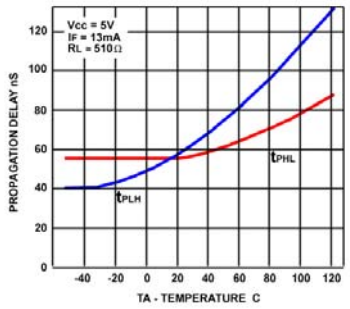
Electrical Characteristics



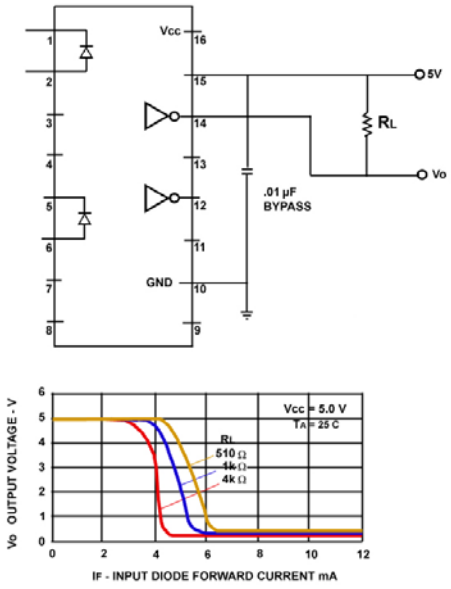
INPUT DIODE FORWARD CHARACTERISTIC



PROPAGATION DELAY, t_{PHL} AND t_{PLH} vs PULSE INPUT CURRENT I_{FH}



PROPAGATION DELAY vs TEMPERATURE



INPUT-OUTPUT CHARACTERISTICS

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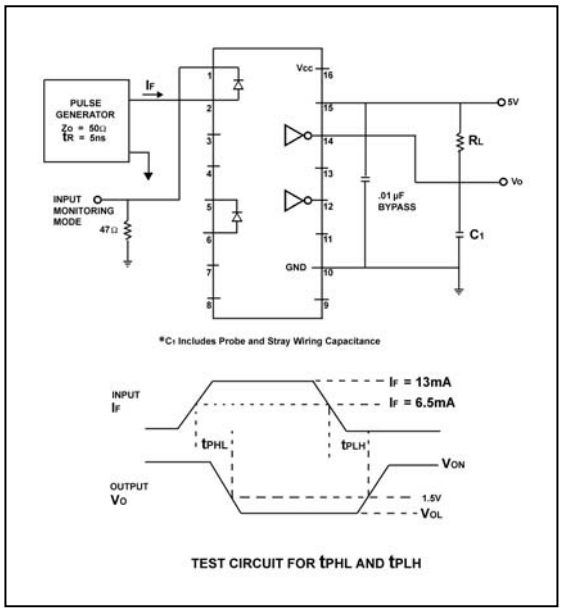
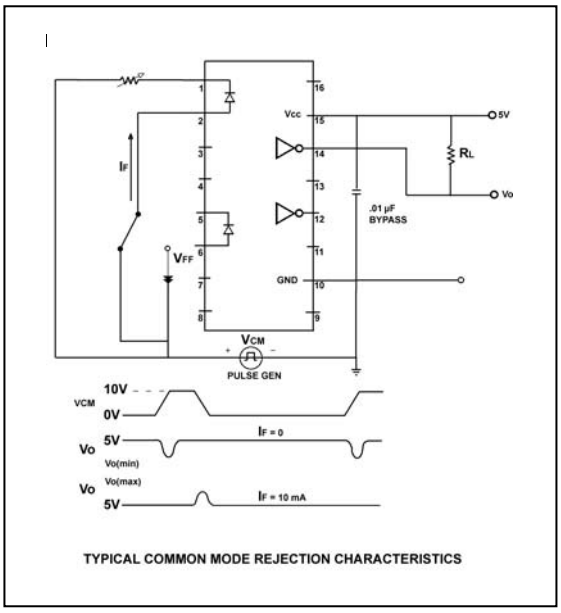
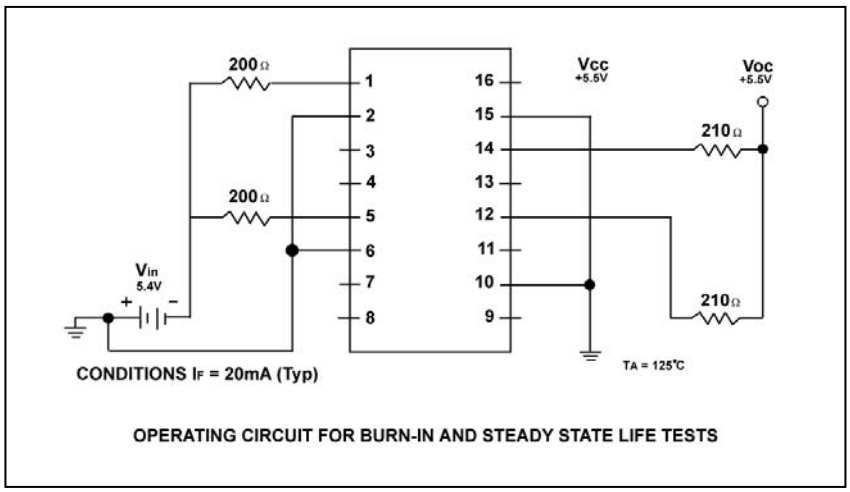


TEST CIRCUIT FOR t_{PHL} AND t_{PLH}



TYPICAL COMMON MODE REJECTION CHARACTERISTICS



OPERATING CIRCUIT FOR BURN-IN AND STEADY STATE LIFE TESTS

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