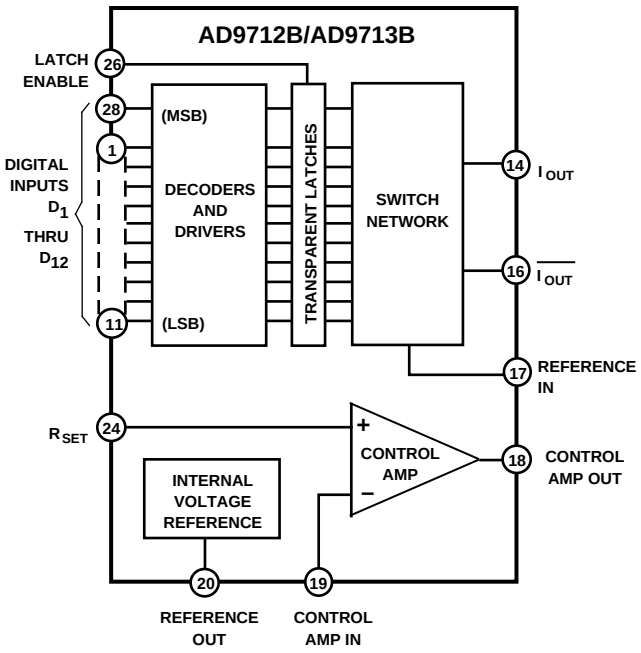
12-Bit, 100 MSPS D/A Converters

AD9712B/AD9713B

FEATURES
100 MSPS Update Rate
ECL/TTL Compatibility
SFDR @ 1 MHz: 70 dBc
Low Glitch Impulse: 28 pV-s
Fast Settling: 27 ns
Low Power: 725 mW
1/2 LSB DNL (B Grade)
40 MHz Multiplying Bandwidth

APPLICATIONS
ATE
Signal Reconstruction
Arbitrary Waveform Generators
Digital Synthesizers
Signal Generators

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9712B and AD9713B D/A converters are replacements for the AD9712 and AD9713 units which offer improved ac and dc performance. Like their predecessors, they are 12-bit, high speed digital-to-analog converters fabricated in an advanced oxide isolated bipolar process. The AD9712B is an ECL-compatible device featuring update rates of 100 MSPS minimum; the TTL-compatible AD9713B will update at 80 MSPS minimum.

Designed for direct digital synthesis, waveform reconstruction, and high resolution imaging applications, both devices feature low glitch impulse of 28 pV-s and fast settling times of 27 ns. Both units are characterized for dynamic performance and have excellent harmonic suppression.

The AD9712B and AD9713B are available in 28-pin plastic DIPs and PLCCs, with an operating temperature range of –25°C to +85°C. Both are also available for extended temperature ranges of –55°C to +125°C in cerdips and 28-pin LCC packages.

REV. B

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AD9712B/AD9713B–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

[$-V_S$ = –5.2 V; $+V_S$ = +5 V (AD9713B only); Reference Voltage = –1.2 V; R_{SET} = 7.5 kΩ; V_{OUT} = 0 V (virtual ground); unless otherwise noted]

Parameter (Conditions)	Temp	Test Level	AD9712B/AD9713B AN/AP Min	AN/AP Typ	AN/AP Max	AD9712B/AD9713B BN/BP Min	BN/BP Typ	BN/BP Max	AD9712B/AD9713B SE/SQ Min	SE/SQ Typ	SE/SQ Max	AD9712B/AD9713B TE/TQ Min	TE/TQ Typ	TE/TQ Max	Units
RESOLUTION				12			12			12			12		Bits
DC ACCURACY															
Differential Nonlinearity	+25°C	I	–1.25	1.0	+1.25	–0.75	0.5	+0.75	–1.5	1.0	+1.5	–1.0	0.5	+1.0	LSB
	Full	VI	–2.0		2.0	–1.5		1.5	–2.0		2.0	–1.5		1.5	LSB
Integral Nonlinearity	+25°C	I	–1.5	1.0	1.5	–1.0	0.75	1.0	–1.75	1.5	1.75	–1.25	1.0	1.25	LSB
(“Best Fit” Straight Line)	Full	VI	–2.0		2.0	–1.75		1.75	–2.0		2.0	–1.75		1.75	LSB

Parameter (Conditions)	Temp	Test Level	AD9712B All Grades Min	AD9712B All Grades Typ	AD9712B All Grades Max	AD9713B All Grades Min	AD9713B All Grades Typ	AD9713B All Grades Max	Units
INITIAL OFFSET ERROR									
Zero-Scale Offset Error	+25°C	I		0.5	2.5		0.5	2.5	µA
	Full	VI			5.0			5.0	µA
Full-Scale Gain Error[1]	+25°C	I		1.0	5		1.0	5	%
	Full	VI			8			8	%
Offset Drift Coefficient	+25°C	V		0.01			0.01		µA/°C
REFERENCE/CONTROL AMP									
Internal Reference Voltage	+25°C	I	–1.14	–1.18	–1.22	–1.14	–1.18	–1.22	V
	Full	VI	–1.12		–1.24	–1.12		–1.24	V
Internal Reference Voltage Drift	Full	V		50			50		ppm/°C
Internal Reference Output Current	Full	IV	–50		+500	–50		+500	µA
Amplifier Input Impedance	+25°C	V		50			50		kΩ
Amplifier Bandwidth	+25°C	V		300			300		kHz
REFERENCE INPUT[2]									
Reference Input Impedance	+25°C	V		3			3		kΩ
Reference Multiplying Bandwidth[3]	+25°C	V		40			40		MHz
DYNAMIC PERFORMANCE									
Full-Scale Output Current[4]	+25°C	V		20.48			20.48		mA
Output Compliance Range	+25°C	IV	–1.2		+2	–1.2		+2	V
Output Resistance	+25°C	IV	2.0	2.5	3.0	2.0	2.5	3.0	kΩ
Output Capacitance	+25°C	V		15			15		pF
Output Update Rate[5]	+25°C	IV	100	110		80	100		MSPS
Output Settling Time (t_{ST})[6]	+25°C	V		27			27		ns
Output Propagation Delay (t_{PD})[7]	+25°C	V		6			7		ns
Glitch Impulse[8]	+25°C	V		28			28		pV-s
Output Rise Time[9]	+25°C	V		2			2		ns
Output Fall Time[9]	+25°C	V		2			2		ns
DIGITAL INPUTS									
Logic “1” Voltage	Full	VI	–1.0	–0.8		2.0			V
Logic “0” Voltage	Full	VI		–1.7	–1.5			0.8	V
Logic “1” Current	Full	VI			20			20	µA
Logic “0” Current	Full	VI			10			600	µA
Input Capacitance	+25°C	V		3			3		pF
Input Setup Time (t_S)[10]	+25°C	IV	0.5	–0.3		0.5	–0.3		ns
	Full	IV	0.8			0.8			ns
Input Hold Time (t_H)[11]	+25°C	IV	1.8	1.2		1.8	1.2		ns
	Full	IV	2.0			2.0			ns
Latch Pulse Width (t_{LPW}) (LOW)	+25°C	IV	2.5	1.7		2.5	1.7		ns
(Transparent)	Full		2.8			2.8			ns
AC LINEARITY[12]									
Spurious-Free Dynamic Range (SFDR)									
1.23 MHz; 10 MSPS; 2 MHz Span	+25°C	V		70			70		dB
5.055 MHz; 20 MSPS; 2 MHz Span	+25°C	V		72			72		dB
10.1 MHz; 50 MSPS; 2 MHz Span	+25°C	V		68			68		dB
16 MHz; 40 MSPS; 10 MHz Span	+25°C	V		68			68		dB

Parameter (Conditions)	Temp	Test Level	AD9712B All Grades Min	AD9712B All Grades Typ	AD9712B All Grades Max	AD9713B All Grades Min	AD9713B All Grades Typ	AD9713B All Grades Max	Units
POWER SUPPLY[13]									
Positive Supply Current (+5.0 V)	+25°C	I					6	12	mA
	Full	VI						14	mA
Negative Supply Current (–5.2 V)[14]	+25°C	I		140	178		145	184	mA
	Full	VI			183			188	mA
Nominal Power Dissipation	+25°C	V		728			784		mW
Power Supply Rejection Radio (PSRR)[15]	+25°C	I		30	100		30	100	µA/V

NOTES
[1]Measured as error in ratio of full-scale current to current through R_{SET} (160 µA nominal); ratio is nominally 128.
[2]Full-scale variations among devices are higher when driving REFERENCE INPUT directly.
[3]Frequency at which the gain is flat ±0.5 dB; R_L = 50 Ω; 50% modulation at midscale.
[4]Based on I_{FS} = 128 (V_{REF}/R_{SET}) when using internal amplifier.
[5]Data registered into DAC accurately at this rate; does not imply settling to 12-bit accuracy.
[6]Measured as voltage settling at midscale transition to ±0.024%, R_L = 50 Ω.
[7]Measured as the time between the 50% point of the falling edge of LATCH ENABLE and the point where the output signal has left a 1 LSB error band around its previous value.
[8]Peak glitch impulse is measured as the largest area under a single positive or negative transient.
[9]Measured with R_L = 50 Ω and DAC operating in latched mode.
[10]Data must remain stable for specified time prior to falling edge of LATCH ENABLE signal.
[11]Data must remain stable for specified time after rising edge of LATCH ENABLE signal.
[12]SFDR is defined as the difference in signal energy between the fundamental and worst case spurious frequencies in the output spectrum window, which is centered at the fundamental frequency and covers the indicated span.
[13]Supply voltages should remain stable within ±5% for normal operation.
[14]108 mA typ on Digital $–V_S$, 37 mA typ on Analog $–V_S$.
[15]Measured at ±5% of $+V_S$ (AD9713B only) and $–V_S$ (AD9712B or AD9713B) using external reference.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) (AD9713B Only) . . . . . +6 V
Negative Supply Voltage ($–V_S$) . . . . . –7 V
Analog-to-Digital Ground Voltage Differential . . . . . 0.5 V
Digital Input Voltages (D_1–D_{12}, LATCH ENABLE)
AD9712B . . . . . 0 V to $–V_S$
AD9713B . . . . . –0.5 V to $+V_S$
Internal Reference Output Current . . . . . 500 µA
Control Amplifier Input Voltage Range . . . . . 0 V to –4 V
Control Amplifier Output Current . . . . . ±2.5 mA
Reference Input Voltage Range (V_{REF}) . . . . . 0 V to $–V_S$
Analog Output Current . . . . . 30 mA
Operating Temperature Range
AD9712B/AD9713BAN/AP/BN/BP . . . . . –25°C to +85°C
AD9712B/AD9713BSE/SQ/TE/TQ . . . . . –55°C to +125°C
Maximum Junction Temperature[2]
AD9712B/AD9713BAN/AP/BN/BP . . . . . +150°C
AD9712B/AD9713BSE/SQ/TE/TQ . . . . . +175°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Storage Temperature Range . . . . . –65°C to +150°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances with parts soldered in place: 28-pin plastic DIP: θ_{JA} = 37°C/W, θ_{JC} = 10°C/W; 28-pin PLCC: θ_{JA} = 44°C/W, θ_{JC} = 14°C/W; Cerdip: θ_{JA} = 32°C/W, θ_{JC} = 10°C/W; LCC: θ_{JA} = 41°C/W, θ_{JC} = 13°C/W. No air flow.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9712BAN	–25°C to +85°C	28-Pin PDIP	N-28
AD9712BBN	–25°C to +85°C	28-Pin PDIP	N-28
AD9712BAP	–25°C to +85°C	28-Pin PLCC	P-28A
AD9712BBP	–25°C to +85°C	28-Pin PLCC	P-28A
AD9712BSQ/883B	–55°C to +125°C	28-Pin Cerdip	Q-28
AD9712BSE/883B	–55°C to +125°C	28-Pin LCC	E-28A
AD9712BTQ/883B	–55°C to +125°C	28-Pin Cerdip	Q-28
AD9712BTE/883B	–55°C to +125°C	28-Pin LCC	E-28A
AD9713BAN	–25°C to +85°C	28-Pin PDIP	N-28
AD9713BBN	–25°C to +85°C	28-Pin PDIP	N-28
AD9713BAP	–25°C to +85°C	28-Pin PLCC	P-28A
AD9713BBP	–25°C to +85°C	28-Pin PLCC	P-28A
AD9713BSQ/883B	–55°C to +125°C	28-Pin Cerdip	Q-28
AD9713BSE/883B	–55°C to +125°C	28-Pin LCC	E-28A
AD9713BTQ/883B	–55°C to +125°C	28-Pin Cerdip	Q-28
AD9713BTE/883B	–55°C to +125°C	28-Pin LCC	E-28A

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

PIN DESCRIPTIONS

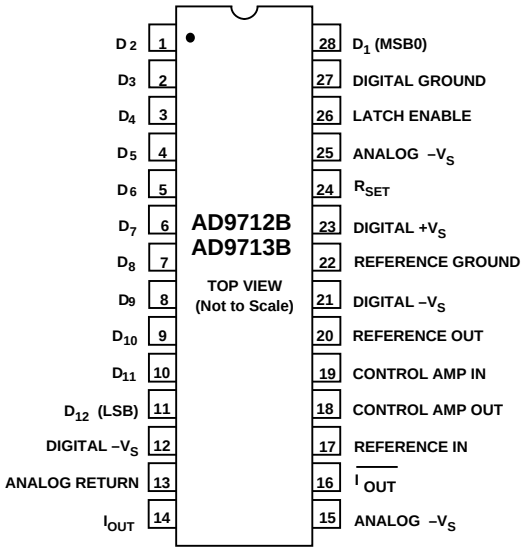
Pin #	Name	Function
1–10	D_2–D_{11}	Ten bits of twelve-bit digital input word.
11	D_{12} (LSB)	Least Significant Bit (LSB) of digital input word.
12	DIGITAL $-V_S$	One of two negative digital supply pins; nominally –5.2 V.
13	ANALOG RETURN	Analog ground return. This point and the reference side of the DAC load resistors should be connected to the same potential (nominally ground).
14	I_{OUT}	Analog current output; full-scale output occurs with digital inputs at all "1."
15	ANALOG $-V_S$	One of two negative analog supply pins; nominally –5.2 V.
16	$\overline{I_{OUT}}$	Complementary analog current output; zero scale output occurs with digital inputs at all "1."
17	REFERENCE IN	Normally connected to CONTROL AMP OUT (Pin 18). Direct line to DAC current source network. Voltage changes at this point have a direct effect on the full-scale output value of unit. Full-scale current output = 128 (Reference voltage/R_{SET}) when using internal amplifier.
18	CONTROL AMP OUT	Normally connected to REFERENCE INPUT (Pin 17). Output of internal control amplifier, which provides a temperature-compensated drive level to the current switch network.
19	CONTROL AMP IN	Normally connected to REFERENCE OUT (Pin 20) if not connected to external reference.
20	REFERENCE OUT	Normally connected to CONTROL AMP IN (Pin 19). Internal voltage reference, nominally –1.18 V.
21	DIGITAL $-V_S$	One of two negative digital supply pins; nominally –5.2 V.
22	REFERENCE GROUND	Ground return for the internal voltage reference and amplifier.
23	DIGITAL $+V_S$	Positive digital supply pin, used only on the AD9713B; nominally +5 V. No connection to this pin on AD9712B.
24	R_{SET}	Connection for external resistance reference. Full-scale current out = 128 (Reference voltage/ R_{SET}) when using internal amplifier. Nominally 7.5 kΩ.
25	ANALOG $-V_S$	One of two negative analog supply pins; nominally –5.2 V.
26	LATCH ENABLE	Transparent latch control line. Register is transparent when LATCH ENABLE is LOW.
27	DIGITAL GROUND	Digital ground return.
28	D_1 (MSB)	Most Significant Bit (MSB) of digital input word.

Input Coding vs. Current Output

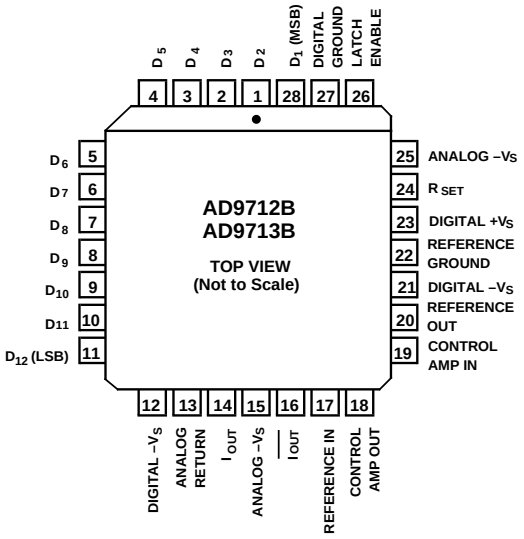
Input Code D_1–D_{12}	I_{OUT} (mA)	$\overline{I_{OUT}}$ (mA)
1111111111	–20.475	0
0000000000	0	–20.475

PIN CONFIGURATIONS

DIP

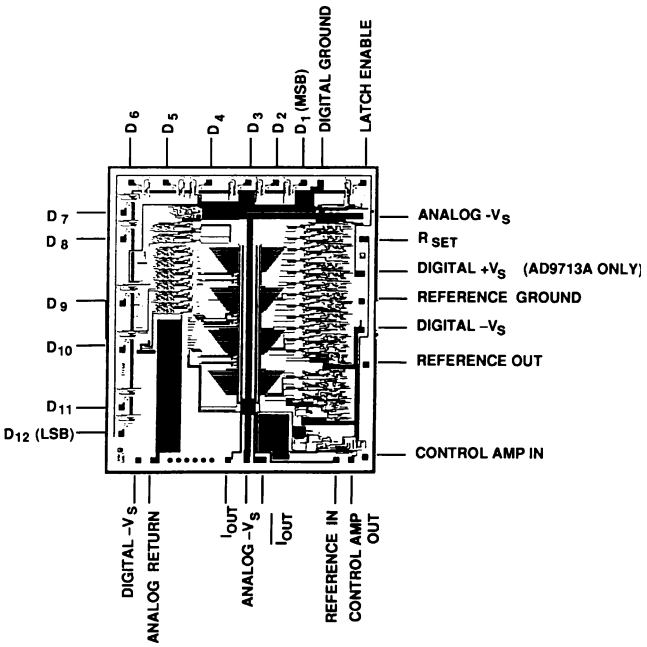


PLCC/LCC



DIE LAYOUT AND METALIZATION INFORMATION

Die Dimensions . . . . . 220 × 196 × 15 (±2) mils
Pad Dimensions . . . . . 4 × 4 mils
Metalization . . . . . Aluminum
Backing . . . . . None
Substrate Potential . . . . . $-V_S$
Passivation . . . . . Nitride



THEORY AND APPLICATIONS

The AD9712B and AD9713B high speed digital-to-analog converters utilize Most Significant Bit (MSB) decoding and segmentation techniques to reduce glitch impulse and maintain 12-bit linearity without trimming.

As shown in the functional block diagram, the design is based on four main subsections: the Decoder/Driver circuits, the Transparent Latches, the Switch Network, and the Control Amplifier. An internal bandgap reference is also included to allow operation with a minimum of external components.

Digital Inputs/Timing

The AD9712B employs single-ended ECL-compatible inputs for data inputs D_1–D_{12} and LATCH ENABLE. The internal ECL midpoint reference is designed to match 10K ECL device thresholds. On the AD9713B, a TTL translator is added at each input; with this exception, the AD9712B and AD9713B are identical.

In the Decoder/Driver section, the four MSBs (D_1–D_4) are decoded to 15 "thermometer code" lines. An equalizing delay is included for the eight Least Significant Bits (LSBs) and LATCH ENABLE. This delay minimizes data skew, and data setup and hold times at the latch inputs; this is important when operating the latches in the transparent mode. Without the delay, skew caused by the decoding circuits would degrade glitch impulse.

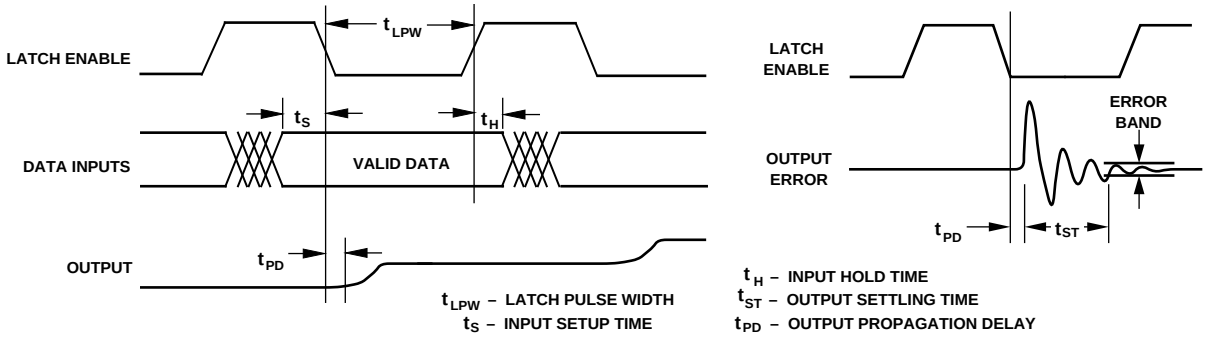
The latches operate in their transparent mode when LATCH ENABLE (Pin 26) is at logic level "0." The latches should be used to synchronize data to the current switches by applying a narrow LATCH ENABLE pulse with proper data setup and hold times as shown in the Timing Diagram. An external latch at each data input, clocked out of phase with the Latch Enable, operates the AD9712B/AD9713B in a master slave (edge-triggered) mode. This is the optimum way to operate the DAC because data is always stable at the DAC input. An external latch eases timing constraints when using the converter.

Although the AD9712B/AD9713B chip is designed to provide isolation from digital inputs to the outputs, some coupling of digital transitions is inevitable, especially with TTL or CMOS inputs applied to the AD9713B. Digital feedthrough can be reduced by forming a low-pass filter using a (200 Ω) series resistor in series with the capacitance of each digital input; this rolls off the slew rate of the digital inputs.

References

As shown in the functional block diagram, the internal bandgap reference, control amplifier, and reference input are pinned out for maximum user flexibility when setting the reference.

When using the internal reference, REFERENCE OUT (Pin 20) should be connected to CONTROL AMP IN (Pin 19). CONTROL AMP OUT (Pin 18) should be connected to REFERENCE IN (Pin 17) through a 20 Ω resistor. A 0.1 µF ceramic capacitor from Pin 17 to $-V_S$ (Pin 15) improves settling by decoupling switching noise from the current sink base line. A reference current cell provides feedback to the control amp by sinking current through R_{SET} (Pin 24).



Timing Diagram

Full-scale output current is determined by CONTROL AMP IN and R_{SET} according to the equation:

$$I_{OUT}\,(FS) = (CONTROL\ AMP\ IN/R_{SET}) \times 128$$

The internal reference is nominally –1.18 V with a tolerance of ±3.5% and typical drift over temperature of 50 ppm/°C. If greater accuracy or better temperature stability is required, an external reference can be utilized. The AD589 reference shown in Figure 1 features ±10 ppm/°C drift over temperatures from 0°C to +70°C.

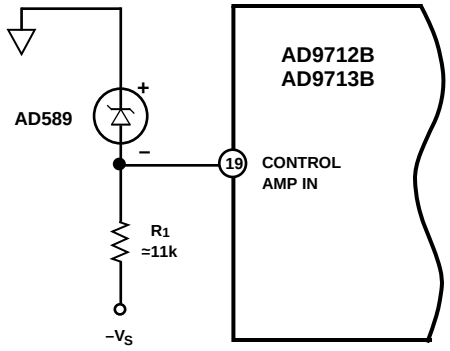


Figure 1. Use of AD589 as External Reference

Two modes of multiplying operation are possible with the AD9712B/AD9713B. Signals with small signal bandwidths up to 300 kHz and input swings of 100 mV, or dc signals from –0.6 V to –1.2 V can be applied to the CONTROL AMP input as shown in Figure 2. Because the control amplifier is internally compensated, the 0.1 µF capacitor at Pin 17 can be reduced to 0.01 µF to maximize the multiplying bandwidth. However, it should be noted that settling time for changes to the digital inputs will be degraded.

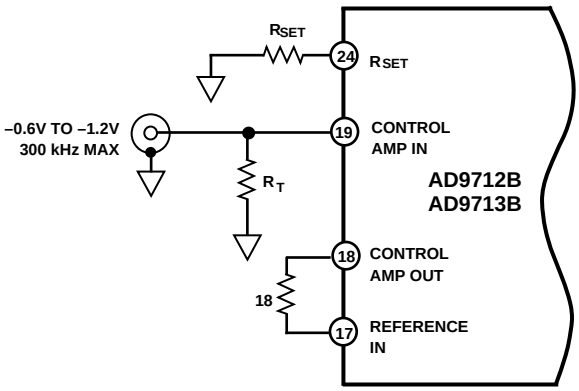


Figure 2. Low Frequency Multiplying Circuit

The REFERENCE IN pin can also be driven directly for wider bandwidth multiplying operation. The analog signal for this mode of operation must have a signal swing in the range of –3.75 V to –4.25 V. This can be implemented by capacitively coupling into REFERENCE IN a signal with a dc bias of –3.75 V to –4.25 V, as shown in Figure 3; or by driving REFERENCE IN with a low impedance op amp whose signal swing is limited to the stated range.

Outputs

As indicated earlier, D_1–D_4 (four MSBs) are decoded and drive 15 discrete current sinks. D5 and D6 are binarily weighted; and D_7–D_{12} are applied to the R-2R network. This segmented architecture reduces frequency domain errors due to glitch impulse.

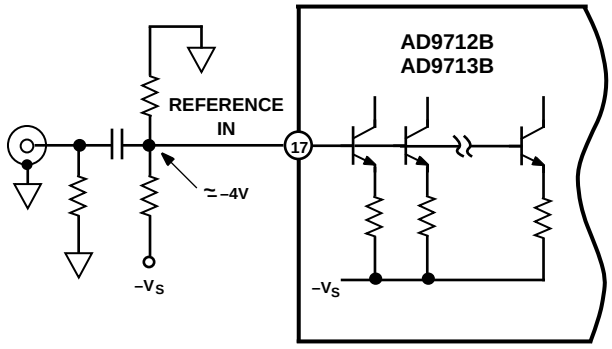


Figure 3. Wideband Multiplying Circuit

The Switch Network provides complementary current outputs I_{OUT} and $\overline{I_{OUT}}$. These current outputs are based on statistical current source matching which provides 12-bit linearity without trim. Current is steered to either I_{OUT} or $\overline{I_{OUT}}$ in proportion to the digital input code. The sum of the two currents is always equal to the full-scale output current minus one LSB.

The current output can be converted to a voltage by resistive loading as shown in Figure 4. Both I_{OUT} and $\overline{I_{OUT}}$ should be loaded equally for best overall performance. The voltage which is developed is the product of the output current and the value of the load resistor.

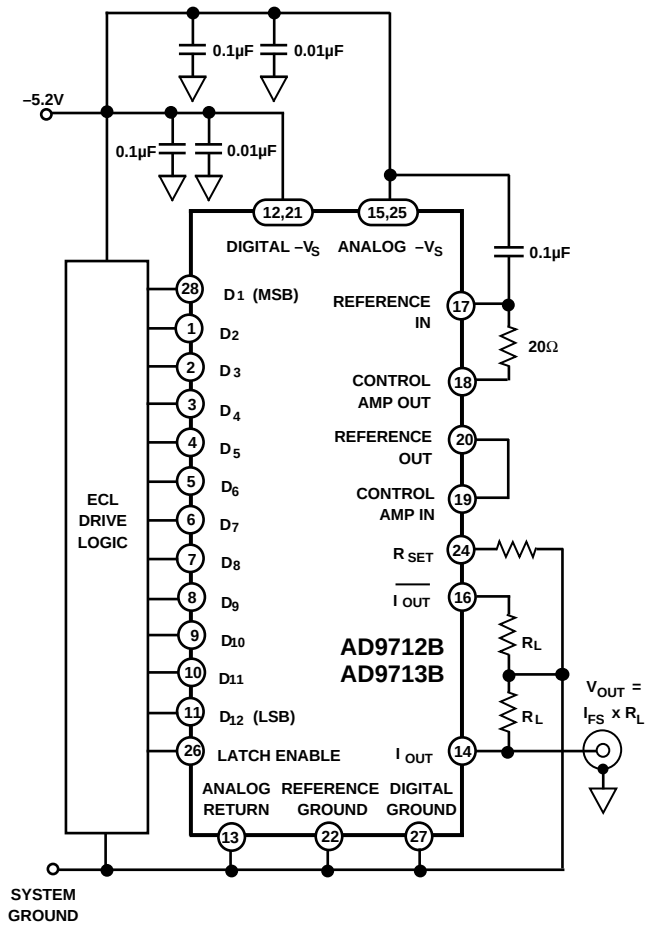


Figure 4. Typical Resistive Load Connection

An operational amplifier can also be used to perform the I to V conversion of the DAC output. Figure 5 shows an example of a circuit which uses the AD9617, a high speed, current feedback amplifier.

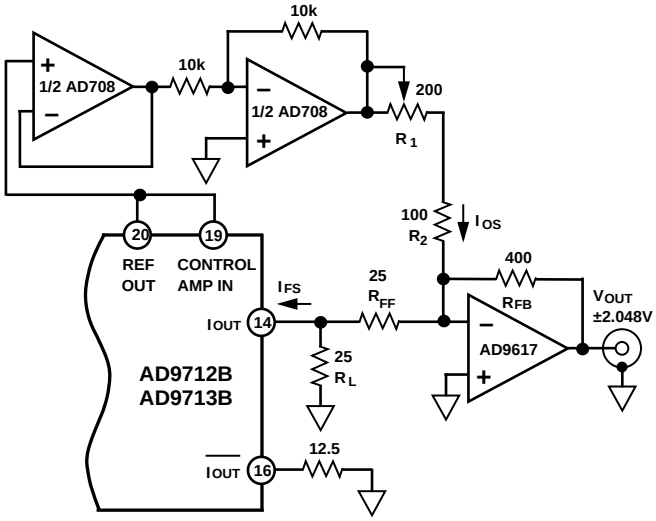


Figure 5. I/VConversion Using Current Feedback

DAC current across feedback resistor R_{FB} determines the AD9617 output swing. A current divider formed by R_L and R_{FF} limits the current used in the I-to-V conversion, and provides an output voltage swing within the specifications of the AD9617. Current through R_2 provides dc offset at the output of the AD9617. Adjusting the value of R_1 adjusts the value of offset current. This offset current is based on the reference of the AD9712B/AD9713B, to avoid coupling noise into the output signal.

The resistor values in Figure 5 provide a 4.096 V swing, centered at ground, at the output of the AD9617 amplifier.

Power and Grounding

Maintaining low noise on power supplies and ground is critical for obtaining optimum results with the AD9712B or AD9713B. DACs are most often used in circuits which are predominantly digital. To preserve 12-bit performance, especially at conversion speeds up to 100 MSPS, special precautions are necessary for power supplies and grounding.

Ideally, the DAC should have a separate analog ground plane. All ground pins of the DAC, as well as reference and analog output components, should be tied directly to this analog ground plane. The DAC's ground plane should be connected to the system ground plane at a single point.

Ferrite beads such as the Stackpole 57-1392 or Amidon FB-43B-101, along with high frequency, low-inductance decoupling capacitors, should be used for the supply connections to isolate digital switching currents from the DAC supply pins. Separate isolation networks for the digital and analog supply connections will further reduce supply noise coupling to the output.

Molded socket assemblies should be avoided even when prototyping circuits with the AD9712B or AD9713B. When the DAC cannot be directly soldered into the board, individual pin sockets such as AMP #6-330808-0 (knock-out end), or #60330808-3 (open end) should be used. These have much less effect on inter-lead capacitance than do molded assemblies.

DDS Applications

Numerically controlled oscillators (NCOs) are digital devices which generate samples of a sine wave. When the NCO is combined with a high performance D/A converter (DAC), the combination system is referred to as a Direct Digital Synthesizer (DDS).

The digital samples generated by the NCO are reconstructed by the DAC and the resulting sine wave is usable in any system which requires a stable, spectrally pure, frequency-agile reference. The DAC is often the limiting factor in DDS applications, since it is the only analog function in the circuit. The AD9712B/AD9713B D/A converters offer the highest level of performance available for DDS applications.

DC linearity errors of a DAC are the dominant effect in low-frequency applications and can affect both noise and harmonic content in the output waveform. Differential Nonlinearity (DNL) errors determine the quantization error between adjacent codes, while Integral Nonlinearity (INL) is a measure of how closely the overall transfer function of the DAC compares with an ideal device. Together, these errors establish the limits of phase and amplitude accuracy in the output waveform.

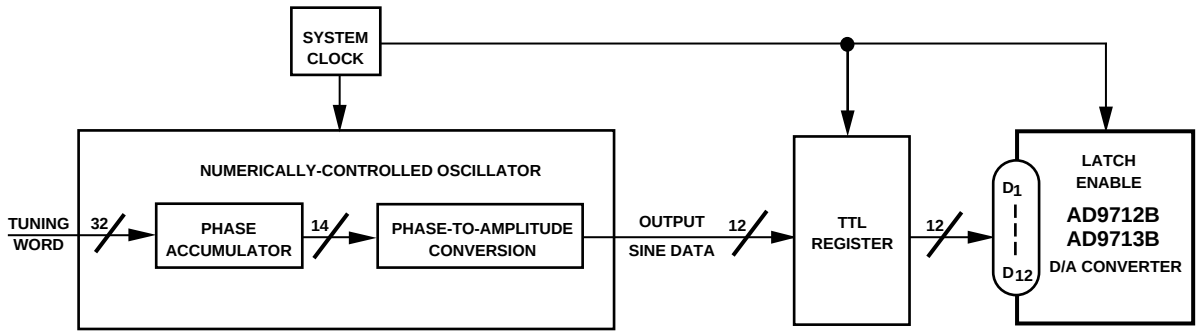


Figure 6. Direct Digital Synthesizer Block Diagram

When the analog frequency (f_A) is exactly f_C/N and N is an even integer, the DDS continually uses a small subset of the available DAC codes. The DNL of the converter is effectively the DNL error of the codes used, and is typically worse than the error measured against all available DAC codes. This increase in DNL is translated into higher harmonic and noise levels at the output.

Glitch impulse, often considered a figure of merit in DDS applications, is simply the initial transient response of the DAC as it moves between two output levels. This nonlinearity is commonly associated with external data skew, but this effect is minimized by using the on-board registers of the AD9712B/AD9713B converters (see Digital Inputs/Timing section). The majority of the glitch impulse, shown below, is produced as the current in the R-2R ladder network settles, and is fairly constant over the full-scale range of the DAC. The fast transients which form the glitch impulse appear as high-frequency spurs in the output spectrum.

While it is difficult to predict the effects of glitch on the output waveform, slew rate limitations translate directly into harmonics. This makes slew rate the dominant effect in ac linearity of the DAC. Applications in which the ratio of analog frequency (f_A) to clock frequency (f_C) is relatively high will benefit from the high slew rate and low output capacitance of the AD9712B/AD9713B devices.

Another concern in DDS applications is the presence of aliased harmonics in the output spectrum. Aliased harmonics appear as spurs in the output spectrum at frequencies which are determined by:

$$MfA \pm Nf_C$$

where M and N are integers.

The effects of these spurs are most easily observed in applications where f_A is nearly equal to an integer fraction of the clock rate. This condition causes the aliased harmonics to fold near the fundamental output frequency (see Performance Curves.)

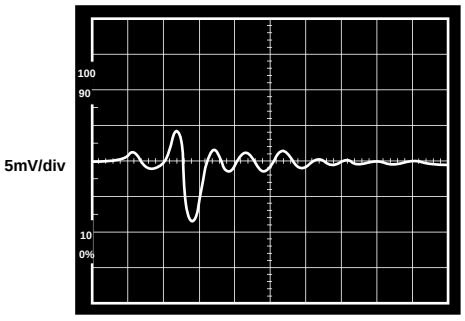


Figure 7. AD9712B/AD9713B Glitch Impulse

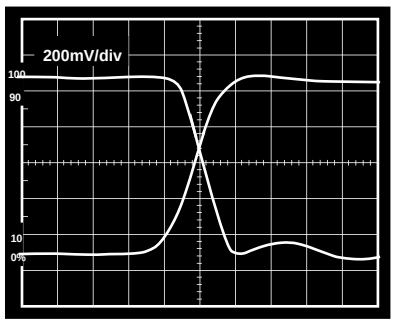


Figure 8. Rise and Fall Characteristics

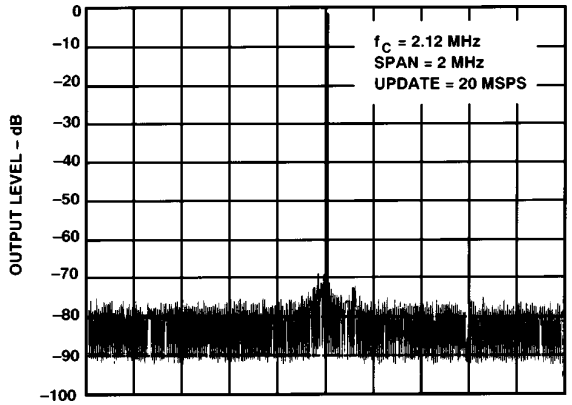


Figure 9a.

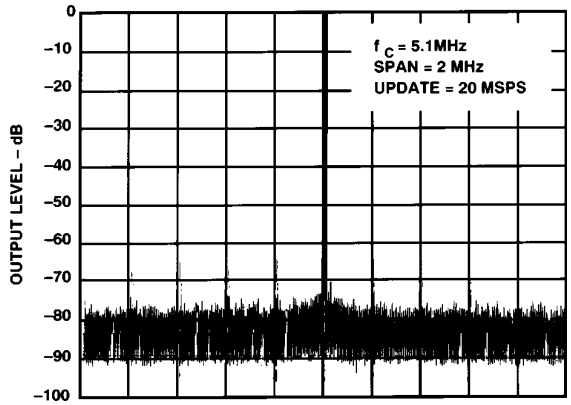


Figure 9b.

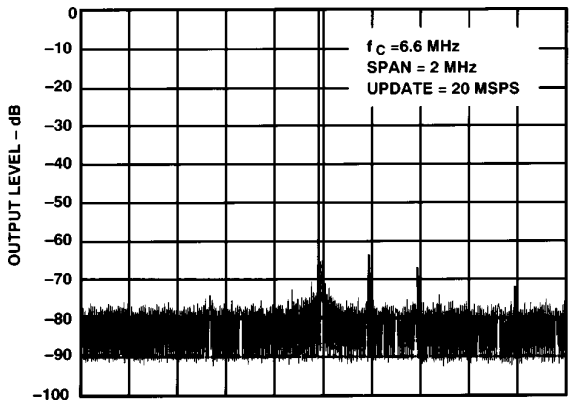


Figure 9c.

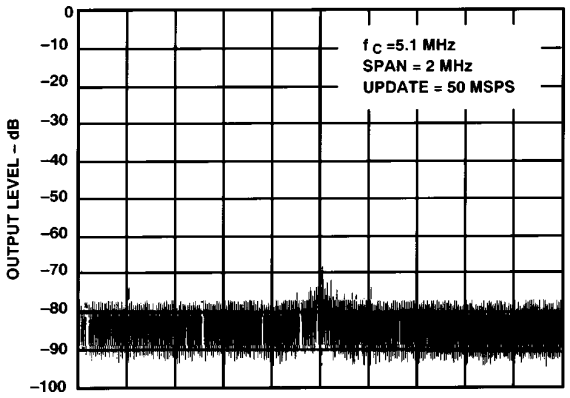


Figure 9d.

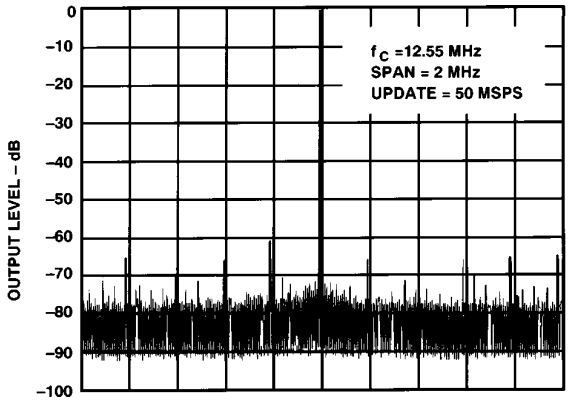


Figure 9e.

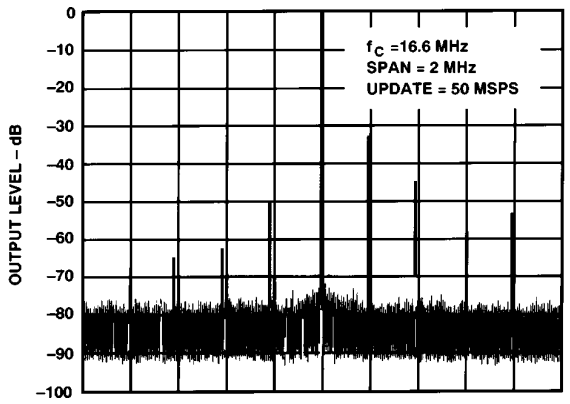


Figure 9f.

Figure 9. Typical Spectral Performance

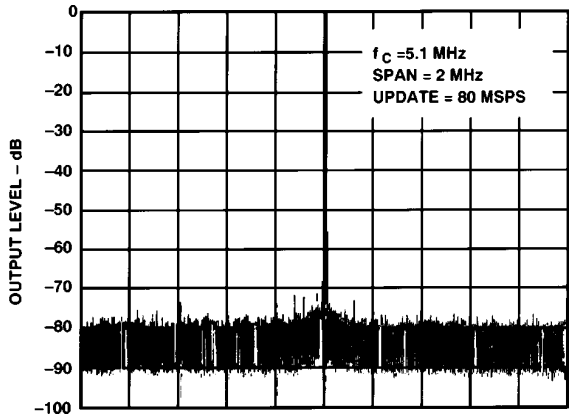


Figure 10a.

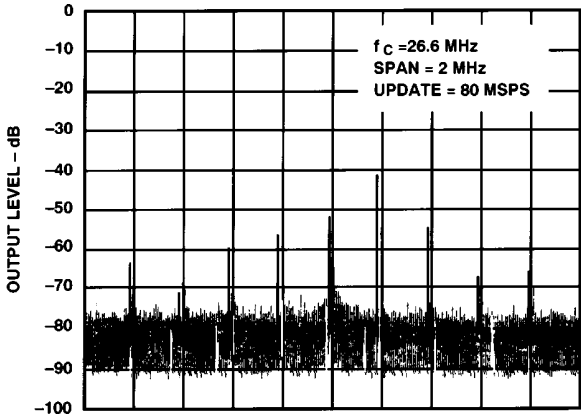


Figure 10c.

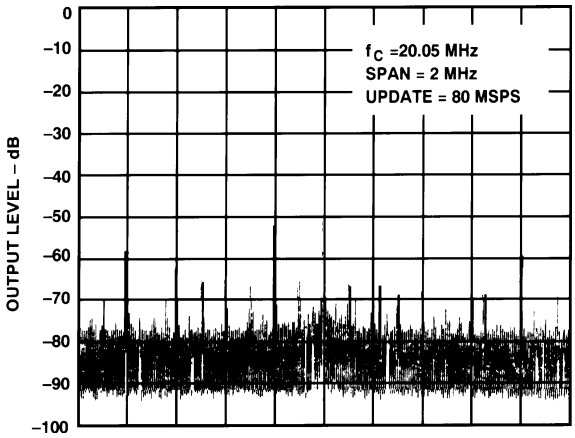


Figure 10b.

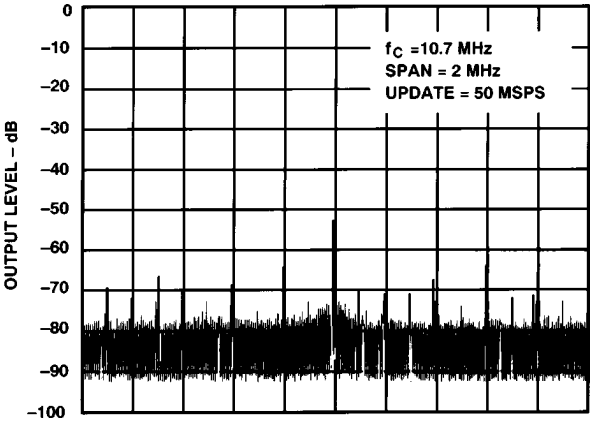


Figure 10d.

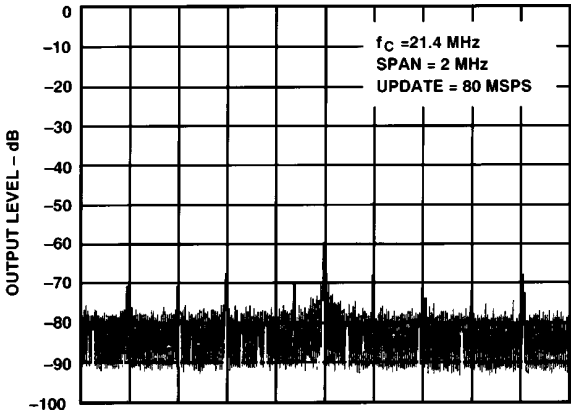
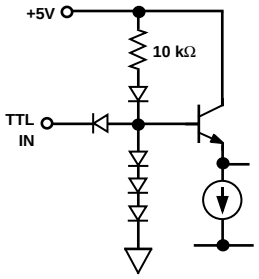
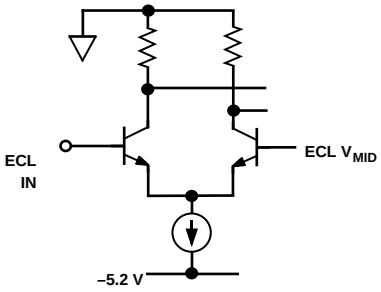


Figure 10e.

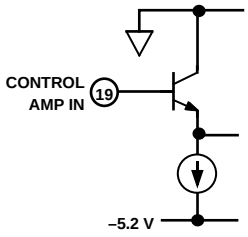
Figure 10. Typical Spectral Performance



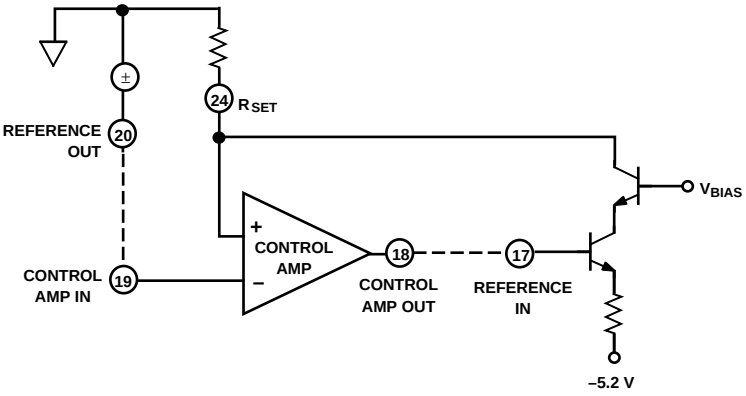
TTL Input Buffer



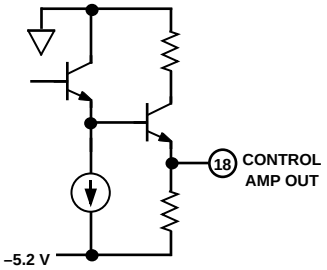
ECL Input Buffer



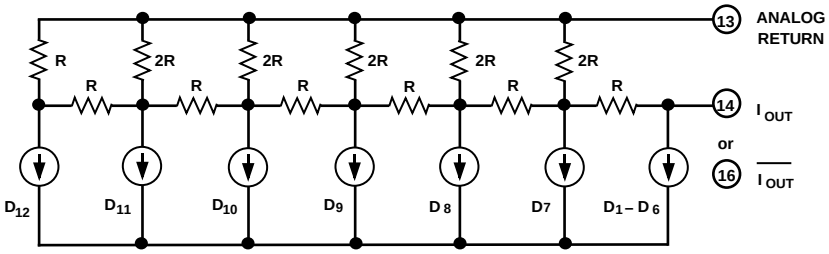
Control Amplifier Input



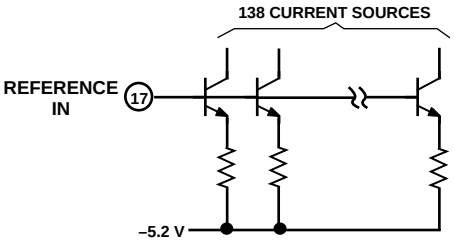
Full-Scale Current Control Loop



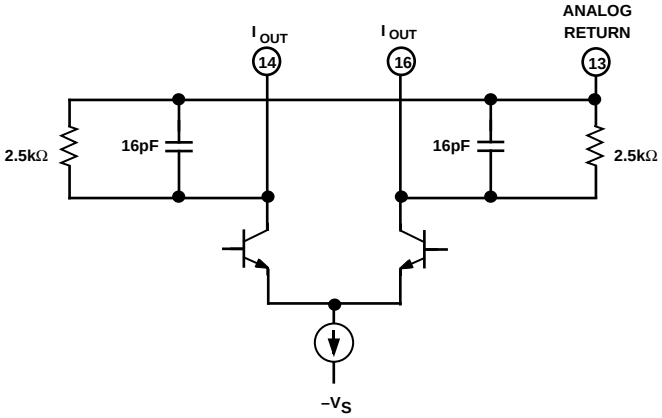
Control Amp Output



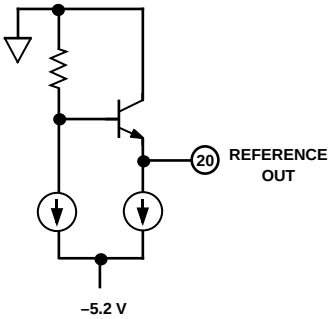
R-2R DAC (for 6 LSBs)



Reference Input



Output Circuit



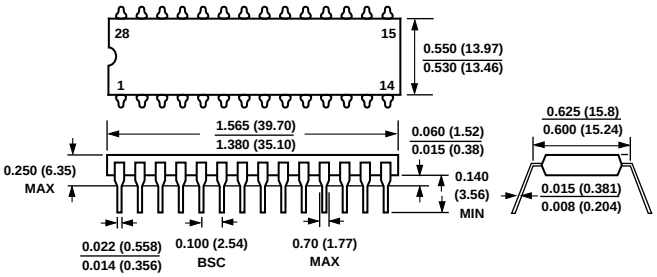
Reference Output

Figure 11. Equivalent Circuits

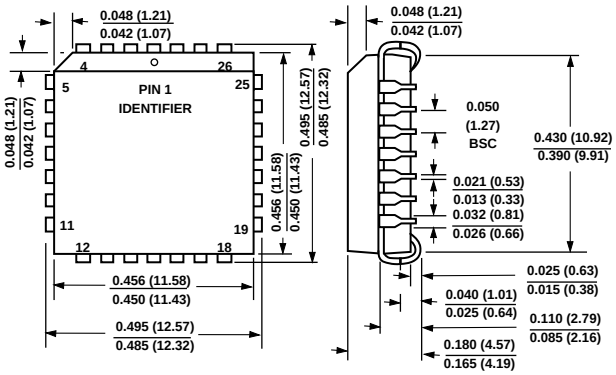
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

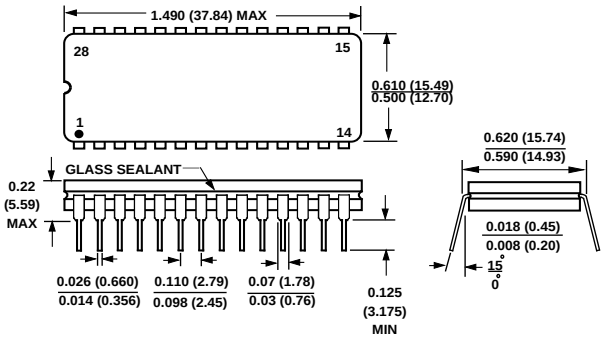
28-Pin Plastic DIP (Suffix N)



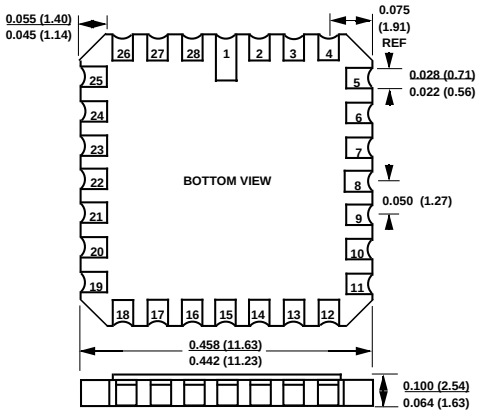
28-Pin Plastic Leaded Chip Carrier (Suffix P)



28-Pin Cerdip (Suffix Q)



28-Pin LCC Package (Suffix E)



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