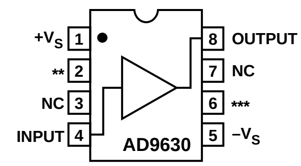
Low Distortion 750 MHz Closed-Loop Buffer Amp

AD9630*

FEATURES
Excellent Gain Accuracy: 0.99 V/V
Wide Bandwidth: 750 MHz
Slew Rate: 1200 V/μs
Low Distortion
–65 dBc @ 20 MHz
–80 dBc @ 4.3 MHz
Settling Time
5 ns to 0.1%
8 ns to 0.02%
Low Noise: 2.4 nV/√Hz
Improved Source for CLC-110

APPLICATIONS
IF/Communications
Impedance Transformations
Drives Flash ADCs
Line Driving

PIN CONFIGURATION



NC = NO CONNECT

**OPTIONAL $+V_S$ ***OPTIONAL $-V_S$

NOTE: FOR BEST SETTLING TIME PERFORMANCE USE OPTIONAL POWER SUPPLIES. ALL SPECIFICATIONS ARE BASED ON USING SINGLE $\pm V_S$ CONNECTIONS, EXCEPT FOR SETTLING TIME TO 0.02% AND SMALL SIGNAL S21. CONSULT THE FACTORY FOR VERSIONS WITH OPTIONAL POWER SUPPLY PINS DISCONNECTED INTERNAL TO THE PACKAGE.

GENERAL DESCRIPTION

The AD9630 is a monolithic buffer amplifier that utilizes a patented, innovative, closed-loop design technique to achieve exceptional gain accuracy, wide bandwidth, and low distortion. Slew rate limiting has been overcome as indicated by the 1200 V/μs slew rate; this improvement allows the user greater flexibility in wideband and pulse applications. The second harmonic distortion terms for an analog input tone of 4.3 MHz and 20 MHz are –80 dBc and –66 dBc, respectively. Clearly, the AD9630 establishes a new standard by combining outstanding dc and dynamic performance in one part.

The large signal bandwidth, low distortion over frequency, and drive capabilities of the AD9630 make the buffer an ideal flash ADC driver. The AD9630 provides better signal fidelity than many of the flash ADCs that it has been designed to drive.

Other applications that require increased current drive at unity voltage gain (such as cable driving) benefit from the AD9630's performance.

The AD9630 is available in plastic DIP (N) and SOIC (R).

*Protected under U.S. patent numbers 5,150,074 and 5,537,079.

REV. B

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AD9630–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (unless otherwise noted, $\pm V_S = \pm 5$ V; $R_{IN} = 50\ \Omega$, $R_{LOAD} = 100\ \Omega$)

Parameter	Conditions	Temp	Test Level	AD9630AN/AR Min	Typ	Max	Units
DC SPECIFICATIONS							
Output Offset Voltage		+25°C	I	–8	±3	+8	mV
Offset Voltage TC		Full	IV	–40	±8	+40	µV/°C
Input Bias Current		+25°C	I	–25	±2	+25	µA
Bias Current TC		Full	IV	–100	±20	+100	nA/°C
Input Resistance		+25 to T_{MAX}	II	300	450		kΩ
		T_{MIN}	VI	150	250		kΩ
Input Capacitance		+25°C	V		1.0		pF
Gain	V_{OUT} = 2 V p-p	+25 to T_{MAX}	II	0.983	0.990		V/V
	V_{OUT} = 2 V p-p	T_{MIN}	VI	0.980	0.985		V/V
Output Voltage Range		Full	VI	+3.2	±3.6	–3.2	V
Output Current (50 Ω Load)		+25 to T_{MAX}	II	50			mA
		T_{MIN}	VI	40			mA
Output Impedance	At DC	+25°C	V		0.6		Ω
PSRR	$\Delta V_S = \pm 5\%$	Full	VI	44	55		dB
DC Nonlinearity	±2 V Full Scale	+25°C	V		0.03		%
FREQUENCY DOMAIN							
Bandwidth (–3 dB)							
Small Signal	$V_O \leq 0.7$ V p-p	T_{MIN} to +25	II	400	750		MHz
	$V_O \leq 0.7$ V p-p	T_{MAX}	II	330	550		MHz
Large Signal	V_O = 5 V p-p	T_{MIN} to +25	V		120		MHz
	V_O = 5 V p-p	T_{MAX}	V		105		MHz
Output Peaking	≤200 MHz	Full	II		0.4	1.2	dB
Output Rolloff	≤200 MHz	Full	II		0	0.3	dB
Group Delay	DC to 150 MHz	+25°C	V		0.7		ns
Linear Phase Deviation	DC to 150 MHz	+25°C	V		0.7		Degrees
2nd Harmonic Distortion	2 V p-p; 4.3 MHz	Full	IV		–80	–73	dBc
	2 V p-p; 20 MHz	Full	IV		–66	–58	dBc
	2 V p-p; 50 MHz	Full	II		–52	–43	dBc
3rd Harmonic Distortion	2 V p-p; 4.3 MHz	Full	IV		–86	–79	dBc
	2 V p-p; 20 MHz	Full	IV		–75	–68	dBc
	2 V p-p; 50 MHz	T_{MIN} to +25	II		–47	–41	dBc
	2 V p-p; 50 MHz	T_{MAX}	II		–46	–40	dBc
Spectral Input Noise Voltage	10 MHz	+25°C	V		2.4		$nV/\sqrt{Hz}$
Integrated Output Noise	100 kHz – 200 MHz	+25°C	V		32		µV
TIME DOMAIN							
Slew Rate	V_{OUT} = 5 V Step	+25°C	IV	700	1200		V/µs
Rise/Fall Time	V_{OUT} = 1 V Step	+25°C	IV		1.1	1.7	ns
	V_{OUT} = 1 V Step	T_{MIN} to T_{MAX}	IV		1.3	1.9	ns
	V_{OUT} = 5 V Step	+25°C	IV		4.2	5.7	ns
	V_{OUT} = 5 V Step	T_{MIN} to T_{MAX}	IV		5.0	6.5	ns
Overshoot Amplitude	V_{OUT} = 2 V Step	Full	IV		2	12	%
Settling Time							
To 0.1%	V_{OUT} = 2 V Step	T_{MIN} to +25	IV		6	10	ns
	V_{OUT} = 2 V Step	T_{MAX}	IV		7	12	ns
To 0.02%[4]	V_{OUT} = 2 V Step	T_{MIN} to +25	IV		8		ns
	V_{OUT} = 2 V Step	T_{MAX}	V		12		ns
Differential Gain	4.4 MHz	+25°C	V		0.015		%
Differential Phase	4.4 MHz	+25°C	V		0.025		Degree
SUPPLY CURRENTS							
V_{CC} ($+I_S$)	V_{CC} = +5 V	Full	II		19	26	mA
V_{EE} ($-I_S$)	V_{EE} = –5 V	Full	II		19	26	mA

NOTES

[1]Short-term settling with 50 Ω source impedance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . ±7 V
Continuous Output Current[2] . . . . 70 mA
Temperature Range over Which Specifications Apply
AD9630AN/AR . . . . –40°C to +85°C
Lead Soldering Temperature (10 sec) . . . . +300°C
Storage Temperature
AD9630AN/AR . . . . –65°C to +150°C
Junction Temperature[3]
AD9630AN/AR . . . . +150°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Output is short-circuit protected to ground, but not to supplies. Prolonged short circuit to ground may affect device reliability.
[3]Typical thermal impedances (part soldered onto board): Plastic DIP (N): θ_{JA} = 110°C/W; θ_{JC} = 30°C/W; SOIC (R): θ_{JA} = 155°C/W; θ_{JC} = 40°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9630AN	–40°C to +85°C	8-Lead Plastic DIP	N-8
AD9630AR	–40°C to +85°C	8-Lead SOIC	SO-8
AD9630AR-REEL	–40°C to +85°C	13" Tape and Reel	SO-8

EXPLANATION OF TEST LEVELS

Test Level

I 100% Production tested.

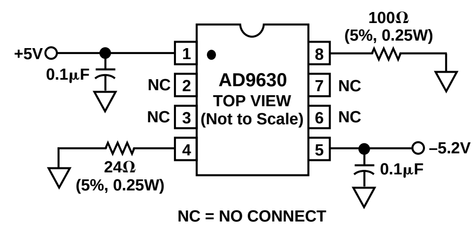
II 100% Production tested at +25°C and sample tested at specified temperatures. AC testing of AN and AR grades done on sample basis only.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Typical value.

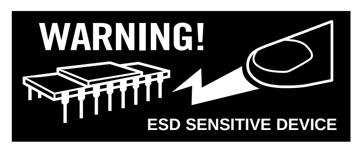
VI S Versions are 100% production tested at temperature extremes. Other grades are sample tested at extremes.



AD9630 Burn-In Circuit

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9630 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



THEORY OF OPERATION

The AD9630 is a wide-bandwidth, closed-loop, unity-gain buffer that makes use of a new voltage-feedback architecture. This architecture brings together wide bandwidth and high slew rate along with exceptional dc linearity. Most previous wide-bandwidth buffers achieved their bandwidth by utilizing an open-loop topology which sacrificed both dc linearity and frequency distortion when driven into low load impedances. The design's high loop correction factor radically improves dc linearity and distortion characteristics without diminishing bandwidth. This, in combination with high slew rate, results in exceptionally low distortion over a wide frequency range.

The AD9630 is an excellent choice to drive high speed and high resolution analog-to-digital converters. Its output stage is designed to drive high speed flash converters with minimal or no series resistance. A current booster built into the output driver helps to maintain low distortion.

Parasitic or load capacitance (>7 pF) connected directly to the AD9630 output will result in frequency peaking. A small series resistor (R_S) connected between the buffer output and capacitive load will negate this effect. Figure 1 shows the optimal value of R_S as a function of C_L to obtain the flattest frequency response. Figure 2 illustrates frequency response for various capacitive loads utilizing the recommended R_S.

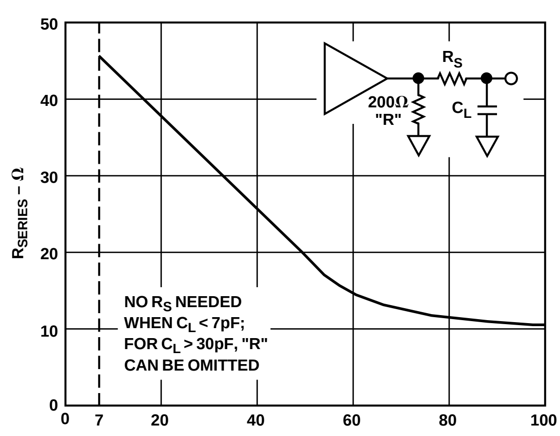


Figure 1. Recommended R_S vs. C_L

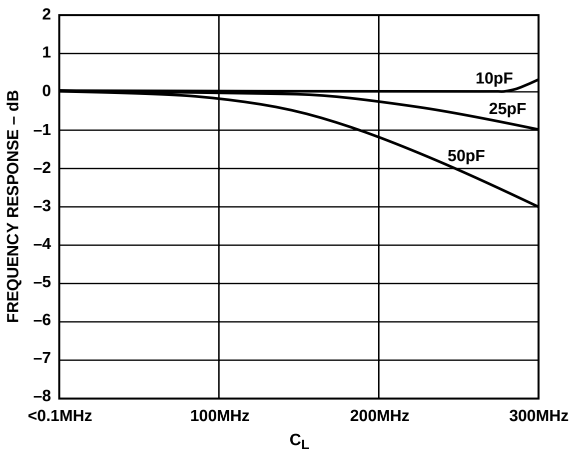


Figure 2. Frequency Response vs. C_L with Recommended R_S

In pulse mode applications, with R_S equal to approximately 12 Ω, capacitive loads of up to 50 pF can be driven with minimal settling time degradation.

The output stage has short circuit protection to ground. The output driver will shut down if more than approximately 130 mA of instantaneous sink or source current is reached. This level of current ensures that output clipping will not result when driving heavy capacitive loads during high slew conditions, although average load currents above 70 mA may reduce device reliability.

LAYOUT CONSIDERATIONS

Due to the high frequency operation of the AD9630 attention to board layout is necessary to achieve optimum dynamic performance. A two ounce copper ground plane on the top side of the board is recommended; it should cover as much of the board as possible with appropriate openings for supply decoupling capacitors as well as for load and source termination resistors, (see Figure 3).

Optimum settling time and ac performance results will be achieved with surface mount 0.1 µF supply decoupling ceramic chip capacitors mounted within 50 mils of the corresponding device pins with the other side soldered directly to the ground plane. For best high resolution (<0.02%) settling times, the optional power supply pins should be decoupled as shown above. If the optional power supply pins are not used, they should be left open.

If surface mount capacitors cannot be used, radial lead ceramic capacitors with leads less than 30 mils long are recommended. Low frequency power supply decoupling is necessary and can be accomplished with 4.7 µF tantalum capacitors mounted within 0.5 inches of the supply pins. Due to the series inductance of these capacitors interacting with the 0.1 µF capacitors and power supply leads, high frequency oscillations might appear on the device output. To avoid this occurrence, the power supply leads should be tightly twisted (if appropriate). Ferrite beads mounted between the tantalum and ceramic capacitors will serve the same purpose.

All unused pins (except the optional power supply pins) should be connected to ground to reduce pin-to-pin capacitive coupling and prevent external RF interference. If the source and drive electronics require "remote" operation (> 1 inch from the AD9630), the PC board line impedances should be matched with the buffer input and output resistances. Basic microstrip techniques should be observed. R_{IN} and R_S should be connected as close to the AD9630 as possible.

With only minimal pulse overshoot and ringing, the AD9630 can drive terminated cables directly without the use of an output termination resistor (R_S). Termination resistors (R_S and R_{IN}) can be either standard carbon composition or microwave type. For matching characteristic impedances, precision microwave resistors of 1% or better tolerance are preferred.

The AD9630 should be soldered directly to the PC board with as little vertical clearance as possible. The use of zero insertion sockets is strongly discouraged because of the high effective pin inductances. Use of this type socket will result in peaking and possibly induce oscillation.

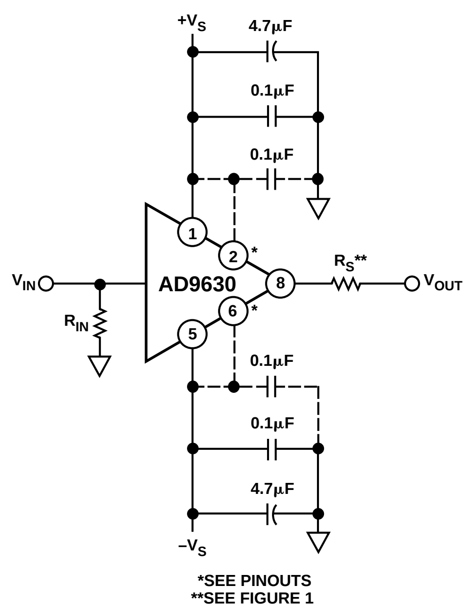


Figure 3. AD9630 Application Circuit

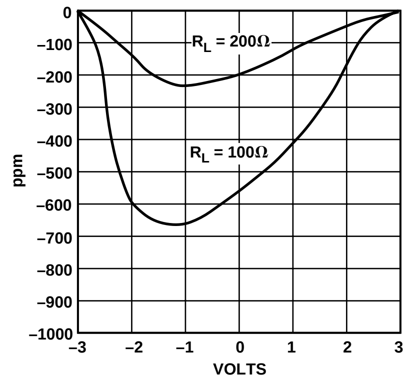


Figure 4. Endpoint DC Linearity

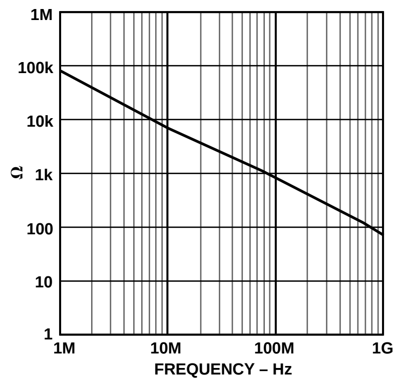


Figure 5. Input Impedance

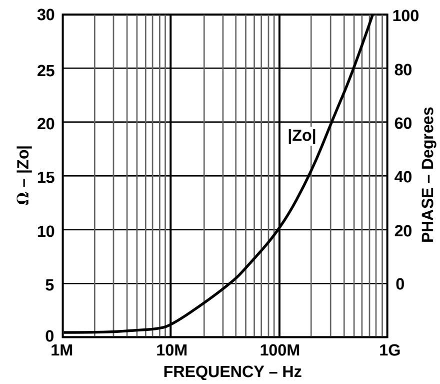


Figure 6. Output Impedance

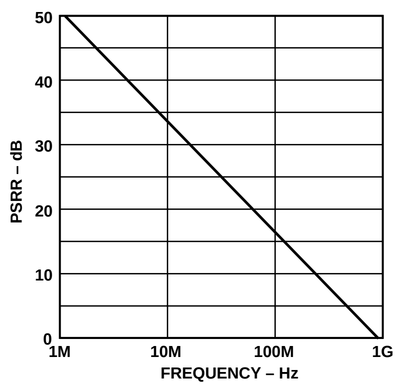


Figure 7. PSRR vs. Frequency

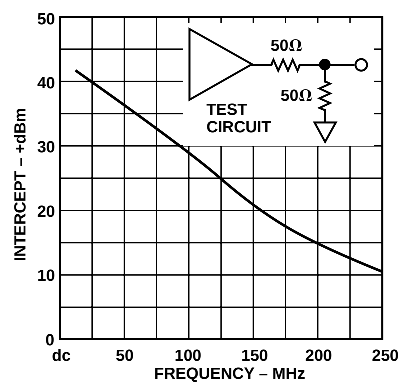


Figure 8. 2-Tone Intermodulation Distortion

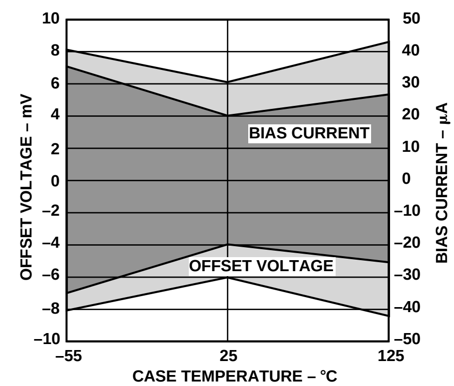


Figure 9. Offset Voltage and Bias Current vs. Temperature

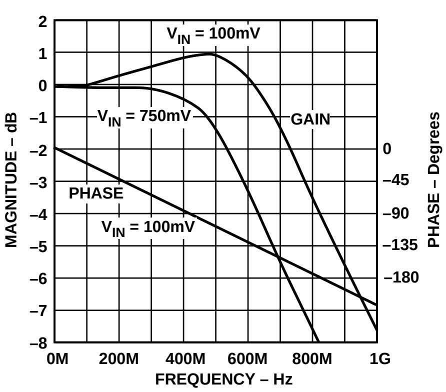


Figure 10 . Forward Gain and Phase

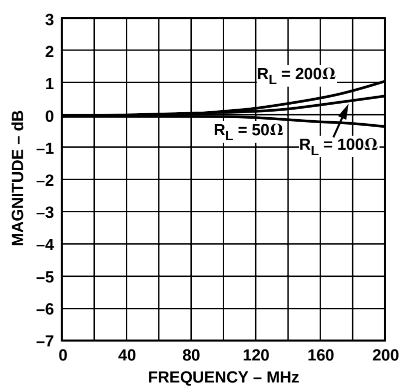


Figure 11. Frequency Response vs. R_{LOAD}

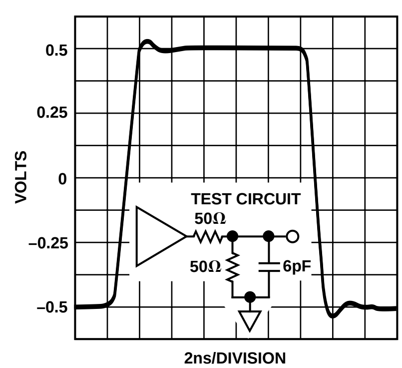


Figure 12. Small-Signal Pulse Response

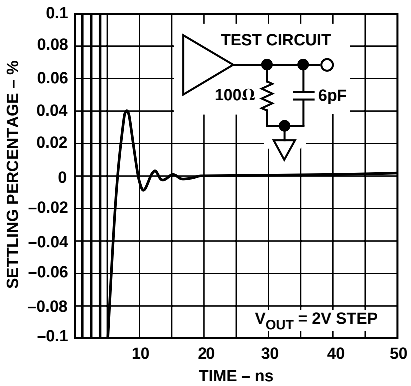


Figure 13. Short-Term Settling Time

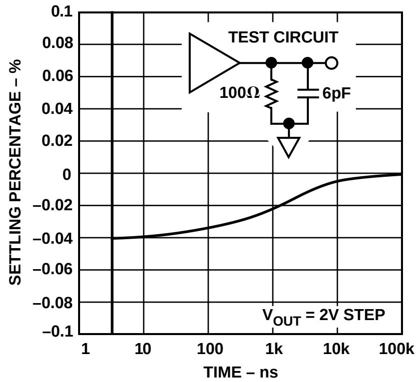


Figure 14. Long-Term Settling Time

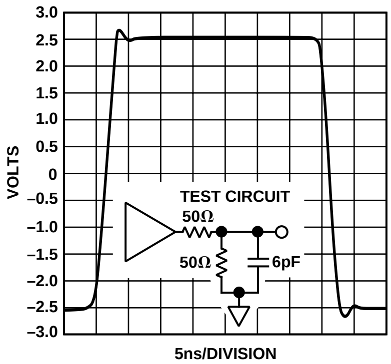


Figure 15. Large-Signal Pulse Response

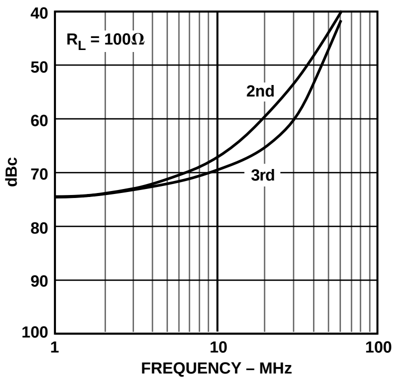


Figure 16. Harmonic Distortion V_{OUT} = 4 V p-p

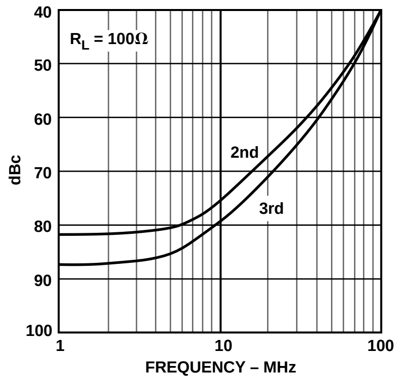
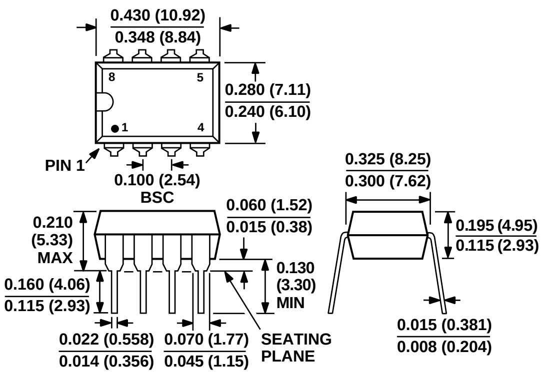


Figure 17. Harmonic Distortion V_{OUT} = 2 V p-p

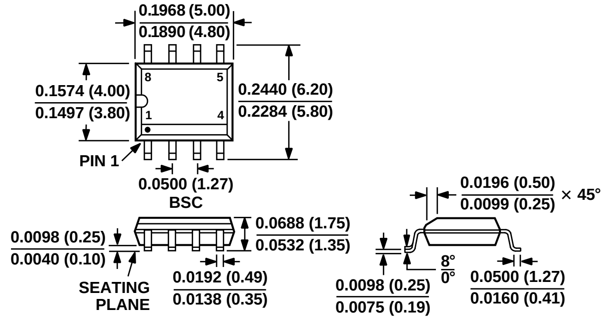
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic DIP (N-8)



8-Lead SOIC (SO-8)



C1401a–0–12/99 (rev. B)

PRINTED IN U.S.A.