14-Channel Clock Generator with Integrated 2.8 GHz VCO

Preliminary Technical Data

AD9516-0

FEATURES

Low Broadband Jitter, < 500 Femtoseconds RMS
On-Chip 2.60 GHz – 2.95 GHz VCO
Low Phase Noise, Integer-N Frequency Synthesizer
- **Digital or Analog PLL Lock Detect**
- **Programmable Delays in R and N path**
- **Supports Internal or External VCO**

Two Reference Clock Inputs, A and B
- **Frequencies to 250 MHz**
- **On-Chip Reference Clock Monitors**
- **Auto and Manual Switchover, Holdover**

Up to 14 Low Jitter Clock Drivers
- **Six LVPECL Outputs Operate to Max VCO Frequency**
- **Four/Eight LVDS/CMOS outputs run 1 GHz/250 MHz**

Programmable Dividers with Phase Offset
Programmable Delay on Four Channels
Serial Control Port
64-lead LFCSP package

APPLICATIONS

Low Jitter Clock Generation and Clock Distribution
Wired and Wireless Infrastructure
Base Stations, Optical Networks, Cable Head-Ends
Instrumentation and Imaging
Test Equipment, ATE
Clean Clocks for ADCs, DACs, DDSs, DDCs, DUCs, MxFEs
Clock Cleanup and Distribution for Line Cards

GENERAL DESCRIPTION

The AD9516-0 generates up to fourteen output clocks from a single input reference frequency. Integrated on chip is a complete PLL with VCO, programmable dividers, adjustable delay blocks, and multiple output logic stages. Sub-picosecond jitter performance is maintained using on-chip 2.60 – 2.95 GHz VCO. The AD9516 also supports the use of an external VCO/VCXO/VCSO up to 2.4 GHz.

The AD9516-0 features six LVPECL outputs (grouped in three pairs), which operate up to the maximum frequency of on-chip VCO. The remaining outputs are user-programmed as either LVDS (four max) or CMOS (eight max). The programmable outputs operate to 1 GHz in LVDS mode and to 250MHz in CMOS mode.

On-chip dividers may be set to any integer value, 1-32. In addition, the LVDS/CMOS channels use cascaded dividers for a maximum divide ratio of 1024. Each LVDS/CMOS channel also offers an adjustable delay from 1.5 ns to 10 ns, programmed as 64 steps.

The AD9516-0 is available in a 64-lead LFCSP and may be operated from a single 3.3 V supply. If an external VCO is used, the VCP pin may be set to a max value of 5.5V. The power supply to the LVPECL outputs may be varied to support 2.5V or 3.3V LVPECL outputs. The AD9516-0 operates over the standard industrial range of-40°C to +85°C.

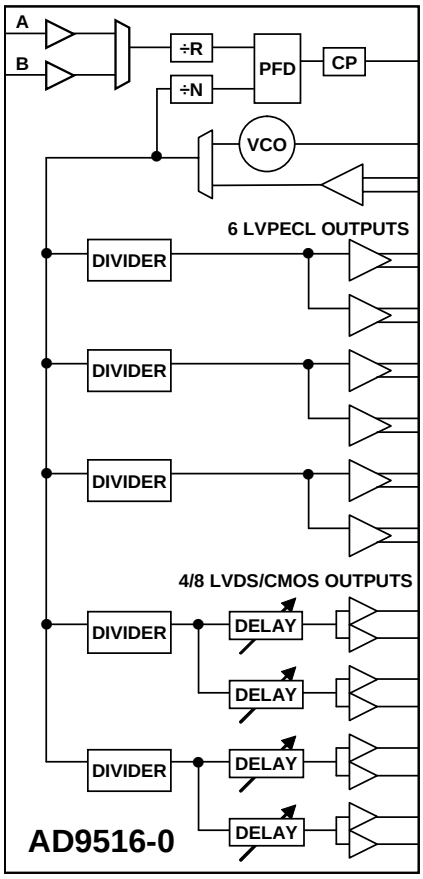

Figure 1. Basic Block Diagram

Rev. prA

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OUTLINE DIMENSIONS

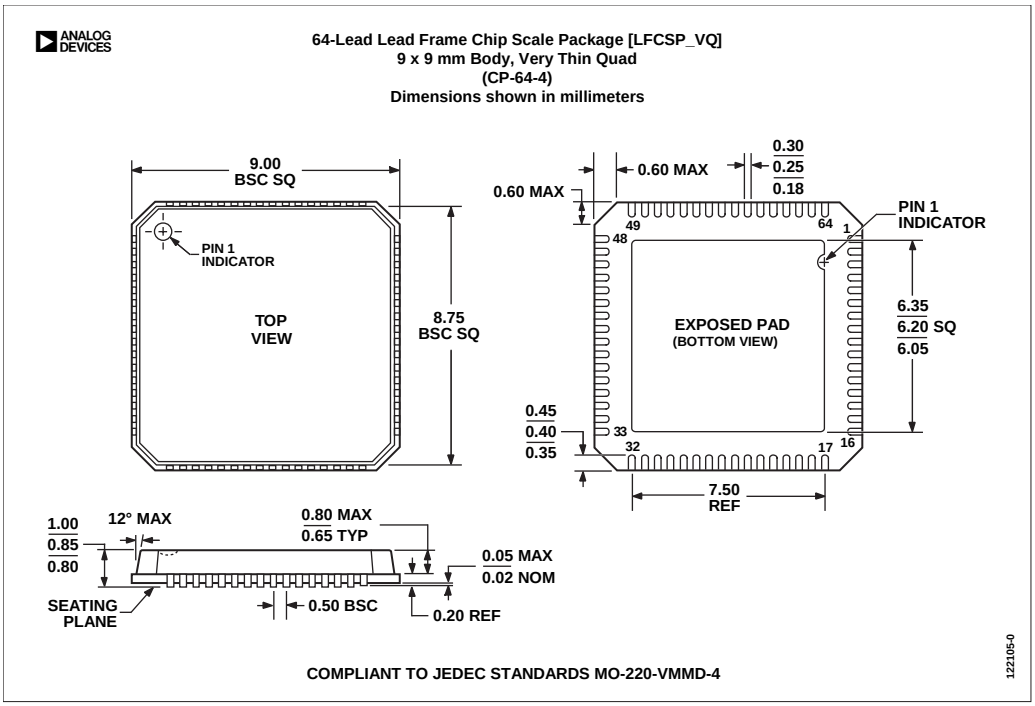

Figure 2. Outline Dimensions

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