Description

The ACS8520 is a highly integrated, single-chip solution for the Synchronous Equipment Timing Source (SETS) function in a SONET or SDH Network Element. The device generates SONET or SDH Equipment Clocks (SEC) and Frame Synchronization clocks. The ACS8520 is fully compliant with the required international specifications and standards.

The device supports Free-run, Locked and Holdover modes. It also supports all three types of reference clock source: recovered line clock, PDH network, and node synchronization. The ACS8520 generates independent SEC and BITS/SSU clocks, an 8 kHz Frame Synchronization clock and a 2 kHz Multi-Frame Synchronization clock.

Two ACS8520 devices can be used together in a Master/Slave configuration mode allowing system protection against a single ACS8520 failure.

A microprocessor port is incorporated, providing access to the configuration and status registers for device setup and monitoring. The ACS8520 supports IEEE 1149.1[5] JTAG boundary scan.

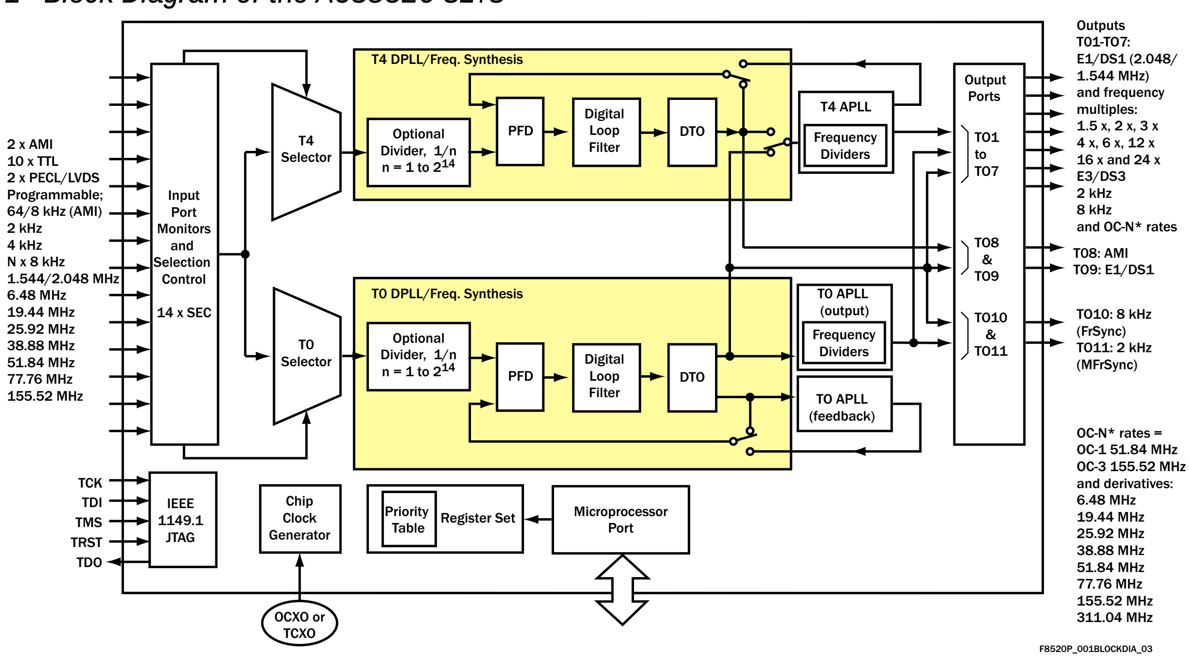
The user can choose between OCXO or TCXO to define the Stratum and/or Holdover performance required.

Features

- Suitable for Stratum 3, 4E, 4 and SONET Minimum Clock (SMC) or SONET/SDH Equipment Clock (SEC) applications
- Meets Telcordia 1244-CORE[19] Stratum 3 and GR-253[17], and ITU-T G.813[11] Options I and II specifications
- Accepts 14 individual input reference clocks, all with robust input clock source quality monitoring.
- Simultaneously generates nine output clocks, plus two Sync pulse outputs
- Absolute Holdover accuracy better than 3 x 10^{-10} (manual), 7.5 x 10^{-14} (instantaneous); Holdover stability defined by choice of external XO
- Programmable PLL bandwidth, for wander and jitter tracking/attenuation, 0.1 Hz to 70 Hz in 10 steps
- Automatic hit-less source switchover on loss of input
- Microprocessor interface - Intel, Motorola, Serial, Multiplexed, or boot from EPROM
- Output phase adjustment in 6 ps steps up to ±200 ns
- IEEE 1149.1 JTAG Boundary Scan
- Single 3.3 V operation. 5 V tolerant
- Available in LQFP 100 package
- Lead (Pb) - free version available (ACS8520T), RoHS and WEEE compliant.

Block Diagram

Figure 1 Block Diagram of the ACS8520 SETS



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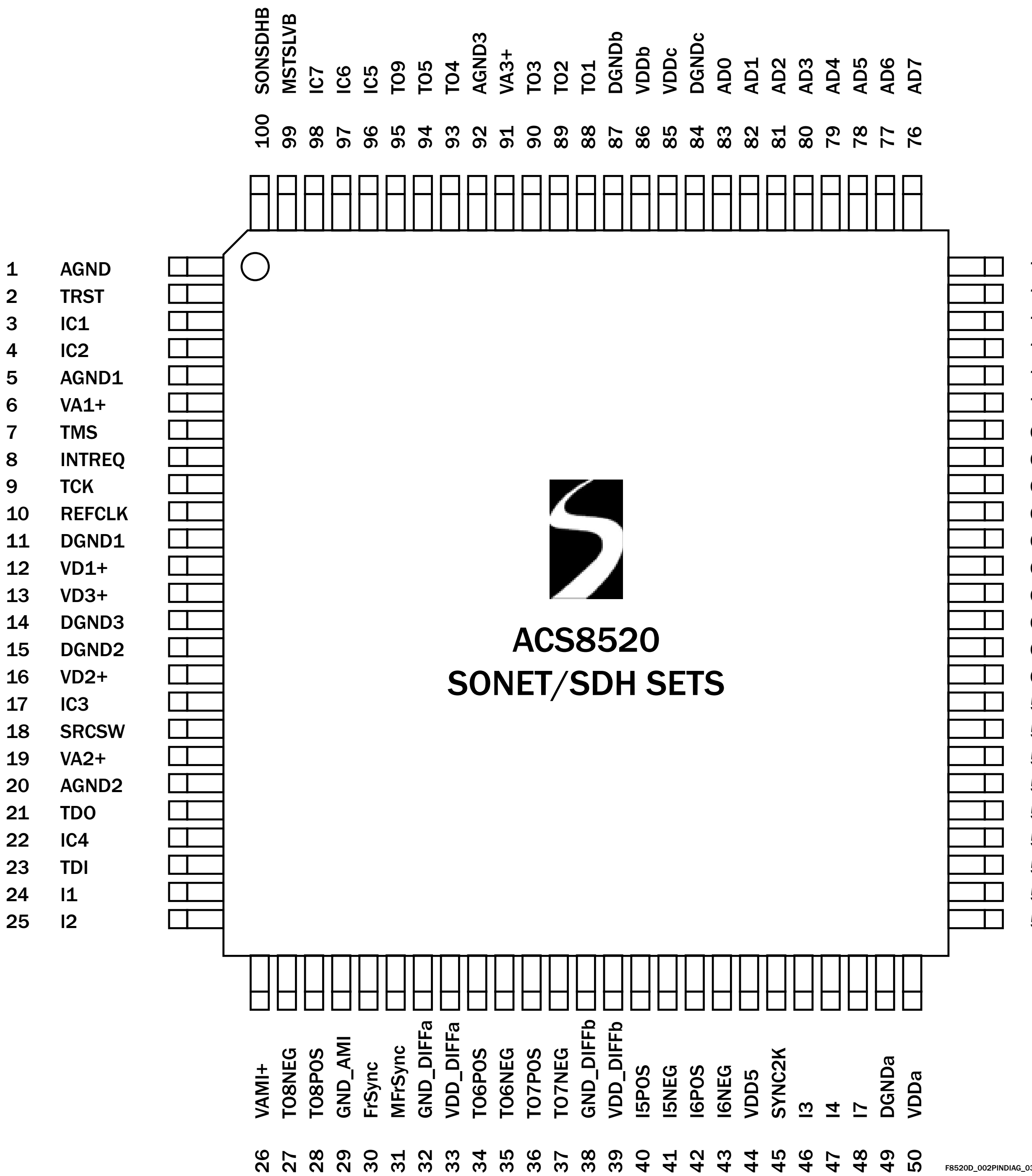
Pin Diagram

Figure 2 ACS8520 Pin Diagram Synchronous Equipment Timing Source for Stratum 3/4E/4 and SMC Systems



Pin Description

Table 1 Power Pins

Pin Number	Symbol	I/O	Type	Description
12, 13, 16	VD1+, VD3+, VD2+	P	-	Supply Voltage: Digital supply to gates in analog section, +3.3 Volts ±10%.
26	VAMI+	P	-	Supply Voltage: Digital supply to AMI output, +3.3 Volts ±10%.
33, 39	VDD_DIFFa, VDD_DIFFb	P	-	Supply Voltage: Digital supply for differential ports, +3.3 Volts ±10%.
44	VDD5	P	-	Digital Supply for +5 Volts Tolerance to Input Pins. Connect to +5 Volts (±10%) for clamping to +5 Volts. Connect to VDD for clamping to +3.3 Volts. Leave floating for no clamping, input pins tolerant up to +5.5 Volts.
50, 61, 85, 86	VDDa, VDDd, VDDc, VDDb	P	-	Supply Voltage: Digital supply to logic, +3.3 Volts ±10%.
6	VA1+	P	-	Supply Voltage: Analog supply to clock multiplying PLL, +3.3 Volts ±10%.
19, 91	VA2+, VA3+	P	-	Supply Voltage: Analog supply to output PLLs, +3.3 Volts ±10%.
11, 14, 15,	DGND1, DGND3, DGND2,	P	-	Supply Ground: Digital ground for components in PLLs.
49, 62, 84, 87	DGNDa, DGNDd, DGNDc, DGNDb	P	-	Supply Ground: Digital ground for logic.
29	GND_AMI	P	-	Supply Ground: Digital ground for AMI output.
32, 38	GND_DIFFa, GND_DIFFb	P	-	Supply Ground: Digital ground for differential ports.
1, 5, 20, 92	AGND, AGND1, AGND2, AGND3	P	-	Supply Ground: Analog grounds.

Note...I = Input, O = Output, P = Power, TTL^U = TTL input with pull-up resistor, TTL_D = TTL input with pull-down resistor.

Table 2 Internally Connected Pins

Pin Number	Symbol	I/O	Type	Description
3, 4, 17, 22, 96, 97, 98	IC1, IC2, IC3, IC4, IC5, IC6, IC7	-	-	Internally Connected: Leave to Float.

Table 3 Other Pins

Pin Number	Symbol	I/O	Type	Description
2	TRST	I	TTL_D	JTAG Control Reset Input: TRST = 1 to enable JTAG Boundary Scan mode. TRST = 0 for Boundary Scan stand-by mode, still allowing correct device operation. If not used connect to GND or leave floating.
7	TMS	I	TTL^U	JTAG Test Mode Select: Boundary Scan enable. Sampled on rising edge of TCK. If not used connect to VDD or leave floating.
8	INTREQ	O	TTL/CMOS	Interrupt Request: Active *High*/*Low* software Interrupt output.
9	TCK	I	TTL_D	JTAG Clock: Boundary Scan clock input. If not used connect to GND or leave floating.
10	REFCLK	I	TTL	Reference Clock: 12.800 MHz (refer to section headed Local Oscillator Clock).
18	SRCSW	I	TTL_D	Source Switching: Force Fast Source Switching. See "Fast External Switching Mode-SCRSW Pin" on page 15.
21	TDO	O	TTL/CMOS	JTAG Output: Serial test data output. Updated on falling edge of TCK. If not used leave floating.
23	TDI	I	TTL^U	JTAG Input: Serial test data Input. Sampled on rising edge of TCK. If not used connect to VDD or leave floating.
24	I1	I	AMI	Input Reference 1: Composite clock 64 kHz + 8 kHz.
25	I2	I	AMI	Input Reference 2: Composite clock 64 kHz + 8 kHz.
27	TO8NEG	O	AMI	Output Reference 8: Composite clock, 64 kHz + 8 kHz negative pulse.
28	TO8POS	O	AMI	Output Reference 8: Composite clock, 64 kHz + 8 kHz positive pulse.
30	FrSync	O	TTL/CMOS	Output Reference 10: 8 kHz Frame Sync output.
31	MFrSync	O	TTL/CMOS	Output Reference 11: 2 kHz Multi-Frame Sync output.
34, 35	TO6POS, TO6NEG	O	LVDS/PECL	Output Reference 6: Programmable, default 38.88 MHz, default type LVDS.
36, 37	TO7POS, TO7NEG	O	PECL/LVDS	Output Reference 7: Programmable, default 19.44 MHz, default type PECL.
40, 41	I5POS, I5NEG	I	LVDS/PECL	Input Reference 5: Programmable, default 19.44 MHz, default type LVDS.
42, 43	I6POS, I6NEG	I	PECL/LVDS	Input Reference 6: Programmable, default 19.44 MHz, default type PECL.
45	SYNC2K	I	TTL_D	External Sync input: 2 kHz, 4 kHz or 8 kHz for frame alignment.
46	I3	I	TTL_D	Input Reference 3: Programmable, default 8 kHz.
47	I4	I	TTL_D	Input Reference 4: Programmable, default 8 kHz.
48	I7	I	TTL_D	Input Reference 7: Programmable, default 19.44 MHz.
51	I8	I	TTL_D	Input Reference 8: Programmable, default 19.44 MHz.
52	I9	I	TTL_D	Input Reference 9: Programmable, default 19.44 MHz.
53	I10	I	TTL_D	Input Reference 10: Programmable, default 19.44 MHz.

Table 3 Other Pins (cont...)

Pin Number	Symbol	I/O	Type	Description
54	I11	I	TTL_D	Input Reference 11: Programmable, default (Master mode) 1.544/2.048 MHz, default (Slave mode) 6.48 MHz.
55	I12	I	TTL_D	Input Reference 12: Programmable, default 1.544/2.048 MHz.
56	I13	I	TTL_D	Input Reference 13: Programmable, default 1.544/2.048 MHz.
57	I14	I	TTL_D	Input Reference 14: Programmable, default 1.544/2.048 MHz.
58 - 60	UPSEL(2:0)	I	TTL_D	Microprocessor Select: Configures the interface for a particular microprocessor type at reset.
63 - 69	A(6:0)	I	TTL_D	Microprocessor Interface Address: Address bus for the microprocessor interface registers. A(0) is SDI in Serial mode - output in EPROM mode only. A(1) is CLKE in serial mode.
70	CSB	I	TTL^U	Chip Select (Active *Low*): This pin is asserted *Low* by the microprocessor to enable the microprocessor interface - output in EPROM mode only.
71	WRB	I	TTL^U	Write (Active *Low*): This pin is asserted *Low* by the microprocessor to initiate a write cycle. In Motorola mode, WRB = 1 for Read.
72	RDB	I	TTL^U	Read (Active *Low*): This pin is asserted *Low* by the microprocessor to initiate a read cycle.
73	ALE	I	TTL_D	Address Latch Enable: This pin becomes the address latch enable from the microprocessor. When this pin transitions from *High* to *Low*, the address bus inputs are latched into the internal registers. ALE = SCLK in Serial mode.
74	PORB	I	TTL^U	Power-On Reset: Master reset. If PORB is forced *Low*, all internal states are reset back to default values.
75	RDY	O	TTL/CMOS	Ready/Data Acknowledge: This pin is asserted *High* to indicate the device has completed a read or write operation.
76 - 83	AD(7:0)	IO	TTL_D	Address/Data: Multiplexed data/address bus depending on the microprocessor mode selection. AD(0) is SDO in Serial mode.
88	TO1	O	TTL/CMOS	Output Reference 1: Programmable, default 6.48 MHz.
89	TO2	O	TTL/CMOS	Output Reference 2: Programmable, default 38.88 MHz.
90	TO3	O	TTL/CMOS	Output Reference 3: Programmable, default 19.44 MHz.
93	TO4	O	TTL/CMOS	Output Reference 4: Programmable, default 38.88 MHz.
94	TO5	O	TTL/CMOS	Output Reference 5: Programmable, default 77.76 MHz.
95	TO9	O	TTL/CMOS	Output Reference 9: 1.544/2.048 MHz, as per ITU G.783[9] BITS requirements.
99	MSTSLVB	I	TTL^U	Master/Slave Select: Sets the state of the Master/Slave selection register, Reg. 34, Bit 1.
100	SONSDHB	I	TTL_D	SONET or SDH Frequency Select: Sets the initial power-up state (or state after a PORB) of the SONET/SDH frequency selection registers, Reg. 34, Bit 2 and Reg. 38, Bit 5, Bit 6 and Reg. 64 Bit 4.When set *Low*, SDH rates are selected (2.048 MHz etc.) and when set *High*, SONET rates are selected (1.544 MHz etc.) The register states can be changed after power-up by software.

Introduction

The ACS8520 is a highly integrated, single-chip solution for the SETS function in a SONET/SDH Network Element, for the generation of SEC and Frame/MultiFrame Synchronization pulses. Digital Phase Locked Loop (DPLL) and direct digital synthesis methods are used in the device so that the overall PLL characteristics are very stable and consistent compared to traditional analog PLLs.

In Free-run mode, the ACS8520 generates a stable, low-noise clock signal at a frequency to the same accuracy as the external oscillator, or it can be made more accurate via software calibration to within ±0.02 ppm. In Locked mode, the ACS8520 selects the most appropriate input reference source and generates a stable, low-noise clock signal locked to the selected reference. In Holdover mode, the ACS8520 generates a stable, low-noise clock signal, adjusted to match the last known good frequency of the last selected reference source. A high level of phase and frequency accuracy is made possible by an internal resolution of up to 54 bits and internal Holdover accuracy of up to 7.5×10^{-14} (instantaneous). In all modes, the frequency accuracy, jitter and drift performance of the clock meet the requirements of ITU G.736[7], G.742[8], G783[9], G.812[10], G.813[11], G.823[13],G.824[14] and Telcordia GR-253-CORE[17] and GR-1244-CORE[19].

The ACS8520 supports all three types of reference clock source: recovered line clock, PDH network synchronization timing, and node synchronization. The ACS8520 generates independent T0 and T4 clocks, an 8 kHz Frame Synchronization clock and a 2 kHz Multi-Frame Synchronization clock.

One key architectural advantage that the ACS8520 has over traditional solutions is in the use of DPLL technology for precise and repeatable performance over temperature or voltage variations and between parts. The overall PLL bandwidth, loop damping, pull-in range and frequency accuracy are all determined by digital parameters that provide a consistent level of performance. An Analog PLL (APLL) takes the signal from the DPLL output and provides a lower jitter output. The APLL bandwidth is set four orders of magnitude higher than the DPLL bandwidth. This ensures that the overall system performance still maintains the advantage of consistent behavior provided by the digital approach.

The DPLLs are clocked by the external Oscillator module (TCXO or OCXO) so that the Free-run or Holdover frequency stability is only determined by the stability of the external oscillator module. This second key advantage confines all temperature critical components to one well defined and pre-calibrated module, whose performance can be chosen to match the application; for example an TCXO for Stratum 3 applications.

All performance parameters of the DPLLs are programmable without the need to understand detailed PLL equations. Bandwidth, damping factor and lock range can all be set directly, for example. The PLL bandwidth can be set over a wide range, 0.1 Hz to 70 Hz in 18 steps, to cover all SONET/SDH clock synchronization applications.

The ACS8520 supports protection. Two ACS8520 devices can be configured to provide protection against a single ACS8520 failure. The protection maintains alignment of the two ACS8520 devices (Master and Slave) and ensures that both ACS8520 devices maintain the same priority table, choose the same reference input and generate the T0 clock, the 8 kHz Frame Synchronization clock and the 2 kHz Multi-Frame Synchronization clock with the same phase. The ACS8520 includes a multi-standard microprocessor port, providing access to the configuration and status registers for device setup and monitoring.

General Description

Overview

The following description refers to the Block Diagram (Figure 1 on page 1).

The ACS8520 SETS device has 14 input clocks, generates 11 output clocks, and has a total of 55 possible output frequencies. There are two main paths through the device: T0 and T4. Each path has an independent DPLL and APLL pair.

The T0 path is a high quality, highly configurable path designed to provide features necessary for node timing synchronization within a SONET/SDH network. The T4 path is a simpler and less configurable path designed to give a totally independent path for internal equipment synchronization. The device supports use of either or both paths, either locked together or independent.

Of the 14 input references, two are AMI composite clock, two are LVDS/PECL and the remaining ten are TTL/CMOS compatible inputs. All the TTL/CMOS are 3 V and 5 V compatible (with clamping if required by connecting the

VDD5 pin). The AMI inputs are ±1 V typically A.C. coupled. Refer to the electrical characteristics section for more information on the electrical compatibility and details. Input frequencies supported range from 2 kHz to 155.52 MHz.

Common E1, DS1, OC3 and sub-divisions are supported as spot frequencies that the DPLLs will directly lock to. Any input frequency, up to 100 MHz, that is a multiple of 8 kHz can also be locked to via an inbuilt programmable divider.

An input reference monitor is assigned to each of the 14 inputs. The monitors operate continuously such that at all times the status of all of the inputs to the device are known. Each input can be monitored for both frequency and activity, activity alone, or the monitors can be disabled.

The frequency monitors have a “hard” (rejection) alarm limit and a “soft” (flag only) alarm limit for monitoring frequency, whilst the reference is still within its allowed frequency band. Each input reference can be programmed with a priority number allowing references to be chosen according to the highest priority valid input. The two paths (T0 and T4) have independent priorities to allow completely independent operation of the two paths. Both paths operate either automatic or external source selection.

For automatic input reference selection, the T0 path has a more complex state machine than the T4 path.

The T0 and T4 PLL paths support the following common features:

- Automatic source selection according to input priorities and quality level
- Different quality levels (activity alarm thresholds) for each input
- Variable bandwidth, lock range and damping factor
- Direct PLL locking to common SONET/SDH input frequencies or any multiple of 8 kHz
- Automatic mode switching between Free-run, Locked and Holdover states
- Fast detection on input failure and entry into Holdover mode (holds at the last good frequency value)
- Frequency translation between input and output rates via direct digital synthesis
- High accuracy digital architecture for stable PLL dynamics combined with an APLL for low jitter final output clocks.

There are a number of features supported by the T0 path that are not supported by the T4 path, although these can also all be externally controlled by software.

The additional T0 features supported are:

- Non-revertive mode
- Phase Build-out on source switch (hit-less source switching)
- I/O phase offset control
- Greater programmable bandwidth from 0.1 Hz to 70 Hz in 10 steps (T4 path programmable bandwidth in 3 steps, 18, 35 and 70 Hz)
- Noise rejection on low frequency input
- Manual Holdover frequency control
- Controllable automatic Holdover frequency filtering
- Frame Sync pulse alignment.

Either the software or an internal state machine controls the operation of the DPLL in the T0 path. The state machine for the T4 path is very simple and cannot be manually/externally controlled, however the overall operation can be controlled by manual reference source selection. One additional feature of the T4 path is the ability to measure a phase difference between two inputs.

The T0 path DPLL always produces an output at 77.76 MHz to feed the APLL, regardless of the frequency selected at the output pins. The T4 path can be operated at a number of frequencies. This is to enable the generation of extra output frequencies, which cannot be easily related to 77.76 MHz. When the T4 path is selected to lock to the T0 path, the T4 DPLL locks to the 8 kHz from the T0 DPLL. This is because all of the frequencies of operation of the T4 path can be divided to 8 kHz and this will ensure synchronization of all the frequencies within the two paths.

Both of the DPLLs’ outputs are connected to multiplying and filtering APLLs. The outputs of these APLLs are divided making a number of frequencies simultaneously available for selection at the output clock ports. The various combinations of DPLL, APLL and divider configurations allow for generation of a comprehensive set of frequencies, as listed in Table 14.

To synchronize the lower output frequencies when the T0 PLL is locked to a high frequency reference input, an additional input is provided. The SYNC2K pin (pin 45) is used to reset the dividers that generate the 2 kHz and 8 kHz outputs such that the output 2/8 kHz clocks are lined up with the input 2 kHz. This synchronization method allows for example, a master and a slave device to be in precise alignment.

The ACS8520 also supports Sync pulse references of 4 kHz or 8 kHz although in these cases frequencies lower than the Sync pulse reference may not necessarily be in phase.

Input Reference Clock Ports

Table 4 gives details of the input reference ports, showing the input technologies and the range of frequencies supported on each port; the default spot frequencies and default priorities assigned to each port on power-up or by reset are also shown. Note that SDH and SONET networks use different default frequencies; the network type is pin-selectable (using either the SONSDHB pin or via software). Specific frequencies and priorities are set by configuration.

SDH and SONET networks use different default frequencies; the network type is selectable using the *cnfg_input_mode* Reg. 34 Bit 2, *ip_sonsdhb*.

- For SONET, *ip_sonsdhb* = 1
- For SDH, *ip_sonsdhb* = 0

On power-up or by reset, the default will be set by the state of the SONSDHB pin (pin 100). Specific frequencies and priorities are set by configuration.

The frequency selection is programmed via the *cnfg_ref_source_frequency* register (Reg. 20 - Reg. 2D).

Locking Frequency Modes

There are three locking frequency modes that can be configured: Direct Lock, Lock 8k and DivN.

Direct Lock Mode

In Direct Lock Mode, the internal DPLL can lock to the selected input at the spot frequency of the input, for example 19.44 MHz performs the DPLL phase comparisons at 19.44 MHz.

In Lock8K and DivN modes (and for special case of 155 MHz), an internal divider is used prior to the DPLL to divide the input frequency before it is used for phase comparisons in the DPLL.

Lock8K Mode

Lock8K mode automatically sets the divider parameters to divide the input frequency down to 8 kHz. Lock8K can only be used on the supported spot frequencies (see Table 4 Note(i)). Lock8k mode is enabled by setting the *Lock8k* bit (Bit 6) in the appropriate *cnfg_ref_source_frequency* register location. Using lower frequencies for phase comparisons in the DPLL results in a greater tolerance to input jitter.It is possible to choose which edge of the input reference clock to lock to, by setting *8K edge polarity* (Bit 2 of Reg. 03, *test_register1).*

DivN Mode

In DivN mode, the divider parameters are set manually by configuration (Bit 7 of the *cnfg_ref_source_frequency* register), but must be set so that the frequency after division is 8 kHz.

The DivN function is defined as:

DivN = “Divide by N+ 1”, i.e. it is the dividing factor used for the division of the input frequency, and has a value of (N+1) where N is an integer from 1 to 12499 inclusive.

Therefore, in DivN mode the input frequency can be divided by any integer value between 2 to 12500. Consequently, any input frequency which is a multiple of 8 kHz, between 8 kHz to 100 MHz, can be supported by using DivN mode.

Note...Any reference input can be set to use DivN independently of the frequencies and configurations of the other inputs. However only one value of N is allowed, so all inputs with DivN selected must be running at the same frequency.

DivN Examples

(a) To lock to 2.000 MHz:

(i) Set the *cnfg_ref_source_frequency* register to 10XX0000 (binary) to enable DivN, and set the frequency to 8 kHz - the frequency required after division. (XX = “Leaky Bucket” ID for this input).

(ii) To achieve 8 kHz, the 2 MHz input must be divided by 250. So, if DivN = 250 = (N + 1) then N must be set to 249. This is done by writing F9 hex (249 decimal) to the DivN register pair Reg. 46/47.

(b) To lock to 10.000 MHz:

(i) The *cnfg_ref_source_frequency* register is set to 10XX0000 (binary) to set the DivN and the frequency to 8 kHz, the post-division frequency. (XX = “Leaky Bucket” ID for this input).

(ii) To achieve 8 kHz, the 10 MHz input must be divided by 1,250. So, if DivN, = 250 = (N+1) then N must be set to 1,249. This is done by writing 4E1 hex (1,249 decimal) to the DivN register pair Reg. 46/47.

Direct Lock Mode 155 MHz.

The max frequency allowed for phase comparison is 77.76MHz, so for the special case of a 155 MHz input set to Direct Lock Mode, there is a divide-by-two function automatically selected to bring the frequency down to within the limits of operation.

PECL/LVDS/AMI Input Port Selection

The choice of PECL or LVDS compatibility is programmed via the *cnfg_differential_inputs* register. Unused PECL differential inputs should be fixed with one input *High* (VDD) and the other input *Low* (GND), or set in LVDS mode and left floating, in which case one input is internally pulled *High* and the other *Low*.

An AMI port supports a composite clock, consisting of a 64 kHz AMI clock with 8 kHz boundaries marked by deliberate violations of the AMI coding rules, as specified in ITU recommendation G.703[6]. Departures from the nominal pattern are detected within the ACS8520, and may cause reference-switching if too frequent. See section DC Characteristics: AMI Input/Output Port, for more details. If the AMI port is unused, the pins (I1 and I2) should be tied to GND.

Table 4 Input Reference Source Selection and Priority Table

Port Number	Channel Number (Bin)	Input Port Technology	Frequencies Supported	Default Priority
I1	0001	AMI	64/8 kHz (composite clock, 64 kHz + 8 kHz) Default (SONET): 64/8 kHz Default (SDH): 64/8 kHz	2
I2	0010	AMI	64/8 kHz (composite clock, 64 kHz + 8 kHz) Default (SONET): 64/8 kHz Default (SDH): 64/8 kHz	3
I3	0011	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 8 kHz Default (SDH): 8 kHz	4
I4	0100	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 8 kHz Default (SDH): 8 kHz	5
I5	0101	LVDS/PECL LVDS default	Up to 155.52 MHz (see Note (ii)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	6
I6	0110	PECL/LVDS PECL default	Up to 155.52 MHz (see Note (ii)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	7
I7	0111	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	8
I8	1000	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	9
I9	1001	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	10
I10	1010	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	11
I11	1011	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (Master) (SONET): 1.544 MHz Default (Master) (SDH): 2.048 MHz Default (Slave) 6.48 MHz	12/1 (Note (iii))
I12	1100	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 1.544 MHz Default (SDH): 2.048 MHz	13

Table 4 Input Reference Source Selection and Priority Table (cont...)

Port Number	Channel Number (Bin)	Input Port Technology	Frequencies Supported	Default Priority
I13	1101	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 1.544 MHz Default (SDH): 2.048 MHz	14
I14	1110	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 1.544 MHz Default (SDH): 2.048 MHz	15

Notes: (i) TTL ports (compatible also with CMOS signals) support clock speeds up to 100 MHz, with the highest spot frequency being 77.76 MHz. The actual spot frequencies are: 2 kHz, 4 kHz, 8 kHz (and N x 8 kHz), 1.544 MHz (SONET)/2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz. SONET or SDH input rate is selected via Reg. 34 Bit 2, ip_sonsdhb).

(ii) PECL and LVDS ports support the spot clock frequencies listed above plus 155.52 MHz (and 311.04 MHz for TO6 only).

(iii) Input port I11 is set at priority 12 on the Master SETS IC and priority 1 on the Slave SETS IC, as default on power up (or PORB). The default setup of Master or Slave I11 priority is determined by the MSTSLVB pin.

Clock Quality Monitoring

Clock quality is monitored and used to modify the priority tables of the local and remote ACS8520 devices. The following parameters are monitored:

1. Activity (toggling).
2. Frequency (this monitoring is only performed when there is no irregular operation of the clock or loss of clock condition).

In addition, input ports I1 and I2 carry AMI-encoded composite clocks which are monitored by the AMI-decoder blocks. Loss of signal is declared by the decoders when either the signal amplitude falls below +0.3 V or there is no activity for 1 ms.

Any reference source that suffers a loss-of-activity or clock-out-of-band condition will be declared as unavailable.

Clock quality monitoring is a continuous process which is used to identify clock problems. There is a difference in dynamics between the selected clock and the other reference clocks. Anomalies occurring on non-selected reference sources affect only that source's suitability for selection, whereas anomalies occurring on the selected clock could have a detrimental impact on the accuracy of the output clock.

Anomalies detected by the activity detector are integrated in a Leaky Bucket Accumulator. Occasional anomalies do not cause the Accumulator to cross the alarm setting threshold, so the selected reference source is retained. Persistent anomalies cause the alarm setting threshold to be crossed and result in the selected reference source being rejected.

Anomalies on the currently locked-to input reference clock, whether affecting signal purity or signal frequency, could induce jitter or frequency offsets in the output clock, leading to anomalous behavior. Anomalies on the selected clock, therefore, have to be detected as they occur and the phase locked loop must be temporarily isolated until the clock is once again pure. The clock monitoring process cannot be used for this because the high degree of accuracy required dictates that the process be slow. To achieve the immediacy required by the phase locked loop requires an alternative mechanism. The phase locked loop itself contains a fast activity detector such that within approximately two missing input clock cycles, a no-activity flag is raised and the DPLL is frozen in Holdover mode. This flag can also be read as the *main_ref_failed* bit (from Reg. 06, Bit 6) and can be set to indicate a phase lost state by enabling Reg. 73, Bit 6. With the DPLL in Holdover mode it is isolated from further disturbances. If the input becomes available again before the activity or frequency monitor rejection alarms have been raised, then the DPLL will continue to lock to the input, with little disturbance. In this scenario, with the DPLL in the “locked” state, the DPLL uses “nearest edge locking” mode (±180° capture) avoiding cycle slips or glitches caused by trying to lock to an edge 360° away, as would happen with traditional PLLs.

Activity Monitoring

The ACS8520 has a combined inactivity and irregularity monitor. The ACS8520 uses a Leaky Bucket Accumulator, which is a digital circuit which mimics the operation of an analog integrator, in which input pulses increase the output amplitude but die away over time. Such integrators are used when alarms have to be triggered either by fairly regular defect events, which occur sufficiently close together, or by defect events which occur in bursts. Events which are sufficiently spread out should not trigger the alarm. By adjusting the alarm setting threshold, the point at which the alarm is triggered can be controlled. The point at which the alarm is cleared depends upon the decay rate and the alarm clearing threshold.

On the alarm setting side, if several events occur close together, each event adds to the amplitude and the alarm will be triggered quickly; if events occur a little more spread out, but still sufficiently close together to overcome the decay, the alarm will be triggered eventually. If events occur at a rate which is not sufficient to overcome the decay, the alarm will not be triggered. On the alarm clearing side, if no defect events occur for a sufficient time, the amplitude will decay gradually and the alarm will be cleared when the amplitude falls below the alarm clearing threshold. The ability to decay the amplitude over time allows the importance of defect events to be reduced as time passes by. This means that, in the case of isolated events, the alarm will not be set, whereas, once the alarm becomes set, it will be held on until normal operation has persisted for a suitable time (but if the operation is still erratic, the alarm will remain set). See Figure 3.

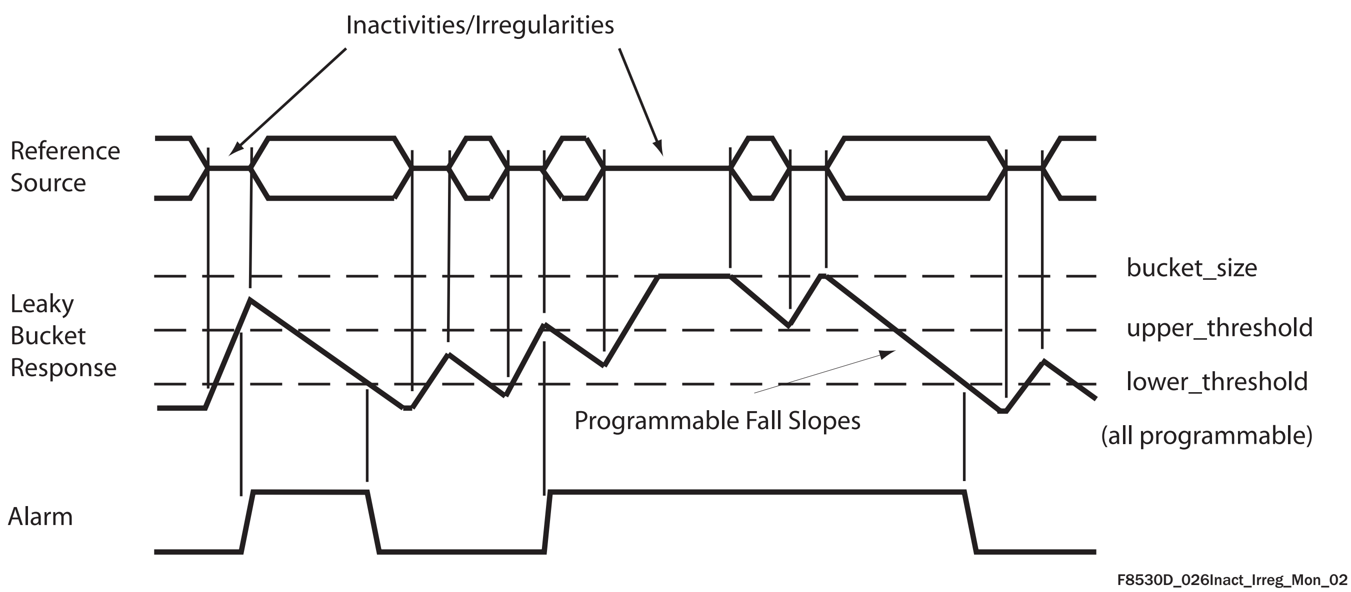
There is one Leaky Bucket Accumulator per input channel. Each Leaky Bucket can select from four Configurations (Leaky Bucket Configuration 0 to 3). Each Leaky Bucket Configuration is programmable for size, alarm set and reset thresholds, and decay rate.

Each source is monitored over a 128 ms period. If, within a 128 ms period, an irregularity occurs that is not deemed to be due to allowable jitter/wander, then the Accumulator is incremented.

The Accumulator will continue to increment up to the point that it reaches the programmed Bucket size. The "fill rate" of the Leaky Bucket is, therefore, 8 units/second. The "leak rate" of the Leaky Bucket is programmable to be in multiples of the fill rate (x 1, x 0.5, x 0.25 and x 0.125) to give a programmable leak rate from 8 units/sec down to 1 unit/sec. A conflict between trying to "leak" at the same time as a "fill" is avoided by preventing a leak when a fill event occurs.

Disqualification of a non-selected reference source is based on inactivity, or on an out-of-band result from the frequency monitors. The currently selected reference source can be disqualified for phase, frequency, inactivity or if the source is outside the DPLL lock range. If the currently selected reference source is disqualified, the next highest priority, qualified reference source is selected.

Figure 3 Inactivity and Irregularity Monitoring



Interrupts for Activity Monitors

The loss of the currently selected reference source will eventually cause the input to be considered invalid, triggering an interrupt. The time taken to raise this interrupt is dependant on the Leaky Bucket Configuration of the activity monitors. The fastest Leaky Bucket setting will still take up to 128 ms to trigger the interrupt. The interrupt caused by the brief loss of the currently selected reference source is provided to facilitate very fast source failure detection if desired. It is triggered after missing just a couple of cycles of the reference source. Some applications require the facility to switch downstream devices based on the status of the reference sources. In order to provide extra flexibility, it is possible to flag the *main_ref_failed* interrupt (Reg. 06 Bit 6) on the pin TDO. This is simply a copy of the status bit in the interrupt register and is independent of the mask register settings. The bit is reset by writing to the interrupt status register in the normal way. This feature can be enabled and disabled by writing to Reg. 48 Bit 6.

Leaky Bucket Timing

The time taken (in seconds) to raise an inactivity alarm on a reference source that has previously been fully active (Leaky Bucket empty) will be:

(cnfg_upper_threshold_n) / 8

where n is the number of the Leaky Bucket Configuration. If an input is intermittently inactive then this time can be longer. The default setting of *cnfg_upper_threshold_n* is 6, therefore the default time is 0.75 s.

The time taken (in seconds) to cancel the activity alarm on a previously completely inactive reference source is calculated, for a particular Leaky Bucket, as:

$$[2^{(a)} \times (b - c)] / 8$$

where:

a = cnfg_decay_rate_n
b = cnfg_bucket_size_n
c = cnfg_lower_threshold_n
(where n = the number of the relevant Leaky Bucket Configuration in each case).

The default setting is shown in the following:

$$[2^{1} \times (8 - 4)] / 8 = 1.0 \text{ secs}$$

Frequency Monitoring

The ACS8520 performs frequency monitoring to identify reference sources which have drifted outside the acceptable frequency range measured with respect either to the output clock or to the XO clock.

The *sts_reference_sources* out-of-band alarm for a particular reference source is raised when the reference source is outside the acceptable frequency range. With the default register settings a soft alarm is raised if the drift is outside ±11.43 ppm and a hard alarm is raised if the drift is outside ±15.24 ppm. Both of these limits are programmable from 3.8 ppm up to 61 ppm.

The ACS8520 DPLL has a programmable lock and capture range frequency limit up to ±80 ppm (default is ±9.2 ppm).

Selection of Input Reference Clock Source

Under normal operation, the input reference sources are selected automatically by an order of priority. But, for special circumstances, such as chip or board testing, the selection may be forced by configuration.

Automatic operation selects a reference source based on its pre-defined priority and its current availability. A table is maintained which lists all reference sources in the order of priority. This is initially defined by the default configuration and can be changed via the microprocessor interface by the Network Manager. In this way, when all the defined sources are active and valid, the source with the highest programmed priority is selected but, if this source fails, the next-highest source is selected, and so on.

Restoration of repaired reference sources is handled carefully to avoid inadvertent disturbance of the output clock. For this, the ACS8520 has two modes of operation; Revertive and Non-revertive.

In Revertive mode, if a re-validated (or newly validated) source has a higher priority than the reference source which is currently selected, a switch over will take place. Many applications prefer to minimize the clock switching events and choose Non-revertive mode.

In Non-revertive mode, when a re-validated (or newly validated) source has a higher priority then the selected source will be maintained. The re-validation of the reference source will be flagged in the *sts_sources_valid* register and, if not masked, will generate an interrupt.

Selection of the re-validated source can take place under software control or if the currently selected source fails.

To enable software control, the software should briefly enable Revertive mode to effect a switch-over to the higher priority source. When there is a reference available with higher priority than the selected reference, there will be NO change of reference source as long as the Non-revertive mode remains on, and the currently selected source is valid. A failure of the selected reference will always trigger a switch-over regardless of whether Revertive or Non-revertive mode has been chosen.

Also, in a Master/Slave redundancy-protection scheme, the Slave device(s) must follow the Master device. The alignment of the Master and Slave devices is part of the protection mechanism. The availability of each source is determined by a combination of local and remote monitoring of each source. Each input reference source supplied to each ACS8520 device is monitored locally and the results are made available to other devices.

Forced Control Selection

A configuration register, *force_select_reference_source* Reg. 33, controls both the choice of automatic or forced selection and the selection itself (when forced selection is required). For Automatic choice of source selection, the 4 LSB bit value is set to all zeros or all ones (default). To force a particular input (I_n), the Bit value is set to n (bin). Forced selection is not the normal mode of operation, and the *force_select_reference_source* variable is defaulted to the all-ones value on reset, thereby adopting the automatic selection of the reference source.

Automatic Control Selection

When an automatic selection is required, the *force_select_reference_source* register LSB 4 bits must be set to all zeros or all ones. The configuration registers, *cnfg_ref_selection_priority*, held in the µP port block, consist of seven, 8-bit registers organized as one 4-bit register per input reference port. Each register holds a 4-bit value which represents the desired priority of that particular port. Unused ports should be given the value, 0000, in the relevant register to indicate they are not to be included in the priority table. On power-up, or following a reset, the whole of the configuration file will be defaulted to the values defined by Table 4. The selection priority values are all relative to each other, with lower-valued numbers taking higher priorities. Each reference source should be given a unique number; the valid values are 1 to 15 (dec). A value of zero disables the reference source. However if two or more inputs are given the same priority number those inputs will be selected on a first in, first out basis. If the first of two same priority number sources goes invalid the second will be switched in. If the first then becomes valid again, it becomes the second source on the first in, first out basis, and there will not be a switch. If a third source with the same priority number as the other two becomes valid, it joins the priority list on the same first in, first out basis. There is no implied priority based on the channel numbers. Revertive/Non-revertive mode has no effect on sources with the same priority value.

The input port I11 is also for the connection of the synchronous clock of the T0 output of the Master device (or the active-Slave device), to be used to align the T0 output with the Master (or active-Slave) device if this device is acting in a subordinate-Slave or subordinate-Master role.

Ultra Fast Switching

A reference source is normally disqualified after the Leaky Bucket monitor thresholds have been crossed. An option for a faster disqualification has been implemented, whereby if Reg. 48 Bit 5 (*ultra_fast_switch*) is set, then a loss of activity of just a few reference clock cycles will set the *main_ref_failed* alarm and cause a reference switch. This can be configured (see Reg. 06, Bit 6) to cause an interrupt to occur instead of, or as well as, causing the reference switch.

The *sts_interrupts* register Reg. 06 Bit 6 (*main_ref_failed*) is used to flag inactivity on the reference that the device is locked to much faster than the activity monitors can support. If Reg. 48 Bit 6 of the *cnfg_monitors* register (*los_flag_on_TDO*) is set, then the state of this bit is driven onto the TDO pin of the device.

Note...The flagging of the loss of the main reference failure on TDO is simply allowing the status of the sts_interrupt bit main_ref_failed (Reg. 06 Bit 6) to be reflected in the state of the TDO output pin. The pin will, therefore, remain High until the interrupt is cleared. This functionality is not enabled by default so the usual JTAG functions can be used. When the TDO output from the ACS8520 is connected to the TDI pin of the next device in the JTAG scan chain, the implementation should be such that a logic change caused by the action of the interrupt on the TDI input should not effect the operation when JTAG is not active.

Fast External Switching Mode-SCRSW Pin

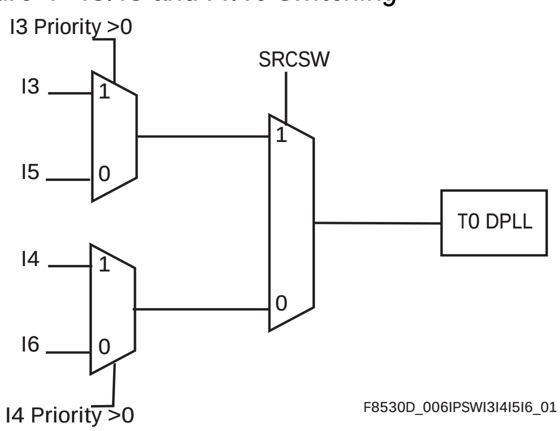
Fast external switching mode, for fast switching between inputs I3 or I5 and I4 or I6, can also be triggered directly from a dedicated pin SRCSW (Figure 4), once the mode has been initialized.

The mode is initialized by either holding SRCSW pin *High* during reset (SRCSW must remain *High* for at least a further 251 ms after PORB has gone *High* - see following Note), or by writing to Reg. 48 Bit 4. After External Protection Switching mode has been initialized, the value on this pin directly selects either I3/I5 (SRCSW *High*) or I4/I6 (SRCSW *Low*). If this mode is initialized at reset by pulling the SRCSW pin *High*, then it configures the default frequency tolerance of I3/I5 and I4/I6 to ±80 ppm (Reg. 41 and Reg. 42) as opposed to the normal frequency tolerance of ±9.2 ppm. Any of these registers can be subsequently set by external software, if required.

Note...The 251 ms comprises 250 ms allowance for the internal reset to be removed plus 1 ms allowance for APLLs to start-up and become stable.

Selection of either input I3 or I5 is determined by the Priority value of I3; if the programmed priority of I3 is 0, then I5 is selected. Similarly, I6 is selected if the programmed priority of I4 is 0.

Figure 4 I3/I5 and I4/I6 Switching



When external protection switching is enabled, the device will operate as a simple switch. All clock monitoring is disabled and the DPLL will simply be forced to try to lock on to the indicated reference source. Consequently the device will always indicate “locked” state in the *sts_operating* register (Reg. 09, Bits [2:0]).

Output Clock Phase Continuity on Source Switchover

If either PBO is selected on (default), or, if DPLL frequency limit is set to less than ±30 ppm or (±9.2 ppm default), the device will always comply with GR-1244-CORE[19] specification for Stratum 3 (maximum rate of phase change of 81 ns/1.326 ms), for all input frequencies.

Modes of Operation

The ACS8520 has three primary modes of operation (Free-run, Locked and Holdover) supported by three secondary, temporary modes (Pre-locked, Lost-phase and Pre-locked2). These are shown in the State Transition Diagram for the T0 DPLL, Figure 5.

The ACS8520 can operate in Forced or Automatic control. On reset, the ACS8520 reverts to Automatic Control, where transitions between states are controlled completely automatically. Forced Control can be invoked by configuration, allowing transitions to be performed under external control. This is not the normal mode of operation, but is provided for special occasions such as testing, or where a high degree of hands-on control is required.

Free-run Mode

The Free-run mode is typically used following a power-on-reset or a device reset before network synchronization has been achieved. In the Free-run mode, the timing and synchronization signals generated from the ACS8520 are based on the 12.800 MHz clock frequency provided from the external oscillator and are not synchronized to an input reference source. By default, the frequency of the output clock is a fixed multiple of the frequency of the external oscillator, and the accuracy of the output clock is equal to the accuracy of the oscillator. However the external oscillator frequency can be calibrated to improve its accuracy by a software calibration routine using register *cnfg_nominal_frequency* (Reg. 3C and 3D). For example a 500 ppm offset crystal could be made to look like one accurate to within ±0.02 ppm.

The transition from Free-run to Pre-locked occurs when the ACS8520 selects a reference source.

Pre-locked Mode

The ACS8520 will enter the Locked state in a maximum of 100 seconds, as defined by GR-1244-CORE[19] specification, if the selected reference source is of good quality. If the device cannot achieve lock within 100 seconds, it reverts to Free-run mode and another reference source is selected.

Locked Mode

The Locked mode is entered from Pre-locked, Pre-locked2 or Phase-lost mode when an input reference source has been selected and the DPLL has locked. The DPLL is considered to be locked when the phase loss/lock detectors (see "Phase Lock/Loss Detection" on page 21) indicate that the DPLL has remained in phase lock continuously for at least one second. When the ACS8520 is in Locked mode, the output frequency and phase tracks that of the selected input reference source.

Lost-phase Mode

Lost-phase mode is used whenever the phase loss/lock detectors (see "Phase Lock/Loss Detection" on page 21) indicate that the DPLL has lost phase lock. The DPLL will still be trying to lock to the input clock reference, if it exists. If the Leaky Bucket Accumulator calculates that the anomaly is serious, the device disqualifies the reference source. If the device spends more than 100 seconds in Lost-phase mode, the reference is disqualified and a phase alarm is raised on it. If the reference is disqualified, one of the following transitions takes place:

1. Go to Pre-locked2;
   - If a known good stand-by source is available.
2. Go to Holdover;
   - If no stand-by sources are available.

Holdover Mode

Holdover mode is the operating condition the device enters when its currently selected input source becomes invalid, and no other valid replacement source is available. In this mode, the device resorts to using stored frequency data, acquired when the input reference source was still valid, to control its output frequency.

In Holdover mode, the ACS8520 provides the timing and synchronization signals to maintain the Network Element but is not phase locked to any input reference source. Its output frequency is determined by an averaged version of the DPLL frequency when last in the Locked Mode.

Holdover can be configured to operate in either:

- Automatic mode
  (Reg. 34 Bit 4, *cnfg_input_mode: man_holdover* set *Low*), or
- Manual mode
  (Reg. 34 Bit 4, *cnfg_input_mode: man_holdover* set *High*).

Automatic Mode

In Automatic mode, the device can be configured to operate using either:

- Averaged - (Reg. 40 Bit 7, *cnfg_holdover_modes, auto_averaging:* set *High*), or
- Instantaneous - (Reg. 40 Bit 7, *cnfg_holdover_modes, auto_averaging:* set *Low*).

Averaged

In the Averaged mode, the frequency (as reported by *sts_current_DPLL_frequency*, see Reg. 0C, Reg. 0D and Reg. 07) is filtered internally using an Infinite Impulse Response filter, which can be set to either:

- Fast - (Reg. 40 Bit 6, *cnfg_holdover_modes, fast_averaging:* set *High*), giving a -3 dB filter response point corresponding to a period of approximately eight minutes, or
- Slow - (Reg. 40 Bit 6, *cnfg_holdover_modes, fast_averaging:* set *Low*) giving a -3 dB filter response point corresponding to a period of approximately 110 minutes.

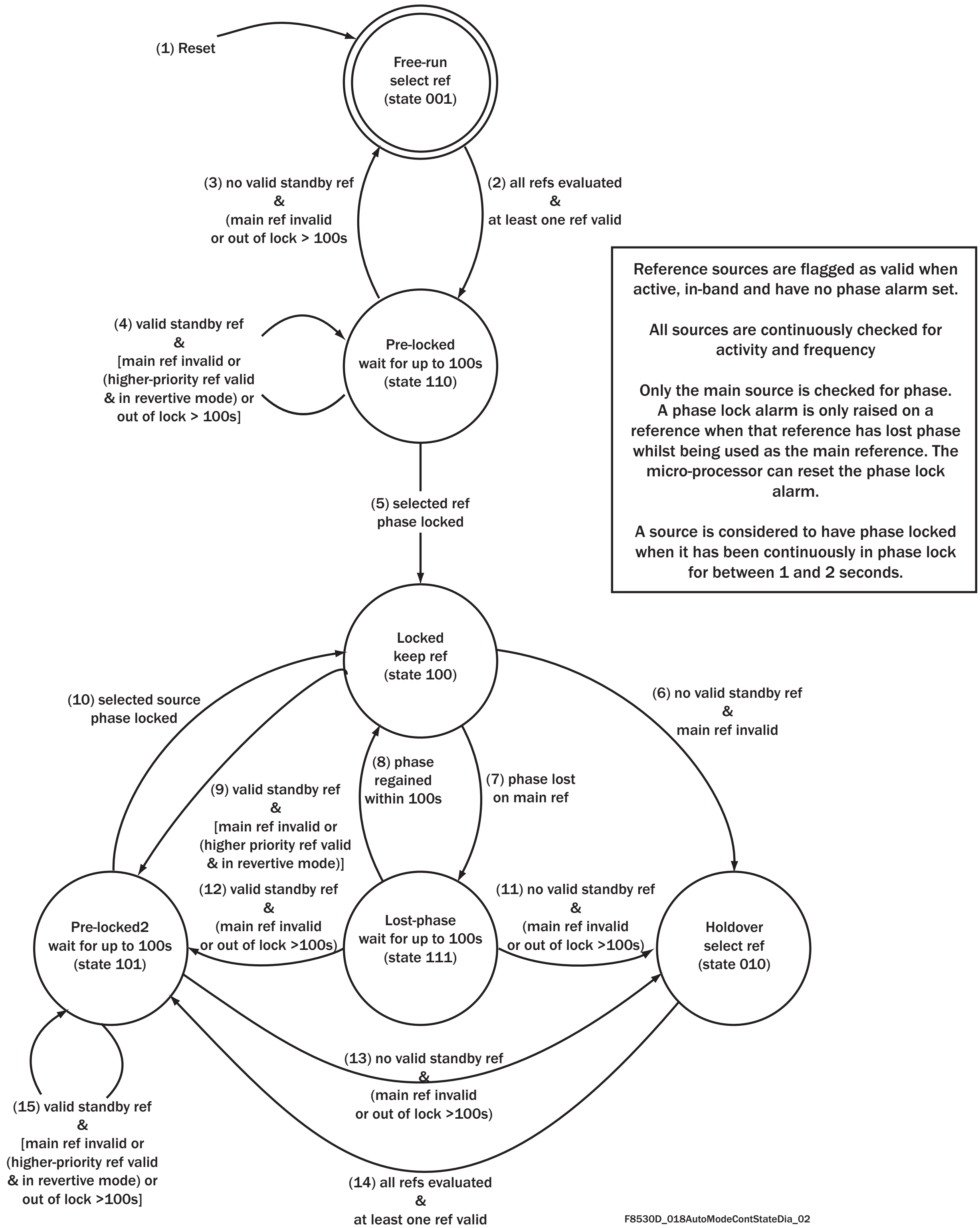
Instantaneous

In Instantaneous mode, the DPLL freezes at the frequency it was operating at the time of entering Holdover mode. It does this by using only its internal DPLL integral path value (as reported in Reg. 0C, 0D, and 07) to determine output frequency. The DPLL proportional path is not used so that any recent phase disturbances have a minimal effect on the Holdover frequency. The integral value used can be viewed as a filtered version of the locked output frequency over a short period of time. The period being in inverse proportion to the DPLL bandwidth setting.

Manual Mode

(Reg. 34 Bit 4, *cnfg_input_mode*, *man_holdover* set *High*.) The Holdover frequency is determined by the value in register *cnfg_holdover_frequency* (Reg. 3E, Reg. 3F, and part of Reg. 40). This is a 19-bit signed number, with a LSB resolution of 0.0003068 ppm, which gives an adjustment range of ±80 ppm. This value can be derived from a reading of register *sts_current_DPLL_frequency* (Reg. 0D, Reg. 0C and Reg. 07), which gives, in the same format, an indication of the current output frequency deviation, which would be read when the device is locked. If required, this value could be read by external software and averaged over time. The averaged value could then be fed to the *cnfg_holdover_frequency* register, ready for setting the averaged frequency value when the device enters Holdover mode. The *sts_current_DPLL_frequency* value is internally derived from the Digital Phase Locked Loop (DPLL) integral path, which represents a short-term average measure of the current frequency, depending on the locked loop bandwidth (Reg. 67) selected.

Figure 5 Automatic Mode Control State Diagram (T0 DPLL)



Note...The state diagram above is for T0 DPLL only, and the 3-bit state value refers to the register sts_operating Reg. 09 Bits [2:0] T0_DPLL_operating _mode. By contrast, the T4 DPLL has only automatic operation and can be in one of only two possible states: "Instantaneous Automatic Holdover" with zero frequency offset (its start-up state), or "Locked". The T4 DPLL states are not configurable by the User and there is no "Free-run" state.

It is also possible to combine the internal averaging filters with some additional software filtering. For example the internal fast filter could be used as an anti-aliasing filter and the software could further filter this before determining the actual Holdover frequency. To support this feature, a facility to read out the internally averaged frequency has been provided. By setting Reg. 40, Bit 5, *cnfg_holdover_modes*, *read_average,* the value read back from the *cnfg_holdover_frequency* register will be the filtered value. The filtered value is available regardless of what actual Holdover mode is selected. Clearly this results in the register not reading back the data that was written to it.

Example: Software averaging to eliminate temperature drift.

Select Manual Holdover mode by setting Reg. 34 Bit 4, *cnfg_input_mode, man_holdover High*.

Select Fast Holdover Averaging mode by setting Reg. 40 Bit 6, *cnfg_holdover_modes*, *auto_averaging High* and Reg. 40 Bit 7 *High*.

Select to be able to read back filtered output by setting Reg. 40 Bit 5, *cnfg_holdover_modes*, *read_average High*.

Software periodically reads averaged value from the *cnfg_holdover_frequency* register and the temperature (not supplied from ACS8520). Software processes frequency and temperature and places data in software look-up table or other algorithm. Software writes back appropriate averaged value into the *cnfg_holdover_frequency* register.

Once Holdover mode is entered, software periodically updates the *cnfg_holdover_frequency* register using the temperature information (not supplied from ACS8520).

Mini-holdover Mode

Holdover mode so far described refers to a state to which the internal state machine switches as a result of activity or frequency alarms, and this state is reported in Reg. 09. To avoid the DPLL's frequency being pulled off as a result of a failed input, then the DPLL has a fast mechanism to freeze its current frequency within one or two cycles of the input clock source stopping. Under these circumstances the DPLL enters Mini-holdover mode; the Mini-holdover frequency used being determined by Reg. 40, Bits [4:3], *cnfg_holdover_modes*, *mini_holdover_mode.*

Mini-holdover mode only lasts until one of the following happens:

- A new source has been selected, or
- The state machine enters Holdover mode, or
- The original fault on the input recovers.

External Factors Affecting Holdover Mode

If the external TCXO/OCXO frequency is varying due to temperature fluctuations in the room, then the instantaneous value can be different from the average value, and then it may be possible to exceed the 0.05 ppm limit (depending on how extreme the temperature fluctuations are). It is advantageous to shield the TCXO/OCXO to slow down frequency changes due to drift and external temperature fluctuations.

The frequency accuracy of Holdover mode has to meet the ITU-T, ETSI and Telcordia performance requirements. The performance of the external oscillator clock is critical in this mode, although only the frequency stability is important - the stability of the output clock in Holdover is directly related to the stability of the external oscillator.

Pre-locked2 Mode

This state is very similar to the Pre-Locked state. It is entered from the Holdover state when a reference source has been selected and applied to the phase locked loop. It is also entered if the device is operating in Revertive mode and a higher-priority reference source is restored.

Upon applying a reference source to the phase locked loop, the ACS8520 will enter the Locked state in a maximum of 100 seconds, as defined by GR-1244-CORE[19] specification, if the selected reference source is of good quality.

If the device cannot achieve lock within 100 seconds, it reverts to Holdover mode and another reference source is selected.

DPLL Architecture and Configuration

A Digital PLL gives a stable and consistent level of performance that can be easily programmed for different dynamic behavior or operating range. It is not affected by operating conditions or silicon process variations. Digital synthesis is used to generate all required SONET/SDH output frequencies. The digital logic operates at 204.8 MHz that is multiplied up from the external 12.800 MHz oscillator module. Hence the best resolution of the output signals from the DPLL is one 204.8 MHz cycle or 4.9 ns.

Additional resolution and lower final output jitter is provided by a de-jittering Analog PLL that reduces the 4.9 ns p-p jitter from the digital down to 500 ps p-p and 60 ps RMS as typical final outputs measured broadband (from 10 Hz to 1 GHz).

This arrangement combines the advantages of the flexibility and repeatability of a DPLL with the low jitter of an APLL. The DPLLs in the ACS8520 are uniquely very programmable for all PLL parameters of bandwidth (from 0.1 Hz up to 70 Hz), damping factor (from 1.2 to 20), frequency acceptance and output range (from 0 to 80 ppm, typically 9.2 ppm), input frequency (12 common SONET/SDH spot frequencies) and input-to-output phase offset (in 6 ps steps up to 200 ns). There is no requirement to understand the loop filter equations or detailed gain parameters since all high level factors such as overall bandwidth can be set directly via registers in the microprocessor interface. No external critical components are required for either the internal DPLLs or APLLs, providing another key advantage over traditional discrete designs.

The T4 DPLL is similar in structure to the T0 DPLL, but since the T4 is only providing a clock synthesis and input to output frequency translation function, with no defined requirement for jitter attenuation or input phase jump absorption, then its bandwidth is limited to the high end and the T4 does not incorporate many of the Phase Build-out and adjustment facilities of the T0 DPLL.

T0 DPLL Main Features

- Two programmable DPLL bandwidth controls (Locked and Acquisition bandwidth), each with 10 steps from 0.1 Hz to 70 Hz
- Programmable damping factor: For optional faster locking and peaking control. Factors = 1.2, 2.5, 5, 10 or 20
- Multiple phase lock detectors
- Input to output phase offset adjustment (Master/Slave), ±200 ns, 6 ps resolution step size
- PBO phase offset on source switching - disturbance down to ±5 ns
- Multi-cycle phase detection and locking, programmable up to ±8192 UI - improves jitter tolerance in direct lock mode
- Holdover frequency averaging with a choice of averaging times: 8 minutes or 110 minutes and value can be read out
- Multiple E1 and DS1 outputs supported
- Low jitter MFrSync (2 kHz) and FrSync (8 kHz) outputs.

T4 DPLL Main Features

- A single programmable DPLL bandwidth control: 18 Hz, 35 Hz, or 70 Hz
- Programmable damping factor: For optional faster locking and peaking control. Factors = 1.2, 2.5, 5, 10 or 20
- Multiple phase lock detectors
- Multi-cycle phase detection and locking, programmable up to ±8192 UI - improves jitter tolerance in direct lock mode
- DS3/E3 support (44.736 MHz / 34.368 MHz) at same time as OC-N rates from T0
- Low jitter E1/DS1 options at same time as OC-N rates from T0
- Frequencies of n x E1/DS1 including 16 and 12 x E1, and 16 and 24 x DS1 supported
- Low jitter MFrSync (2 kHz) and FrSync (8 kHz) outputs
- Can use the T4 DPLL as an Independent FrSync DPLL
- Can use the phase detector in T4 DPLL to measure the input phase difference between two inputs.

The structure of the T0 and T4 PLLs are shown later in Figure 11 in the section on output clock ports. That section also details how the DPLLs and particular output frequencies are configured. The following sections detail some component parts of the DPLL.

T0 DPLL Automatic Bandwidth Controls

In Automatic Bandwidth Selection mode (Reg. 3B Bit 7), the T0 DPLL bandwidth setting is selected automatically from the Acquisition Bandwidth or Locked Bandwidth configurations programmed in *cnfg_T0_DPLL_acq_bw* Reg. 69 and *cnfg_T0_DPLL_locked_bw* Reg. 67 respectively. If this mode is not selected, the DPLL acquires and locks using only the bandwidth set by .

Phase Detectors

A Phase and Frequency detector is used to compare input and feedback clocks. This operates at input frequencies up to 77.76 MHz. The whole DPLL can operate at spot frequencies from 2 kHz up to 77.76 MHz (155.52 MHz is internally divided down to 77.76 MHz). A common arrangement however is to use Lock8k mode (See Reg. 22 to 2D, Bit 6) where all input frequencies are divided down to 8 kHz internally. Marginally better MTIE figures may be possible in direct lock mode due to more regular phase updates. This direct locking capability is one of the unique features of the ACS8520.

A patented multi-phase detector is used in order to give an infinitesimally small input phase resolution combined with large jitter tolerance. The following phase detectors are used:

- Phase and frequency detector (±360° or ±180° range)
- An Early/ Late Phase detector for fine resolution
- A multi-cycle phase detector for large input jitter tolerance (up to 8191 UI), which captures and remembers phase differences of many cycles between input and feedback clocks.

The phase detectors can be configured to be immune to occasional missing input clock pulses by using nearest edge detection (±180° capture) or the normal ±360° phase capture range which gives frequency locking. The device will automatically switch to nearest edge locking when the multi-UI phase detector is not enabled, and the other phase detectors have detected that phase lock has been achieved. It is possible to disable the selection of nearest edge locking via Reg. 03 Bit 6 set to 1. In this setting, frequency locking will always be enabled.

The balance between the first two types of phase detector employed can be adjusted via registers 6A to 6D. The default settings should be sufficient for all modes. Adjustment of these settings affects only small signal overshoot and bandwidth.

The multi-cycle phase detector is enabled via Reg. 74, Bit 6 set to 1 and the range is set in exponentially increasing steps from ±1 UI, 3 UI, 7 UI, 15 UI ... up to 8191 UI via Reg. 74, Bits [3:0]. When this detector is enabled it keeps a track of the correct phase position over many cycles of phase difference to give excellent jitter tolerance. This provides an alternative to switching to Lock8k mode as a method of achieving high jitter tolerance.

An additional control (Reg. 74 Bit 5) enables the multi-phase detector value to be used in the final phase value as part of the DPLL loop. When enabled by setting *High*, the multi cycle phase value will be used in the loop and gives faster pull in (but more overshoot). The characteristics of the loop will be similar to Lock8k mode where again large input phase differences contribute to the loop dynamics. Setting the bit *Low* only uses a max figure of 360 degrees in the loop and will give slower pull-in but gives less overshoot. The final phase position that the loop has to pull in to is still tracked and remembered by the multi-cycle phase detector in either case.

Phase Lock/Loss Detection

Phase lock/loss detection is handled in several ways. Phase loss can be triggered from:

- The fine phase lock detector, which measures the phase between input and feedback clock
- The coarse phase lock detector, which monitors whole cycle slips
- Detection that the DPLL is at min or max frequency
- Detection of no activity on the input.

Each of these sources of phase loss indication is individually enabled via register bits (see Reg. 73, 74 and 4D). Phase lock or lost is used to determine whether to switch to nearest edge locking and whether to use acquisition or normal bandwidth settings for the DPLL. Acquisition bandwidth is used for faster pull in from an unlocked state.

The coarse phase lock detector detects phase differences of n cycles between input and feedback clocks, where n is set by Reg. 74, Bits [3:0]; the same register that is used for the coarse phase detector range, since these functions go hand in hand. This detector may be used in the case where it is required that a phase loss indication is not given for reasonable amounts of input jitter and so the fine phase loss detector is disabled and the coarse detector is used instead.

Damping Factor Programmability

The DPLL damping factor is set by default to provide a maximum wander gain peak of around 0.1 dB. Many of the specifications (e.g. GR-1244-CORE[19], G.812[10] and G.813[11]) specify a wander transfer gain of less than 0.2 dB. GR-253[17] specifies jitter (not wander) transfer of less than 0.1 dB. To accommodate the required levels of transfer gain, the ACS8520 provides a choice of damping factors, with more choice given as the bandwidth setting increases into the frequency regions classified as jitter. Table 5 shows which damping factors are available for selection at the different bandwidth settings, and what the corresponding jitter transfer approximate gain peak will be.

Table 5 Available Damping Factors for different DPLL Bandwidths, and associated Jitter Peak Values

Bandwidth	Reg. 6B [2:0]	Damping Factor selected	Gain Peak/ dB
0.1 Hz to 4 Hz	1, 2, 3, 4, 5	5	0.1
8 Hz	1	2.5	0.2
	2, 3, 4, 5	5	0.1
18 Hz	1	1.2	0.4
	2	2.5	0.2
	3, 4, 5	5	0.1
35 Hz	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4, 5	10	0.06
70 Hz	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4	10	0.06
	5	20	0.03

Local Oscillator Clock

The Master system clock on the ACS8520 should be provided by an external clock oscillator of frequency 12.800 MHz. The clock specification is important for meeting the ITU/ETSI and Telcordia performance requirements for Holdover mode. ITU and ETSI specifications permit a combined drift characteristic, at constant temperature, of all non-temperature-related parameters, of up to 10 ppb per day. The same specifications allow a drift of 1 ppm over a temperature range of 0 to +70°C.

Table 6 ITU and ETSI Specification

Parameter	Value
Tolerance	±4.6 ppm over 20 year lifetime
Drift (Frequency Drift over supply voltage range of +2.7 V to +3.3 V)	±0.05 ppm/15 seconds @ constant temp.
	±0.01 ppm/day @ constant temp.
	±1 ppm over temp. range 0 to +70°C

Telcordia specifications are somewhat tighter, requiring a non-temperature-related drift of less than 40 ppb per day and a drift of 280 ppb over the temperature range 0 to +50°C. Please contact Semtech for information on crystal oscillator suppliers

Table 7 Telcordia GR-1244 CORE Specification

Parameter	Value
Tolerance	±4.6 ppm over 20 year lifetime
Drift (Frequency Drift over supply voltage range of +2.7 V to +3.3 V)	±0.05 ppm/15 seconds @ constant temp.
	±0.04 ppm/15 seconds @ constant temp.
	±0.28 ppm/over temp. range 0 to +50°C

Crystal Frequency Calibration

The absolute crystal frequency accuracy is less important than the stability since any frequency offset can be compensated by adjustment of register values in the IC. This allows for calibration and compensation of any crystal frequency variation away from its nominal value. ±50 ppm adjustment would be sufficient to cope with most crystals, in fact the range is an order of magnitude larger due to the use of two 8-bit register locations. The setting of the *conf_nominal_frequency* register allows for this adjustment. An increase in the register value increases the output frequencies by 0.0196229 ppm for each LSB step.

The default register value (in decimal) = 39321 (9999 hex) = 0 ppm offset. The minimum to maximum offset range of the register is 0 to 65535 dec, giving an adjustment range of -771 ppm to +514 ppm of the output frequencies, in 0.0196229 ppm steps.

Example: If the crystal was oscillating at 12.800 MHz + 5 ppm, then the calibration value in the register to give a - 5 ppm adjustment in output frequencies to compensate for the crystal inaccuracy, would be:
39321 - (5/0.0196229) = 39066 (dec) = 989A (hex).

Output Wander

Wander and jitter present on the output clocks are dependent on:

- The magnitudes of wander and jitter on the selected input reference clock (in Locked mode)
- The internal wander and jitter transfer characteristic (in Locked mode)
- The jitter on the local oscillator clock
- The wander on the local oscillator clock (in Holdover mode).

Wander and jitter are treated in different ways to reflect their differing impacts on network design. Jitter is always strongly attenuated, whilst wander attenuation can be varied to suit the application and operating state. Wander and jitter attenuation is performed using a digital phase locked loop (DPLL) with a programmable bandwidth. This gives a transfer characteristic of a low pass filter, with a programmable pole. It is sometimes necessary to change the filter dynamics to suit particular circumstances - one example being when locking to a new source, the filter can be opened up to reduce locking time and can then be tightened again to remove wander. A change between different bandwidths for locking and for acquisition is handled automatically within the ACS8520.

There may be a phase shift across the ACS8520 between the selected input reference source and the output clock over time, mainly caused by frequency wander in the external oscillator module. Higher stability XOs will give better performance for MTIE. The oscillator becomes more critical at DPLL bandwidth near to or below 0.1 Hz since the rate of change of the DPLL may be slow compared to the rate of change of the oscillator frequency. Shielding of the OCXO or TCXO can further slow down the rate of change of temperature and hence frequency, thus improving output wander performance.

The phase shift may vary over time but will be constrained to lie within specified limits. The phase shift is characterized using two parameters, MTIE (Maximum Time Interval Error) and TDEV (Time Deviation) which, although being specified in all relevant specifications, differ in acceptable limits in each one.

Typical measurements for the ACS8520 are shown in Figure 6, for Locked mode operation. Figure 7 shows a typical measurement of Phase Error accumulation in Holdover mode operation.

The required performance for phase variation during Holdover is specified in several ways and depends on the relevant specification (See “References” on page 146), for example:

1. ETSI ETS-300 462-5[4], Section 9.1, requires that the short-term phase error during switchover (i.e. Locked to Holdover to Locked) be limited to an accumulation rate no greater than 0.05 ppm during a 15 second interval.
2. ETSI ETS-300 462-5[4], Section 9.2, requires that the long-term phase error in the Holdover mode should not exceed
   $\{(a1 + a2)S + 0.5bS^2 + c\}$
   where
   a1 = 50 ns/s (allowance for initial frequency offset)
   a2 = 2000 ns/s (allowance for temperature variation)
   b = 1.16×10^{-4} ns/s^2 (allowance for ageing)
   c = 120 ns (allowance for entry into Holdover mode).
   S = Elapsed time (s) after loss of external ref. input
3. ANSI Tin1.101-1999[1], Section 8.2.2, requires that the phase variation be limited so that no more than 255 slips (of 125 µs each) occur during the first day of Holdover. This requires a frequency accuracy better than:
   ((24x60x60)+(255x125µs))/(24x60x60) = 0.37 ppm
   Temperature variation is not restricted, except to within the normal bounds of 0 to 50°C.
4. Telcordia GR-1244-CORE[19], Section 5.2, shows that an initial frequency offset of 50 ppb is permitted on entering Holdover, whilst a drift over temperature of 280 ppb is allowed; an allowance of 40 ppb is permitted for all other effects.
5. ITU G.822[12], Section 2.6, requires that the slip rate during category (b) operation (interpreted as being applicable to Holdover mode operation) be limited to less than 30 slips (of 125 µs each) per hour.

   ((60 x 60) + (30 x 125 µs))/(60 x 60)) = 1.042 ppm

Figure 6 Maximum Time Interval Error and Time Deviation of T0 PLL Output Port

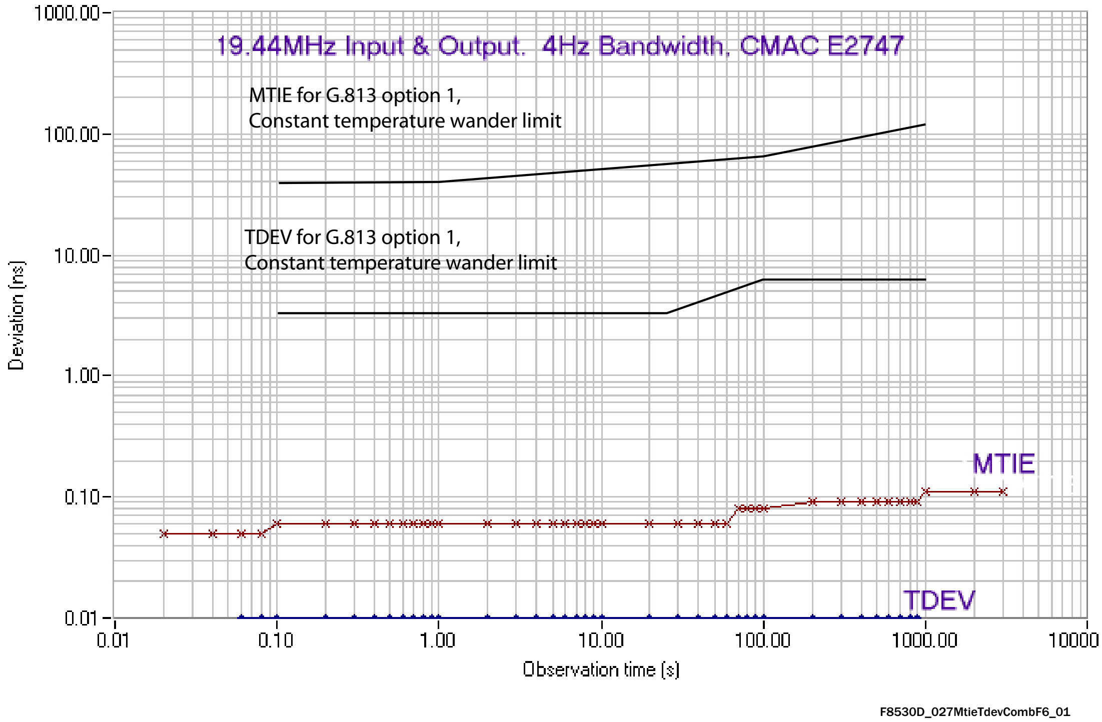
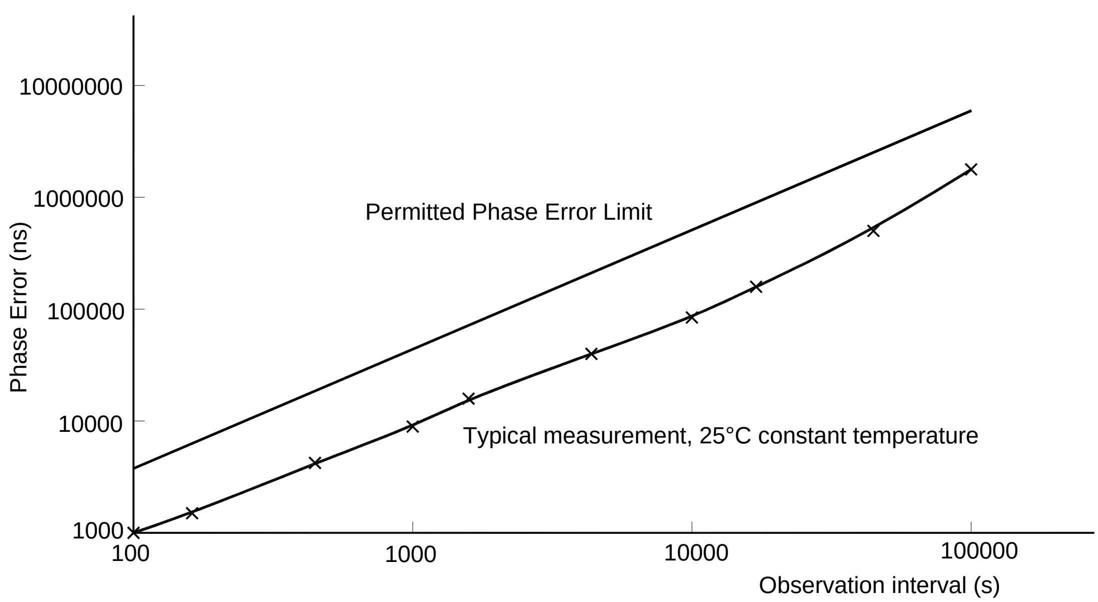


Figure 7 Phase Error Accumulation of T0 PLL Output Port in Holdover Mode



Jitter and Wander Transfer

The ACS8520 has a programmable jitter and wander transfer characteristic. This is set by the DPLL bandwidth. The -3 dB jitter transfer attenuation point can be set in the range from 0.1 Hz to 70 Hz in 10 steps. The wander and jitter transfer characteristic is shown in Figure 8. Wander on the local oscillator clock will not have a significant effect on the output clock whilst in Locked mode, provided that the DPLL bandwidth is set high enough so that the DPLL can compensate quickly enough for any frequency changes in the crystal.

In Free-run or Holdover mode wander on the crystal is more significant. Variation in crystal temperature or supply voltage both cause drifts in operating frequency, as does ageing. These effects must be limited by careful selection of a suitable component for the local oscillator, as specified in the section See Local Oscillator Clock.

Phase Build-out

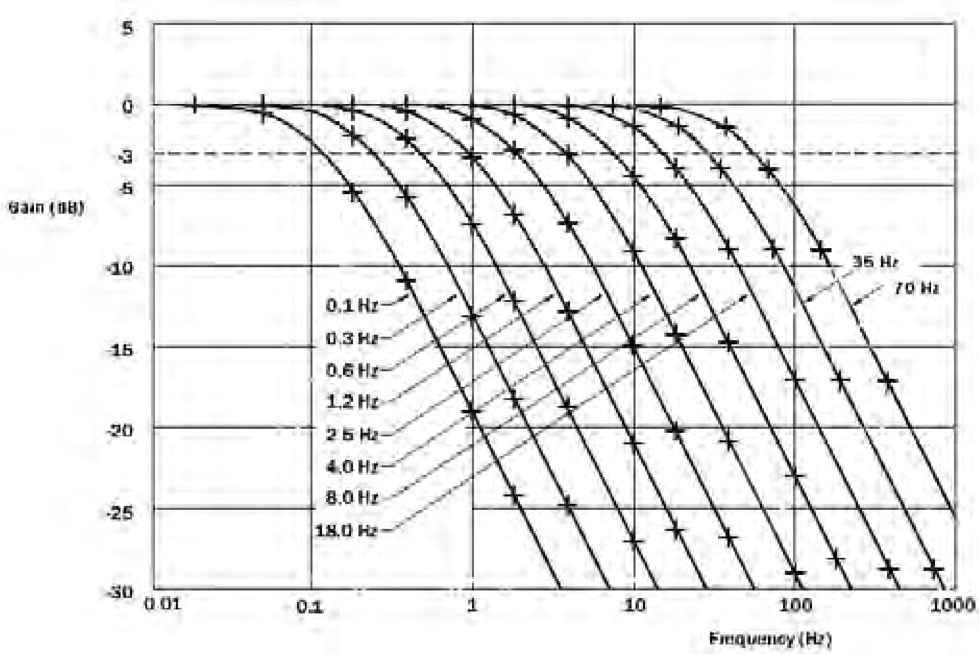
Phase Build-out (PBO) is the function to minimize phase transients on the output SEC clock during input reference switching. If the currently selected input reference clock source is lost (due to a short interruption, out of frequency detection, or complete loss of reference) the second, next highest priority reference source will be selected, and a PBO event triggered.

ITU-T G.813[11] states that the maximum allowable short-term phase transient response, resulting from a switch from one clock source to another, with Holdover mode entered in between, should be a maximum of 1 µs over a 15 second interval. The maximum phase transient or jump should be less than 120 ns at a rate of change of less than 7.5 ppm and the Holdover performance should be better than 0.05 ppm. The ACS8520 performance is well within this requirement. The typical phase disturbance on clock reference source switching will be less than 5 ns on the ACS8520.

When a PBO event is triggered, the device enters a temporary Holdover state. When in this temporary state, the phase of the input reference is measured, relative to the output. The device then automatically accounts for any measured phase difference and adds the appropriate phase offset into the DPLL to compensate. Following a PBO event, whatever the phase difference on change of input, the output phase transient is minimized to be no greater than 5 ns.

On the ACS8520, PBO can be enabled, disabled or frozen using the microprocessor interface. By default, it is enabled. When PBO is enabled, PBO can also be frozen (at the current offset setting). The device will then ignore any further PBO events occurring on any subsequent

Figure 8 Sample of Wander and Jitter Measured Transfer Characteristics



reference switch, and maintain the current phase offset. If PBO is disabled while the device is in the Locked mode, there may be a phase shift on the output SEC clocks as the DPLL locks back to 0 degrees phase error. The rate of phase shift will depend on the programmed bandwidth. Enabling PBO whilst in the Locked stated will also trigger a PBO event.

PBO Phase Offset

In order to minimize the systematic (average) phase error for PBO, a PBO Phase Offset can be programmed in 0.101 ns steps in the *cnfg_phase_offset_pbo* register, Reg.72. The range of the programmable PBO phase offset is restricted to ±1.4 ns. This can be used to eliminate an accumulation of phase shifts in one direction.

Input to Output Phase Adjustment

When PBO is off, such that the system always tries to align the outputs to the inputs at the 0° position, there is a mechanism provided in the ACS8520 for precise fine tuning of the output phase position with respect to the input. This can be used to compensate for circuit and board wiring delays. The output phase can be adjusted in 6 ps steps up to 200 ns in a positive or negative direction. The phase adjustment actually changes the phase position of the feedback clock so that the DPLL adjusts the output clock phases to compensate. The rate of change of phase is therefore related to the DPLL bandwidth. For the DPLL to track large instant changes in phase, either Lock8k mode should be on, or the coarse phase detector should be enabled. Register *cnfg_phase_offset* at Reg. 70 and 71 controls the output phase, which is only used when Phase Build-out is off (Reg. 48, Bit 2 = 0 and Reg. 76, Bit 4 =0).

Input Wander and Jitter Tolerance

The ACS8520 is compliant to the requirements of all relevant standards, principally ITU Recommendation G.825[15], ANSI DS1.101-1999[1], Telcordia GR1244, GR253, G812, G813 and ETS 300 462-5 (1997).

All reference clock inputs have a tight frequency tolerance but a generous jitter tolerance. Pull-in, hold-in and pull-out ranges are specified in Table 8. Minimum jitter tolerance masks are specified in Figures 9 and 10, and Tables 8 and 10, respectively. The ACS8520 will tolerate wander and jitter components greater than those shown in Figure 9 and Figure 10, up to a limit determined by a combination of the apparent long-term frequency offset caused by wander and the eye-closure caused by jitter (the input source will be rejected if the offset pushes the frequency outside the hold-in range for long enough to be detected, whilst the signal will also be rejected if the eye closes sufficiently to affect the signal purity). Either the Lock8k mode, or one of the extended phase capture ranges should be engaged for high jitter tolerance according to these masks.

All reference clock ports are monitored for quality, including frequency offset and general activity. Single short-term interruptions in selected reference clocks may not cause re- arrangements, whilst longer interruptions, or multiple, short-term interruptions, will cause re-arrangements, as will frequency offsets which are sufficiently large or sufficiently long to cause loss-of-lock in the phase-locked loop. The failed reference source will be removed from the priority table and declared as unserviceable, until its perceived quality has been restored to an acceptable level.

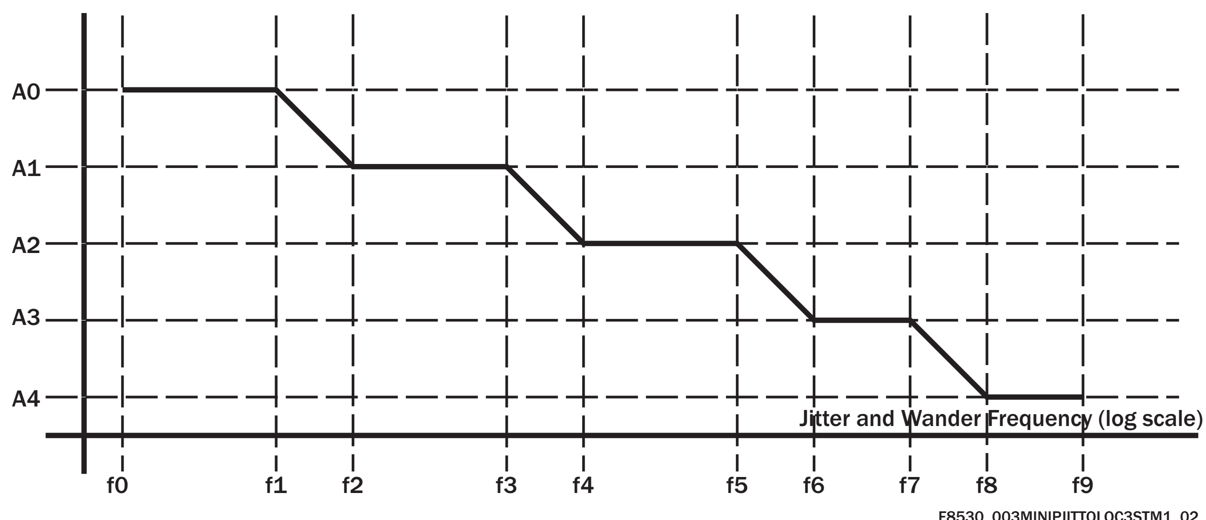
Table 8 Input Reference Source Jitter Tolerance

Jitter Tolerance	Frequency Monitor Acceptance Range	Frequency Acceptance Range (Pull-in)	Frequency Acceptance Range (Hold-in)	Frequency Acceptance Range (Pull-out)
G.703[6]	±16.6 ppm	±4.6 ppm (see Note (i)) ±9.2 ppm (see Note (ii))	±4.6 ppm (see Note (i)) ±9.2 ppm (see Note (ii))	±4.6 ppm (see Note (i)) ±9.2 ppm (see Note (ii))
G.783[9]				
G.823[13]				
GR-1244-CORE[19]				

Notes: (i) The frequency acceptance and generation range will be ±4.6 ppm around the required frequency when the external crystal frequency accuracy is within a tolerance of ±4.6 ppm.

(ii) The fundamental acceptance range and generation range is ±9.2 ppm with an exact external crystal frequency of 12.800 MHz. This is the default DPLL range, the range is also programmable from 0 to 80 ppm in 0.08 ppm steps.

Figure 9 Minimum Input Jitter Tolerance (OC-3/STM-1)



Note...For inputs supporting G.783[9] compliant sources.)

Table 9 Amplitude and Frequency Values for Jitter Tolerance (OC-3/STM-1)

STM level	Peak to peak amplitude (unit Interval)					Frequency (Hz)									
	A0	A1	A2	A3	A4	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9
STM-1	2800	311	39	1.5	0.15	12 u	178 u	1.6 m	15.6 m	0.125	19.3	500	6.5 k	65 k	1.3

Figure 10 Minimum Input Jitter Tolerance (DS1/E1)

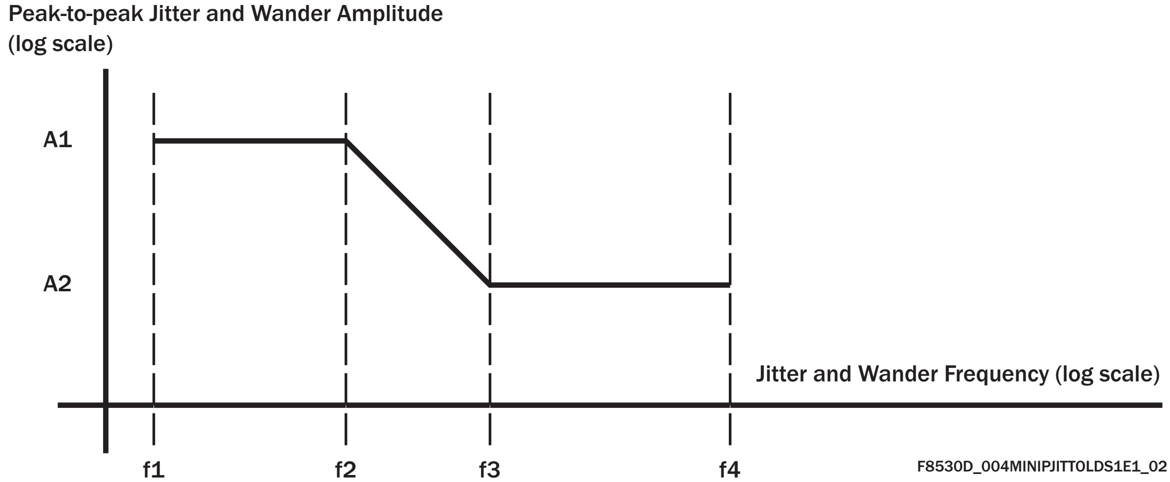


Table 10 Amplitude and Frequency Values for Jitter Tolerance (DS1/E1)

Type	Spec.	Amplitude (UI p-p)		Frequency (Hz)			
		A1	A2	F1	F2	F3	F4
DS1	GR-1244-CORE[19]	5	0.1	10	500	8 k	40 k
E1	ITU G.823[13]	1.5	0.2	20	2.4 k	18 k	100

Using the DPLLs for Accurate Frequency and Phase Reporting

The frequency monitors in the ACS8520 perform frequency monitoring with a programmable acceptable limit of up to ±60.96 ppm. The resolution of the measurement is 3.8 ppm and the measured frequency can be read back from Reg. 4C, with channel selection at Reg. 4B. For more accurate measurement of both frequency and phase, the T0 and T4 DPLLs and their phase detectors, can be used to monitor both input frequency and phase. The T0 DPLL is always monitoring the currently locked to source, but if the T4 path is not used then the T4 DPLL can be used as a roving phase and frequency meter. Via software control it could be switched to monitor each input in turn and both the phase and frequency can be reported with a very fine resolution.

The registers *sts_current_dpll_frequency* (Reg. 0C, Reg. 0D and Reg. 07) report the frequency of either the T0 or T4 DPLL with respect to the external crystal XO frequency (after calibration via Reg. 3C, 3D if used). The selection of T4 or T0 DPLL reporting is made via Reg. 4B, Bit 4. The value is a 19-bit signed number with one LSB representing 0.0003068 ppm (range of ±80 ppm). This value is actually the integral path value in the DPLL, and as such corresponds to an averaged measurement of the input frequency, with an averaging time inversely proportional to the DPLL bandwidth setting. Reading this regularly can show how the currently locked source is varying in value e.g. due to frequency wander on its input.

The input phase, as seen at the DPLL phase detector, can be read back from register *sts_current_phase*, Reg. 77 and 78. T0 or T4 DPLL phase detector reporting is again controlled by Reg. 4B, Bit 4. One LSB corresponds to approximately 0.7 degrees phase difference. For the T0 DPLL this will be reporting the phase difference between the input and the internal feedback clock. The phase result is internally averaged or filtered with a -3 dB attenuation point at approximately 100 Hz. For low DPLL bandwidths, 0.1 Hz for example, this measured phase information from the T0 DPLL gives input phase wander in the frequency band from for example 0.1 Hz to 100 Hz. This could be used to give a crude input MTIE measurement up to an observation period of approximately 1000 seconds using external software.

In addition, the T4 DPLL phase detector can be used to make a phase measurement between two inputs. Reg. 65, Bit 7 is used to switch one input to the T4 phase detector over to the current T0 input. The other phase detector input remains connected to the selected T4 input source, the selected source can be forced via Reg. 35, Bits [3:0], or changed via the T4 priority (Reg. 18 to 1E, when Reg. 4B, Bit 4 = 1).

Consequently the phase detector from the T4 DPLL could be used to measure the phase difference between the currently selected source and the stand-by source, or it could be used to measure the phase wander of all stand-by sources with respect to the current source by selecting each input in sequence. An MTIE and TDEV calculation could be made for each input via external processing.

Configuration for Redundancy Protection

When two ACS8520 devices are to be used in a redundancy-protection scheme within a Network Element (NE), one will be designated as Master, one as Slave.

Table 11 How to Align Outputs of Two ACS8520 Devices

Action	Result
If possible, one device (the nominated Slave) should lock to the other device (the nominated Master).	With the Slave locked to the Master, their output frequencies will be guaranteed to be the same.
All programmed priorities within the two devices should be the same, except for the fact that (1)the Master output is designated the highest priority input on the Slave.(2) the Slave output is designated zero priority (disabled) on the Master. (Reg. 18 to 1E)	These two actions ensure that if the Master device fails, the Slave device will switch to lock to the same source that the Master was locked to before it failed.
Any input detected as invalid in one device should be disabled within the other device. (Reg. 0E/0F & 30/31)	
Phase Build-out should be disabled on the Slave whilst it is locked to the Master.	This will ensure that the phase of the Slave is locked to the phase of the Master. It also enables the use of the Phase offset control register to compensate for delays between the Master and Slave.
Revertive mode should be enabled.	This will ensure that the Slave locks to the Master although it may have been locked to another source previously.
The bandwidth of the Slave should be set higher than that of the Master (it is recommended to configure the slave with the highest supported bandwidth).	This ensures that any transient occurring on the output of the Master is followed as closely as possible on the Slave.

It is expected that an NE will use the T0 output for its internal operations. The phase of the outputs from the T4 path (TO8 & TO9) will not be aligned, unless the T4 outputs are locked to the T0 outputs.

In many applications, the clocks supplied into the system are required to be aligned not only in frequency, but also in phase between the Master and Slave devices. This ensures minimal disturbance when any clock sink switches between Master and Slave.

In order to ensure that the outputs of the two ACS8520s are always aligned in frequency and phase, the procedures in Table 11 should be followed.

In order to maintain the conditions outlined in Table 11 it is necessary for software systems to maintain monitoring and control functions. These monitoring functions should either poll the device or respond to interrupts in order to maintain the correct settings within the two devices. Please refer to the descriptions or registers mentioned in Table 11 and also Regs 34, 3B, 48, 67 and 69, for more details on these associated settings. See also Application Note AN-SETS-7.

Table 12 MSTSLVB Pin Operation

MSTSLVB	Feature	Setting	Reason
1 = Master	Priority of input I11	As programmed (program 0 to ensure it gets disabled)	Make sure that the designated Master device cannot lock to the output of the Slave device.
	Phase Build-out	As programmed in register.	If the system requires PBO, then this being enabled on the Master will give the overall system performance with PBO. The slave only needs to track the Master (no PBO).
	Revertive mode	As programmed in register.	Revertive behavior of the Master in a Master/Slave system will define the overall Revertive behavior of the system.
	T0 DPLL bandwidth	As programmed in register (automatic or manual).	Device selects locked or acquisition bandwidth.

Table 12 MSTSLVB Pin Operation (cont...)

MSTSLVB	Feature	Setting	Reason
0 = Slave	Priority of input I11	1 (highest priority).	When a Slave, this input is designated as that connected to the output of the Master.
	Phase Build-out	Disabled.	This ensures that the Slave locks to the Master with the minimum phase offset possible.
	Revertive mode	Enabled	This ensures that the Slave always locks to the Master when it is available.
	T0 DPLL bandwidth	Forced to the acquisition bandwidth setting.	A higher bandwidth on the Slave ensures closer phase tracking.

For direct hardware control of Master or Slave operation the Master/Slave control pin (MSTSLVB) can be used to externally control some of these functions according to Table 12. These functions can also be controlled via software.

Whilst the Master and Slave outputs could be cross-connected and connected to any input on the alternative device, input I11 has been chosen as the input controlled by the MSTSLVB pin.

Alignment of Priority Tables in Master and Slave ACS8520

In a redundant system where the Slave is normally locked to the Master device, if the Master device fails the Slave device must revert to locking to the same external reference that the Master was locked to. This will ensure that minimum disturbance, both in frequency and phase, is created on the output of the Slave device due to the failure of the Master device. As stated previously (Table 11), it is recommended that the programmed priorities of the reference sources are the same in both devices, apart from the Master/Slave cross-connect inputs.

Both devices can also monitor all their reference sources and determine the validity of each source. It is recommended that the availability of valid sources are also aligned between the two devices. This is achieved by writing the value, as reported by *sts_sources_valid* Reg. 0E & 0F), from one device into the *cnfg_sts_remote_sources_valid* register (Reg. 30 & 31) of the other. This will ensure that any source considered invalid by one device is also considered invalid by the other. If a failure of the Master does occur, this will ensure that the Slave will always select the reference that the Master was locked to.

T4 Generation in Master and Slave ACS8520

As specified by the I.T.U., there is no need to align the phases of the T4 outputs in Master and Slave devices. For a fully redundant system, there is a need, however, to ensure that all devices select the same reference source. As there is no need to guarantee the alignment of phase of the T4 outputs, the Slave devices T4 input does not need to lock to the Masters T4 output, but only needs to ensure that it locks to the same external reference source. The actions of aligning the priority tables and available reference sources performed for the T0 outputs will be equally valid for the T4 outputs. The only difference being that the input connected to the Master's output is disabled for the T4 path (allowing it only to lock to external references). This can be easily achieved as the T4 and T0 paths have separate programmed priorities. There is no defined Holdover requirement for the T4 path.

Alignment of the Output Clock Phases in Master and Slave ACS8520

When the **ACS8520** is locked to a reference source of frequency f, the output clocks of frequency f will be in-phase with the reference source (with Phase Build-out disabled). As all T0 output clocks from the **ACS8520** are derived from the same T0 frequency, any frequency greater than f at the output will be “falling edge aligned” with the output at frequency f. Any frequency less than f will be effectively a division of f, if possible. Similarly for T4, all T4 output clocks will be phase-related to the T4 input.

The effect of this relationship is that if the Master and Slave devices are cross-connected with 19.44 MHz clocks, their output clocks at 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz & 311.04 MHz will be aligned between the 2 devices. However, their outputs of 6.48 MHZ, 1.544 MHz, 2.048 MHz, 2 kHz and 8 kHz etc. would not necessarily be aligned. Whilst most applications would not be affected by the non-alignment of most of these clocks, the non-alignment of the 2 kHz and/or the 8 kHz may cause framing errors.

There are 2 ways to align the 2 kHz and/or 8 kHz outputs:

1. the use of the External syncing function, or
2. directly locking the Slave to 2 kHz or 8 kHz from the Master.

By directly locking the Slave to the 2 kHz (MFrSync) output of the Master, all frequencies output from the Slave will be in phase alignment with the same frequency generated from the Master. If the Slave is directly locked to the 8 kHz (FrSync) output from the Master, then all frequencies except for 2 kHz MFrSync outputs will be in alignment.

If using the external syncing function then two signals need to be interconnected between the Master and Slave:

1. the clock and,
2. the Sync signal.

This requires some configuration enhancements. The Sync signal is not locked to, it is sampled using the reference clock and used to realign the generated outputs. The generated outputs are still always locked to the reference clock and related to each other. Details on the Master and Slave interconnection wiring and software configuration can be found in refer to the application note AN-SETS-2. The following section describes the resynchronization operation of the MFrSync via the SYNC2K input.

MFrSync and FrSync Alignment-SYNC2K

The SYNC2K input (pin 45) is monitored by the ACS8520 for consistent phase and correct frequency and if it does not pass these quality checks, an alarm flag is raised (Reg. 08, Bit 7 and Reg. 09, Bit 7). The check for consistent phase involves checking that each input edge is within an expected timing window. The window size is set by Reg. 7C, Bits [6:4]. An internal detector senses that a correct SYNC2K signal is present and only then allows the signal to resynchronize the internal dividers that generate the 8 kHz FrSync and 2 kHz MFrSync outputs. This sequence avoids spurious resynchronizations that may otherwise occur with connections and disconnections of the SYNC2K input.

The SYNC2K input will normally be a 2 kHz frequency, only its falling edge is used. It can however be at a frequencies of 4 kHz or 8 kHz without any change to the register setups. Only alignment of the 8 kHz will be achieved in this case.

Safe sampling of the SYNC2K input is achieved by using the currently selected clock reference source to do the input sampling. This is based on the principle that FrSync alignment is being used on a Slave device that is locked to the clock reference of a Master device that is also providing the 2 kHz SYNC2K input. Phase Build-out mode should be off (Reg. 48, Bit 2 = 0). The 2 kHz MFrSync output from the Master device has its falling edge aligned with the falling edge of the other output clocks, hence the SYNC2K input is normally sampled on the rising edge of the current input reference clock, in order to provide the most margin. Some modification of the expected timing of the SYNC2K with respect to the reference clock can be achieved via Reg. 7B, Bits [1:0]. This allows for the SYNC2K input to arrive either half a reference clock cycle early or up to one and a half cycle late, hence allowing a safe sampling margin to be maintained.

A different sampling resolution is used depending on the input reference frequency and the setting of Reg. 7B Bit 6, *cnfg_sync_phase*. With this bit *Low*, the SYNC2K input sampling has a 6.48 MHz resolution, this being the preferred reference frequency to lock to from the Master, in conjunction with the SYNC2K 2 kHz, since it gives the most timing margin on the sampling and aligns all of the higher rate OC-3 derived clocks. When Bit 6 is high the SYNC2K can have a sampling resolution of either 19.44 MHz (when the current locked to reference is 19.44 MHz) or 38.88 MHz (all other frequencies). This would allow for instance a 19.44 MHz and 2 kHz pair to be used for Slave synchronization or for Line card synchronization. Reg. 7B Bit 7, *indep_FrSync/MFrSync* controls whether the 2 kHz MFrSync and 8 kHz FrSync outputs keep their precise alignment with the other output clocks.

When *indep_FrSync/MFrSync* Reg. 7B Bit 7 is *Low* the FrSyncs and the other higher rate clocks are not independent and their alignment on the falling 8kHz edge is maintained. This means that when Bit *Sync_OC-N_rates* is *High*, the OC-N rate dividers and clocks are also synchronized by the SYNC2K input. On a change of phase position of the SYNC2K, this could result in a shift in phase of the 6.48 MHz output clock when a 19.44 MHz precision is used for the SYNC2K input. To avoid disturbing any of the output clocks and only align the MFrSync and FrSync outputs, at the chosen level of precision, then independent Frame Sync mode can be used (Reg. 7B, Bit 7 = 1). Edge alignment of the FrSync output with other clocks outputs may then change depending on the SYNC2K sampling precision used. For example, with a 19.44 MHz reference input clock and Reg. 7B, Bits 6 and 7 both *High* (independent mode and Sync OC-N rates), then the FrSync output will still align with the 19.44 MHz output but not with the 6.48 MHz output clock.

The FrSync and MFrSync outputs always come from the T0 DPLL path. 2kHz and 8kHz outputs can also be produced at the TO1 to TO7 outputs. These can come from either the T0 DPLL or from the T4 DPLL, controlled by Reg. 7A, Bit 7.

If required, this allows the T4 DPLL to be used as a separate PLL for the FrSync and MFrSync path with a 2 kHz input and 2 kHz and 8 kHz Frame Sync outputs.

Output Clock Ports

The device supports a set of main output clocks, T0 and T4, and a pair of secondary Sync outputs, FrSync and MFrSync. The two main output clocks, T0 and T4, are independent of each other and are individually selectable. The two secondary output clocks, FrSync and MFrSync, are derived from either T0 or T4. The frequencies of the main output clocks are selectable from a range of pre-defined spot frequencies and a variety of output technologies are supported, as defined in Table 13.

PECL/LVDS/AMI Output Port Selection

The choice of PECL or LVDS compatibility is programmed via the *cnfg_differential_outputs* register, Reg. 3A.

AMI port, TO8, supports a composite clock, consisting of a 64 kHz AMI clock with 8 kHz boundaries marked by deliberate violations of the AMI coding rules, as specified in ITU recommendation G.703[6]. Departures from the nominal pattern are detected within the ACS8520, and may cause reference-switching if too frequent. See “DC Characteristics: AMI Input/Output Port” on page 138., for more details.

Output Frequency Selection and Configuration

The output frequency at many of the outputs is controlled by a number of inter-dependent parameters. These parameters control the selections within the various blocks shown in Figure 11.

The ACS8520 contains two main DPLL/APLL paths. Whilst they are largely independent, there are a number of ways in which these two structures can interact. Figure 11 shows an expansion of the original Block Diagram (Figure 1) for the PLL paths.

T0 DPLL and APLLs

The T0 DPLL always produces 77.76 MHz regardless of either the reference frequency (frequency at the input pin of the device) or the locking frequency (frequency at the input of the DPLL Phase and Frequency Detector (PFD)).

The input reference is either passed directly to the PFD or via a pre-divider (not shown) to produce the reference input. The feedback 77.76 MHz is either divided or synthesized to generate the locking frequency.

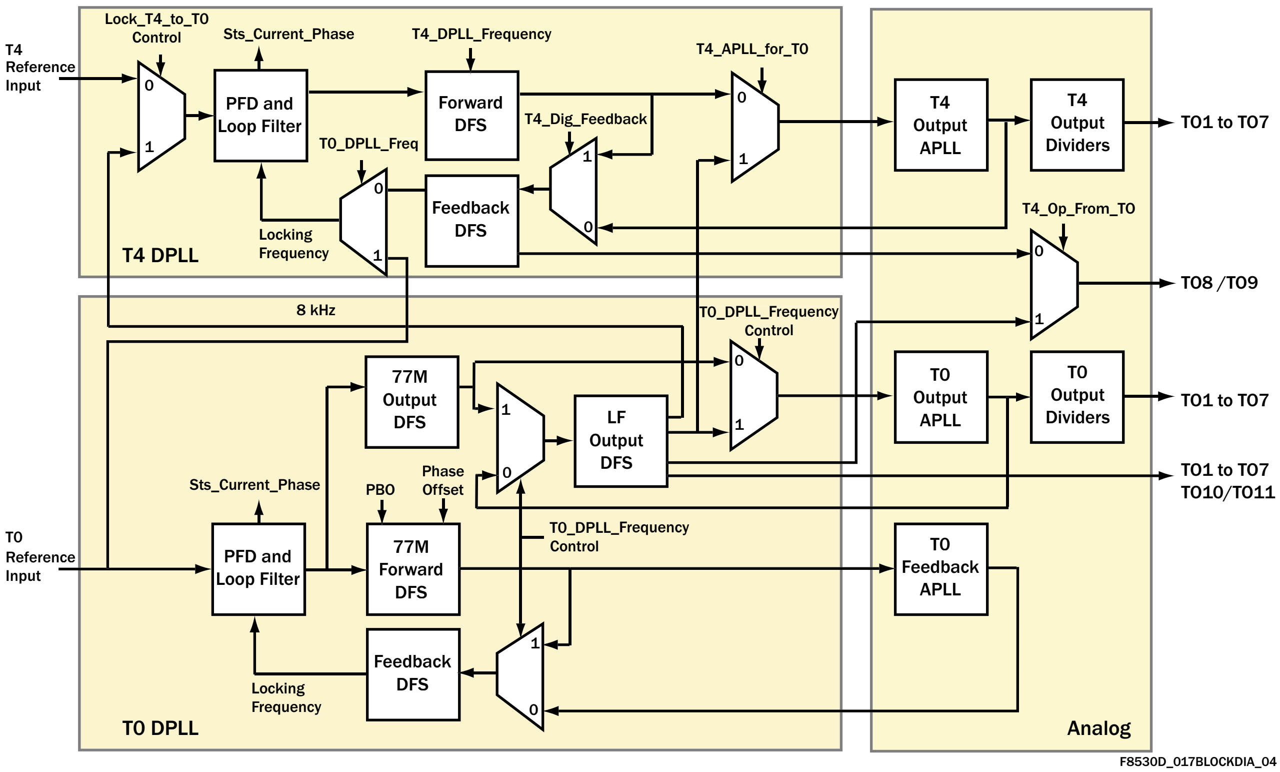
Digital Frequency Synthesis (DFS) is a technique for generating an output frequency using a higher frequency system clock (204.8 MHz in the case of the 77.76 MHz synthesis). However, the edges of the output clock are not ideally placed in time, since all edges of the output clock will be aligned to the active edge of the system clock. This will mean that the generated clock will inherently have jitter on it equivalent to one period of the system clock.

The T0 77M forward DFS block uses DFS clocked by the 204.8 MHz system clock to synthesize the 77.76 MHz and, therefore, has an inherent 4.9 ns of p-p jitter. There is an option to use an APLL, the T0 feedback APLL, to filter out this jitter before the 77.76 MHz is used to generate the feedback locking frequency in the T0 feedback DFS block. This analog feedback option allows a lower jitter (<1 ns) feedback signal to give maximum performance. The digital feedback option is present so that when the output path is switched to digital feedback the two paths remain synchronized.

The T0 77M forward DFS block is also the block that handles Phase Build-out and any phase offset programmed into the device. Hence, the T0 77M forward DFS and the T0 77M output DFS blocks are locked in frequency but may be offset in phase.

The T0 77M output DFS block also uses the 204.8 MHz system clock and always generates 77.76 MHz for the output clocks (with inherent 4.9 ns of jitter). This is fed to another DFS block and to the T0 output APLL. The low frequency T0 LF output DFS block is used to produce three frequencies; two of them, Digital1 and Digital2, are available for selection to be produced at outputs TO1-TO7, and the third frequency can produce multiple E1/DS1 rates via the filtering APLLs. The input clock to the T0 LF output DFS block is either 77.76 MHz from the T0 output APLL (post jitter filtering) or 77.76 MHz direct from the T0 77M output DFS. Utilizing the clock from the T0 output APLL will result in lower jitter outputs from the T0 LF output DFS block.

Figure 11 PLL Block Diagram



However, when the input to the T0 APLL is taken from the T0 LF output DFS block, the input to that block comes directly from the T0 77M output DFS block so that a “loop” is not created.

The T0 output APLL is for multiplying and filtering. The input to the T0 output APLL can be either 77.76 MHz from the T0 77M output DFS block or an alternative frequency from the T0 LF output DFS block (offering 77.76 MHz, 12E1, 16E1, 24DS1 or 16DS1). The frequency from the T0 output APLL is four times its input frequency i.e. 311.04 MHz when used with a 77.76 MHz input. The T0 output APLL is subsequently divided by 1, 2, 4, 6, 8, 12, 16 and 48 and these are available at the T01-T07 outputs.

T4 DPLL & APLL

The T4 path is much simpler than the T0 path. This path offers no Phase Build-out or phase offset. The T4 input can be used to either lock to a reference clock input independent of the T0 path, or lock to the T0 path. Unlike the T0 path, the T4 forward DFS block does not always generate 77.76 MHz. The possible frequencies are listed in the table. Similar to the T0 path, the output of the T4 forward DFS block is generated using DFS clocked by the 204.8 MHz system clock and will have an inherent jitter of 4.9 ns.

The T4 feedback DFS also has the facility to be able to use the post T4 APLL (jitter-filtered) clock to generate the feedback locking frequency. Again, this will give the maximum performance by using a low jitter feedback.

The T4 output APLL block is also for multiplying and filtering. The input to the T4 output APLL can come either from the T4 forward DFS block or from the T0 path. The input to the T4 output APLL can be programmed to be one of the following:

(a) Output from the T4 forward DFS block (12E1, 24DS1, 16E1, 16DS1, E3, DS3, OC-N),

(b) 12E1 from T0,

(c) 16E1 from T0,

(d) 24DS1 from T0,

(e) 16DS1 from T0.

The frequency generated from the T4 output APLL block is four times its input frequency i.e. 311.04 MHz when used with a 77.76 MHz input. The T4 output APLL is subsequently divided by 2, 4, 8, 12, 16, 48 and 64 and these are available at the TO1-TO7 outputs.

The TO8 and TO9 outputs are driven from either the T4 or the T0 path. The TO10 and TO11 outputs are always generated from the T0 path. Reg.7A Bit 7 selects whether the source of the 2 kHz and 8 kHz outputs available from TO1-TO7 is derived from either the T0 or the T4 paths.

Output Frequency Configuration Steps

The output frequency selection is performed in the following steps:

1. Does the application require the use of the T4 path as an independent PLL path or not. If not, then the T4 path can be utilized to produce extra frequencies locked to the T0 path.
2. Refer to Table 15, Frequency Divider Look-up, to choose a set of output frequencies- one for each path, T4 and T0. Only one set of frequencies can be generated simultaneously from each path.
3. Refer to the Table 15 to determine the required APLL frequency to support the frequency set.
4. Refer to Table 16, T0 APLL Frequencies, and Table 17, T4 APLL Frequencies, to determine what mode the T0 and T4 paths need to be configured in, considering the output jitter level.
5. Refer to Table 18, TO1 - TO7 output Frequency Selection, and the column headings in Table 15, Frequency Divider Look-up, to select the appropriate frequency from either of the APLLs on each output as required.

Table 13 Output Reference Source Selection Table

Port Name	Output Port Technology	Frequencies Supported
T01	TTL/CMOS	Frequency selection as per Table 14 and Table 18
T02	TTL/CMOS	
T03	TTL/CMOS	
T04	TTL/CMOS	
T05	TTL/CMOS	
T06	LVDS/PECL (LVDS default)	
T07	PECL/LVDS (PECL default)	
T08	AMI	64/8 kHz (composite clock, 64 kHz + 8 kHz), fixed frequency.
T09	TTL/CMOS	Fixed frequency, either 1.544 MHz or 2.048 MHz.
T010	TTL/CMOS	FrSync, 8 kHz programmable pulse width and polarity, see Reg. 7A.
T011	TTL/CMOS	MFrSync, 2 kHz programmable pulse width and polarity, see Reg. 7A.

Note...1.544 MHz/2.048 MHz are shown for SONET/SDH respectively. Pin SONSDHB controls default, when High SONET is default.

Table 14 Output Frequency Selection

Frequency (MHz, unless stated otherwise)		T0 DPLL Mode	T4 DPLL Mode	T4 APLL Input Mux	Jitter Level (typ)	
					rms (ps)	p-p (ns)
2 kHz		77.76 MHz Analog	-	-	60	0.6
2 kHz		Any digital feedback mode	-	-	1400	5
8 kHz		77.76 MHz Analog	-	-	60	0.6
8 kHz		Any digital feedback mode	-	-	1400	5
1.536	(not TO4/TO5)	-	12E1 mode	Select T4 DPLL	500	2.3
1.536	(not TO4/TO5)	-	-	Select T0 DPLL 12E1	250	1.5
1.544	(not TO4/TO5)	-	16DS1 mode	Select T4 DPLL	200	1.2
1.544	(not TO4/TO5)	-	-	Select T0 DPLL 16DS1	150	1.0
1.544	via Digital1 (not TO7) or Digital2 (not TO6)	77.76 MHz Analog	-	-	3800	13
1.544	via Digital1 (not TO7) or Digital2 (not TO6)	Any digital feedback mode	-	-	3800	18
2.048		-	12E1 mode	Select T4 DPLL	500	2.3
2.048		-	-	Select T0 DPLL 12E1	250	1.5
2.048	(not TO4/TO5)	-	16E1 mode	Select T4 DPLL	400	2.0
2.048	(not TO4/TO5)	-	-	Select T0 DPLL 16E1	220	1.2
2.048	(not TO6)	12E1 mode	-	-	900	4.5
2.048	via Digital1 (not TO7) or Digital2 (not TO6)	77.76 MHz Analog	-	-	3800	13
2.048	via Digital1 (not TO7) or Digital2 (not TO6)	Any digital feedback mode	-	-	3800	18
2.059		-	16DS1 mode	Select T4 DPLL	200	1.2
2.059		-	-	Select T0 DPLL 16DS1	150	1.0
2.059	(not TO6)	16DS1 mode	-	-	760	2.6
2.316	(not TO4/TO5)	-	24DS1 mode	Select T4 DPLL	110	0.75
2.316	(not TO4/TO5)	-	-	Select T0 DPLL 24DS1	110	0.75
2.731		-	16E1 mode	Select T4 DPLL	400	1.5
2.731		-	-	Select T0 DPLL 16E1	220	1.2
2.731	(not TO6)	16E1 mode	-	-	250	1.6
2.796	(not TO4/TO5)	-	DS3 mode	Select T4 DPLL	110	1.0
3.088		-	24DS1 mode	Select T4 DPLL	110	0.75
3.088		-	-	Select T0 DPLL 24DS1	110	0.75
3.088	(not TO6)	24DS1 mode	-	-	110	0.75
3.088	via Digital1 (not TO7) or Digital2 (not TO6)	77.76 MHz Analog	-	-	3800	13
3.088	via Digital1 (not TO7) or Digital2 (not TO6)	Any digital feedback mode	-	-	3800	18

Table 14 Output Frequency Selection (cont...)

Frequency (MHz, unless stated otherwise)		T0 DPLL Mode	T4 DPLL Mode	T4 APLL Input Mux	Jitter Level (typ)	
					rms (ps)	p-p (ns)
3.728		-	DS3 mode	Select T4 DPLL	110	1.0
4.096	via Digital1 (not TO7) or Digital2 (not TO6)	77.76 MHz Analog	-	-	3800	13
4.096	via Digital1 (not TO7) or Digital2 (not TO6)	Any digital feedback mode	-	-	3800	18
4.296	(not TO4/TO5)	-	E3 mode	Select T4 DPLL	120	1.0
4.86	(not TO4/TO5)	-	77.76 MHz mode	Select T4 DPLL	60	0.6
5.728		-	E3 mode	Select T4 DPLL	120	1.0
6.144		12E1 mode	-	-	900	4.5
6.144		-	12E1 mode	Select T4 DPLL	500	2.3
6.144		-	-	Select T0 DPLL 12E1	250	1.5
6.176		16DS1 mode	-	-	760	2.6
6.176		-	16DS1 mode	Select T4 DPLL	200	1.2
6.176		-	-	Select T0 DPLL 16DS1	150	1.0
6.176	via Digital1 (not TO7) or Digital2 (not TO6)	77.76 MHz Analog	-	-	3800	13
6.176	via Digital1 (not TO7) or Digital2 (not TO6)	Any digital feedback mode	-	-	3800	18
6.48		-	77.76 MHz mode	Select T4 DPLL	60	0.6
6.48	(not TO6)	77.76 MHz analog	-	-	60	0.6
6.48	(not TO6)	77.76 MHz digital	-	-	60	0.6
8.192		12E1 mode	-	-	900	4.5
8.192		16E1 mode	-	-	250	1.6
8.192		-	16E1 mode	Select T4 DPLL	400	2.0
8.192		-	-	Select T0 DPLL 16E1	220	1.2
8.192	via Digital1 (not TO7) or Digital2 (not TO6)	77.76 MHz Analog	-	-	3800	13
8.192	via Digital1 (not TO7) or Digital2 (not TO6)	Any digital feedback mode	-	-	3800	18
8.235		16DS1 mode	-	-	760	2.6
9.264		24DS1 mode	-	-	110	0.75
9.264		-	24DS1 mode	Select T4 DPLL	110	0.75
9.264		-	-	Select T0 DPLL 24DS1	110	0.75
10.923		16E1 mode	-	-	250	1.6
11.184		-	DS3 mode	Select T4 DPLL	110	1.0
12.288		12E1 mode	-	-	900	4.5
12.288		-	12E1 mode	Select T4 DPLL	500	2.3

Table 14 Output Frequency Selection (cont...)

Frequency (MHz, unless stated otherwise)	T0 DPLL Mode	T4 DPLL Mode	T4 APLL Input Mux	Jitter Level (typ)	
				rms (ps)	p-p (ns)
12.288	-	-	Select T0 DPLL 12E1	250	1.5
12.352	24DS1 mode	-	-	110	0.75
12.352	16DS1 mode	-	-	760	2.6
12.352	-	16DS1 mode	Select T4 DPLL	200	1.2
12.352	-	-	Select T0 DPLL 16DS1	150	1.0
12.352 via Digital1 (not TO7) or Digital2 (not TO6)	77.76 MHz Analog	-	-	3800	13
12.352 via Digital1 (not TO7) or Digital2 (not TO6)	Any digital feedback mode	-	-	3800	18
16.384	12E1 mode	-	-	900	4.5
16.384	16E1 mode	-	-	250	1.6
16.384	-	16E1 mode	Select T4 DPLL	400	2.0
16.384	-	-	Select T0 DPLL 16E1	220	1.2
16.384 via Digital1 (not TO7) or Digital2 (not TO6)	77.76 MHz Analog	-	-	3800	13
16.384 via Digital1 (not TO7) or Digital2 (not TO6)	Any digital feedback mode	-	-	3800	18
16.469	16DS1 mode	-	-	760	2.6
17.184	-	E3 mode	Select T4 DPLL	120	1.0
18.528	24DS1 mode	-	-	110	0.75
18.528	-	24DS1 mode	Select T4 DPLL	110	0.75
18.528	-	-	Select T0 DPLL 24DS1	110	0.75
19.44	77.76 MHz analog	-	-	60	0.6
19.44	77.76 MHz digital	-	-	60	0.6
19.44	-	77.76MHz mode	Select T4 DPLL	60	0.6
21.845	16E1 mode	-	-	250	1.6
22.368	-	DS3 mode	Select T4 DPLL	110	1.0
24.576	12E1 mode	-	-	900	4.5
24.576	-	12E1 mode	Select T4 DPLL	500	2.3
24.576	-	-	Select T0 DPLL 12E1	250	1.5
24.704	24DS1 mode	-	-	110	0.75
24.704	16DS1 mode	-	-	760	2.6
24.704	-	16DS1 mode	Select T4 DPLL	200	1.2
24.704	-	-	Select T0 DPLL 16DS1	150	1.0
25.92	77.76 MHz analog	-	-	60	0.6

Table 14 Output Frequency Selection (cont...)

Frequency (MHz, unless stated otherwise)	T0 DPLL Mode	T4 DPLL Mode	T4 APLL Input Mux	Jitter Level (typ)	
				rms (ps)	p-p (ns)
25.92	77.76 MHz digital	-	-	60	0.6
32.768	16E1 mode	-	-	250	1.6
32.768	-	16E1 mode	Select T4 DPLL	400	2.0
32.768	-	-	Select T0 DPLL 16E1	220	1.2
34.368	-	E3 mode	Select T4 DPLL	120	1.0
37.056	24DS1 mode	-	-	110	0.75
37.056	-	24DS1 mode	Select T4 DPLL	110	0.75
37.056	-	-	Select T0 DPLL 24DS1	110	0.75
38.88	77.76 MHz analog	-	-	60	0.6
38.88	77.76 MHz digital	-	-	60	0.6
38.88	-	77.76 MHz mode	Select T4 DPLL	60	0.6
44.736	-	DS3 mode	Select T4 DPLL	110	1.0
49.152 (TO4/TO5 only)	-	12E1 mode	Select T4 DPLL	500	2.3
49.152 (TO4/TO5 only)	-	-	Select T0 DPLL 12E1	250	1.5
49.152 (TO6/TO7 only)	12E1 mode	-	-	900	4.5
49.408 (TO4/TO5 only)	-	16DS1 mode	Select T4 DPLL	200	1.2
49.408 (TO4/TO5 only)	-	-	Select T0 DPLL 16DS1	150	1.0
49.408 (TO6/TO7 only)	16DS1 mode	-	-	760	2.6
51.84	77.76 MHz analog	-	-	60	0.6
51.84	77.76 MHz digital	-	-	60	0.6
65.536 (TO4/TO5 only)	-	16E1 mode	Select T4 DPLL	400	2.0
65.536 (TO4/TO5 only)	-	-	Select T0 DPLL 16E1	220	1.2
65.536 (TO6/TO7 only)	16E1 mode	-	-	250	1.6
68.736	-	E3 mode	Select T4 DPLL	120	1.0
74.112 (TO4/TO5 only)	-	24DS1 mode	Select T4 DPLL	110	0.75
74.112 (TO4/TO5 only)	-	-	Select T0 DPLL 24DS1	110	0.75
74.112 (TO6/TO7 only)	24DS1 mode	-	-	110	0.75
77.76	77.76 MHz analog	-	-	60	0.6
77.76	77.76 MHz digital	-	-	60	0.6
77.76	-	77.76 MHz mode	Select T4 DPLL	60	0.6
89.472 (TO4/TO5 only)	-	DS3 mode	Select T4 DPLL	110	1.0

Table 14 Output Frequency Selection (cont...)

Frequency (MHz, unless stated otherwise)	T0 DPLL Mode	T4 DPLL Mode	T4 APLL Input Mux	Jitter Level (typ)	
				rms (ps)	p-p (ns)
98.304 (TO6 only)	12E1 mode	-	-	900	4.5
98.816 (TO6 only)	16DS1 mode	-	-	760	2.6
131.07 (TO6 only)	16E1 mode	-	-	250	1.6
137.47 (TO4/TO5 only)	-	E3 mode	Select T4 DPLL	120	1.0
148.22 (TO6 only)	24DS1 mode	-	-	110	0.75
155.52 (TO4/TO5 only)	-	77.76 MHz mode	Select T4 DPLL	60	0.6
155.52 (TO6/TO7 only)	77.76 MHz analog	-	-	60	0.6
155.52 (TO6/TO7 only)	77.76 MHz digital	-	-	60	0.6
311.04 (TO6 only)	77.76 MHz analog	-	-	60	0.6
311.04 (TO6 only)	77.76 MHz digital	-	-	60	0.6

Table 15 Frequency Divider Look-up

APLL Frequency	APLL/2	APLL/4	APLL/6	APLL/8	APLL/12	APLL/16	APLL/48	APLL/64
311.04	155.52	77.76	51.84	38.88	25.92	19.44	6.48	4.86
274.944	137.472	68.376	-	34.368	-	17.184	5.728	4.296
178.944	89.472	44.736	-	22.368	-	11.184	3.728	2.796
148.224	74.112	37.056	24,704	18.528	12.352	9.264	3.088	2.316
131.072	65.536	32.768	21.84533	16.384	10.92267	8.192	2.730667	2.048
98.816	49.408	24.704	16.46933	12.352	8.234667	6.176	2.058667	1.544
98.304	49.152	24.576	16.384	12.288	8.192	6.144	2.048	1.536

Note...All frequencies in MHz

Table 16 T0 APLL Frequencies

T0 APLL Frequency	T0 Mode	T0 DPLL Frequency Control Register Bits Reg. 65 Bits[2:0]	Output Jitter Level ns (p-p)
311.04	Normal (digital feedback)	000	<0.5
311.04 MHz	Normal (analog feedback)	001	<0.5
98.304 MHz	12E1 (digital feedback)	010	<2
131.072 MHz	16E1 (digital feedback)	011	<2
148.224 MHz	24DS1 (digital feedback)	100	<2
98.816 MHz	16DS1 (digital feedback)	101	<2
-	Do not use	110	-
-	Do not use	111	-

Table 17 T4 APLL Frequencies

T4 APLL Frequency	T4 Mode	T4 Forward DFS Frequency (MHz)	T4 DPLL Frequency Control Register Bits Reg. 64 Bits [2:0]	T4 APLL for T0 Enable Register Bit Reg. 65 Bit 6	T0 Frequency to T4 APLL Register Bits Reg. 65 Bits [5:4]	Output Jitter Level ns (p-p)
311.04 MHz	Squelched	77.76	000	0	XX	<0.5
311.04 MHz	Normal	77.76	001	0	XX	<0.5
98.304 MHz	12E1	24.576	010	0	XX	<0.5
131.072 MHz	16E1	32.768	011	0	XX	<0.5
148.224 MHz	24DS1	37.056 (2*18.528)	100	0	XX	<0.5
98.816 MHz	16DS1	24.704	101	0	XX	<0.5
274.944 MHz	E3	68.736 (2*34.368)	110	0	XX	<0.5
178.944 MHz	DS3	44.736	111	0	XX	<0.5
98.304 MHz	T0-12E1	-	XXX	1	00	<2
131.072 MHz	T0-16E1	-	XXX	1	01	<2
148.224 MHz	T0-24DS1	-	XXX	1	10	<2
98.816 MHz	T0-16DS1	-	XXX	1	11	<2

Table 18 TO1 - TO7 Output Frequency Selection

Value in Register	Output Frequency for given "Value in Register" for each Output Port's *Cnfg_output_frequency* Register						
	TO1, Reg. 60 Bits [3:0]	TO2, Reg. 60 Bits [7:4]	TO3, Reg. 61 Bits [3:0]	TO4, Reg. 61 Bits [7:4]	TO5, Reg. 62 Bits [3:0]	TO6, Reg. 62 Bits [7:4]	TO7, Reg. 63 Bits [3:0]
0000	Off	Off	Off	Off	Off	Off	Off
0001	2 kHz	2 kHz	2 kHz	2 kHz	2 kHz	2 kHz	2 kHz
0010	8 kHz	8 kHz	8 kHz	8 kHz	8 kHz	8 kHz	8 kHz
0011	Digital2	Digital2	Digital2	Digital2	Digital2	T0 APLL/2	Digital2
0100	Digital1	Digital1	Digital1	Digital1	Digital1	Digital1	T0 APLL/2
0101	T0 APLL/48	T0 APLL/48	T0 APLL/48	T0 APLL/48	T0 APLL/48	T0 APLL/1	T0 APLL/48
0110	T0 APLL/16	T0 APLL/16	T0 APLL/16	T0 APLL/16	T0 APLL/16	T0 APLL/16	T0 APLL/16
0111	T0 APLL/12	T0 APLL/12	T0 APLL/12	T0 APLL/12	T0 APLL/12	T0 APLL/12	T0 APLL/12
1000	T0 APLL/8	T0 APLL/8	T0 APLL/8	T0 APLL/8	T0 APLL/8	T0 APLL/8	T0 APLL/8
1001	T0 APLL/6	T0 APLL/6	T0 APLL/6	T0 APLL/6	T0 APLL/6	T0 APLL/6	T0 APLL/6
1010	T0 APLL/4	T0 APLL/4	T0 APLL/4	T0 APLL/4	T0 APLL/4	T0 APLL/4	T0 APLL/4
1011	T4 APLL/64	T4 APLL/64	T4 APLL/64	T4 APLL/2	T4 APLL/2	T4 APLL/64	T4 APLL/64
1100	T4 APLL/48	T4 APLL/48	T4 APLL/48	T4 APLL/48	T4 APLL/48	T4 APLL/48	T4 APLL/48
1101	T4 APLL/16	T4 APLL/16	T4 APLL/16	T4 APLL/16	T4 APLL/16	T4 APLL/16	T4 APLL/16
1110	T4 APLL/8	T4 APLL/8	T4 APLL/8	T4 APLL/8	T4 APLL/8	T4 APLL/8	T4 APLL/8
1111	T4 APLL/4	T4 APLL/4	T4 APLL/4	T4 APLL/4	T4 APLL/4	T4 APLL/4	T4 APLL/4

T4 Low Frequency Outputs

TO8 is an AMI composite clock output. If enabled, this always produces a 64 kHz/8 kHz composite clock. If enabled, TO9 always produces an E1 or DS1 frequency output. Both TO8 and TO9 are generated by DFS within either the T0 or T4 path, as controlled by Reg. 35 Bit 4. The frequencies generated from TO8 and TO9 are independent of the Mode (frequency) of either the T4 or the T0 paths. The amount of jitter generated on the TO8 and TO9 outputs will be related to the clock period of the source DFS block added to any jitter present on that clock. This is detailed in the following text.

As can be seen in the block diagram, the DFS blocks used to generate these outputs are the T4 feedback DFS block in the case of the T4 path and the T0 LF output DFS block for the T0 path. The T4 feedback DFS block is clocked by the T4 forward DFS, or its APLL. The frequency of the T4 forward DFS block can be determined by referring to Table 17 (T4 APLL frequencies). This is in the region of 65 MHz to89 MHz and can be approximated to have a period of between 11 ns and 15 ns. The output of the T4 forward DFS block will have an inherent p-p jitter of approximately 4.9 ns. The clock to the T4 feedback DFS block will have <1 ns of jitter when the T4 path is in analog feedback mode (Reg. 35 Bit 6 = 0). However, it will have 4.9 ns when in digital feedback mode.

The TO8 output, being 64 kHz/8 kHz, can be directly divided from the clock to the T4 feedback DFS block; therefore, it will have a similar amount of jitter on it, i.e. <1 ns when using analog feedback, and 4.9 ns when using digital feedback.

The TO9 output will have more jitter because it is synthesized from the clock to the T4 feedback DFS block. The jitter, in addition to that present on the clock to the T4 feedback DFS block, will be equivalent to a period of that clock, i.e. between 11 ns and 15 ns. The jitter present on the TO9 output will range from 11 ns (when the T4 path is in DS3 mode - 89 MHz combined with analog feedback) to 20 ns (when in 16E1 mode - 65 MHz combined with digital feedback).

The T4 outputs TO8 and TO9 can be enabled/disabled via Reg. 63 Bits [5:4].

"Digital" Frequencies

It can be seen from Table 18 (TO1-TO7 output frequency selection) that frequencies listed as Digital1 and Digital2 can be selected. Digital1 is a single frequency selected from the range shown in Table 19. Digital2 is another single frequency selected from the same range. The T0 LF output DFS block shown in the diagram and clocked either by the T0 77M output DFS block or via the T0 output APLL, generates these two frequencies. The input clock frequency of the DFS is always 77.76 MHz and as such has a period of approximately 12 ns. The jitter generated on the Digital outputs is relatively high, due to the fact that they do not pass through an APLL for jitter filtering. The minimum level of jitter is when the T0 path is in analog feedback mode, when the p-p jitter will be approximately 12 ns (equivalent to a period of the DFS clock). The maximum jitter is generated when in digital feedback mode, when the total is approximately 17 ns.

TO10, TO11, 2 kHz and 8 kHz Clock Outputs

It can be seen from Table 18 (TO1 - TO7 Output Frequency Selection) that frequencies listed as 2 kHz and 8 kHz can be selected. Whilst the TO10 and TO11 outputs are always supplied from the T0 path, the 2 kHz and 8 kHz options available from the TO1 - TO7 outputs are all supplied from either the T0 or T4 path (Reg. 7A Bit 7).

The outputs can be either clocks (50:50 mark-space) or pulses and can be inverted. When pulses are configured on the output, the pulse width will be one cycle of the output of TO3 (TO3 must be configured to generate at least 1544 kHz to ensure that pulses are generated correctly). Figure 12 shows the various options with the 8 kHz controls in Reg. 7A. There is an identical arrangement with Reg. 7A Bits [1:0] and the 2 kHz/TO11 outputs. Outputs TO10 and TO11 can be disabled via Reg. 63 Bits [7:6].

Figure 12 Control of 8k Options.

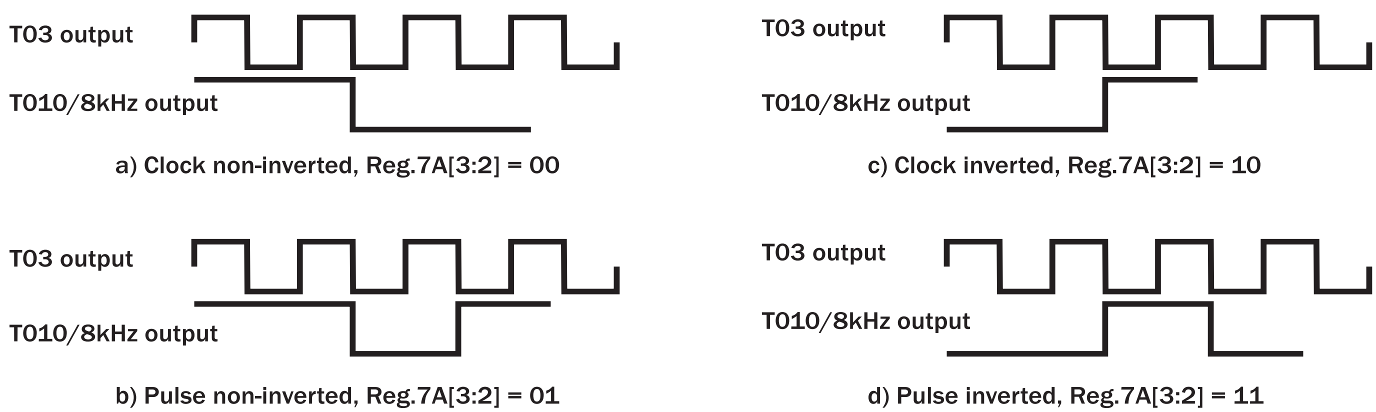


Table 19 Digital Frequency Selections

Digital1 Control Reg.39 Bits [5:4]	Digital1 SONET/ SDH Reg. 38 Bit5	Digital1 Frequency (MHz)
00	0	2.048
01	0	4.096
10	0	8.192
11	0	16.384
00	1	1.544
01	1	3.088
10	1	6.176
11	1	12.352

Digital2 Control Reg. 39 Bits[7:6]	Digital2 SONET/SDH Reg.38 Bit6	Digital2 Frequency (MHz)
00	0	2.048
01	0	4.096
10	0	8.192
11	0	16.384
00	1	1.544
01	1	3.088
10	1	6.176
11	1	12.352

Microprocessor Interface

Introduction to Microprocessor Modes

The ACS8520 incorporates a microprocessor interface, which can be configured for all common microprocessor interface types, via the bus interface mode control pins UPSEL(2:0) as defined in Table 20.

These pins are read at power up and set the interface mode.

The optional EPROM mode allows the internal registers to be loaded from the EPROM when the device comes out of "Power-On Reset" mode. The microprocessor interface type can be altered after power up by Reg. 7F, such that for instance the device could boot up in EPROM mode and then switch to Motorola mode, for example, after the EPROM data has preconditioned the device. Reading of Data from the EPROM at boot up time is handled automatically by the ACS8520. The chip select of the EPROM should be driven from the micro in the case of mixed EPROM and micro communication, in order to avoid conflict between EPROM and ACS8520 access from the microprocessor.

The following sections show the interface timings for each interface type.

Table 20 Microprocessor Interface Mode Selection

UPSEL(2:0)	Mode	Description
111 (7)	OFF	Interface disabled
110 (6)	OFF	Interface disabled
101 (5)	SERIAL	Serial uP bus interface
100 (4)	MOTOROLA	Motorola interface
011 (3)	INTEL	Intel compatible bus interface
010 (2)	MULTIPLEXED	Multiplexed bus interface
001 (1)	EPROM	EPROM read mode
000 (0)	OFF	Interface disabled

Timing diagrams for the different microprocessor modes are presented on pages 44 to 52.

Motorola Mode

In MOTOROLA mode, the device is configured to interface with a microprocessor using a 680x0 type bus as parallel data + address. Figure 13 and Figure 14 show the timing diagrams of read and write accesses for this mode.

Figure 13 Read Access Timing in MOTOROLA Mode

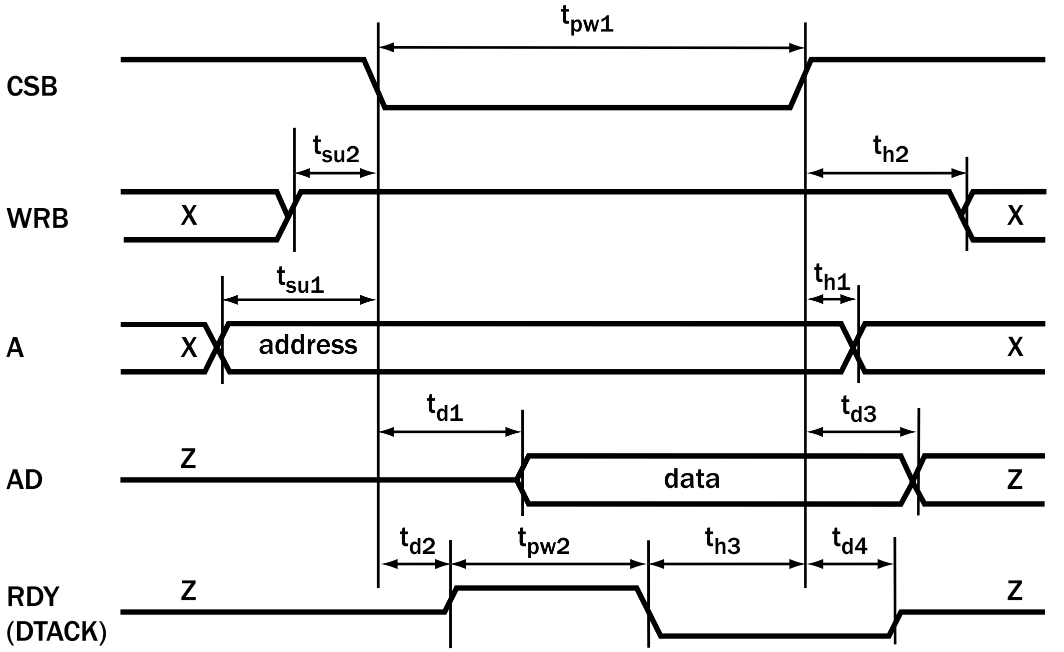


Table 21 Read Access Timing in MOTOROLA Mode (for use with Figure 13)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup A valid to $CSB_{falling\ edge}$	4 ns	-	-
t_{su2}	Setup WRB valid to $CSB_{falling\ edge}$	0 ns	-	-
t_{d1}	Delay $CSB_{falling\ edge}$ to AD valid (consecutive Read - Read)	12 ns	-	40 ns
	Delay $CSB_{falling\ edge}$ to AD valid (consecutive Write - Read)	16 ns	-	192 ns
t_{d2}	Delay $CSB_{falling\ edge}$ to $DTACK_{rising\ edge}$	-	-	13 ns
t_{d3}	Delay $CSB_{rising\ edge}$ to AD high-Z	-	-	10 ns
t_{d4}	Delay $CSB_{rising\ edge}$ to RDY high-Z	-	-	9 ns
t_{pw1}	CSB *Low* time (consecutive Read - Read)	25 ns	62 ns	-
	CSB *Low* time (consecutive Write - Read)	25 ns	193 ns	-
t_{pw2}	RDY *High* time (consecutive Read - Read)	12 ns	-	49 ns
	RDY *High* time (consecutive Write - Read)	12 ns	-	182 ns
t_{h1}	Hold A valid after $CSB_{rising\ edge}$	0 ns	-	-
t_{h2}	Hold WRB valid after $CSB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold CSB *Low* after $RDY_{falling\ edge}$	0 ns	-	-
t_p	Time between (consecutive Read - Read) accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	15 ns	-	-
t_p	Time between (consecutive Write - Read) accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	160 ns	-	-

Figure 14 Write Access Timing in MOTOROLA Mode

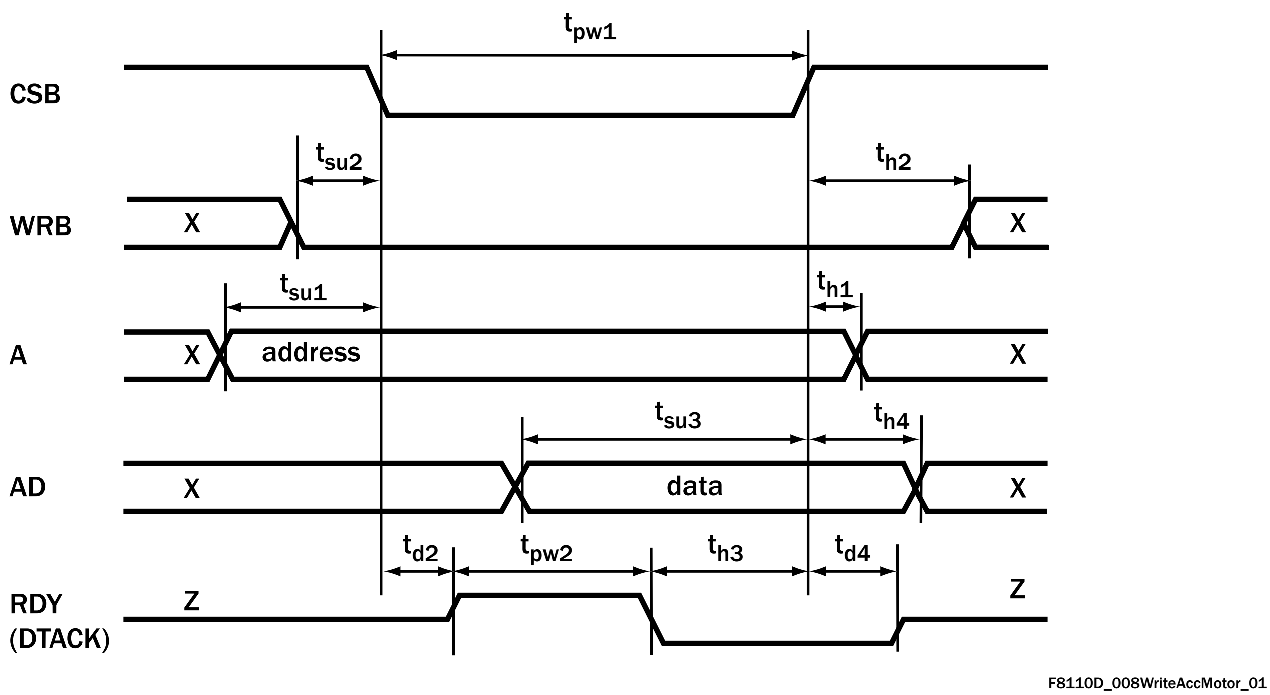


Table 22 Write Access Timing in MOTOROLA Mode (for use with Figure 14)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup A valid to $CSB_{falling\ edge}$	4 ns	-	-
t_{su2}	Setup WRB valid to $CSB_{falling\ edge}$	0 ns	-	-
t_{su3}	Setup AD valid before $CSB_{rising\ edge}$	8 ns	-	-
t_{d2}	Delay $CSB_{falling\ edge}$ to $RDY_{rising\ edge}$	-	-	13 ns
t_{d4}	Delay $CSB_{rising\ edge}$ to RDY *High-Z*	-	-	7 ns
t_{pw1}	CSB *Low* time	25 ns	-	180 ns
t_{pw2}	RDY *High* time	12 ns	-	166 ns
t_{h1}	Hold A valid after $CSB_{rising\ edge}$	8 ns	-	-
t_{h2}	Hold WRB *Low* after $CSB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold CSB *Low* after $RDY_{falling\ edge}$	0 ns	-	-
t_{h4}	Hold AD valid after $CSB_{rising\ edge}$	9 ns	-	-
t_p	Time between consecutive accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	160 ns	-	-

Intel Mode

In Intel mode, the device is configured to interface with a microprocessor using a 80x86 type bus as parallel data + address. Figure 15 and Figure 16 show the timing diagrams of read and write accesses for this mode.

Figure 15 Read Access Timing in INTEL Mode

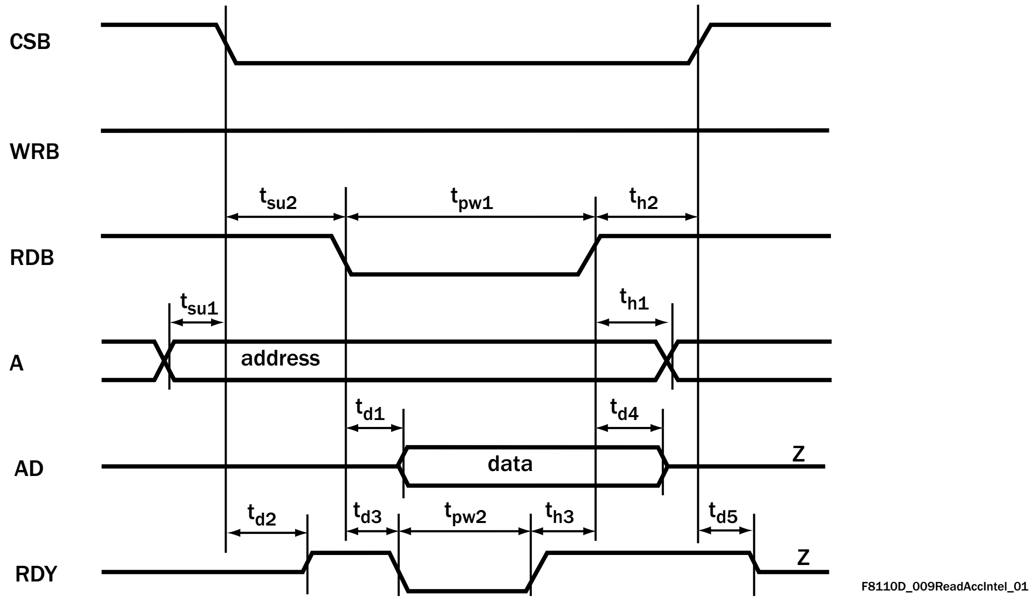


Table 23 Read Access Timing in INTEL Mode (for use with Figure 15)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup A valid to $CSB_{falling\ edge}$	4 ns	-	-
t_{su2}	Setup $CSB_{falling\ edge}$ to $RDB_{falling\ edge}$	0 ns	-	-
t_{d1}	Delay $RDB_{falling\ edge}$ to AD valid (consecutive Read - Read)	12 ns	-	40 ns
	Delay $RDB_{falling\ edge}$ to AD valid (consecutive Write - Read)	12 ns	-	193 ns
t_{d2}	Delay $CSB_{falling\ edge}$ to RDY active	-	-	13 ns
t_{d3}	Delay $RDB_{falling\ edge}$ to $RDY_{falling\ edge}$	-	-	14 ns
t_{d4}	Delay $RDB_{rising\ edge}$ to AD high-Z	-	-	10 ns
t_{d5}	Delay $CSB_{rising\ edge}$ to RDY high-Z	-	-	11 ns
t_{pw1}	RDB *Low* time (consecutive Read - Read)	35 ns	60 ns	-
	RDB *Low* time (consecutive Write - Read)	35 ns	195 ns	-
t_{pw2}	RDY *Low* time (consecutive Read - Read)	20 ns	-	45 ns
	RDY *Low* time (consecutive Write - Read)	20 ns	-	182 ns
t_{h1}	Hold A valid after $RDB_{rising\ edge}$	0 ns	-	-
t_{h2}	Hold CSB *Low* after $RDB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold RDB *Low* after $RDY_{rising\ edge}$	0 ns	-	-
t_p	Time between (consecutive Read - Read) accesses ($RDB_{rising\ edge}$ to $RDB_{falling\ edge}$, or $RDB_{rising\ edge}$ to $WRB_{falling\ edge}$)	15 ns	-	-
t_p	Time between (consecutive Write - Read) accesses ($RDB_{rising\ edge}$ to $RDB_{falling\ edge}$, or $RDB_{rising\ edge}$ to $WRB_{falling\ edge}$)	160 ns	-	-

Figure 16 Write Access Timing in INTEL Mode

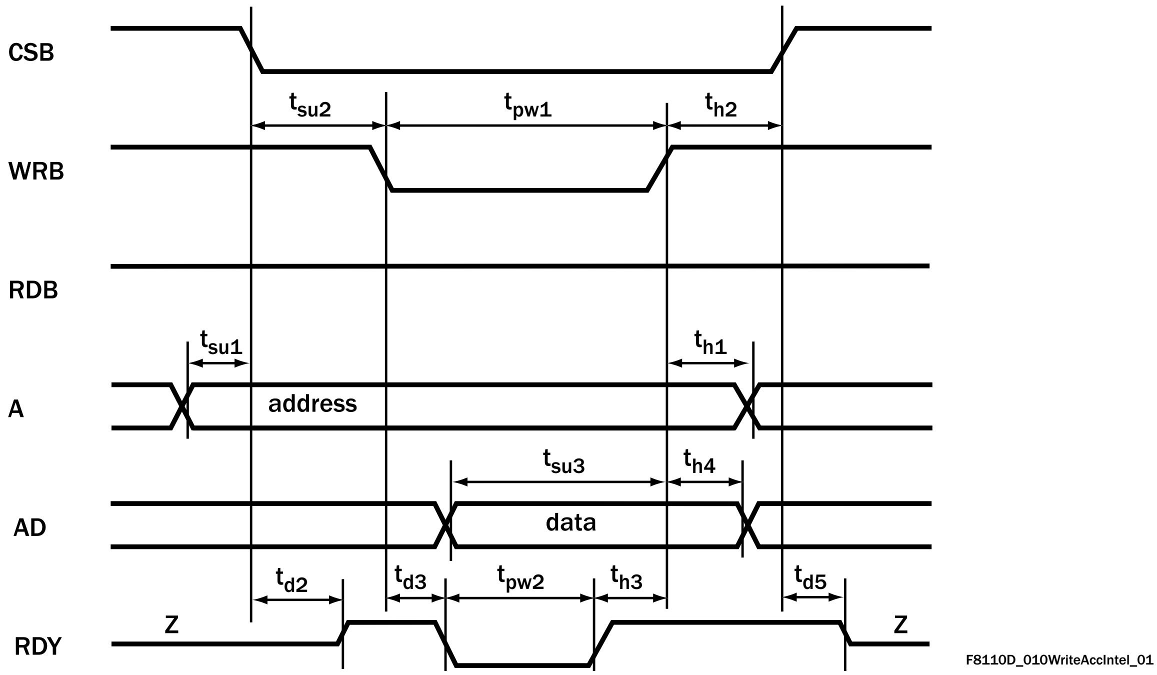


Table 24 Write Access Timing in INTEL Mode (for use with Figure 16)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup A valid to $CSB_{falling\ edge}$	4 ns	-	-
t_{su2}	Setup $CSB_{falling\ edge}$ to $WRB_{falling\ edge}$	0 ns	-	-
t_{su3}	Setup AD valid before $WRB_{rising\ edge}$	6 ns	-	-
t_{d2}	Delay $CSB_{falling\ edge}$ to RDY active	-	-	13 ns
t_{d3}	Delay $WRB_{falling\ edge}$ to $RDY_{falling\ edge}$	-	-	14 ns
t_{d5}	Delay $CSB_{rising\ edge}$ to RDY high-Z	-	-	10 ns
t_{pw1}	WRB *Low* time	25 ns	185 ns	-
t_{pw2}	RDY *Low* time	10 ns	-	173 ns
t_{h1}	Hold A valid after $WRB_{rising\ edge}$	12 ns	-	-
t_{h2}	Hold CSB *Low* after $WRB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold WRB *Low* after $RDY_{rising\ edge}$	0 ns	-	-
t_{h4}	Hold AD valid after $WRB_{rising\ edge}$	4 ns	-	-
t_p	Time between consecutive accesses ($WRB_{rising\ edge}$ to $WRB_{falling\ edge}$, or $WRB_{rising\ edge}$ to $RDB_{falling\ edge}$)	160 ns	-	-

Multiplexed Mode

In Multiplexed Mode, the device is configured to interface with microprocessors (e.g., Intel's 80x86 family) which share bus signals between address and data. Figures 17 and 18 show the timing diagrams of read and write accesses.

Figure 17 Read Access Timing in MULTIPLEXED Mode

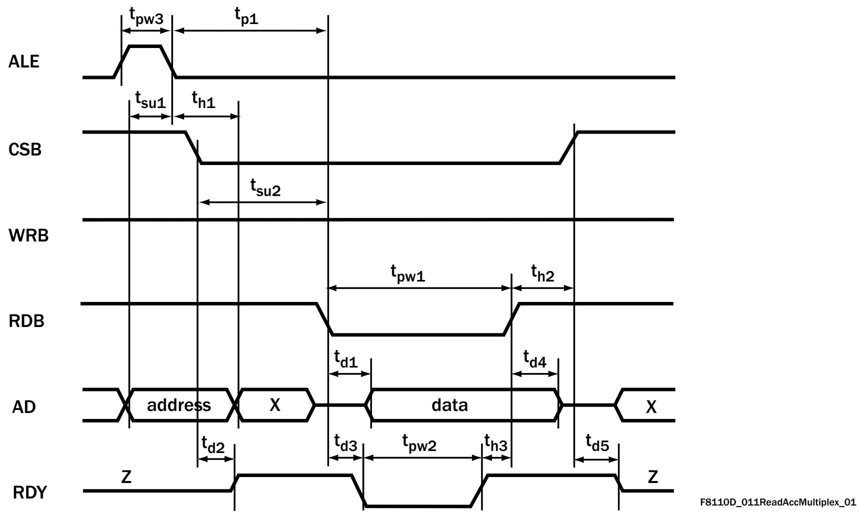


Table 25 Read Access Timing in MULTIPLEXED Mode (for use with Figure 17)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup AD address valid to $ALE_{falling\ edge}$	5 ns	-	-
t_{su2}	Setup $CSB_{falling\ edge}$ to $RDB_{falling\ edge}$	0 ns	-	-
t_{d1}	Delay $RDB_{falling\ edge}$ to AD data valid (consecutive Read - Read)	12 ns	-	40 ns
	Delay $RDB_{falling\ edge}$ to AD data valid (consecutive Write - Read)	17 ns	-	193 ns
t_{d2}	Delay $CSB_{falling\ edge}$ to RDY active	-	-	13 ns
t_{d3}	Delay $RDB_{falling\ edge}$ to $RDY_{falling\ edge}$	-	-	15 ns
t_{d4}	Delay $RDB_{rising\ edge}$ to AD data high-Z	-	-	10 ns
t_{d5}	Delay $CSB_{rising\ edge}$ to RDY high-Z	-	-	10 ns
t_{pw1}	RDB *Low* time (consecutive Read - Read)	35 ns	60 ns	-
	RDB *Low* time (consecutive Write - Read)	35 ns	200 ns	-
t_{pw2}	RDY *Low* time (consecutive Read - Read)	20 ns	-	40 ns
	RDY *Low* time (consecutive Write - Read)	20 ns	-	185 ns
t_{pw3}	ALE *High* time	5 ns	-	-
t_{h1}	Hold AD address valid after $ALE_{falling\ edge}$	9 ns	-	-
t_{h2}	Hold CSB *Low* after $RDB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold RDB *Low* after $RDY_{rising\ edge}$	0 ns	-	-
t_{p1}	Time between $ALE_{falling\ edge}$ and $RDB_{falling\ edge}$	0 ns	-	-
t_{p2}	Time between (consecutive Read - Read) accesses ($RDB_{rising\ edge}$ to $ALE_{rising\ edge}$)	20 ns	-	-
t_{p2}	Time between (consecutive Write - Read) accesses ($RDB_{rising\ edge}$ to $ALE_{rising\ edge}$)	160 ns	-	-

Figure 18 Write Access Timing in MULTIPLEXED Mode

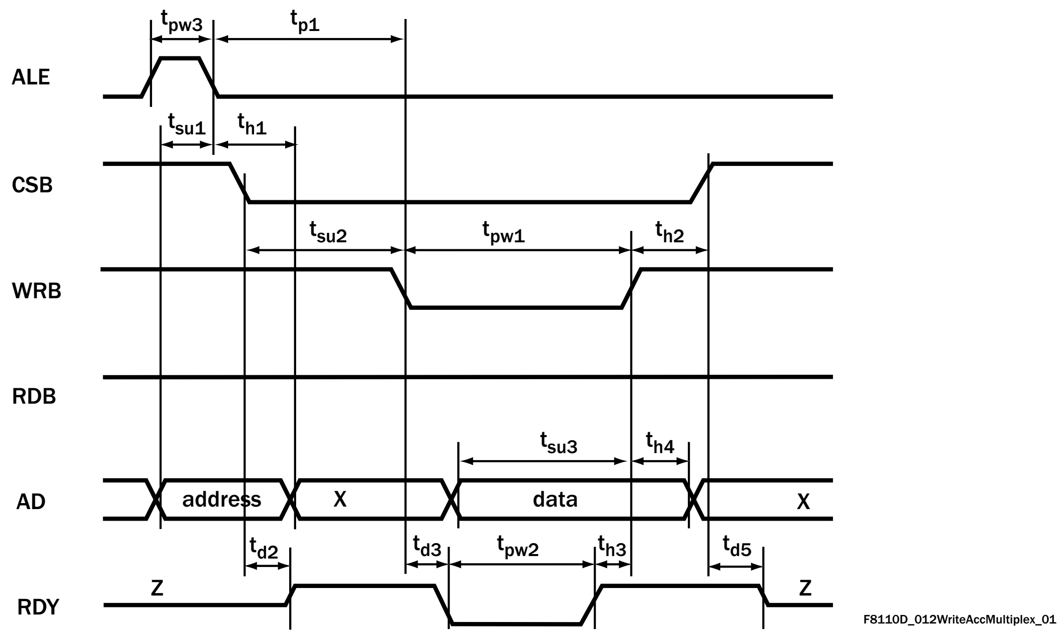


Table 26 Write Access Timing in MULTIPLEXED Mode (For use with Figure 18)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Set up AD address valid to $ALE_{falling\ edge}$	5 ns	-	-
t_{su2}	Set up $CSB_{falling\ edge}$ to $WRB_{falling\ edge}$	0 ns	-	-
t_{su3}	Set up AD data valid to $WRB_{rising\ edge}$	5 ns	-	-
t_{d2}	Delay $CSB_{falling\ edge}$ to RDY active	-	-	13 ns
t_{d3}	Delay $WRB_{falling\ edge}$ to $RDY_{falling\ edge}$	-	-	15 ns
t_{d5}	Delay $CSB_{rising\ edge}$ to RDY high-Z	-	-	9 ns
t_{pw1}	WRB *Low* time	30 ns	188 ns	-
t_{pw2}	RDY *Low* time	15 ns	-	173 ns
t_{pw3}	ALE *High* time	5 ns	-	-
t_{h1}	Hold AD address valid after $ALE_{falling\ edge}$	9 ns	-	-
t_{h2}	Hold CSB *Low* after $WRB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold WRB *Low* after $RDY_{rising\ edge}$	0 ns	-	-
t_{h4}	AD data hold valid after $WRB_{rising\ edge}$	7 ns	-	-
t_{p1}	Time between $ALE_{falling\ edge}$ and $WRB_{falling\ edge}$	0 ns	-	-
t_{p2}	Time between consecutive accesses ($WRB_{rising\ edge}$ to $ALE_{rising\ edge}$)	1600 ns	-	-

Serial Mode

In SERIAL Mode, the device is configured to interface with a serial microprocessor bus. Figure 19 and Figure 20 show the timing diagrams of read and write accesses for this mode. The serial interface can be SPI compatible.

The Motorola SPI convention is such that address and data is transmitted and received MSB first. On the ACS8520, device address and data are transmitted and received LSB first. Address, read/write control and data on the SDI pin is latched into the device on the rising edge of the SCLK. During a read operation, serial data output on the SDO pin can be read out of the device on either the rising or falling edge of the SCLK depending on the logic level of CLKE (note CLKE=A(1)). For standard Motorola SPI compliance, data should be clocked out of the SDO pin on the rising edge of the SCLK so that it may be latched into the microprocessor on the falling edge of the SCLK.

The serial interface clock (SCLK) is not required to run between accesses (i.e., when CSB = 1).

Figure 19 Read Access Timing in SERIAL Mode

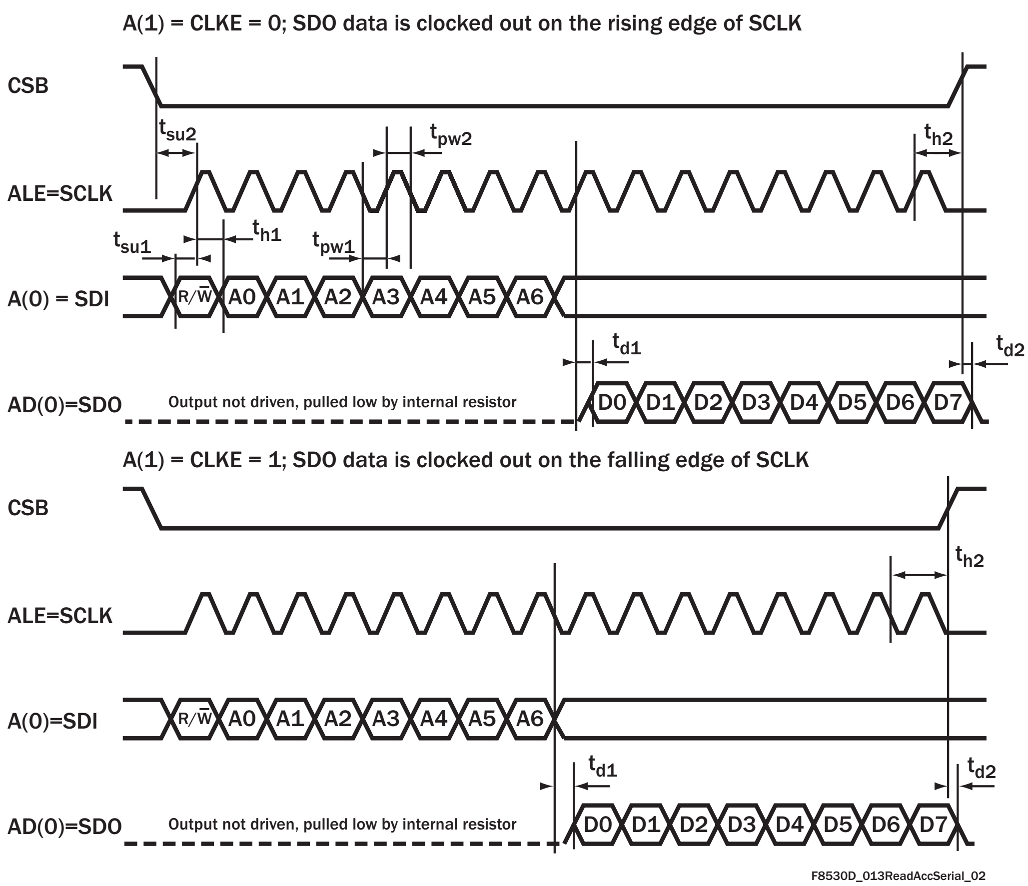


Table 27 Read Access Timing in SERIAL Mode (For use with Figure 19)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup SDI valid to SCLK$_{\text{rising edge}}$	4 ns	-	-
t_{su2}	Setup CSB$_{\text{falling edge}}$ to SCLK$_{\text{rising edge}}$	14 ns	-	-
t_{d1}	Delay SCLK$_{\text{rising edge}}$ (SCLK$_{\text{falling edge}}$ for CLKE = 1) to SDO valid	-	-	18 ns
t_{d2}	Delay CSB$_{\text{rising edge}}$ to SDO high-Z	-	-	16 ns

Table 27 Read Access Timing in SERIAL Mode (For use with Figure 19) (cont...)

Symbol	Parameter	MIN	TYP	MAX
t_{pw1}	SCLK *Low* time	22 ns	-	-
t_{pw2}	SCLK *High* time	22 ns	-	-
t_{h1}	Hold SDI valid after $SCLK_{rising\ edge}$	6 ns	-	-
t_{h2}	Hold CSB *Low* after $SCLK_{rising\ edge}$, for CLKE = 0 Hold CSB *Low* after $SCLK_{falling\ edge}$, for CLKE = 1	5 ns	-	-
t_p	Time between consecutive accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	10 ns	-	-

Figure 20 Write Access Timing in SERIAL Mode

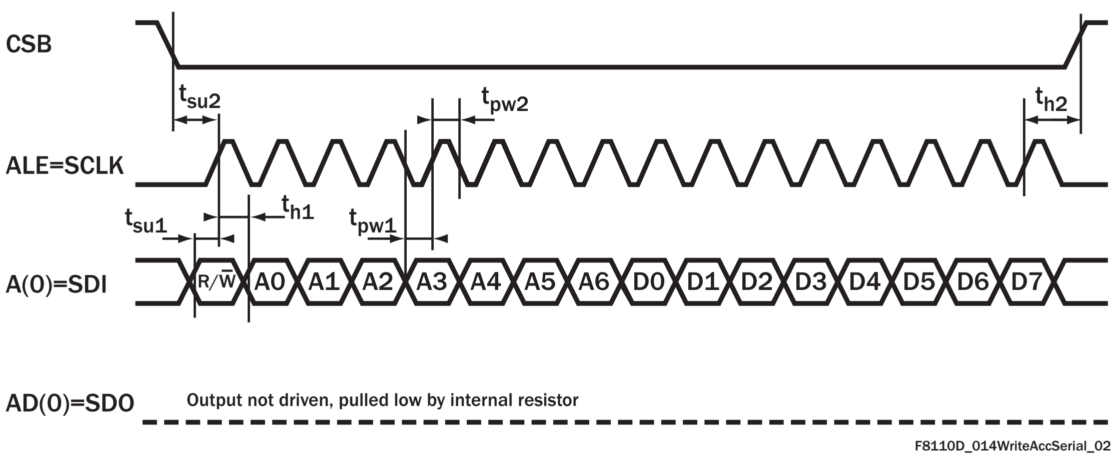


Table 28 Write Access Timing in SERIAL Mode (For use with Figure 20)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup SDI valid to $SCLK_{rising\ edge}$	4 ns	-	-
t_{su2}	Setup $CSB_{falling\ edge}$ to $SCLK_{rising\ edge}$	14 ns	-	-
t_{pw1}	SCLK *Low* time	22 ns	-	-
t_{pw2}	SCLK *High* time	22 ns	-	-
t_{h1}	Hold SDI valid after $SCLK_{rising\ edge}$	6 ns	-	-
t_{h2}	Hold CSB *Low* after $SCLK_{rising\ edge}$	5 ns	-	-
t_p	Time between consecutive accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	10 ns	-	-

EPROM Mode

This mode is suitable for use with an EPROM, in which configuration data is stored (one-way communication - status information will not be accessible). A state machine internal to the ACS8520 device will perform numerous EPROM read operations to read the data out of the EPROM. In EPROM Mode, the ACS8520 takes control of the bus as Master and reads the device set-up from an AMD AM27C64 type EPROM at lowest speed (250ns) after device set-up (system reset). The EPROM access state machine in the up interface sequences the accesses. Figure 21 shows the access timing of the device in EPROM mode.

Further information can be found in the AMD AM27C64 datasheet.

Figure 21 Access Timing in EPROM mode

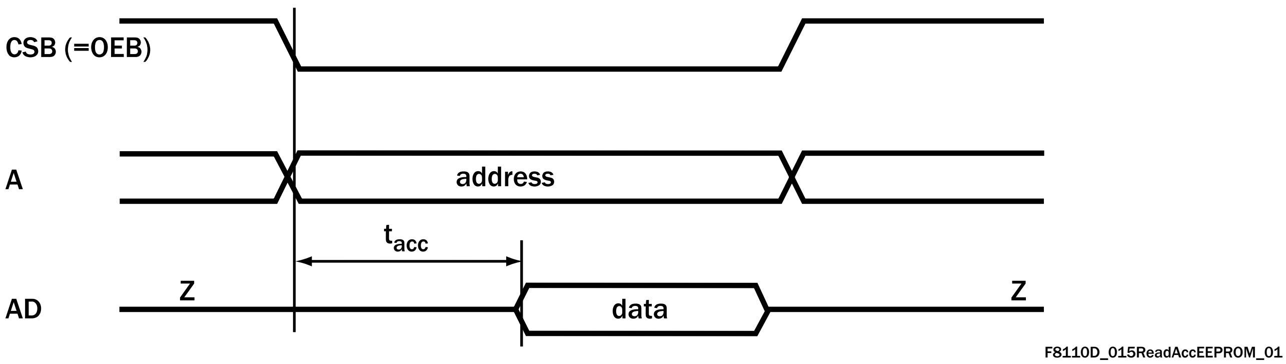


Table 29 Access Timing in EPROM mode (For use with Figure 21)

Symbol	Parameter	MIN	TYP	MAX
t_{acc}	Delay $CSB_{falling\ edge}$ or A change to AD valid	-	-	920 ns

Power-On Reset

The Power-On Reset (PORB) pin resets the device if forced *Low*. The reset is asynchronous, the minimum *Low* pulse width is 5 ns. Reset is needed to initialize all of the register values to their defaults. Reset must be asserted at power on, and may be re-asserted at any time to restore defaults. This is implemented simply using an external capacitor to GND along with the internal pull-up resistor. The ACS8520 is held in a reset state for 250 ms after the PORB pin has been pulled *High*. In normal operation PORB should be held *High*.

Register Map

Each Register, or register group, is described in the following Register Map (Table 30) and subsequent Register Description Tables.

Register Organization

The ACS8520 SETS uses a total of 118 8-bit register locations, identified by a Register Name and corresponding hexadecimal Register Address. They are presented here in ascending order of Reg. address. and each Register is organized with the most-significant bit positioned in the left-most bit, and bit significance decreasing towards the right-most bit. Some registers carry several individual data fields of various sizes, from single-bit values (e.g. flags) upwards. Several data fields are spread across multiple registers, as shown in the Register Map, Table 30. Shaded areas in the map are “don’t care” and writing either 0 or 1 will not affect any function of the device. Bits labelled “Set to zero” or “Set to one” must be set as stated during initialization of the device, either following power- up, or after a Power-On Reset (POR). Failure to correctly set these bits may result in the device operating in an unexpected way.

CAUTION! Do not write to any undefined register addresses as this may cause the device to operate in a test mode. If an undefined register has been inadvertently addressed, the device should be reset to ensure the undefined registers are at default values.

Multi-word Registers

For Multi-word Registers (e.g. Reg. 0C and 0D), all the words have to be written to their separate addresses, and without any other access taking place, before their combined value can take effect. If the sequence is interrupted, the sequence of writes will be ignored. Reading a multi-word address freezes the other address words of a multi-word address so that the bytes all correspond to the same complete word.

Register Access

Most registers are of one of two types, configuration registers or status registers, the exceptions being the *chip_id* and *chip_revision* registers. Configuration registers may be written to or read from at any time (the complete 8-bit register must be written, even if only one bit is being modified). All status registers may be read at any time and, in some status registers (such as the *sts_interrupts* register), any individual data field may be cleared by writing a 1 into each bit of the field (writing a 0 value into a bit will not affect the value of the bit).

Configuration Registers

Each configuration register reverts to a default value on power-up or following a reset. Most default values are fixed, but some will be pin-settable. All configuration registers can be read out over the microprocessor port.

Status Registers

The Status Registers contain readable registers. They may all be read from outside the chip but are not writeable from outside the chip (except for a clearing operation). All status registers are read via shadow registers to avoid data hits due to dynamic operation. Each individual status register has a unique location.

Interrupt Enable and Clear

Interrupt requests are flagged on pin INTREQ; the active state (*High* or *Low*) is programmable and the pin can either be driven, or set to high impedance when non-active (Reg 7D refers).

Bits in the interrupt status register are set (*High*) by:

1. Any reference source becoming valid or going invalid.
2. Change in the operating state (e.g. Locked, Holdover)
3. A brief loss of the currently selected reference source.
4. An AMI input error.

All interrupt sources, see Reg. 05, Reg. 06 and Reg. 08, are maskable via the mask register, each one being enabled by writing a 1 to the appropriate bit. Any unmasked bit set in the interrupt status register will cause the interrupt request pin to be asserted. All interrupts are cleared by writing a 1 to the bit(s) to be cleared in the status register. When all pending unmasked interrupts are cleared the interrupt pin will go inactive.

Defaults

Each Register is given a defined default value at reset and these are listed in the Map and Description Tables. However, some read-only status registers may not necessarily show the same default values after reset as those given in the tables. This is because they reflect the status of the device which may have changed in the time it takes to carry out the read, or through reasons of configuration. In the same way, the default values given for shaded areas could also take different values to those stated.

Table 30 Register Map

Register Name RO = Read Only R/W = Read/Write	Address (hex)	Default (hex)	Data Bit 7 (MSB)	6	5	4	3	2	1	0 (LSB)
chip_id (RO)	00	48	Device part number [7:0] 8 least significant bits of the chip ID							
	01	21	Device part number [15:8] 8 most significant bits of the chip ID							
chip_revision (RO)	02	00	Chip revision number [7:0]							
test_register1 (R/W)	03	14	phase_alarm	disable_180		resync_ analog	Set to 0	8K edge polarity	Set to zero	Set to zero
sts_interrupts (R/W)	05	FF	I8 valid change	I7 valid change	I6 valid change	I5 valid change	I4 valid change	I3 valid change	I2 valid change	I1 valid change
	06	3F	operating_ mode	main_ref_ failed	I14 valid change	I13 valid change	I12 valid change	I11 valid change	I10 valid change	I9 valid change
sts_current_DPLL_frequency, see OC/OD	07	00						Bits [18:16] of current DPLL frequency		
sts_interrupts (R/W)	08	50	Sync_ip_alarm	T4_status		T4_inputs_ failed	AMI2_Viol	AMI2_LOS	AMI1_Viol	AMI1_LOS
sts_operating (RO)	09	41	SYNC2K_ alarm	T4_DPLL_lock	T0_DPLL_freq _soft_alarm	T4_DPLL_freq _soft_alarm		T0_DPLL_operating_mode		
sts_priority_table (RO)	0A	00	Highest priority validated source				Currently selected source			
	0B	00	3rd highest priority validated source				2nd highest priority validated source			
sts_current_DPLL_frequency[7:0]	0C	00	Bits [7:0] of current DPLL frequency							
(RO) [15:8]	0D	00	Bits [15:8] of current DPLL frequency							
[18:16]	07	00						Bits [18:16] of current DPLL frequency		
sts_sources_valid (RO)	0E	00	I8	I7	I6	I5	I4	I3	I2	I1
	0F	00			I14	I13	I12	I11	I10	I9
sts_reference_sources (RO) Status of inputs:			Out-of-band alarm (soft)	Out-of-band alarm (hard)	No activity alarm	Phase lock alarm	Out-of-band alarm (soft)	Out-of band alarm (hard)	No activity alarm	Phase lock alarm
Input pairs (1 & 2)	10	66	Status of I2 Input				Status of I1 Input			
(3 & 4)	11	66	Status of I4 Input				Status of I3 Input			
(5 & 6)	12	66	Status of I6 Input				Status of I5 Input			
(7 & 8)	13	66	Status of I8 Input				Status of I7 Input			
(9 & 10)	14	66	Status of I10 Input				Status of I9 Input			
(11 & 12)	15	66	Status of I12 Input				Status of I11 Input			
(13 & 14)	16	66	Status of I14 Input				Status of I13 Input			
cnfg_ref_selection_priority (1 & 2)	18	32	programmed_priority I2				programmed_priority I1			
(R/W) (3 & 4)	19	54	programmed_priority I4				programmed_priority I3			
(5 & 6)	1A	76	programmed_priority I6				programmed_priority I5			
(7 & 8)	1B	98	programmed_priority I8				programmed_priority I7			
(9 & 10)	1C	BA	programmed_priority I10				programmed_priority I9			
(11 & 12)	1D	DC	programmed_priority I12				programmed_priority I11			
(13 & 14)	1E	FE	programmed_priority I14				programmed_priority I13			
cnfg_ref_source_frequency_ _1	20	00	Set to zero		bucket_id_1		Set to zero			
(R/W) _2	21	00	Set to zero		bucket_id_2		Set to zero			
3	22	00	divn_3	lock8k_3	bucket_id_3		reference_source_frequency_3			
4	23	00	divn_4	lock8k_4	bucket_id_4		reference_source_frequency_4			
5	24	03	divn_5	lock8k_5	bucket_id_5		reference_source_frequency_5			
6	25	03	divn_6	lock8k_6	bucket_id_6		reference_source_frequency_6			
7	26	03	divn_7	lock8k_7	bucket_id_7		reference_source_frequency_7			
8	27	03	divn_8	lock8k_8	bucket_id_8		reference_source_frequency_8			
9	28	03	divn_9	lock8k_9	bucket_id_9		reference_source_frequency_9			
10	29	03	divn_10	lock8k_10	bucket_id_10		reference_source_frequency_10			
11	2A	03	divn_11	lock8k_11	bucket_id_11		reference_source_frequency_11			
12	2B	01	divn_12	lock8k_12	bucket_id_12		reference_source_frequency_12			
13	2C	01	divn_13	lock8k_13	bucket_id_13		reference_source_frequency_13			
14	2D	01	divn_14	lock8k_14	bucket_id_14		reference_source_frequency_14			
cnfg_sts_remote_sources_valid (R/W)	30	FF	Remote status, channels <8:1>							
	31	3F			Remote status, channels <14:9>					
cnfg_operating_mode (R/W)	32	00						T0_DPLL_operating_mode		
force_select_reference_source (R/W)	33	0F					forced_reference_source			

Table 30 Register Map (cont...)

Register Name RO = Read Only R/W = Read/Write	Address (hex)	Default (hex)	Data Bit 7 (MSB)	6	5	4	3	2	1	0 (LSB)
cnfg_input_mode (Bit 1 RO, otherwise R/W)	34	C2	auto_extsync_ en	phalarm_ timeout	XO_ edge	man_holdover	extsync_en	ip_sonsdhb	master_slaveb	reversion_ mode
cnfg_T4_path (R/W)	35	40	lock_T4_to_T0	T4_dig_ feedback		T4_op_ from_T0	T4_forced_reference_source			
cnfg_differential_inputs (R/W)	36	02							I6_PECL	I5_LVDS
cnfg_uPsel_pins (RO)	37	02						Microprocessor type		
cnfg_dig_outputs_sonsdh (R/W)	38	1F		dig2_sonsdh	dig1_sonsdh					
cnfg_digtial_frequencies (R/W)	39	08	digital2_frequency		digital1_frequency					
cnfg_differential_outputs (R/W)	3A	C6					T07_PECL_LVDS		T06_LVDS_PECL	
cnfg_auto_bw_sel (R/W)	3B	FB	auto_BW_sel				T0_lim_int			
cnfg_nominal_frequency [7:0]	3C	99	Nominal frequency [7:0]							
(R/W) [15:8]	3D	99	Nominal frequency [15:8]							
cnfg_holdover_frequency [7:0]	3E	00	Holdover frequency [7:0]							
(R/W) [15:8]	3F	00	Holdover frequency [15:8]							
cnfg_holdover_modes (R/W)	40	88	auto_ averaging	fast_averaging	read_average	mini_holdover_mode		Holdover frequency [18:16] (with Registers 3E and 3F above)		
cnfg_DPLL_freq_limit (R/W) [7:0]	41	76	DPLL frequency offset limit [7:0]							
[9:8]	42	00							DPLL frequency offset limit [9:8]	
cnfg_interrupt_mask (R/W) [7:0]	43	00	I8 interrupt not masked	I7 interrupt not masked	I6 interrupt not masked	I5 interrupt not masked	I4 interrupt not masked	I3 interrupt not masked	I2 interrupt not masked	I1 interrupt not masked
[15:8]	44	00	Operating_ mode interrupt not masked	Main_ref_ failed interrupt not masked	I14 interrupt not masked	I13 interrupt not masked	I12 interrupt not masked	I11 interrupt not masked	I10 interrupt not masked	I9 interrupt not masked
[23:16]	45	00	Sync_ip_ alarm interrupt not masked	T4_status interrupt not masked		T4_inputs_ failed interrupt not masked	AMI2_Viol interrupt not masked	AMI2_LOS interrupt not masked	AMI1_Viol interrupt not masked	AMI1_LOS interrupt not masked
cnfg_freq_divn (R/W) [7:0]	46	FF	divn_value [7:0]							
[13:8]	47	3F			divn_value [13:8]					
cnfg_monitors (R/W)	48	05	freq_mon_clk	los_flag_ on_ TDO	ultra_fast_ switch	ext_switch	PBO_freeze	PBO_en	freq_monitor_ soft_enable	freq_monitor_ hard_enable
cnfg_freq_mon_threshold (R/W)	49	23	soft_frequency_alarm_threshold [3:0]				hard_frequency_alarm_threshold [3:0]			
cnfg_current_freq_mon_ threshold (R/W)	4A	23	current_soft_frequency_alarm_threshold [3:0]				current_hard_frequency_alarm_threshold [3:0]			
cnfg_registers_source_select (R/W)	4B	00				T4_T0_select	frequency_measurement_channel_select [3:0]			
sts_freq_measurement (R/W)	4C	00	freq_measurement_value [7:0]							
cnfg_DPLL_soft_limit (R/W)	4D	8E	Freq limit Phase loss enable	DPLL Frequency Soft Alarm Limit [6:0] Resolution = 0.628 ppm						
cnfg_upper_threshold_0 (R/W)	50	06	Configuration 0: Activity alarm set threshold [7:0]							
cnfg_lower_threshold_0 (R/W)	51	04	Configuration 0: Activity alarm reset threshold [7:0]							
cnfg_bucket_size_0 (R/W)	52	08	Configuration 0: Activity alarm bucket size [7:0]							
cnfg_decay_rate_0 (R/W)	53	01							Cfg 0:decay_rate [1:0]	
cnfg_upper_threshold_1 (R/W)	54	06	Configuration 1: Activity alarm set threshold [7:0]							
cnfg_lower_threshold_1 (R/W)	55	04	Configuration 1: Activity alarm reset threshold [7:0]							
cnfg_bucket_size_1 (R/W)	56	08	Configuration 1: Activity alarm bucket size [7:0]							
cnfg_decay_rate_1 (R/W)	57	01							Cfg 1:decay_rate [1:0]	
cnfg_upper_threshold_2 (R/W)	58	06	Configuration 2: Activity alarm set threshold [7:0]							
cnfg_lower_threshold_2 (R/W)	59	04	Configuration 2: Activity alarm reset threshold [7:0]							
cnfg_bucket_size_2 (R/W)	5A	08	Configuration 2: Activity alarm bucket size [7:0]							
cnfg_decay_rate_2 (R/W)	5B	01							Cfg 2:decay_rate [1:0]	
cnfg_upper_threshold_3 (R/W)	5C	06	Configuration 3: Activity alarm set threshold [7:0]							
cnfg_lower_threshold_3 (R/W)	5D	04	Configuration 3: Activity alarm reset threshold [7:0]							
cnfg_bucket_size_3 (R/W)	5E	08	Configuration 3: Activity alarm bucket size [7:0]							
cnfg_decay_rate_3 (R/W)	5F	01							Cfg 3:decay_rate [1:0]	

Table 30 Register Map (cont...)

Register Name RO = Read Only R/W = Read/Write	Address (hex)	Default (hex)	Data Bit 7 (MSB)	6	5	4	3	2	1	0 (LSB)
cnfg_output_frequency (R/W)										
(TO1 & TO2)	*60*	*85*	*output_freq_2 (TO2)*				*output_freq_1 (TO1)*			
(TO3 & TO4)	*61*	*86*	*output_freq_4 (TO4)*				*output_freq_3 (TO3)*			
(TO5 & TO6)	*62*	*8A*	*output_freq_6 (TO6)*				*output_freq_5 (TO5)*			
(TO7 to TO11)	*63*	*F6*	*MFrSync enable*	*FrSync enable*	*TO9 enable*	*TO8 enable*	*output_freq_7 <TO7>*			
cnfg_T4_DPLL_frequency (R/W)	*64*	*01*		*Auto Disable T4 output*	*AMI Duty cycle*	*T4 SONET/ SDH selection*		*T4_DPLL_frequency*		
cnfg_T0_DPLL_frequency (R/W)	*65*	*01*	*T4 for measuring T0 phase*	*T4 APLL for T0 E1/DS1*	*T0 Freq to T4 APLL*			*T0_DPLL_frequency*		
cnfg_T4_DPLL_bw (R/W)	*66*	*00*							*T4_DPLL_bandwidth [1:0]*	
cnfg_T0_DPLL_locked_bw (R/W)	*67*	*0B*					*T0_DPLL_locked_bandwidth [4:0]*			
cnfg_T0_DPLL_acq_bw (R/W)	*69*	*0F*					*T0_DPLL_acquisition_bandwidth [4:0]*			
cnfg_T4_DPLL_damping (R/W)	*6A*	*13*		*T4_PD2_gain_alog_8K [6:4]*				*T4_damping [2:0]*		
cnfg_T0_DPLL_damping (R/W)	*6B*	*13*		*T0_PD2_gain_alog_8K [6:4]*				*T0_damping [2:0]*		
cnfg_T4_DPLL_PD2_gain (R/W)	*6C*	*C2*	*T4_PD2_gain_ enable*	*T4_PD2_gain_alog [6:4]*				*T4_PD2_gain_digital [2:0]*		
cnfg_T0_DPLL_PD2_gain (R/W)	*6D*	*C2*	*T0_PD2_gain_ enable*	*T0_PD2_gain_alog [6:4]*				*T0_PD2_gain_digital [2:0]*		
cnfg_phase_offset (R/W) [7:0]	*70*	*00*	*phase_offset_value[7:0]*							
[15:8]	*71*	*00*	*phase_offset_value[15:8]*							
cnfg_PBO_phase_offset (R/W)	*72*	*00*			*PBO_phase_offset [5:0]*					
cnfg_phase_loss_fine_limit (R/W)	*73*	*A2*	*Fine limit Phase loss enable (1)*	*No activity for phase loss*	*Test bit Set to 1*			*phase_loss_fine_limit [2:0]*		
cnfg_phase_loss_coarse_limit (R/W)	*74*	*85*	*Coarse limit Phase loss enable (2)*	*Wide range enable*	*Enable Multi Phase resp.*		*Phase loss coarse limit in UI p-p [3:0]*			
cnfg_phasemon (R/W)	*76*	*06*	*Input noise window enable*							
sts_current_phase (RO) [7:0]	*77*	*00*	*current_phase[7:0]*							
[15:8]	*78*	*00*	*current_phase[15:8]*							
cnfg_phase_alarm_timeout (R/W)	*79*	*32*			*Timeout value in 2s intervals [5:0]*					
cnfg_sync_pulses (R/W)	*7A*	*00*	*2 k/8 k out from T4*				*8 k invert*	*8 k pulse enable*	*2 k invert*	*2 k pulse enable*
cnfg_sync_phase (R/W)	*7B*	*00*	*indep_FrSync/ MFrSync*	*Sync_OC-N_ rates*					*Sync_phase*	
cnfg_sync_monitor (R/W)	*7C*	*2B*	*ph_offset_ ramp*	*Sync_monitor_limit*			*Sync_reference_source*			
cnfg_interrupt (R/W)	*7D*	*02*						*GPO interrupt enable*	*Interrupt tristate enable*	*Interrupt polarity enable*
cnfg_protection(R/W)	*7E*	*85*	*protection_value*							
cnfg_uPsel (R/W)	*7F*	*02 **						*Microprocessor type (*Default value depends on value on UPSEL[2:0] pins)*		

Register Descriptions

Address (hex): 00

Register Name	*chip_id*			Description	(RO) 8 least significant bits of the chip ID.	Default Value	0100 1000
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
chip_id[7:0]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*chip_id* Least significant byte of the 2-byte device ID	48 (hex)	

Address (hex): 01

Register Name	*chip_id*			Description	(RO) 8 most significant bits of the chip ID.	Default Value	0010 0001
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
chip_id[15:8]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*chip_id* Most significant byte of the 2-byte device ID	21 (hex)	

Address (hex): 02

Register Name	*chip_revision*			Description	(RO) Silicon revision of the device.	Default Value	0000 0000
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
chip_revision[7:0]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*chip_revision* Silicon revision of the device	00 (hex)	

Address (hex): 03

Register Name	*test_register1*	Description	(R/W) Register containing various test controls (not normally used).	Default Value	0001 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
phase_alarm	*disable_180*		*resync_analog*	Set to zero	*8k Edge Polarity*	Set to zero	Set to zero

Bit No.	Description	Bit Value	Value Description
7	*phase_alarm* (phase alarm (R/O)) Instantaneous result from T0 DPLL	0 1	T0 DPLL reporting phase locked. T0 DPLL reporting phase lost.
6	*disable_180* Normally the DPLL will try to lock to the nearest edge (±180°) for the first 2 seconds when locking to a new reference. If the DPLL does not determine that it is phase locked after this time, then the capture range reverts to ±360°, which corresponds to frequency and phase locking. Forcing the DPLL into frequency locking mode may reduce the time to frequency lock to a new reference by up to 2 seconds. However, this may cause an unnecessary phase shift of up to 360° when the new and old references are very close in frequency and phase.	0 1	T0 DPLL automatically determines frequency lock enable. T0 DPLL forced to always frequency and phase lock.
5	Not used.	-	-
4	*resync_analog* (analog dividers re-synchronization) The analog output dividers include a synchronization mechanism to ensure phase lock at low frequencies between the input and the output.	0 1	Analog divider only synchronized during first 2 seconds after power-up. Analog dividers always synchronized.This keeps the clocks divided down from the APLL output, in sync with equivalent frequency digital clocks in the DPLL. Hence ensuring that 6.48 MHz output clocks, and above, are in sync with the DPLL even though only a 77.76 MHz clock drives the APLL.
3	Test Control Leave unchanged or set to 0	0	-
2	*8k Edge Polarity* When lock 8k mode is selected for the current input reference source, this bit allows the system to lock on either the rising or the falling edge of the input clock.	0 1	Lock to falling clock edge. Lock to rising clock edge.
1	Test Control Leave unchanged or set to zero	0	-
0	Test Control Leave unchanged or set to zero	0	-

Address (hex): 05

Register Name	*sts_interrupts*	Description	(R/W) Bits [7:0] of the interrupt status register.	Default Value	1111 1111		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
I8	*I7*	*I6*	*I5*	*I4*	*I3*	*I2*	*I1*

Bit No.	Description	Bit Value	Value Description
7	*I8* Interrupt indicating that input I8 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I8 has not changed status (valid/invalid). Input I8 has changed status (valid/invalid). Writing 1 resets the input to 0.
6	*I7* Interrupt indicating that input I7 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I7 has not changed status (valid/invalid). Input I7 has changed status (valid/invalid). Writing 1 resets the input to 0.
5	*I6* Interrupt indicating that input I6 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I6 has not changed status (valid/invalid). Input I6 has changed status (valid/invalid). Writing 1 resets the input to 0.
4	*I5* Interrupt indicating that input I5 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I5 has not changed status (valid/invalid). Input I5 has changed status (valid/invalid). Writing 1 resets the input to 0.
3	*I4* Interrupt indicating that input I4 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I4 has not changed status (valid/invalid). Input I4 has changed status (valid/invalid). Writing 1 resets the input to 0.
2	*I3* Interrupt indicating that input I3 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I3 has not changed status (valid/invalid). Input I3 has changed status (valid/invalid). Writing 1 resets the input to 0.
1	*I2* Interrupt indicating that input I2 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I2 has not changed status (valid/invalid). Input I2 has changed status (valid/invalid). Writing 1 resets the input to 0.
0	*I1* Interrupt indicating that input I1 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I1 has not changed status (valid/invalid). Input I1 has changed status (valid/invalid). Writing 1 resets the input to 0.

Address (hex): 06

Register Name	*sts_interrupts*		Description	(R/W) bits [15:8] of the interrupt status register.		Default Value	0011 1111
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
operating_ mode	*main_ref_failed*	*I14*	*I13*	*I12*	*I11*	*I10*	*I9*

Bit No.	Description	Bit Value	Value Description
7	*operating_mode* Interrupt indicating that the operating mode has changed. Latched until reset by software writing a 1 to this bit.	0 1	Operating mode has not changed. Operating mode has changed. Writing 1 resets the input to 0.
6	*main_ref_failed* Interrupt indicating that input to the T0 DPLL has failed. This interrupt will be raised after 2 missing input cycles. This is much quicker than waiting for the input to become invalid. This input is not generated in *Free-run* or *Holdover* modes. Latched until reset by software writing a 1 to this bit.	0 1	Input to the T0 DPLL is valid. Input to the T0 DPLL has failed. Writing 1 resets the input to 0.
5	*I14* Interrupt indicating that input I14 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I14 has not changed status (valid/invalid). Input I14 has changed status (valid/invalid). Writing 1 resets the input to 0.
4	*I13* Interrupt indicating that input I13 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I13 has not changed status (valid/invalid). Input I13 has changed status (valid/invalid). Writing 1 resets the input to 0.
3	*I12* Interrupt indicating that input I12 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I12 has not changed status (valid/invalid). Input I12 has changed status (valid/invalid). Writing 1 resets the input to 0.
2	*I11* Interrupt indicating that input I11 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I11 has not changed status (valid/invalid). Input I11 has changed status (valid/invalid). Writing 1 resets the input to 0.
1	*I10* Interrupt indicating that input I10 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I10 has not changed status (valid/invalid). Input I10 has changed status (valid/invalid). Writing 1 resets the input to 0.
0	*I9* Interrupt indicating that input I9 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I9 has not changed status (valid/invalid). Input I9 has changed status (valid/invalid). Writing 1 resets the input to 0.

Address (hex): 07

Register Name	*sts_current_DPLL_frequency [18:16]*	Description	(RO) Bits [18:16] of the current DPLL frequency.	Default Value	0000 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
					sts_current_DPLL_frequency[18:16]		

Bit No.	Description	Bit Value	Value Description
[7:3]	Not used.	-	-
[2:0]	*sts_current_DPLL_frequency[18:16]* When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the frequency for the T0 path is reported. When this Bit 4 = 1 the frequency for the T4 path is reported.	-	See register description of sts_current_DPLL_frequency at address 0D hex.

Address (hex): 08

Register Name	*sts_interrupts*	Description	(R/W) Bits [23:16] of the interrupt status register.	Default Value	0101 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Sync_ip_alarm	*T4_status*		*T4_inputs_ failed*	*AMI2_Viol*	*AMI2_LOS*	*AMI1_Viol*	*AMI1_LOS*

Bit No.	Description	Bit Value	Value Description
7	*Sync_ip_alarm* Interrupt indicating that the Frame Sync input monitor has hit its alarm limit. Latched until reset by software writing a 1 to this bit.	0 1	Input Frame Sync alarm has not occurred. Input Frame Sync alarm has occurred. Writing 1 resets the input to 0.
6	*T4_status* Interrupt indicating that the T4 DPLL has lost lock (if it was locked) or gained lock (if it was not locked). Latched until reset by software writing a 1 to this bit.	0 1	Input to the T4 DPLL has not changed. Input to the T4 DPLL has lost/gained lock. Writing 1 resets the input to 0.
5	Not used.	-	-
4	*T4_inputs_failed* Interrupt indicating that no valid inputs are available to the T4 DPLL. Latched until reset by software writing a 1 to this bit.	0 1	T4 DPLL has valid inputs. T4 DPLL has no valid inputs. Writing 1 resets the input to 0.
3	*AMI2_Viol* Interrupt indicating that an AMI Violation error has occurred on input I2. Latched until reset by software writing a 1 to this bit.	0 1	Input I2 has had no violation error. Input I2 has had a violation error. Writing 1 resets the input to 0.

Address (hex): 08 (cont...)

Register Name	*sts_interrupts*	Description	(R/W) Bits [23:16] of the interrupt status register.	Default Value	0101 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Sync_ip_alarm	*T4_status*		*T4_inputs_ failed*	*AMI2_Viol*	*AMI2_LOS*	*AMI1_Viol*	*AMI1_LOS*

Bit No.	Description	Bit Value	Value Description
2	*AMI2_LOS* Interrupt indicating that an AMI LOS error has occurred on input I2. Latched until reset by software writing a 1 to this bit.	0 1	Input I2 has had no LOS error. Input I2 has had a LOS error. Writing 1 resets the input to 0.
1	*AMI1_Viol* Interrupt indicating that an AMI Violation error has occurred on input I1. Latched until reset by software writing a 1 to this bit.	0 1	Input I1 has had no violation error. Input I1 has had a violation error. Writing 1 resets the input to 0.
0	*AMI1_LOS* Interrupt indicating that an AMI LOS error has occurred on input I1. Latched until reset by software writing a 1 to this bit.	0 1	Input I1 has had no LOS error. Input I1 has had a LOS error. Writing 1 resets the input to 0.

Address (hex): 09

Register Name	*sts_operating*	Description	(RO) Current operating state of the device's internal state machine.	Default Value	0100 0001		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
SYNC2K_alarm	*T4_DPLL_Lock*	*T0_DPLL_freq_ soft_alarm*	*T4_DPLL_freq_ soft_alarm*		*T0_DPLL_operating_mode*		

Bit No.	Description	Bit Value	Value Description
7	*SYNC2K_alarm* Reports current status of the external Sync monitor alarm.	0 1	External Sync monitor not in alarm condition. External Sync monitor in alarm condition.

Address (hex): 09 (cont...)

Register Name	*sts_operating*	Description	(RO) Current operating state of the device's internal state machine.	Default Value	0100 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYNC2K_alarm	*T4_DPLL_Lock*	*T0_DPLL_freq_soft_alarm*	*T4_DPLL_freq_soft_alarm*		*T0_DPLL_operating_mode*		

Bit No.	Description	Bit Value	Value Description
6	*T4_DPLL_Lock* Reports current phase lock status of the T4 DPLL. The T4 DPLL does not have the same state machine as the T0 DPLL, as it does not support all the features of the TO DPLL. It can only report its state as locked or unlocked. The bit indicates that the T4 DPLL is locked by monitoring the T4 DPLL phase loss indicators, which potentially come from four sources. The four phase loss indicators are enabled by the same registers that enable them for the T0 DPLL, as follows: the fine phase loss detector enabled by Reg. 73 Bit 7, the coarse phase loss detector enabled by Reg. 74 Bit 7, the phase loss indication from no activity on the input enabled by Reg. 73 Bit 6 and phase loss from the DPLL being at its minimum or maximum frequency limits enabled by Reg. 4D Bit 7. For the T4 DPLL lock indicator (at Reg. 09 Bit 6) the bit will latch an indication of phase lost from the coarse phase lock detector such that when an indication of phase lost (or not locked) is set it stays in that phase lost or not locked state (so Reg. 09 Bit 6 =0). For this bit to give a correct current reading of the T4 DPLL locked state, then the coarse phase loss detector should be temporarily disabled (set Reg. 74 Bit 7 = 0), then the T4 locked bit can be read (Reg. 09 Bit 6), then the coarse phase loss detector should be re-enabled again (set Reg. 74 Bit 7 = 1). Once the bit is indicating "locked" (Reg. 09 Bit 6=1), it is always a correct indication and no change to the coarse phase loss detector enable is required. If at any time any cycle slips occur that trigger the coarse phase loss detector (which monitors cycle slips) then this information is latched so that the lock bit (Reg. 09 Bit 6) will go low and stay low, indicating that a problem has occurred. It is then a requirement that the coarse phase loss detector's disable/re-enable sequence is performed during a read of the T4 locked bit, in order to get a current indication of whether the T4 DPLL is locked.	0 1	T4 DPLL not phase locked to reference source. T4 DPLL phase locked to reference source.

Address (hex): 09 (cont...)

Register Name	*sts_operating*	Description	(RO) Current operating state of the device's internal state machine.	Default Value	0100 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYNC2K_alarm	*T4_DPLL_Lock*	*T0_DPLL_freq_soft_alarm*	*T4_DPLL_freq_soft_alarm*		*T0_DPLL_operating_mode*		

Bit No.	Description	Bit Value	Value Description
5	*T0_DPLL_freq_soft_alarm* The T0 DPLL has a programmable frequency limit and "soft" alarm limit. The frequency limit is the extent to which it will track a reference before limiting. The "soft" limit is the point beyond which the DPLL tracking a reference will cause an alarm. This bit reports the status of the "soft" alarm.	0 1	T0 DPLL tracking its reference within the limits of the programmed "soft" alarm. T0 DPLL tracking its reference beyond the limits of the programmed "soft" alarm.
4	*T4_DPLL_freq_soft_alarm* The T4 DPLL has a programmable frequency limit and "soft" alarm limit. The frequency limit is the extent to which it will track a reference before limiting. The "soft" limit is the point beyond which the DPLL tracking a reference will cause an alarm. This bit reports the status of the "soft" alarm.	0 1	T4 DPLL tracking its reference within the limits of the programmed "soft" alarm. T4 DPLL tracking its reference beyond the limits of the programmed "soft" alarm.
3	Not used.	-	-
[2:0]	*T0_DPLL_operating_mode* This field is used to report the state of the internal finite state machine controlling the T0 DPLL.	000 001 010 011 100 101 110 111	Not used. Free Run. Holdover. Not used. Locked. Pre-locked2. Pre-locked. Phase Lost.

Address (hex): 0A

Register Name	*sts_priority_table*	Description	(RO) Bits [7:0] of the validated priority table.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Highest priority validated source				*Currently selected source*			

Bit No.	Description	Bit Value	Value Description
[7:4]	*Highest priority validated source* Reports the input channel number of the highest priority validated source. *Note...If an input is valid and it does not appear in this field when otherwise it might, then the input may have been disallowed in Reg. 30 and Reg. 31 (cnfg_sts_remote_sources_valid).* *When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the highest priority validated source for the T0 path is reported. When this Bit 4 = 1 the highest priority validated source for the T4 path is reported.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	No valid source available. Input I1 is the highest priority valid source. Input I2 is the highest priority valid source. Input I3 is the highest priority valid source. Input I4 is the highest priority valid source. Input I5 is the highest priority valid source. Input I6 is the highest priority valid source. Input I7 is the highest priority valid source. Input I8 is the highest priority valid source. Input I9 is the highest priority valid source. Input I10 is the highest priority valid source. Input I11 is the highest priority valid source. Input I12 is the highest priority valid source. Input I13 is the highest priority valid source. Input I14 is the highest priority valid source. Not used.
[3:0]	*Currently selected source* Reports the input channel number of the currently selected source. When in Non-revertive mode, this is not necessarily the same as the highest priority validated source. *Note...If an input is valid and it does not appear in this field when otherwise it might, then the input may have been disallowed in Reg. 30 and Reg. 31 (cnfg_sts_remote_sources_valid).* *When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the currently selected source for the T0 path is reported. When this Bit 4 = 1 the currently selected source for the T4 path is reported. The T4 path does not have a Non-revertive mode so this will always be the same as the highest priority validated source.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	No source currently selected. Input I1 is the currently selected source. Input I2 is the currently selected source. Input I3 is the currently selected source. Input I4 is the currently selected source. Input I5 is the currently selected source. Input I6 is the currently selected source. Input I7 is the currently selected source. Input I8 is the currently selected source. Input I9 is the currently selected source. Input I10 is the currently selected source. Input I11 is the currently selected source. Input I12 is the currently selected source. Input I13 is the currently selected source. Input I14 is the currently selected source. Not used.

Address (hex): 0B

Register Name	*sts_priority_table*	Description	(RO) Bits [15:8] of the validated priority table.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3rd highest priority validated source				*2nd highest priority validated source*			

Bit No.	Description	Bit Value	Value Description
[7:4]	*3rd highest priority validated source* Reports the input channel number of the 3rd highest priority validated source. *Note...If an input is valid and it does not appear in this field when otherwise it might, then the input may have been disallowed in Reg. 30 and Reg. 31 (cnfg_sts_remote_sources_valid).* *When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the 3rd highest priority validated source for the T0 path is reported. When this Bit 4 = 1 the value will always be zero as the T4 path does not maintain the 3rd highest priority validated source.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Less than 3 valid sources available. Input I1 is the 3rd highest priority valid source. Input I2 is the 3rd highest priority valid source. Input I3 is the 3rd highest priority valid source. Input I4 is the 3rd highest priority valid source. Input I5 is the 3rd highest priority valid source. Input I6 is the 3rd highest priority valid source. Input I7 is the 3rd highest priority valid source. Input I8 is the 3rd highest priority valid source. Input I9 is the 3rd highest priority valid source. Input I10 is the 3rd highest priority valid source. Input I11 is the 3rd highest priority valid source. Input I12 is the 3rd highest priority valid source. Input I13 is the 3rd highest priority valid source. Input I14 is the 3rd highest priority valid source. Not used.
[3:0]	*2nd highest priority validated* Reports the input channel number of the 2nd highest priority validated source. *Note...If an input is valid and it does not appear in this field when otherwise it might, then the input may have been disallowed in Reg. 30 and Reg. 31 (cnfg_sts_remote_sources_valid).* *When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the 2nd highest priority validated source for the T0 path is reported. When this Bit 4 = 1 the 2nd highest priority validated source for the T4 path is reported.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Less than 2 valid sources available. Input I1 is the 2nd highest priority valid source. Input I2 is the 2nd highest priority valid source. Input I3 is the 2nd highest priority valid source. Input I4 is the 2nd highest priority valid source. Input I5 is the 2nd highest priority valid source. Input I6 is the 2nd highest priority valid source. Input I7 is the 2nd highest priority valid source. Input I8 is the 2nd highest priority valid source. Input I9 is the 2nd highest priority valid source. Input I10 is the 2nd highest priority valid source. Input I11 is the 2nd highest priority valid source. Input I12 is the 2nd highest priority valid source. Input I13 is the 2nd highest priority valid source. Input I14 is the 2nd highest priority valid source. Not used.

Address (hex): 0C

Register Name	*sts_current_DPLL_frequency [7:0]*	Description	(RO) Bits [7:0] of the current DPLL frequency.	Default Value	0000 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bits [7:0] of sts_current_DPLL_frequency							

Bit No.	Description	Bit Value	Value Description
[7:0]	*Bits [7:0] of sts_current_DPLL_frequency* *When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the frequency for the T0 path is reported. When this Bit 4 = 1 the frequency for the T4 path is reported.	-	See register description of *sts_current_DPLL_frequency* at address 0D hex.

Address (hex): 0D

Register Name	*sts_current_DPLL_frequency [15:8]*	Description	(RO) Bits [15:8] of the current DPLL frequency.	Default Value	0000 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
sts_current_DPLL_frequency[15:8]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*sts_current_DPLL_frequency[15:8]* This value in this register is combined with the value in Reg. 0C and Reg. 07 to represent the current frequency offset of the DPLL. *When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the frequency for the T0 path is reported. When this Bit 4 = 1 the frequency for the T4 path is reported.	-	In order to calculate the ppm offset of the DPLL with respect to the crystal oscillator frequency, the value in Reg. 07, Reg. 0D and Reg. 0C need to be concatenated. This value is a 2's complement signed integer. The value multiplied by 0.0003068 dec will give the value in ppm offset with respect to the XO frequency, allowing for any crystal calibration that has been performed, via *cnfg_nominal_frequency*, Reg. 3C and 3D. The value is actually the DPLL integral path value so it can be viewed as an average frequency, where the rate of change is related to the DPLL bandwidth. If Bit 3 of Reg. 3B is *High* then this value will freeze if the DPLL has been pulled to its min or max frequency.

Address (hex): 0E

Register Name	*sts_sources_valid*	Description	(RO) 8 least significant bits of the *sts_sources_valid* register.	Default Value	0000 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
I8	*I7*	*I6*	*I5*	*I4*	*I3*	*I2*	*I1*

Bit No.	Description	Bit Value	Value Description
7	*I8* Bit indicating if I8 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I8 is invalid. Input I8 is valid.
6	*I7* Bit indicating if I7 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I7 is invalid. Input I7 is valid.
5	*I6* Bit indicating if I6 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I6 is invalid. Input I6 is valid.
4	*I5* Bit indicating if I5 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I5 is invalid. Input I5 is valid.
3	*I4* Bit indicating if I4 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I4 is invalid. Input I4 is valid.
2	*I3* Bit indicating if I3 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I3 is invalid. Input I3 is valid.
1	*I2* Bit indicating if I2 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I2 is invalid. Input I2 is valid.
0	*I1* Bit indicating if I1 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I1 is invalid. Input I1 is valid.

Address (hex): 0F

Register Name	*sts_sources_valid*	Description	(RO) 8 most significant bits of the *sts_sources_valid* register.	Default Value	0000 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		I14	*I13*	*I12*	*I11*	*I10*	*I9*

Bit No.	Description	Bit Value	Value Description
[7:6]	Not used.	-	-
5	*I14* Bit indicating if I14 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I14 is invalid. Input I14 is valid.
4	*I13* Bit indicating if I13 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I13 is invalid. Input I13 is valid.
3	*I12* Bit indicating if I12 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I12 is invalid. Input I12 is valid.
2	*I11* Bit indicating if I11 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I11 is invalid. Input I11 is valid.
1	*I10* Bit indicating if I10 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I10 is invalid. Input I10 is valid.
0	*I9* Bit indicating if I9 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I9 is invalid. Input I9 is valid.

Address (hex): 10

Register Name	*sts_reference_sources Input pairs (1 & 2)*	Description	(RO except for test when R/W) Reports any alarms active on inputs.	Default Value	0110 0110

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 10: Status of I2 Input Address 11: Status of I4 Input Address 12: Status of I6 Input Address 13: Status of I8 Input Address 14: Status of I10 Input Address 15: Status of I12 Input Address 16: Status of I14 Input				*Address 10: Status of I1 Input Address 11: Status of I3 Input Address 12: Status of I5 Input Address 13: Status of I7 Input Address 14: Status of I9 Input Address 15: Status of I11 Input Address 16: Status of I13 Input*			

Bit No.	Description	Bit Value	Value Description
7 & 3	*Out-of-band alarm (soft)* Soft out of band alarm bit for input. A “soft” alarm will not invalidate an input.	0 1	No alarm. Alarm armed. Alarm thresholds (range) set by Reg. 49, or by Reg. 4A, Bits [7:4] if the input is currently selected.
6 & 2	*Out-of-band alarm (hard)* Hard out of band alarm bit for input. A “hard” alarm will invalidate an input.	0 1	No alarm. Alarm armed. Alarm thresholds set by Reg. 49 Bits [3:0], or by Reg. 4A Bits [3:0] if the input is currently selected.
5 & 1	*No activity alarm* Alarm indication from the activity monitors.	0 1	No alarm. Input has an active no activity alarm.
4 & 0	*Phase lock alarm* If the DPLL can not indicate that it is phase locked onto the current source within 100 seconds this alarm will be raised.	0 1	No alarm. Phase lock alarm.

Address (hex): 11 As Reg. 10, but for *sts_reference_sources,* Input pairs *(3 & 4)*

Address (hex): 12 As Reg. 10, but for *sts_reference_sources,* Input pairs *(5 & 6)*

Address (hex): 13 As Reg. 10, but for *sts_reference_sources,* Input pairs *(7 & 8)*

Address (hex): 14 As Reg. 10, but for *sts_reference_sources,* Input pairs *(9 & 10)*

Address (hex): 15 As Reg. 10, but for *sts_reference_sources,* Input pairs *(11 & 12)*

Address (hex): 16 As Reg. 10, but for *sts_reference_sources,* Input pairs *(13 & 14)*

Address (hex): 18

Register Name	*cnfg_ref_selection_priority (1 & 2)*	Description	(R/W) Configures the relative priority of input sources I1 and I2.	Default Value (T0)* 0011 0010 (T4)* 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
cnfg_ref_selection_priority_2				*cnfg_ref_selection_priority_1*			

Bit No.	Description	Bit Value	Value Description
[7:4]	*cnfg_ref_selection_priority_2* This 4-bit value represents the relative priority of input I2. The smaller the number, the higher the priority; zero disables the input. *When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the priority for the T0 path is configured. When this Bit 4 = 1 the priority for the T4 path is configured.	0000 0001-1111	Input I2 unavailable for automatic selection. Input I2 priority value.
[3:0]	*cnfg_ref_selection_priority_1* This 4-bit value represents the relative priority of input I1. The smaller the number, the higher the priority; zero disables the input. *When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the priority for the T0 path is configured. When this Bit 4 = 1 the priority for the T4 path is configured.	0000 0001-1111	Input I1 unavailable for automatic selection. Input I1 priority value.

Address (hex): 19

Register Name	*cnfg_ref_selection_priority (3 & 4)*	Description	(R/W) Configures the relative priority of input sources I3 and I4.	Default Value (T0)* 0101 0100 (T4)* 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
cnfg_ref_selection_priority_4				*cnfg_ref_selection_priority_3*			

Bit No.	Description	Bit Value	Value Description
[7:4]	*cnfg_ref_selection_priority_4* This 4-bit value represents the relative priority of input I4. The smaller the number, the higher the priority; zero disables the input. *When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the priority for the T0 path is configured. When this Bit 4 = 1 the priority for the T4 path is configured.	0000 0001-1111	Input I4 unavailable for automatic selection. Input I4 priority value.

Address (hex): 19 (cont...)

Register Name	*cnfg_ref_selection_priority (3 & 4)*	Description	(R/W) Configures the relative priority of input sources I3 and I4.	Default Value (T0)* 0101 0100 (T4)* 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
cnfg_ref_selection_priority_4				*cnfg_ref_selection_priority_3*			

Bit No.	Description	Bit Value	Value Description
[3:0]	*cnfg_ref_selection_priority_3* This 4-bit value represents the relative priority of input I3. The smaller the number, the higher the priority; zero disables the input. *When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the priority for the T0 path is configured. When this Bit 4 = 1 the priority for the T4 path is configured.	0000 0001-1111	Input I3 unavailable for automatic selection. Input I3 priority value.

Address (hex): 1A

Register Name	*cnfg_ref_selection_priority (5 & 6)*	Description	(R/W) Configures the relative priority of input sources I5 and I6.	Default Value (T0)* 0111 0110 (T4)* 0111 0110

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
cnfg_ref_selection_priority_6				*cnfg_ref_selection_priority_5*			

Bit No.	Description	Bit Value	Value Description
[7:4]	*cnfg_ref_selection_priority_6* This 4-bit value represents the relative priority of input I6. The smaller the number, the higher the priority; zero disables the input. *When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the priority for the T0 path is configured. When this Bit 4 = 1 the priority for the T4 path is configured.	0000 0001-1111	Input I6 unavailable for automatic selection. Input I6 priority value.
[3:0]	*cnfg_ref_selection_priority_5* This 4-bit value represents the relative priority of input I5. The smaller the number, the higher the priority; zero disables the input. *When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the priority for the T0 path is configured. When this Bit 4 = 1 the priority for the T4 path is configured.	0000 0001-1111	Input I5 unavailable for automatic selection. Input I5 priority value.

Address (hex): 1B

Register Name	*cnfg_ref_selection_priority (7 & 8)*	Description	(R/W) Configures the relative priority of input sources I7 and I8.	Default Value (T0)* 1001 1000 (T4)* 1001 1000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
cnfg_ref_selection_priority_8				cnfg_ref_selection_priority_7			

Bit No.	Description	Bit Value	Value Description
[7:4]	*cnfg_ref_selection_priority_8* This 4-bit value represents the relative priority of input I8. The smaller the number, the higher the priority; zero disables the input. *When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the priority for the T0 path is configured. When this Bit 4 = 1 the priority for the T4 path is configured.	0000 0001-1111	Input I8 unavailable for automatic selection. Input I8 priority value.
[3:0]	*cnfg_ref_selection_priority_7* This 4-bit value represents the relative priority of input I7. The smaller the number, the higher the priority; zero disables the input. *When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the priority for the T0 path is configured. When this Bit 4 = 1 the priority for the T4 path is configured.	0000 0001-1111	Input I7 unavailable for automatic selection. Input I7 priority value.

Address (hex): 1C

Register Name	*cnfg_ref_selection_priority (9 & 10)*	Description	(R/W) Configures the relative priority of input sources I9 and I10.	Default Value (T0)* 1011 1010 (T4)* 1011 1010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
cnfg_ref_selection_priority_10				*cnfg_ref_selection_priority_9*			

Bit No.	Description	Bit Value	Value Description
[7:4]	*cnfg_ref_selection_priority_10* This 4-bit value represents the relative priority of input I10. The smaller the number, the higher the priority; zero disables the input. *When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the priority for the T0 path is configured. When this Bit 4 = 1 the priority for the T4 path is configured.	0000 0001-1111	Input I10 unavailable for automatic selection. Input I10 priority value.

Address (hex): 1C (cont...)

Register Name	*cnfg_ref_selection_priority (9 & 10)*	Description	(R/W) Configures the relative priority of input sources I9 and I10.	Default Value (T0)* 1011 1010 (T4)* 1011 1010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
cnfg_ref_selection_priority_10				*cnfg_ref_selection_priority_9*			

Bit No.	Description	Bit Value	Value Description
[3:0]	*cnfg_ref_selection_priority_9* This 4-bit value represents the relative priority of input I9. The smaller the number, the higher the priority; zero disables the input. *When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the priority for the T0 path is configured. When this Bit 4 = 1 the priority for the T4 path is configured.	0000 0001-1111	Input I9 unavailable for automatic selection. Input I9 priority value.

Address (hex): 1D

Register Name	*cnfg_ref_selection_priority (11 & 12)*	Description	(R/W) Configures the relative priority of input sources I11 and I12.	Default Value (T0)* 1101 1100 (T4)* 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
cnfg_ref_selection_priority_12				*cnfg_ref_selection_priority_11*			

Bit No.	Description	Bit Value	Value Description
[7:4]	*cnfg_ref_selection_priority_12* This 4-bit value represents the relative priority of input I12. The smaller the number, the higher the priority; zero disables the input. *When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the priority for the T0 path is configured. When this Bit 4 = 1 the priority for the T4 path is configured.	0000 0001-1111	Input I12 unavailable for automatic selection. Input I12 priority value.

Address (hex): 1D (cont...)

Register Name	*cnfg_ref_selection_priority (11 & 12)*	Description	(R/W) Configures the relative priority of input sources I11 and I12.	Default Value (T0)* 1101 1100 (T4)* 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
cnfg_ref_selection_priority_12				*cnfg_ref_selection_priority_11*			

Bit No.	Description	Bit Value	Value Description
[3:0]	*cnfg_ref_selection_priority_11* This 4-bit value represents the relative priority of input I11. The smaller the number, the higher the priority; zero disables the input. *The priority of input I11 depends on the value of the MASTSLVB pin at power-up. If MASTSLVB is *High* (master) at power-up, then the priority will default to 12. If MASTSLVB is *Low* (slave) at power-up, then the priority will default to 1. *When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the priority for the T0 path is configured. When this Bit 4 = 1 the priority for the T4 path is configured.	0000 0001-1111	Input I11 unavailable for automatic selection. Input I11 priority value.

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Address (hex): 1E

Register Name	*cnfg_ref_selection_priority (13 & 14)*	Description	(R/W) Configures the relative priority of input sources I13 and I14.	Default Value (T0)* 1111 1110 (T4)* 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
cnfg_ref_selection_priority_14				*cnfg_ref_selection_priority_13*			

Bit No.	Description	Bit Value	Value Description
[7:4]	*cnfg_ref_selection_priority_14* This 4-bit value represents the relative priority of input I14. The smaller the number, the higher the priority; zero disables the input. *When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the priority for the T0 path is configured. When this Bit 4 = 1 the priority for the T4 path is configured.	0000 0001-1111	Input I14 unavailable for automatic selection. Input I14 priority value.

Address (hex): 1E (cont...)

Register Name	*cnfg_ref_selection_priority (13 & 14)*	Description	(R/W) Configures the relative priority of input sources I13 and I14.	Default Value	(T0)* 1111 1110 (T4)* 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
cnfg_ref_selection_priority_14				*cnfg_ref_selection_priority_13*			

Bit No.	Description	Bit Value	Value Description
[3:0]	*cnfg_ref_selection_priority_13* This 4-bit value represents the relative priority of input I13. The smaller the number, the higher the priority; zero disables the input. *When Bit 4 (*T4_T0_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the priority for the T0 path is configured. When this Bit 4 = 1 the priority for the T4 path is configured.	0000 0001-1111	Input I13 unavailable for automatic selection. Input I13 priority value.

Address (hex): 20

Register Name	*cnfg_ref_source_frequency _1*	Description	(R/W) Configuration of the frequency and input monitoring for input I1.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Set to zero		*bucket_id_1*		Set to zero			

Bit No.	Description	Bit Value	Value Description
[7:6]	Set to zero	00	Set to zero
[5:4]	*bucket_id_1* Every input has its own Leaky Bucket used for activity monitoring. There are four possible configurations for each Leaky Bucket- see Reg. 50 to 5F. This 2-bit field selects the configuration used for input I1.	00 01 10 11	Input I1 activity monitor uses Leaky Bucket Configuration 0. Input I1 activity monitor uses Leaky Bucket Configuration 1. Input I1 activity monitor uses Leaky Bucket Configuration 2. Input I1 activity monitor uses Leaky Bucket Configuration 3.
[3:0]	Set to zero	0000	8 kHz only

Address (hex): 21

Register Name	*cnfg_ref_source_frequency_2*	Description	(R/W) Configuration of the frequency and input monitoring for input I2.	Default Value	0000 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Set to zero		*bucket_id_2*		Set to zero			

Bit No.	Description	Bit Value	Value Description
[7:6]	Set to zero	00	Set to zero
[5:4]	*bucket_id_2* Every input has its own Leaky Bucket used for activity monitoring. There are four possible configurations for each Leaky Bucket- see Reg. 50 to Reg. 5F. This 2-bit field selects the configuration used for input I2.	00 01 10 11	Input I2 activity monitor uses Leaky Bucket Configuration 0. Input I2 activity monitor uses Leaky Bucket Configuration 1. Input I2 activity monitor uses Leaky Bucket Configuration 2. Input I2 activity monitor uses Leaky Bucket Configuration 3.
[3:0]	Set to zero	0000	8 kHz only

Address (hex): 22

Use <n> = 3

Register Name	*cnfg_ref_source_frequency_<n>, where for Reg 22, n = 3*	Description	(R/W) Configuration of the frequency and input monitoring for input I<n>.	Default Value	0000 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
divn_<n>	*lock8k_<n>*	*bucket_id_<n>*		*reference_source_frequency_<n>*			

Bit No.	Description	Bit Value	Value Description
7	*divn_<n>* This bit selects whether or not input I<n> is divided in the programmable pre-divider prior to being input to the DPLL and frequency monitor- see Reg. 46 and Reg. 47 (*cnfg_freq_divn*).	0 1	Input I<n> fed directly to DPLL and monitor. Input I<n> fed to DPLL and monitor via pre-divider.
6	*lock8k_<n>* This bit selects whether or not input I<n> is divided in the preset pre-divider prior to being input to the DPLL. This results in the DPLL locking to the reference after it has been divided to 8 kHz. This bit is ignored when *divn_<n>* is set (bit =1).	0 1	Input I<n> fed directly to DPLL. Input I<n> fed to DPLL via preset pre-divider.

Address (hex): 22 (cont...)

Use <n> = 3

Register Name	*cnfg_ref_source_frequency _<n>, where for Reg 22, n = 3*	Description	(R/W) Configuration of the frequency and input monitoring for input I<n>.	Default Value	0000 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
divn_<n>	*lock8k_<n>*	*bucket_id_<n>*		*reference_source_frequency_<n>*			

Bit No.	Description	Bit Value	Value Description
[5:4]	*bucket_id_<n>* Every input has its own Leaky Bucket used for activity monitoring. There are four possible configurations for each Leaky Bucket- see Reg. 50 to Reg. 5F. This 2-bit field selects the configuration used for input I<n>.	00	Input I<n> activity monitor uses Leaky Bucket Configuration 0.
		01	Input I<n> activity monitor uses Leaky Bucket Configuration 1.
		10	Input I<n> activity monitor uses Leaky Bucket Configuration 2.
		11	Input I<n> activity monitor uses Leaky Bucket Configuration 3.
[3:0]	*reference_source_frequency_<n>* Programs the frequency of the reference source connected to input I<n>. If *divn_<n>* is set, then this value should be set to 0000 (8 kHz).	0000	8 kHz.
		0001	1544/2048 kHz (dependant on Bit 2 (*ip_sonsdhb*) in Reg. 34).
		0010	6.48 MHz.
		0011	19.44 MHz.
		0100	25.92 MHz.
		0101	38.88 MHz.
		0110	51.84 MHz.
		0111	77.76 MHz.
		1000	155.52 MHz.
		1001	2 kHz.
		1010	4 kHz.
		1011-1111	Not used.

Address	Register	Description	n	Default
Address (hex): 23	*cnfg_ref_source_frequency_4*	Use description for Reg. 22, but use <n> =	*4*	Default = 0000 0000
Address (hex): 24	*cnfg_ref_source_frequency_5*	Use description for Reg. 22, but use <n> =	*5*	Default = 0000 0011
Address (hex): 25	*cnfg_ref_source_frequency_6*	Use description for Reg. 22, but use <n> =	*6*	Default = 0000 0011
Address (hex): 26	*cnfg_ref_source_frequency_7*	Use description for Reg. 22, but use <n> =	*7*	Default = 0000 0011
Address (hex): 27	*cnfg_ref_source_frequency_8*	Use description for Reg. 22, but use <n> =	*8*	Default = 0000 0011
Address (hex): 28	*cnfg_ref_source_frequency_9*	Use description for Reg. 22, but use <n> =	*9*	Default = 0000 0011
Address (hex): 29	*cnfg_ref_source_frequency_10*	Use description for Reg. 22, but use <n> =	*10*	Default = 0000 0011
Address (hex): 2A	*cnfg_ref_source_frequency_11*	Use description for Reg. 22, but use <n> =	*11*	Default = 0000 0011
Address (hex): 2B	*cnfg_ref_source_frequency_12*	Use description for Reg. 22, but use <n> =	*12*	Default = 0000 0001
Address (hex): 2C	*cnfg_ref_source_frequency_13*	Use description for Reg. 22, but use <n> =	*13*	Default = 0000 0001
Address (hex): 2D	*cnfg_ref_source_frequency_14*	Use description for Reg. 22, but use <n> =	*14*	Default = 0000 0001

Address (hex): 30

Register Name	*cnfg_sts_remote_sources_valid*	Description	(R/W) Bits [7:0] of the remote sources valid register. A register used to disable sources that are invalid in another device in a redundancy pair.	Default Value	1111 1111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I8	*I7*	*I6*	*I5*	*I4*	*I3*	*I2*	*I1*

Bit No.	Description	Bit Value	Value Description
7	*I8* Bit enabling input I8 to be considered for locking to. If this bit is not set, then even if this input I8 is valid, it will still not appear in Reg. 0A and 0B (*sts_priority_table*).	0 1	Locking to input I8 disallowed. Locking to input I8 allowed.
6	*I7* Bit enabling input I7 to be considered for locking to. If this bit is not set, then even if this input I7 is valid, it will still not appear in Reg. 0A and 0B (*sts_priority_table*).	0 1	Locking to input I7 disallowed. Locking to input I7 allowed.
5	*I6* Bit enabling input I6 to be considered for locking to. If this bit is not set, then even if this input I6 is valid, it will still not appear in Reg. 0A and 0B (*sts_priority_table*).	0 1	Locking to input I6 disallowed. Locking to input I6 allowed.
4	*I5* Bit enabling input I5 to be considered for locking to. If this bit is not set, then even if this input I5 is valid, it will still not appear in Reg. 0A and 0B (*sts_priority_table*).	0 1	Locking to input I5 disallowed. Locking to input I5 allowed.
3	*I4* Bit enabling input I4 to be considered for locking to. If this bit is not set, then even if this input I4 is valid, it will still not appear in Reg. 0A and 0B (*sts_priority_table*).	0 1	Locking to input I4 disallowed. Locking to input I4 allowed.
2	*I3* Bit enabling input I3 to be considered for locking to. If this bit is not set, then even if this input I3 is valid, it will still not appear in Reg. 0A and 0B (*sts_priority_table*).	0 1	Locking to input I3 disallowed. Locking to input I3 allowed.
1	*I2* Bit enabling input I2 to be considered for locking to. If this bit is not set, then even if this input I2 is valid, it will still not appear in Reg. 0A and 0B (*sts_priority_table*).	0 1	Locking to input I2 disallowed. Locking to input I2 allowed.

Address (hex): 30 (cont...)

Register Name	*cnfg_sts_remote_sources_valid*	Description	(R/W) Bits [7:0] of the remote sources valid register. A register used to disable sources that are invalid in another device in a redundancy pair.	Default Value	1111 1111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I8	*I7*	*I6*	*I5*	*I4*	*I3*	*I2*	*I1*

Bit No.	Description	Bit Value	Value Description
0	*I1* Bit enabling input I1 to be considered for locking to. If this bit is not set, then even if this input I1 is valid, it will still not appear in Reg. 0A and 0B (*sts_priority_table*).	0 1	Locking to input I1 disallowed. Locking to input I1 allowed.

Address (hex): 31

Register Name	*cnfg_sts_remote_sources_valid*	Description	(R/W) Bits [13:8] of the remote sources valid register. A register used to disable source that are invalid in another device in a redundancy pair.	Default Value	0011 1111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		I14	*I13*	*I12*	*I11*	*I10*	*I9*

Bit No.	Description	Bit Value	Value Description
[7:6]	Not used.	-	-
5	*I14* Bit enabling input I14 to be considered for locking to. If this bit is not set, then even if this input I14 is valid, it will still not appear in Reg. 0A and 0B (*sts_priority_table*).	0 1	Locking to input I14 disallowed. Locking to input I14 allowed.
4	*I13* Bit enabling input I13 to be considered for locking to. If this bit is not set, then even if this input I13 is valid, it will still not appear in Reg. 0A and 0B (*sts_priority_table*).	0 1	Locking to input I13 disallowed. Locking to input I13 allowed.
3	*I12* Bit enabling input I12 to be considered for locking to. If this bit is not set, then even if this input I12 is valid, it will still not appear in Reg. 0A and 0B (*sts_priority_table*).	0 1	Locking to input I12 disallowed. Locking to input I12 allowed.

Address (hex): 31 (cont...)

Register Name	*cnfg_sts_remote_sources_valid*	Description	(R/W) Bits [13:8] of the remote sources valid register. A register used to disable source that are invalid in another device in a redundancy pair.	Default Value	0011 1111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		I14	*I13*	*I12*	*I11*	*I10*	*I9*

Bit No.	Description	Bit Value	Value Description
2	*I11* Bit enabling input I11 to be considered for locking to. If this bit is not set, then even if this input I11 is valid, it will still not appear in Reg. 0A and 0B (*sts_priority_table*).	0 1	Locking to input I11 disallowed. Locking to input I11 allowed.
1	*I10* Bit enabling input I10 to be considered for locking to. If this bit is not set, then even if this input I10 is valid, it will still not appear in Reg. 0A and 0B (*sts_priority_table*).	0 1	Locking to input I10 disallowed. Locking to input I10 allowed.
0	*I9* Bit enabling input I9 to be considered for locking to. If this bit is not set, then even if this input I9 is valid, it will still not appear in Reg. 0A and 0B (sts_priority_table).	0 1	Locking to input I9 disallowed. Locking to input I9 allowed.

Address (hex): 32

Register Name	*cnfg_operating_mode*	Description	(R/W) Register to force the state of the TO DPLL controlling state machine.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					T0_DPLL_operating_mode		

Bit No.	Description	Bit Value	Value Description
[7:3]	Not used.	-	-

Address (hex): 32 (cont...)

Register Name	*cnfg_operating_mode*	Description	(R/W) Register to force the state of the T0 DPLL controlling state machine.	Default Value	0000 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
					T0_DPLL_operating_mode		

Bit No.	Description	Bit Value	Value Description
[2:0]	*T0_DPLL_operating_mode* This field is used to control the state of the internal finite state machine controlling the T0 DPLL. A value of zero is used to allow the finite state machine to control itself. Any other value will force the state machine to jump into that state. Care should be taken when forcing the state machine. Whilst it is forced, the internal monitoring functions cannot affect the internal state machine, therefore, the user is responsible for all monitoring and control functions required to achieve the desired functionality.	000 001 010 011 100 101 110 111	Automatic (internal state machine controlled). Free Run. Holdover. Not used. Locked. Pre-locked2. Pre-locked. Phase Lost.

Address (hex): 33

Register Name	*force_select_reference_source*	Description	(R/W) Register used to force the selection of a particular reference source for the T0 DPLL.	Default Value	0000 1111		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
				forced_reference_source			

Bit No.	Description	Bit Value	Value Description
[7:4]	Not used.	-	-
[3:0]	*forced_reference_source* Value representing the source to be selected by the T0 DPLL. Value of 0 hex will leave the selection to the automatic control mechanism within the device. Using this mechanism will bypass all the monitoring functions assuming the selected input to be valid. If the device is not in state “Locked” then it will progress to state locked in the usual manner. If the input fails, the device will not change state to Holdover, as it is not allowed to disqualify the source. The effect of this register is simply to raise the priority of the selected input to “1” (highest). To ensure selection of the programmed input reference under all circumstances, revertive mode should be enabled (Reg. 34 bit 0 set to “1”).	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Automatic state machine source selection T0 DPLL forced to select input I1. T0 DPLL forced to select input I2. T0 DPLL forced to select input I3. T0 DPLL forced to select input I4. T0 DPLL forced to select input I5. T0 DPLL forced to select input I6. T0 DPLL forced to select input I7. T0 DPLL forced to select input I8. T0 DPLL forced to select input I9. T0 DPLL forced to select input I10. T0 DPLL forced to select input I11. T0 DPLL forced to select input I12. T0 DPLL forced to select input I13. T0 DPLL forced to select input I14. Not used.

Address (hex): 34

Register Name	*cnfg_input_mode*	Description	(Bit 1 RO, otherwise R/W) Register controlling various input modes of the device.	Default Value	1100 0010*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
auto_extsync_en	*phalarm_time-out*	*XO_edge*	*man_holdover*	*extsync_en*	*ip_sonsdhb*	*master_slaveb*	*reversion_mode*

Bit No.	Description	Bit Value	Value Description
7	*auto_extsync_en* Bit to enable automatic enabling of the external Frame Sync input when locked to source defined in Reg. 7C Bits [3:0] (*Sync_reference_source*).	0 1	External Frame Sync enabled/disabled according to *extsync_en*. External Frame Sync enabled if *extsync_en* = 1 AND T0 DPLL locked to source assigned to *Sync_reference_source*.
6	*phalarm_timeout* Bit to enable the automatic time-out facility on phase alarms. When enabled, any source with a phase alarm set will have its phase alarm cancelled after 128 seconds.	0 1	Phase alarms on sources only cancelled by software. Phase alarms on sources automatically time out.
5	*XO_edge* If the 12.800 MHz oscillator module connected to REFCLK has one edge faster than the other, then for jitter performance reasons, the faster edge should be selected. This bit allows either the rising edge or the falling edge to be selected.	0 1	Device uses the rising edge of the external oscillator. Device uses the falling edge of the external oscillator.
4	*man_holdover* Bit to select whether or not the Holdover frequency is taken directly from Reg. 3E/Reg. 3F/Reg. 40 (*cnfg_holdover_frequency*). If this bit is set then it overrides any other Holdover control bits.	0 1	Holdover frequency is determined automatically. Holdover frequency is taken from *cnfg_holdover_frequency* register.
3	*extsync_en* Bit to select whether or not the T0 DPLL will look for a reference Sync pulse on the *SYNC2K* input pin. Even though this bit may enable the external Sync reference, it may be disabled according to *auto_extsync_en*.	0 1	No external Sync signal- *SYNC2K* pin ignored. External Sync derived from *SYNC2K* pin according to *auto_extsync_en*.
2	*ip_sonsdhb* Bit to configure input frequencies to be either SONET or SDH derived. This applies only to selections of 0001 (bin) in the *cnfg_ref_source_frequency* registers when the input frequency is either 1544 kHz or 2048 kHz. *Note...this bit affects the SONET/SDH output on TO9-refer to Reg. 64 Bit 4 and Reg. 35 Bit 4.* *The default value of this bit is taken from the value of the SONSDHB pin at power-up.	0 1	SDH- inputs set to 0001 expected to be 2048 kHz. SONET- inputs set to 0001 expected to be 1544 kHz.

Address (hex): 34 (cont...)

Register Name	*cnfg_input_mode*	Description	(Bit 1 RO, otherwise R/W) Register controlling various input modes of the device.	Default Value	1100 0010*		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
auto_extsync_en	*phalarm_time-out*	*XO_edge*	*man_holdover*	*extsync_en*	*ip_sonsdhb*	*master_slaveb*	*reversion_mode*

Bit No.	Description	Bit Value	Value Description
1	*master_slaveb (R/O)* Bit to reflect the value of the MASTSLVB pin. *As this always reflects the value on the pin, the default value of this bit will be according to the value on the pin at power-up. For software control, set MASTSLVB pin to Master mode at all times and program the individual registers (as per Value Description) to give Master or Slave mode functionality.	0 1	Slave mode. I11 set to highest priority. T0 DPLL set to acquisition bandwidth. Revertive mode enabled. Phase Build-out disabled. Master mode. I11 priority, T0 DPLL bandwidth, Revertive mode, Phase Build-out, all as programmed in the registers.
0	*reversion_mode* Bit to select Revertive/Non-revertive mode. When in Non-revertive mode, the device will not automatically switch to a higher priority source, unless the current source fails. When in Revertive mode the device will always select the highest priority source.	0 1	Non-revertive mode. Revertive mode.

Address (hex): 35

Register Name	*cnfg_T4_path*	Description	Register to configure the inputs and other features in the T4 path.	Default Value	0100 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
lock_T4_to_T0	*T4_dig_feed-back*		*T4_op_from_T0*	*T4_forced_reference_source*			

Bit No.	Description	Bit Value	Value Description
7	*lock_T4_to_T0* Bit selects either the T4 direct inputs, or T0 DPLL as the input of the T4 path. This allows the T4 DPLL to be used to produce different sets of frequencies to the T0 DPLL but still maintain lock.	0 1	T4 path locks independently from the T0 path. T4 DPLL locks to the output of the T0 DPLL.
6	*T4_dig_feedback* Bit to select digital feedback mode for the T4 DPLL.	0 1	T4 DPLL in analog feedback mode. T4 DPLL in digital feedback mode.
5	Not used.	-	-
4	*T4_op_from_T0*	0 1	T08 and T09 will be generated from T4 DPLL T08 and T09 will be generated from T0 DPLL

Address (hex): 35 (cont...)

Register Name	*cnfg_T4_path*	Description	Register to configure the inputs and other features in the T4 path.	Default Value	0100 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
lock_T4_to_T0	*T4_dig_feed-back*		*T4_op_from_T0*	*T4_forced_reference_source*			

Bit No.	Description	Bit Value	Value Description
[3:0]	*T4_forced_reference_source* This field can be used to force the T4 DPLL to select a particular input. A value of zero in this field allows the T4 input to be selected automatically via the priority and input monitoring functions.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	T4 DPLL automatic source selection. T4 DPLL forced to select input I1. T4 DPLL forced to select input I2. T4 DPLL forced to select input I3. T4 DPLL forced to select input I4. T4 DPLL forced to select input I5. T4 DPLL forced to select input I6. T4 DPLL forced to select input I7. T4 DPLL forced to select input I8. T4 DPLL forced to select input I9. T4 DPLL forced to select input I10. T4 DPLL forced to select input I11. T4 DPLL forced to select input I12. T4 DPLL forced to select input I13. T4 DPLL forced to select input I14. Not used.

Address (hex): 36

Register Name	*cnfg_differential_inputs*	Description	(R/W) Configures the differential inputs to be PECL or LVDS type inputs.	Default Value	0000 0010		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
						I6_PECL	*I5_LVDS*

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
1	*I6_PECL* Configures the I6 input to be compatible with either 3 V LVDS or 3 V PECL electrical levels.	0 1	I6 input LVDS compatible. I6 input PECL compatible (Default).
0	*I5_LVDS* Configures the I5 input to be compatible with either 3 V LVDS or 3 V PECL electrical levels.	0 1	I5 input LVDS compatible (Default). I5 input PECL compatible.

Address (hex): 37

Register Name	*cnfg_uPsel_pins*	Description	(RO) Register reflecting the value on the UPSEL device pins.	Default Value	0000 0010*		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
					upsel_pins_value		

Bit No.	Description	Bit Value	Value Description
[7:3]	Not used.	-	-
[2:0]	*upsel_pins_value* This register always reflects the value present on the UPSEL pins of the device. At reset this is used to set the mode of the microprocessor interface. Following power-up, these pins have no further effect on the microprocessor interface, hence it is possible to use the pins and register combination as a general purpose input for software. *The default of this register is entirely dependent on the value of the pins at reset.	000 001 010 011 100 101 110 111 (value at reset)	Not used. Interface in EPROM boot mode. Interface in Multiplexed mode. Interface in Intel mode. Interface in Motorola mode. Interface in Serial mode. Not used. Not used.

Address (hex): 38

Register Name	*cnfg_dig_outputs_sonsdh*	Description	Configures *Digital1* and *Digital2* output frequencies to be SONET or SDH compatible frequencies.	Default Value	0001 1111*		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	dig2_sonsdh	*dig1_sonsdh*					

Bit No.	Description	Bit Value	Value Description
7	Not used.	-	-
6	*dig2_sonsdh* Selects whether the frequencies generated by the *Digital2* frequency generator are SONET derived or SDH. *Default value of this bit is set by the SONSDHB pin at power-up.	1 0	*Digital2* can be selected from 1544/3088/6176/12352 kHz. *Digital2* can be selected from 2048/4096/8192/16384 kHz.
5	*dig1_sonsdh* Selects whether the frequencies generated by the *Digital1* frequency generator are SONET derived or SDH. *Default value of this bit is set by the SONSDHB pin at power-up.	1 0	*Digital1* can be selected from 1544/3088/6176/12352 kHz. *Digital1* can be selected from 2048/4096/8192/16384 kHz.
[4:0]	Not used.	-	-

Address (hex): 39

Register Name	*cnfg_digtial_frequencies*	Description	(R/W) Configures the actual frequencies of *Digital1* & *Digital2*.	Default Value	0000 1000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
digital2_frequency		*digital1_frequency*					

Bit No.	Description	Bit Value	Value Description
[7:6]	*digital2_frequency* Configures the frequency of *Digital2*. Whether this is SONET or SDH based is configured by Bit 6 (*dig2_sonsdh*) of Reg. 38.	00 01 10 11	*Digital2* set to 1544 kHz or 2048 kHz. *Digital2* set to 3088 kHz or 4096 kHz. *Digital2* set to 6176 kHz or 8192 kHz. *Digital2* set to 12353 kHz or 16384 kHz.
[5:4]	*digital1_frequency* Configures the frequency of *Digital1*. Whether this is SONET or SDH based is configured by Bit 5 (*dig1_sonsdh*) of Reg. 38.	00 01 10 11	*Digital1* set to 1544 kHz or 2048 kHz. *Digital1* set to 3088 kHz or 4096 kHz. *Digital1* set to 6176 kHz or 8192 kHz. *Digital1* set to 12353 kHz or 16384 kHz.
[3:0]	Not used.		

Address (hex): 3A

Register Name	*cnfg_differential_outputs*	Description	(R/W) Configures the electrical compatibility of the differential output drivers to be 3 V PECL or 3 V LVDS.	Default Value	1100 0110

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				TO7_PECL_LVDS		*TO6_LVDS_PECL*	

Bit No.	Description	Bit Value	Value Description
[7:4]	Not used.	-	-
[3:2]	*TO7_PECL_LVDS* Selection of the electrical compatibility of TO7 between 3 V PECL and 3 V LVDS.	00 01 10 11	Output TO7 disabled. Output TO7 3 V PECL compatible. Output TO7 3 V LVDS compatible. Not used.
[1:0]	*TO6_LVDS_PECL* Selection of the electrical compatibility of TO6 between 3 V PECL and 3 V LVDS.	00 01 10 11	Output TO6 disabled. Output TO6 3 V PECL compatible. Output TO6 3 V LVDS compatible. Not used.

Address (hex): 3B

Register Name	*cnfg_auto_bw_sel*	Description	(R/W) Register to select automatic BW selection for the T0 DPLL path	Default Value	1111 1011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
auto_BW_sel				T0_lim_int			

Bit No.	Description	Bit Value	Value Description
7	*auto_BW_sel* Bit to select locked bandwidth (Reg. 67) or acquisition bandwidth (Reg. 69) for the T0 DPLL	1 0	Automatically selects either locked or acquisition bandwidth as appropriate Always selects locked bandwidth
[6:4]	Not used.	-	-
3	T0_lim_int When set to 1 the integral path value of the DPLL is limited or frozen when the DPLL reaches either min or max frequency. This can be used to minimize subsequent overshoot when the DPLL is pulling in. Note that when this happens, the reported frequency value via *current_DPLL_freq* (Reg. 0C, 0D and 07) is also frozen.	1 0	DPLL value frozen DPLL not frozen
[2:0]	Not used.	-	-

Address (hex): 3C

Register Name	*cnfg_nominal_frequency [7:0]*	Description	(R/W) Bits [7:0] of the register used to calibrate the crystal oscillator used to clock the device.	Default Value	1001 1001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
cnfg_nominal_frequency_value[7:0]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*cnfg_nominal_frequency_value[7:0]*	-	See register description of Reg. 3D (*cnfg_nominal_frequency_value[15:8]*).

Address (hex): 3D

Register Name	*cnfg_nominal_frequency [15:8]*	Description	(R/W) Bits [15:8] of the register used to calibrate the crystal oscillator used to clock the device.	Default Value	1001 1001		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
cnfg_nominal_frequency_value[15:8]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*cnfg_nominal_frequency_value[15:8]* This register is used in conjunction with Reg. 3C (*cnfg_nominal_frequency_value[7:0]*) to be able to offset the frequency of the crystal oscillator by up to +514 ppm and –771 ppm. The default value represents 0 ppm offset from 12.800 MHz. This value is an unsigned integer. The value in Reg. 3C/3D is used within the DPLL to offset the frequency value used in the DPLL only. This means that the value programmed will affect the value reported in the *sts_current_DPLL_frequency* (Reg 07/0D/0C). It will also affect the value programmed into *holdover_frequency_value* in the *cnfg_holdover_frequency* register (Reg 3E/3F/40) and the DPLL frequency offset limit programmed into the *cnfg_DPLL_freq_limit* (Reg 41/42). It must be noted, however, that this “calibrated” frequency is NOT used in the frequency monitors affecting Regs 49, 4A, 4C & 4D. These registers (*cnfg_freq_mon_threshold*, *cnfg_current_freq_mon_ threshold*, *sts_freq_measurement*, *cnfg_DPLL_soft_limit*) which all use the uncalibrated crystal frequency. The frequency monitors can also use the clock from the output of the DPLL by programming bit *freq_mon_clock* in *cnfg_monitors* (Reg 48).	-	In order to program the ppm offset of the crystal oscillator frequency, the value in Reg. 3C and Reg. 3D hex need to be concatenated. This value is an unsigned integer. The value multiplied by 0.0196229 dec will give the value in ppm. To calculate the absolute value, the default (39321) needs to be subtracted.

Address (hex): 3E

Register Name	*cnfg_holdover_frequency [7:0]*	Description	(R/W) Bits [7:0] of the manual Holdover frequency register.	Default Value	0000 0000		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
holdover_frequency_value[7:0]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*holdover_frequency_value[7:0]*	-	See Reg. 3F (*cnfg_holdover_frequency*) for details.

Address (hex): 3F

Register Name	*cnfg_holdover_frequency [15:8]*	Description	(R/W) Bits [15:8] of the manual Holdover frequency register.	Default Value	0000 0000		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
holdover_frequency_value[15:8]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*holdover_frequency_value[15:8]* This value in this register is combined with the value in Reg. 3E and Bits [2:0] of Reg. 40 to represent the programmed Holdover frequency of the T0 DPLL. This register is designed such that software can read the *sts_current_DPLL_frequency* register (Reg. 0C, Reg. 0D and Reg. 07) and filter the value. The result will then be in a suitable format to simply write back to the *cnfg_holdover_frequency* register. *This register can be programmed to read back the internally averaged Holdover frequency rather than the programmed value, see Bit 5 of Reg. 40 *cnfg_holdover_modes*.	-	In order to calculate the Holdover ppm offset of the DPLL with respect to the crystal oscillator frequency, the value in Reg. 3E hex and Bits [2:0] of Reg. 40 need to be concatenated. This value is a 2's complement signed integer. The value multiplied by 0.0003068 dec will give the value in ppm.

Address (hex): 40

Register Name	*cnfg_holdover_modes*	Description	(R/W) Register to control the Holdover modes of the T0 DPLL.	Default Value	1000 1000		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
auto_averaging	*fast_averaging*	*read_average*	*mini_holdover_mode*		*holdover_frequency_value [18:16]*		

Bit No.	Description	Bit Value	Value Description
7	*auto_averaging* Bit to enable the use of the averaged frequency value during Holdover. This bit is overridden by the manual Holdover control (Bit 4, *man_holdover*, in Reg. 34).	0 1	Averaged frequency not used, Holdover frequency either manual or instantaneously frozen. Averaged frequency used, providing manual Holdover mode is not engaged.
6	*fast_averaging* Bit to control the rate of averaging of the Holdover frequency. Fast averaging gives a -3db response point of approximately 8 minutes. Slow averaging give a -3db response point of approximately 110 minutes.	0 1	Slow Holdover frequency averaging enabled. Fast Holdover frequency averaging enabled.

Address (hex): 40 (cont...)

Register Name	*cnfg_holdover_modes*	Description	(R/W) Register to control the Holdover modes of the T0 DPLL.	Default Value	1000 1000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
auto_averaging	*fast_averaging*	*read_average*	*mini_holdover_mode*		*holdover_frequency_value [18:16]*		

Bit No.	Description	Bit Value	Value Description
5	*read_average* Bit to control whether the value read from the *holdover_frequency_value* register is the value written to that register, or the averaged Holdover frequency. This allows software to use the internal averager as part of the Holdover algorithm, but use manual Holdover mode plus software to enhance the performance.	0 1	Value read from *holdover_frequency_value* is the value written to it. Value read from a *holdover_frequency_value* is either the fast or slow averaged frequency as determined by *fast_averaging*.
[4:3]	*mini_holdover_mode* Mini-holdover is a term used to describe the state of the DPLL when it is in locked mode, but it has temporarily lost its input. This may be a temporary state, or last for many seconds whilst an input is checked for inactivity. The DPLL behaves exactly as in Holdover, and the frequency can be determined in the same selection of ways (instantaneously, fast averaged or slow averaged).	00 01 10 11	Mini-holdover frequency determined in the same way as for full Holdover mode. Mini-holdover frequency frozen instantaneously. Mini-holdover frequency taken from fast averager. Mini-holdover frequency taken from slow averager.
[2:0]	*holdover_frequency_value [18:16]*	-	See Reg. 3F (*cnfg_holdover_frequency*) for details.

Address (hex): **41**

Register Name	*cnfg_DPLL_freq_limit [7:0]*	Description	(R/W) Bits [7:0] of the DPLL frequency limit register.	Default Value	0111 0110		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DPLL_freq_limit_value[7:0]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*DPLL_freq_limit_value[7:0]* This register defines the extent of frequency offset to which either the T0 or the T4 DPLL will track a source before limiting- i.e. it represents the pull-in range of the DPLLs. The offset of the device is determined by the frequency offset of the DPLL when compared to the offset of the external crystal oscillator clocking the device. If the oscillator is calibrated using *cnfg_nominal_frequency* Reg. 3C and 3D, then this calibration is automatically taken into account. The DPLL frequency limit limits the offset of the DPLL when compared to the calibrated oscillator frequency.	-	In order to calculate the frequency limit in ppm, Bits [1:0] of Reg. 42 and Bits [7:0] of Reg. 41 need to be concatenated. This value is a unsigned integer and represents limit *both* positive and negative in ppm. The value multiplied by 0.078 will give the value in ppm.

Address (hex): **42**

Register Name	*cnfg_DPLL_freq_limit [9:8]*	Description	(R/W) Bits [9:8] of the DPLL frequency limit register.	Default Value	0000 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
						DPLL_freq_limit_value[9:8]	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	*DPLL_freq_limit_value[9:8]*	-	See Reg. 41 (*cnfg_DPLL_freq_limit*) for details.

Address (hex): 43

Register Name	*cnfg_interrupt_mask [7:0]*	Description	(R/W) Bits [7:0] of the interrupt mask register.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I8	*I7*	*I6*	*I5*	*I4*	*I3*	*I2*	*I1*

Bit No.	Description	Bit Value	Value Description
7	*I8* Mask bit for input I8 interrupt.	0 1	Input I8 cannot generate interrupts. Input I8 can generate interrupts.
6	*I7* Mask bit for input I7 interrupt.	0 1	Input I7 cannot generate interrupts. Input I7 can generate interrupts.
5	*I6* Mask bit for input I6 interrupt.	0 1	Input I6 cannot generate interrupts. Input I6 can generate interrupts.
4	*I5* Mask bit for input I5 interrupt.	0 1	Input I5 cannot generate interrupts. Input I5 can generate interrupts.
3	*I4* Mask bit for input I4 interrupt.	0 1	Input I4 cannot generate interrupts. Input I4 can generate interrupts.
2	*I3* Mask bit for input I3 interrupt.	0 1	Input I3 cannot generate interrupts. Input I3 can generate interrupts.
1	*I2* Mask bit for input I2 interrupt.	0 1	Input I2 cannot generate interrupts. Input I2 can generate interrupts.
0	*I1* Mask bit for input I1 interrupt.	0 1	Input I1 cannot generate interrupts. Input I1 can generate interrupts.

Address (hex): 44

Register Name	*cnfg_interrupt_mask [15:8]*	Description	(R/W) Bits [15:8] of the interrupt mask register.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
operating_ mode	*main_ref_failed*	*I14*	*I13*	*I12*	*I11*	*I10*	*I9*

Bit No.	Description	Bit Value	Value Description
7	*operating_mode* Mask bit for *operating_mode* interrupt.	0 1	Operating mode cannot generate interrupts. Operating mode can generate interrupts.
6	*main_ref_failed* Mask bit for *main_ref_failed* interrupt.	0 1	Main reference failure cannot generate interrupts. Main reference failure can generate interrupts.
5	*I14* Mask bit for input I14 interrupt.	0 1	Input I14 cannot generate interrupts. Input I14 can generate interrupts.

Address (hex): 44 (cont...)

Register Name	*cnfg_interrupt_mask [15:8]*	Description	(R/W) Bits [15:8] of the interrupt mask register.	Default Value	0000 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
operating_ mode	*main_ref_failed*	*I14*	*I13*	*I12*	*I11*	*I10*	*I9*

Bit No.	Description	Bit Value	Value Description
4	*I13* Mask bit for input I13 interrupt.	0 1	Input I13 cannot generate interrupts. Input I13 can generate interrupts.
3	*I12* Mask bit for input I12 interrupt.	0 1	Input I12 cannot generate interrupts. Input I12 can generate interrupts.
2	*I11* Mask bit for input I11 interrupt.	0 1	Input I11 cannot generate interrupts. Input I11 can generate interrupts.
1	*I10* Mask bit for input I10 interrupt.	0 1	Input I10 cannot generate interrupts. Input I10 can generate interrupts.
0	*I9* Mask bit for input I9 interrupt.	0 1	Input I9 cannot generate interrupts. Input I9 can generate interrupts.

Address (hex): 45

Register Name	*cnfg_interrupt_mask [23:16]*	Description	(R/W) Bits [23:16] of the interrupt mask register.	Default Value	0000 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Sync_ip_alarm	*T4_status*		*T4_inputs_ failed*	*AMI2_Viol*	*AMI2_LOS*	*AMI1_Viol*	*AMI1_LOS*

Bit No.	Description	Bit Value	Value Description
7	*Sync_ip_alarm* Mask bit for *Sync_ip_alarm* interrupt.	0 1	The external Sync input cannot generate interrupts. The external Sync input can generate interrupts.
6	*T4_status* Mask bit for *T4_status* interrupt.	0 1	Change in T4 status cannot generate interrupts. Change in T4 status can generate interrupts.
5	Not used.	-	-
4	*T4_inputs_failed* Mask bit for *T4_inputs_failed* interrupt.	0 1	Failure of T4 inputs cannot generate interrupts. Failure of T4 inputs can generate interrupts.
3	*AMI2_Viol* Mask bit for *AMI2_Viol* interrupt.	0 1	Input I2 cannot generate AMI violation interrupts. Input I2 can generate AMI violation interrupts.
2	*AMI2_LOS* Mask bit for *AMI2_LOS* interrupt.	0 1	Input I2 cannot generate AMI LOS interrupts. Input I2 can generate AMI LOS interrupts.

Address (hex): 45 (cont...)

Register Name	*cnfg_interrupt_mask [23:16]*	Description	(R/W) Bits [23:16] of the interrupt mask register.	Default Value	0000 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Sync_ip_alarm	*T4_status*		*T4_inputs_ failed*	*AMI2_Viol*	*AMI2_LOS*	*AMI1_Viol*	*AMI1_LOS*

Bit No.	Description	Bit Value	Value Description
1	*AMI1_Viol* Mask bit for *AMI1_Viol* interrupt.	0 1	Input I1 cannot generate AMI violation interrupts. Input I1 can generate AMI violation interrupts.
0	*AMI1_LOS* Mask bit for *AMI1_LOS* interrupt.	0 1	Input I1 cannot generate AMI LOS interrupts. Input I1 can generate AMI LOS interrupts.

Address (hex): 46

Register Name	*cnfg_freq_divn [7:0]*	Description	(R/W) Bits [7:0] of the division factor for inputs using the DivN feature.	Default Value	1111 1111		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
divn_value[7:0]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*divn_value[7:0]*	-	See Reg. 47 (*cnfg_freq_divn*) for details.

Address (hex): 47

Register Name	*cnfg_freq_divn [13:8]*	Description	(R/W) Bits [13:8] of the division factor for inputs using the DivN feature.	Default Value	0011 1111		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		divn_value[13:8]					

Bit No.	Description	Bit Value	Value Description
[7:6]	Not used.	-	-

Address (hex): 47 (cont...)

Register Name	*cnfg_freq_divn [13:8]*	Description	(R/W) Bits [13:8] of the division factor for inputs using the DivN feature.	Default Value	0011 1111		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		divn_value[13:8]					

Bit No.	Description	Bit Value	Value Description
[5:0]	*divn_value[13:8]* This register, in conjunction with Reg. 46 (*cnfg_freq_divn*) represents the integer value by which to divide inputs that use the DivN pre-divider. The divn feature supports input frequencies up to a maximum of 100 MHz; therefore, the maximum value that should be written to this register is 30D3 hex (12499 dec). Use of higher DivN values may result in unreliable behavior.	-	The input frequency will be divided by the value in this register plus 1. i.e. to divide by 8, program a value of 7.

Address (hex): 48

Register Name	*cnfg_monitors*	Description	(R/W) Configuration register controlling several input monitoring and switching options.	Default Value	0000 0101*		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
freq_mon_clk	*los_flag_on_ TDO*	*ultra_fast_ switch*	*ext_switch*	*PBO_freeze*	*PBO_en*	*freq_monitor_ soft_enable*	*freq_monitor_ hard_enable*

Bit No.	Description	Bit Value	Value Description
7	*freq_mon_clk* Bit to select the source of the clock to the frequency monitors to be either from the output clock or directly from the crystal oscillator.	0 1	Frequency monitors clocked by output of T0 DPLL. Frequency monitors clocked by crystal oscillator frequency.
6	*los_flag_on_TDO* Bit to select whether the *main_ref_fail* interrupt from the T0 DPLL is flagged on the TDO pin. If enabled this will not strictly conform to the IEEE 1149.1 JTAG standard for the function of the TDO pin. When enabled the TDO pin will simply mimic the state of the *main_ref_fail* interrupt status bit.	0 1	Normal mode, TDO complies with IEEE 1149.1. TDO pin used to indicate the state of the *main_ref_fail* interrupt status. This allows a system to have a hardware indication of a source failure very rapidly.
5	*ultra_fast_switch* Bit to enable ultra-fast switching mode. When in this mode, the device will disqualify a locked-to source as soon as it detects a few missing input cycles.	0 1	Currently selected source only disqualified by Leaky Bucket or frequency monitors. Currently selected source disqualified after less than 3 missing input cycles.

Address (hex): 48 (cont...)

Register Name	*cnfg_monitors*	Description	(R/W) Configuration register controlling several input monitoring and switching options.	Default Value	0000 0101*		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
freq_mon_clk	*los_flag_on_ TDO*	*ultra_fast_ switch*	*ext_switch*	*PBO_freeze*	*PBO_en*	*freq_monitor_ soft_enable*	*freq_monitor_ hard_enable*

Bit No.	Description	Bit Value	Value Description
4	*ext_switch* Bit to enable external switching mode. When in external switching mode, the device is only allowed to lock to a pair of sources. If the programmed priority of input I3 is non-zero, then the SRCSW pin is *High*, the device will be forced to lock to input I3 regardless of the signal present on that input. If the programmed priority of input I3 is zero, then it will be forced to lock to input I5 instead. If the programmed priority of input I4 is non-zero, then the SRCSW pin is *Low*, the device will be forced to lock to input I4 regardless of the signal present on that input. If the programmed priority of input I4 is zero, then it will be forced to lock to input I6 instead. * The default value of this bit is dependent on the value of the SRCSWIT pin at power-up.	0 1	Normal operation mode. External source switching mode enabled. Operating mode of the device is always forced to be "locked" when in this mode.
3	*PBO_freeze* Bit to control the freezing of Phase Build-out operation. If Phase Build-out has been enabled and there have been some source switches, then the input-output phase relationship of the T0 DPLL is unknown. If Phase Build-out is no longer required, then it can be frozen. This will maintain the current input-output phase relationship, but not allow further Phase Build-out events to take place. Simply disabling Phase Build-out could cause a phase shift in the output, as the T0 DPLL re-locks the phase to zero degrees.	0 1	Phase Build-out not frozen. Phase Build-out frozen, no further Phase Build-out events will occur.
2	*PBO_en* Bit to enable Phase Build-out events on source switching. When enabled a Phase Build-out event is triggered every time the T0 DPLL selects a new source- this includes exiting the Holdover or Free-run states.	0 1	Phase Build-out not enabled. T0 DPLL locks to zero degrees phase. Phase Build-out enabled on source switching.
1	*freq_monitor_soft_enable* Control to enable frequency monitoring of input reference sources using soft frequency alarms.	0 1	Soft frequency monitor alarms disabled. Soft frequency monitor alarms enabled.
0	*freq_monitor_hard_enable* Control to enable frequency monitoring of input reference sources using hard frequency alarms.	0 1	Hard frequency monitor alarms disabled. Hard frequency monitor alarms enabled.

Address (hex): 49

Register Name	*cnfg_freq_mon_threshold*	Description	(R/W) Register to set both the hard and soft frequency alarm limits for the monitors on the input reference sources.	Default Value	0010 0011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
soft_frequency_alarm_threshold				*hard_frequency_alarm_threshold*			

Bit No.	Description	Bit Value	Value Description
[7:4]	*soft_frequency_alarm_threshold* Threshold to trigger the soft frequency alarms in the *sts_reference_sources* registers. This is only used for monitoring.	-	To calculate the limit in ppm, add one to the 4-bit value in the register, and multiply by 3.81 ppm. The limit is symmetrical about zero. A value of 0010 bin corresponds to an alarm limit of ±11.43 ppm.
[3:0]	*hard_frequency_alarm_threshold* Threshold to trigger the hard frequency alarms in the *sts_reference_sources* registers, which can cause a reference source rejection.		To calculate the limit in ppm, add one to the 4-bit value in the register, and multiply by 3.81 ppm. The limit is symmetrical about zero. A value of 0011 bin corresponds to an alarm limit of ±15.24 ppm.

Address (hex): 4A

Register Name	*cnfg_current_freq_mon_threshold*	Description	(R/W) Register to set both the hard and soft frequency alarm limits for the monitors on the currently selected reference source.	Default Value	0010 0011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
current_soft_frequency_alarm_threshold				*current_hard_frequency_alarm_threshold*			

Bit No.	Description	Bit Value	Value Description
[7:4]	*current_soft_frequency_alarm_threshold* Threshold to trigger the soft frequency alarm in the *sts_reference_sources* register applying to the currently selected source.The currently selected source can be monitored for frequency using different limits to all other sources.	-	To calculate the limit in ppm, add one to the 4-bit value in the register, and multiply by 3.81 ppm. The limit is symmetrical about zero. A value of 0010 bin corresponds to an alarm limit of ±11.43 ppm.
[3:0]	*current_hard_frequency_alarm_threshold* Threshold to trigger the hard frequency alarm in the *sts_reference_sources* register applying to the currently selected source.		To calculate the limit in ppm, add one to the 4-bit value in the register, and multiply by 3.81 ppm. The limit is symmetrical about zero. A value of 0011 bin corresponds to an alarm limit of ±15.24 ppm.

Address (hex): 4B

Register Name	*cnfg_registers_source_select*	Description	(R/W) Register to select the source of many of the registers.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			T4_T0_select	*frequency_measurement_channel_select*			

Bit No.	Description	Bit Value	Value Description
[7:5]	Not used.	-	-
4	*T4_T0_select* Bit to select between the T0 and T4 path for: Reg. 0A, 0B (*sts_priority_table)* Reg. 0C, 0D and 07 (*sts_current_DPLL_frequency)* Reg. 18 to 1E (*cnfg_ref_selection_priority*) Reg. 77, 78 (*sts_current_phase)*	0 1	T0 path registers selected. T4 path registers selected.
[3:0]	*frequency_measurement_channel_select* Register to select which input channel the frequency measurement result in Reg. 4C (*sts_freq_measurement*) is taken from.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Not used- refers to no input channel. Frequency measurement taken from input I1. Frequency measurement taken from input I2. Frequency measurement taken from input I3. Frequency measurement taken from input I4. Frequency measurement taken from input I5. Frequency measurement taken from input I6. Frequency measurement taken from input I7. Frequency measurement taken from input I8. Frequency measurement taken from input I9. Frequency measurement taken from input I10. Frequency measurement taken from input I11. Frequency measurement taken from input I12. Frequency measurement taken from input I13. Frequency measurement taken from input I14. Not used- refers to no input channel.

Address (hex): 4C

Register Name	*sts_freq_measurement*	Description	(R/W) Register from which the frequency measurement result can be read.	Default Value	0000 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
freq_measurement_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*freq_measurement_value* This represents the value of the frequency measurement on the channel number selected in Reg. 4B (*cnfg_registers_source_select*). This value will represent the offset in frequency from the clock to the frequency monitors. This can be either the crystal oscillator to the device, or the output of the T0 DPLL as selected in Bit 7 *(freq_mon_clk)* of Reg. 48 *cnfg_monitors.*	-	This is an 8-bit 2's complement signed integer. To calculate the offset in ppm of the selected input channel, this value should be multiplied by 3.81 ppm.

Address (hex): 4D

Register Name	*cnfg_DPLL_soft_limit*	Description	(R/W) Register to program the soft frequency limit of the two DPLLs. Exceeding this limit will have no effect beyond triggering a flag.	Default Value	1000 1110		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
freq_lim_ph_loss	*DPLL_soft_limit_value*						

Bit No.	Description	Bit Value	Value Description
7	*freq_lim_ph_loss* Bit to enable the phase lost indication when the DPLL hits its *hard* frequency limit as programmed in Reg. 41 and Reg. 42 (*cnfg_DPLL_freq_limit*). This results in the DPLL entering the phase lost state any time the DPLL tracks to the extent of its hard limit.	0 1	Phase lost/locked determined normally. Phase lost forced when DPLL tracks to hard limit.
[6:0]	*DPLL_soft_limit_value* Register to program to what extent either of the DPLLs tracks a source before raising its soft frequency alarm flag (Bits 5 and 4 of Reg. 09, *sts_operating*). This offset is compared to the crystal oscillator frequency taking into account any programmed calibration.	-	To calculate the ppm offset multiply this 7-bit value by 0.628 ppm. The limit is symmetrical about zero. A value of 0001110 bin is equivalent to ±8.79 ppm.

Address (hex): 50

Register Name	*cnfg_upper_threshold_0*	Description	(R/W) Register to program the activity alarm setting limit for Leaky Bucket Configuration 0.	Default Value	0000 0110		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
upper_threshold_0_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*upper_threshold_0_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 53 (*cnfg_decay_rate_0*), in which this does not occur, the accumulator is decremented by 1. When the accumulator count reaches the value programmed as the *upper_threshold_0_value,* the Leaky Bucket raises an input inactivity alarm.	-	Value at which the Leaky Bucket will raise an inactivity alarm.

Address (hex): 51

Register Name	*cnfg_lower_threshold_0*	Description	(R/W) Register to program the activity alarm resetting limit for Leaky Bucket Configuration 0.	Default Value	0000 0100		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
lower_threshold_0_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*lower_threshold_0_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 53 (*cnfg_decay_rate_0*), in which this does not occur, the accumulator is decremented by 1. The *lower_threshold_0_value* is the value at which the Leaky Bucket will reset an inactivity alarm.	-	Value at which the Leaky Bucket will reset an inactivity alarm.

Address (hex): 52

Register Name	*cnfg_bucket_size_0*	Description	(R/W) Register to program the maximum size limit for Leaky Bucket Configuration 0.	Default Value	0000 1000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
bucket_size_0_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*bucket_size_0_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 53 (*cnfg_decay_rate_0*), in which this does not occur, the accumulator is decremented by 1. The number in the Bucket cannot exceed the value programmed into this register.	-	Value at which the Leaky Bucket will stop incrementing, even with further inactive periods.

Address (hex): 53

Register Name	*cnfg_decay_rate_0*	Description	(R/W) Register to program the “decay” or “leak” rate for Leaky Bucket Configuration 0.	Default Value	0000 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						decay_rate_0_value	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	*decay_rate_0_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in this register, in which this does not occur, the accumulator is decremented by 1. The Leaky Bucket can be programmed to “leak” or “decay” at the same rate as the “fill” cycle, or effectively at one half, one quarter, or one eighth of the fill rate.	00 01 10 11	Bucket decay rate of 1 every 128 ms. Bucket decay rate of 1 every 256 ms. Bucket decay rate of 1 every 512 ms. Bucket decay rate of 1 every 1024 ms.

Address (hex): 54

Register Name	*cnfg_upper_threshold_1*	Description	(R/W) Register to program the activity alarm setting limit for Leaky Bucket Configuration 1.	Default Value	0000 0110

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
upper_threshold_1_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*upper_threshold_1_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 57 (*cnfg_decay_rate_1*), in which this does not occur, the accumulator is decremented by 1. When the accumulator count reaches the value programmed as the *upper_threshold_1_value,* the Leaky Bucket raises an input inactivity alarm.	-	Value at which the Leaky Bucket will raise an inactivity alarm.

Address (hex): 55

Register Name	*cnfg_lower_threshold_1*	Description	(R/W) Register to program the activity alarm resetting limit for Leaky Bucket Configuration 1.	Default Value	0000 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
lower_threshold_1_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*lower_threshold_1_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 57 (*cnfg_decay_rate_1*), in which this does not occur, the accumulator is decremented by 1. The *lower_threshold_1_value* is the value at which the Leaky Bucket will reset an inactivity alarm.	-	Value at which the Leaky Bucket will reset an inactivity alarm.

Address (hex): 56

Register Name	*cnfg_bucket_size_1*	Description	(R/W) Register to program the maximum size limit for Leaky Bucket Configuration 1.	Default Value	0000 1000		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
bucket_size_1_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*bucket_size_1_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 57 (*cnfg_decay_rate_1*), in which this does not occur, the accumulator is decremented by 1. The number in the Bucket cannot exceed the value programmed into this register.	-	Value at which the Leaky Bucket will stop incrementing, even with further inactive periods.

Address (hex): 57

Register Name	*cnfg_decay_rate_1*	Description	(R/W) Register to program the “decay” or “leak” rate for Leaky Bucket Configuration 1.	Default Value	0000 0001		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						decay_rate_1_value	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	*decay_rate_1_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in this register, in which this does not occur, the accumulator is decremented by 1. The Leaky Bucket can be programmed to “leak” or “decay” at the same rate as the “fill” cycle, or effectively at one half, one quarter, or one eighth of the fill rate.	00 01 10 11	Bucket decay rate of 1 every 128 ms. Bucket decay rate of 1 every 256 ms. Bucket decay rate of 1 every 512 ms. Bucket decay rate of 1 every 1024 ms.

Address (hex): 58

Register Name	*cnfg_upper_threshold_2*	Description	(R/W) Register to program the activity alarm setting limit for Leaky Bucket Configuration 2.	Default Value	0000 0110		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
upper_threshold_2_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*upper_threshold_2_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 5B (*cnfg_decay_rate_2*), in which this does not occur, the accumulator is decremented by 1. When the accumulator count reaches the value programmed as the *upper_threshold_2_value,* the Leaky Bucket raises an input inactivity alarm.	-	Value at which the Leaky Bucket will raise an inactivity alarm.

Address (hex): 59

Register Name	*cnfg_lower_threshold_2*	Description	(R/W) Register to program the activity alarm resetting limit for Leaky Bucket Configuration 2.	Default Value	0000 0100		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
lower_threshold_2_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*lower_threshold_2_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 5B (*cnfg_decay_rate_2*), in which this does not occur, the accumulator is decremented by 1. The *lower_threshold_2_value* is the value at which the Leaky Bucket will reset an inactivity alarm.	-	Value at which the Leaky Bucket will reset an inactivity alarm.

Address (hex): 5A

Register Name	*cnfg_bucket_size_2*	Description	(R/W) Register to program the maximum size limit for Leaky Bucket Configuration 2.	Default Value	0000 1000		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
bucket_size_2_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*bucket_size_2_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 5B (*cnfg_decay_rate_2*), in which this does not occur, the accumulator is decremented by 1. The number in the Bucket cannot exceed the value programmed into this register.	-	Value at which the Leaky Bucket will stop incrementing, even with further inactive periods.

Address (hex): 5B

Register Name	*cnfg_decay_rate_2*	Description	(R/W) Register to program the “decay” or “leak” rate for Leaky Bucket Configuration 2.	Default Value	0000 0001		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						decay_rate_2_value	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	*decay_rate_2_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in this register, in which this does not occur, the accumulator is decremented by 1. The Leaky Bucket can be programmed to “leak” or “decay” at the same rate as the “fill” cycle, or effectively at one half, one quarter, or one eighth of the fill rate.	00 01 10 11	Bucket decay rate of 1 every 128 ms. Bucket decay rate of 1 every 256 ms. Bucket decay rate of 1 every 512 ms. Bucket decay rate of 1 every 1024 ms.

Address (hex): 5C

Register Name	*cnfg_upper_threshold_3*	Description	(R/W) Register to program the activity alarm setting limit for Leaky Bucket Configuration 3.	Default Value	0000 0110

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
upper_threshold_3_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*upper_threshold_3_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 5F (*cnfg_decay_rate_3*), in which this does not occur, the accumulator is decremented by 1. When the accumulator count reaches the value programmed as the *upper_threshold_3_value,* the Leaky Bucket raises an input inactivity alarm.	-	Value at which the Leaky Bucket will raise an inactivity alarm.

Address (hex): 5D

Register Name	*cnfg_lower_threshold_3*	Description	(R/W) Register to program the activity alarm resetting limit for Leaky Bucket Configuration 3.	Default Value	0000 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
lower_threshold_3_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*lower_threshold_3_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 5F (*cnfg_decay_rate_3*), in which this does not occur, the accumulator is decremented by 1. The *lower_threshold_3_value* is the value at which the Leaky Bucket will reset an inactivity alarm.	-	Value at which the Leaky Bucket will reset an inactivity alarm.

Address (hex): 5E

Register Name	*cnfg_bucket_size_3*	Description	(R/W) Register to program the maximum size limit for Leaky Bucket Configuration 3.	Default Value	0000 1000		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
bucket_size_3_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*bucket_size_3_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 5F (*cnfg_decay_rate_3*), in which this does not occur, the accumulator is decremented by 1. The number in the Bucket cannot exceed the value programmed into this register.	-	Value at which the Leaky Bucket will stop incrementing, even with further inactive periods.

Address (hex): 5F

Register Name	*cnfg_decay_rate_3*	Description	(R/W) Register to program the “decay” or “leak” rate for Leaky Bucket Configuration 3.	Default Value	0000 0001		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						decay_rate_3_value	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	*decay_rate_3_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in this register, in which this does not occur, the accumulator is decremented by 1. The Leaky Bucket can be programmed to “leak” or “decay” at the same rate as the “fill” cycle, or effectively at one half, one quarter, or one eighth of the fill rate.	00 01 10 11	Bucket decay rate of 1 every 128 ms. Bucket decay rate of 1 every 256 ms. Bucket decay rate of 1 every 512 ms. Bucket decay rate of 1 every 1024 ms.

Address (hex): 60

Register Name	*cnfg_output_frequency (TO1 & TO2)*	Description	(R/W) Register to configure and enable the frequencies available on outputs TO1 and TO2.	Default Value	1000 0101

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
output_freq_2				*output_freq_1*			

Bit No.	Description	Bit Value	Value Description
[7:4]	*output_freq_2* Configuration of the output frequency available at output TO2. Many of the frequencies available are dependent on the frequencies of the T0 APLL and the T4 APLL. These are configured in Reg. 64 and Reg. 65. For more detail see the detailed section on configuring the output frequencies.	0000	Output disabled.
		0001	2 kHz.
		0010	8 kHz.
		0011	Digital2 (Reg. 39 *cnfg_digital_frequencies*).
		0100	Digital1 (Reg. 39 *cnfg_digital_frequencies*).
		0101	T0 APLL frequency/48.
		0110	T0 APLL frequency/16.
		0111	T0 APLL frequency/12.
		1000	T0 APLL frequency/8.
		1001	T0 APLL frequency/6.
		1010	T0 APLL frequency/4.
		1011	T4 APLL frequency/64.
		1100	T4 APLL frequency/48.
		1101	T4 APLL frequency/16.
		1110	T4 APLL frequency/8.
		1111	T4 APLL frequency/4.
[3:0]	*output_freq_1* Configuration of the output frequency available at output TO1. Many of the frequencies available are dependent on the frequencies of the T0 APLL and the T4 APLL. These are configured in Reg. 64 and Reg. 65. For more detail see the detailed section on configuring the output frequencies.	0000	Output disabled.
		0001	2 kHz.
		0010	8 kHz.
		0011	Digital2 (Reg. 39 *cnfg_digital_frequencies*).
		0100	Digital1 (Reg. 39 *cnfg_digital_frequencies*).
		0101	T0 APLL frequency/48.
		0110	T0 APLL frequency/16.
		0111	T0 APLL frequency/12.
		1000	T0 APLL frequency/8.
		1001	T0 APLL frequency/6.
		1010	T0 APLL frequency/4.
		1011	T4 APLL frequency/64.
		1100	T4 APLL frequency/48.
		1101	T4 APLL frequency/16.
		1110	T4 APLL frequency/8.
		1111	T4 APLL frequency/4.

Address (hex): 61

Register Name	*cnfg_output_frequency (TO3 & TO4)*	Description	(R/W) Register to configure and enable the frequencies available on outputs TO3 and TO4.	Default Value	1000 0110		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
output_freq_4				*output_freq_3*			

Bit No.	Description	Bit Value	Value Description
[7:4]	*output_freq_4* Configuration of the output frequency available at output TO4. Many of the frequencies available are dependent on the frequencies of the T0 APLL and the T4 APLL. These are configured in Reg. 64 and Reg. 65. For more detail see the detailed section on configuring the output frequencies.	0000	Output disabled.
		0001	2 kHz.
		0010	8 kHz.
		0011	Digital2 (Reg. 39 *cnfg_digital_frequencies*).
		0100	Digital1 (Reg. 39 *cnfg_digital_frequencies*).
		0101	T0 APLL frequency/48.
		0110	T0 APLL frequency/16.
		0111	T0 APLL frequency/12.
		1000	T0 APLL frequency/8.
		1001	T0 APLL frequency/6.
		1010	T0 APLL frequency/4.
		1011	T4 APLL frequency/2.
		1100	T4 APLL frequency/48.
		1101	T4 APLL frequency/16.
		1110	T4 APLL frequency/8.
		1111	T4 APLL frequency/4.
[3:0]	*output_freq_3* Configuration of the output frequency available at output TO3. Many of the frequencies available are dependent on the frequencies of the T0 APLL and the T4 APLL. These are configured in Reg. 64 and Reg. 65. For more detail see the detailed section on configuring the output frequencies.	0000	Output disabled.
		0001	2 kHz.
		0010	8 kHz.
		0011	Digital2 (Reg. 39 *cnfg_digital_frequencies*).
		0100	Digital1 (Reg. 39 *cnfg_digital_frequencies*).
		0101	T0 APLL frequency/48.
		0110	T0 APLL frequency/16.
		0111	T0 APLL frequency/12.
		1000	T0 APLL frequency/8.
		1001	T0 APLL frequency/6.
		1010	T0 APLL frequency/4.
		1011	T4 APLL frequency/64.
		1100	T4 APLL frequency/48.
		1101	T4 APLL frequency/16.
		1110	T4 APLL frequency/8.
		1111	T4 APLL frequency/4.

Address (hex): 62

Register Name	*cnfg_output_frequency (TO5 & TO6)*	Description	(R/W) Register to configure and enable the frequencies available on outputs TO5 and TO6.	Default Value	1000 1010		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
output_freq_6				*output_freq_5*			

Bit No.	Description	Bit Value	Value Description
[7:4]	*output_freq_6* Configuration of the output frequency available at output TO6. Many of the frequencies available are dependent on the frequencies of the T0 APLL and the T4 APLL. These are configured in Reg. 64 and Reg. 65. For more detail see the detailed section on configuring the output frequencies.	0000	Output disabled.
		0001	2 kHz.
		0010	8 kHz.
		0011	T0 APLL frequency/2.
		0100	Digital1 (Reg. 39 *cnfg_digital_frequencies*).
		0101	T0 APLL frequency.
		0110	T0 APLL frequency/16.
		0111	T0 APLL frequency/12.
		1000	T0 APLL frequency/8.
		1001	T0 APLL frequency/6.
		1010	T0 APLL frequency/4.
		1011	T4 APLL frequency/64.
		1100	T4 APLL frequency/48.
		1101	T4 APLL frequency/16.
		1110	T4 APLL frequency/8.
		1111	T4 APLL frequency/4.
[3:0]	*output_freq_5* Configuration of the output frequency available at output TO5. Many of the frequencies available are dependent on the frequencies of the T0 APLL and the T4 APLL. These are configured in Reg. 64 and Reg. 65. For more detail see the detailed section on configuring the output frequencies.	0000	Output disabled.
		0001	2 kHz.
		0010	8 kHz.
		0011	Digital2 (Reg. 39 *cnfg_digital_frequencies*).
		0100	Digital1 (Reg. 39 *cnfg_digital_frequencies*).
		0101	T0 APLL frequency/48.
		0110	T0 APLL frequency/16.
		0111	T0 APLL frequency/12.
		1000	T0 APLL frequency/8.
		1001	T0 APLL frequency/6.
		1010	T0 APLL frequency/4.
		1011	T4 APLL frequency/2.
		1100	T4 APLL frequency/48.
		1101	T4 APLL frequency/16.
		1110	T4 APLL frequency/8.
		1111	T4 APLL frequency/4.

Address (hex): 63

Register Name	*cnfg_output_frequency (TO7 to TO11)*	Description	(R/W) Register to configure and enable the frequencies available on outputs TO7 through to TO11.	Default Value	1111 0110

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MFrSync_en	*FrSync_en*	*TO9_en*	*TO8_en*	*output_freq_7*			

Bit No.	Description	Bit Value	Value Description
7	*MFrSync_en* Register bit to enable the 2 kHz Sync output (TO11).	0 1	Output TO11 disabled. Output TO11 enabled.
6	*FrSync_en* Register bit to enable the 8 kHz Sync output (TO10).	0 1	Output TO10 disabled. Output TO10 enabled.
5	*TO9_en* Register bit to enable the BITS output from the TO9.	0 1	Output TO9 disabled. Output TO9 enabled.
4	*TO8_en* Register bit to enable the AMI composite clock output from TO8.	0 1	Output TO8 disabled. Output TO8 enabled.
[3:0]	*output_freq_7* Configuration of the output frequency available at output TO7. Many of the frequencies available are dependent on the frequencies of the T0 APLL and the T4 APLL. These are configured in Reg. 64 and Reg. 65. For more detail see the detailed section on configuring the output frequencies.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Output disabled. 2 kHz. 8 kHz. Digital2 (Reg. 39 *cnfg_digital_frequencies*). T0 APLL frequency/2. T0 APLL frequency/48. T0 APLL frequency/16. T0 APLL frequency/12. T0 APLL frequency/8. T0 APLL frequency/6. T0 APLL frequency/4. T4 APLL frequency/64. T4 APLL frequency/48. T4 APLL frequency/16. T4 APLL frequency/8. T4 APLL frequency/4.

Address (hex): 64

Register Name	*cnfg_T4_DPLL_frequency*	Description	(R/W) Register to configure the T4 DPLL and several other parameters for the T4 path.	Default Value	0000 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Auto_squelch_ T4	*AMI_op_duty*	*T4_op_ SONSDH*		*T4_DPLL_frequency*		

Bit No.	Description	Bit Value	Value Description
7	Not used.	-	-
6	*Auto_squelch_T4* Register bit to automatically squelch the T4 outputs on TO8 and TO9 when the T4 inputs have failed.	0 1	Outputs TO8 and TO9 enabled as in Reg. 63. Outputs TO8 and TO9 disabled when T4 inputs fail.
5	*AMI_op_duty* Register bit to configure whether the composite clock output of TO8 is 50:50 or 5:8 duty cycle.	0 1	TO8 output 50:50 duty cycle. TO8 output 5:8 duty cycle.
4	*T4_op_SONSDH* Register bit to configure the BITS output on TO9 to be either SONET or SDH frequency, only when Reg. 35 Bit 4 = 0, otherwise this bit is ignored and SONET/SDH selection for TO9 is controlled by Reg. 34 Bit 2. Default set by SONSDHB pin - same as Reg. 34 Bit 2.	0 1	TO9 output 2.048 MHz (SDH). TO9 output 1.544 MHz (SONET).
3	Not used.	-	-
[2:0]	*T4_DPLL_frequency* Register to configure the frequency of operation of the DPLL in the T4 path. The frequency of the DPLL will also affect the frequency of the T4 APLL which, in turn, affects the frequencies available at outputs TO1 - TO7 see Reg. 60 - Reg. 63. It is also possible to not use the T4 DPLL at all, but use the T4 APLL to run directly from the T0 DPLL output, see Reg. 65 (*cnfg_T0_DPLL_frequency*). If any frequencies are required from the T4 APLL then the T4 DPLL should not be squelched, as the T4 APLL input is squelched and the T4 APLL will free run.	000 001 010 011 100 101 110 111	T4 DPLL mode = squelched (clock off). T4 DPLL mode = 77.76 MHz (OC-N rates), giving T4 APLL output frequency (before dividers) = 311.04 MHz. T4 DPLL mode = 12E1, giving T4 APLL output frequency (before dividers) = 98.304 MHz. T4 DPLL mode = 16E1, giving T4 APLL output frequency (before dividers) = 131.072 MHz. T4 DPLL mode = 24DS1, giving T4 APLL output frequency (before dividers) = 148.224 MHz. T4 DPLL mode = 16DS1, giving T4 APLL output frequency (before dividers) = 98.816 MHz. T4 DPLL mode = E3, giving T4 APLL output frequency (before dividers) = 274.944 MHz. T4 DPLL mode = DS3, giving T4 APLL output frequency (before dividers) = 178.944 MHz.

Address (hex): 65

Register Name	*cnfg_T0_DPLL_frequency*	Description	(R/W) Register to configure the T0 DPLL and several other parameters for the T0 path.	Default Value	0000 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T4_meas_T0_ph	*T4_APLL_for_T0*	*T0_freq_to_T4_APLL*			*T0_DPLL_frequency*		

Bit No.	Description	Bit Value	Value Description
7	*T4_meas_T0_ph* Register bit to control the feature to use the T4 path to measure phase offset from the T0 path. When enabled the T4 path is disabled and the phase detector is used to measure the phase between the input to the T0 DPLL and the selected T4 input.	0 1	Normal- T4 Path normal operation. T4 DPLL disabled, T4 phase detector used to measure phase between selected T0 input and selected T4 input.
6	*T4_APLL_for_T0* Register bit to select whether the T4 APLL takes its input from the T4 DPLL or the T0 DPLL. If the T0 DPLL is selected then the frequency is controlled by Bits [5:4], *T0_freq_to_T4_APLL*.	0 1	T4 APLL takes its input from the T4 DPLL. T4 APLL takes its input from the T0 DPLL.
[5:4]	*T0_freq_to_T4_APLL* Register to select the T0 frequency driven to the T4 APLL (T0 DPLL mode*) when selected by Bit 6, *T4_APLL_for_T0*; and consequently the APLL output frequency in the T4 path. *Note that this is not the operating frequency of the T0 DPLL itself - which is fixed at outputting 77.76 MHz - but is the multiplied output from the LF Output DFS block. See "PLL Block Diagram" on page 33.	00 01 10 11	T0 DPLL mode = 12E1, giving T4 APLL output frequency (before dividers) = 98.304 MHz. T0 DPLL mode = 16E1, giving T4 APLL output frequency (before dividers) = 131.072 MHz. T0 DPLL mode = 24DS1, giving T4 APLL output frequency (before dividers) = 148.224 MHz. T0 DPLL mode = 16DS1, giving T4 APLL output frequency (before dividers) = 98.816 MHz.
3	Not used.	-	-
[2:0]	*T0_DPLL_frequency* Register to configure the frequency driven to the T0 APLL (T0 DPLL mode*) and consequently the APLL output frequency in the T0 path. This register affects the frequencies available at TO1 - TO7 see Reg. 60 - Reg. 63. *Note that this is not the operating frequency of the T0 DPLL itself - which is fixed at outputting 77.76 MHz - but is the multiplied output from the LF Output DFS block. See "PLL Block Diagram" on page 33.	000 001 010 011 100 101 110 111	T0 DPLL mode = 77.76 MHz, digital feedback, T0 APLL output frequency (before dividers) = 311.04 MHz. T0 DPLL mode = 77.76 MHz, analog feedback, T0 APLL output frequency (before dividers) = 311.04 MHz. T0 DPLL mode = 12E1, giving T0 APLL output frequency (before dividers) = 98.304 MHz. T0 DPLL mode = 16E1, giving T0 APLL output frequency (before dividers) = 131.072 MHz. T0 DPLL mode = 24DS1, giving T0 APLL output frequency (before dividers) = 148.224 MHz. T0 DPLL mode = 16DS1, giving T0 APLL output frequency (before dividers) = 98.816 MHz. Not used. Not used.

Address (hex): 66

Register Name	cnfg_T4_DPLL_bw	Description	(R/W) Register to configure the bandwidth of the T4 DPLL.	Default Value	0000 0000		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						T4_DPLL_bandwidth	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	*T4_DPLL_bandwidth* Register to configure the bandwidth of the T4 DPLL.	00 01 10 11	T4 DPLL 18 Hz bandwidth. T4 DPLL 35 Hz bandwidth. T4 DPLL 70 Hz bandwidth. Not used.

Address (hex): 67

Register Name	cnfg_T0_DPLL_locked_bw	Description	(R/W) Register to configure the bandwidth of the T0 DPLL, when phase locked to an input.	Default Value	0000 1011		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				T0_DPLL_locked_bandwidth			

Bit No.	Description	Bit Value	Value Description
[7:4]	Not used.	-	-
[3:0]	*T0_DPLL_locked_bandwidth* Register to configure the bandwidth of the T0 DPLL when locked to an input reference. Reg. 3B Bit 7 is used to control whether this bandwidth is used all of the time or automatically switched to when phase locked.	1000 1001 1010 1011 1100 1101 1110 1111 0000 0001 All other values	T0 DPLL 0.1 Hz locked bandwidth. T0 DPLL 0.3 Hz locked bandwidth. T0 DPLL 0.6 Hz locked bandwidth. T0 DPLL 1.2 Hz locked bandwidth. T0 DPLL 2.5 Hz locked bandwidth. T0 DPLL 4 Hz locked bandwidth. T0 DPLL 8 Hz locked bandwidth. T0 DPLL 18 Hz locked bandwidth. T0 DPLL 35 Hz locked bandwidth. T0 DPLL 70 Hz locked bandwidth. Not used.

Address (hex): 69

Register Name	*cnfg_T0_DPLL_acq_bw*	Description	(R/W) Register to configure the bandwidth of the T0 DPLL, when not phase locked to an input.	Default Value	0000 1111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				T0_DPLL_acquisition_bandwidth			

Bit No.	Description	Bit Value	Value Description
[7:4]	Not used.	-	-
[3:0]	*T0_DPLL_acquisition_bandwidth* Register to configure the bandwidth of the T0 DPLL when acquiring phase lock on an input reference. Reg. 3B Bit 7 is used to control whether this bandwidth is not used or automatically switched to when not phase locked.	1000 1001 1010 1011 1100 1101 1110 1111 0000 0001 All other values	T0 DPLL 0.1 Hz acquisition bandwidth. T0 DPLL 0.3 Hz acquisition bandwidth. T0 DPLL 0.6 Hz acquisition bandwidth. T0 DPLL 1.2 Hz acquisition bandwidth. T0 DPLL 2.5 Hz acquisition bandwidth. T0 DPLL 4 Hz acquisition bandwidth. T0 DPLL 8 Hz acquisition bandwidth. T0 DPLL 18 Hz acquisition bandwidth. T0 DPLL 35 Hz acquisition bandwidth. T0 DPLL 70 Hz acquisition bandwidth. Not used.

Address (hex): 6A

Register Name	*cnfg_T4_DPLL_damping*	Description	(R/W) Register to configure the damping factor of the T4 DPLL, along with the gain of Phase Detector 2 in some modes.	Default Value	0001 0011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	T4_PD2_gain_alog_8k				*T4_damping*		

Bit No.	Description	Bit Value	Value Description
7	Not used.	-	-
[6:4]	*T4_PD2_gain_alog_8k* Register to control the gain of the Phase Detector 2 when locking to a reference of 8 kHz or less in analog feedback mode. This setting is only used if automatic gain selection is enabled in Reg. 6C Bit 7, *cnfg_T4_DPLL_PD2_gain*.	-	Gain value of the Phase Detector 2 when locking to an 8 kHz reference in analog feedback mode.
3	Not used.	-	-

Address (hex): 6A (cont...)

Register Name	*cnfg_T4_DPLL_damping*	Description	(R/W) Register to configure the damping factor of the T4 DPLL, along with the gain of Phase Detector 2 in some modes.	Default Value	0001 0011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	T4_PD2_gain_alog_8k				*T4_damping*		

Bit No.	Description	Bit Value	Value Description
[2:0]	*T4_damping* Register to configure the damping factor of the T4 DPLL. The bit values corresponds to different damping factors, depending on the bandwidth selected. Damping factor of 5 being the default (011). The Gain Peak for the Damping Factors given in the Value Description (right) are tabulated below.		T4 DPLL damping factor at the following bandwidths frequency selections: 18 Hz / 35 Hz / 70 Hz
		001	1.2 / 1.2 / 1.2
		010	2.5 / 2.5 / 2.5
		011	5 / 5 / 5
		100	5 / 10 / 10
		101	5 / 10 / 20
		000	Not used.
		110	Not used.
		111	Not used.

Damping Factor	Gain Peak
1.2	0.4 dB
2.5	0.2 dB
5	0.1 dB
10	0.06 dB
20	0.03 dB

Address (hex): 6B

Register Name	*cnfg_T0_DPLL_damping*	Description	(R/W) Register to configure the damping factor of the T0 DPLL, along with the gain of the Phase Detector 2 in some modes.	Default Value	0001 0011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	T0_PD2_gain_alog_8k				*T0_damping*		

Bit No.	Description	Bit Value	Value Description
7	Not used.	-	-
[6:4]	*T0_PD2_gain_alog_8k* Register to control the gain of the Phase Detector 2 when locking to a reference of 8 kHz or less in analog feedback mode. This setting is only used if automatic gain selection is enabled in Reg. 6D Bit 7, *cnfg_T0_DPLL_PD2_gain*.	-	Gain value of the Phase Detector 2 when locking to an 8 kHz reference in analog feedback mode.
3	Not used.	-	-

Address (hex): 6B (cont...)

Register Name	*cnfg_T0_DPLL_damping*	Description	(R/W) Register to configure the damping factor of the T0 DPLL, along with the gain of the Phase Detector 2 in some modes.	Default Value	0001 0011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	T0_PD2_gain_alog_8k				*T0_damping*		

Bit No.	Description	Bit Value	Value Description
[2:0]	*T0_damping* Register to configure the damping factor of the T0 DPLL. The bit values corresponds to different damping factors, depending on the bandwidth selected. Damping factor of 5 being the default (011). The Gain Peak for the Damping Factors given in the Value Description (right) are tabulated below.		T0 DPLL damping factor at the following bandwidths frequency selections:

Bit Value	≤4 Hz	8 Hz	18 Hz	35 Hz	70 Hz
001	5	2.5	1.2	1.2	1.2
010	5	5	2.5	2.5	2.5
011	5	5	5	5	5
100	5	5	5	10	10
101	5	5	5	10	20
000	Not used.				
110	Not used.				
111	Not used.				

Damping Factor	Gain Peak
1.2	0.4 dB
2.5	0.2 dB
5	0.1 dB
10	0.06 dB
20	0.03 dB

Address (hex): 6C

Register Name	*cnfg_T4_DPLL_PD2_gain*	Description	(R/W) Register to configure the gain of Phase Detector 2 in some modes for the T4 DPLL.	Default Value	1100 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T4_PD2_gain_ enable	*T4_PD2_gain_alog*				*T4_PD2_gain_digital*		

Bit No.	Description	Bit Value	Value Description
7	*T4_PD2_gain_enable*	0 1	T4 DPLL Phase Detector 2 not used. T4 DPLL Phase Detector 2 gain enabled and choice of gain determined according to the locking mode: - digital feedback mode - analog feedback mode - analog feedback at 8 kHz.

Address (hex): 6C (cont...)

Register Name	*cnfg_T4_DPLL_PD2_gain*	Description	(R/W) Register to configure the gain of Phase Detector 2 in some modes for the T4 DPLL.	Default Value	1100 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T4_PD2_gain_enable	*T4_PD2_gain_alog*				*T4_PD2_gain_digital*		

Bit No.	Description	Bit Value	Value Description
[6:4]	*T4_PD2_gain_alog* Register to control the gain of Phase Detector 2 when locking to a reference, higher than 8 kHz, in analog feedback mode. This setting is not used if automatic gain selection is disabled in Bit 7, *T4_PD2_gain_enable*.	-	Gain value of Phase Detector 2 when locking to a high frequency reference in analog feedback mode.
3	Not used.	-	-
[2:0]	*T4_PD2_gain_digital* Register to control the gain of Phase Detector 2 when locking to a reference in digital feedback mode. This setting is always used if automatic gain selection is disabled in Bit 7, *T4_PD2_gain_enable*.	-	Gain value of Phase Detector 2 when locking to any reference in digital feedback mode.

Address (hex): 6D

Register Name	*cnfg_T0_DPLL_PD2_gain*	Description	(R/W) Register to configure the gain of Phase Detector 2 in some modes for the T0 DPLL.	Default Value	1100 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T0_PD2_gain_enable	*T0_PD2_gain_alog*				*T0_PD2_gain_digital*		

Bit No.	Description	Bit Value	Value Description
7	*T0_PD2_gain_enable*	0 1	T0 DPLL Phase Detector 2 not used. T0 DPLL Phase Detector 2 gain enabled and choice of gain determined according to the locking mode: - digital feedback mode - analog feedback mode - analog feedback at 8 kHz.
[6:4]	*T0_PD2_gain_alog* Register to control the gain of Phase Detector 2 when locking to a reference, higher than 8 kHz, in analog feedback mode. This setting is not used if automatic gain selection is disabled in Bit 7, *T0_PD2_gain_enable*.	-	Gain value of Phase Detector 2 when locking to a high frequency reference in analog feedback mode.
3	Not used.	-	-

Address (hex): 6D (cont...)

Register Name	*cnfg_T0_DPLL_PD2_gain*		Description	(R/W) Register to configure the gain of Phase Detector 2 in some modes for the T0 DPLL.		Default Value	1100 0010
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
T0_PD2_gain_enable	*T0_PD2_gain_alog*				*T0_PD2_gain_digital*		

Bit No.	Description	Bit Value	Value Description
[2:0]	*T0_PD2_gain_digital* Register to control the gain of Phase Detector 2 when locking to a reference in digital feedback mode. This setting is always used if automatic gain selection is disabled in Bit 7, *T0_PD2_gain_enable*.	-	Gain value of Phase Detector 2 when locking to any reference in digital feedback mode.

Address (hex): 70

Register Name	*cnfg_phase_offset [7:0]*		Description	(R/W) Bits [7:0] of the phase offset control register.		Default Value	0000 0000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
phase_offset_value[7:0]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*phase_offset_value[7:0]* Register forming part of the phase offset control.	-	See Reg. 71, *cnfg_phase_offset[15:8]* for more details.

Address (hex): 71

Register Name	*cnfg_phase_offset [15:8]*	Description	(R/W) Bits [15:8] of the phase offset control register.	Default Value	0000 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
phase_offset_value[15:8]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*phase_offset_value[15:8]* Register forming part of the phase offset control. If the phase offset register is written to when the DPLL is locked to an input, then it is possible that some internal signals become out of synchronization. In order to avoid this, the phase offset is automatically "ramped" to the new value. If the phase offset is only ever adjusted when the device is in Holdover, then this is not necessary, and this automatic "ramping" can be disabled, see Reg. 7C, *cnfg_sync_monitor*. This register is ignored and has no affect when Phase Build-out is enabled in either Reg. 48 or Reg. 76.	-	The value in this register is to be concatenated with the contents of Reg. 70 *cnfg_phase_offset[7:0]*. This value is a 16-bit 2's complement signed number. The value multiplied by 6.279 represents the extent of the applied phase offset in picoseconds. The phase offset register is not a control to a "traditional" delay line. This number 6.279 actually represents a fractional portion of the period of an internal 77.76 MHz cycle and can, therefore, be represented more accurately as follows. Each bit value of the register represents the period of the internal 77.76 MHz clock divided by 2^{11}. If, for example, the DPLL is locked to a reference that is +1 ppm in frequency with respect to a perfect oscillator, then the period, and hence the phase offset, will be decreased by 1 ppm. Programming a value of 1024 into the phase offset register will produce a complete inversion of the 77.76 MHz output clock. *Note...The exact period of the internal 77.76 MHz clock is determined by the current state of the DPLL i.e. in Locked mode its accuracy depends on that of the locked to input, in Holdover or Free-run it depends on the accuracy of the external oscillator.*

Address (hex): 72

Register Name	*cnfg_PBO_phase_offset*	Description	(R/W) Register to offset the mean time error of Phase Build-out events.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		PBO_phase_offset					

Bit No.	Description	Bit Value	Value Description
[7:6]	Not used.	-	-
[5:0]	*PBO_phase_offset* Each time a Phase Build-out event is triggered, there is an uncertainty of up to 5 ns introduced which translates to a phase hit on the output. The mean error over a large number of events is designed to be zero. This register can be used to introduce a fixed offset into each PBO event. This will have the effect of moving the mean error positive or negative in time.	-	The value in this register is a 6-bit 2's complement number. The value multiplied by 0.101 gives the programmed offset in nanoseconds. Values greater than +1.4 ns or less than -1.4 ns should NOT be used as they may cause internal mathematical errors.

Address (hex): 73

Register Name	*cnfg_phase_loss_fine_limit*	Description	(R/W) Register to configure some of the parameters of the T0 DPLL phase detector.	Default Value	1010 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
fine_limit_en	*noact_ph_loss*	*narrow_en*			*phase_loss_fine_limit*		

Bit No.	Description	Bit Value	Value Description
7	*fine_limit_en* Register bit to enable the *phase_loss_fine_limit* Bits [2:0]. When disabled, phase lock/loss is determined by the other means within the device. This must be disabled when multi-UI jitter tolerance is required, see Reg. 74, *cnfg_phase_loss_course_limit*.	0 1	Phase loss indication only triggered by other means. Phase loss triggered when phase error exceeds the limit programmed in *phase_loss_fine_limit*, Bits [2:0].
6	*noact_ph_loss* The DPLL detects that an input has failed very rapidly. Normally, when the DPLL detects this condition, it does not consider phase lock to be lost and will phase lock to the nearest edge (±180º) when a source becomes available again, hence giving tolerance to missing cycles. If phase loss is indicated, then frequency and phase locking is instigated (±360º locking). This bit can be used to force the DPLL to indicate phase loss immediately when no activity is detected.	0 1	No activity on reference does not trigger phase lost indication. No activity triggers phase lost indication.

Address (hex): 73 (cont...)

Register Name	*cnfg_phase_loss_fine_limit*	Description	(R/W) Register to configure some of the parameters of the T0 DPLL phase detector.	Default Value	1010 0010		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
fine_limit_en	*noact_ph_loss*	*narrow_en*			*phase_loss_fine_limit*		

Bit No.	Description	Bit Value	Value Description
5	*narrow_en* (test control bit) Set to 1 (default value)	0 1	 Set to 1
[4:3]	Not used.	-	-
[2:0]	*phase_loss_fine_limit* When enabled by Bit 7, this register coarsely sets the phase limit at which the device indicates phase lost or locked. The default value of 2 (010) gives a window size of around ±(90º to 180º). The phase position of the inputs to the DPLL has to be within the window limit for 1 to 2 seconds before the device indicates phase lock. If it is outside the window for any time then phase loss is immediately indicated. For most cases the default value of 2 (010) is satisfactory. The window size changes in proportion to the value, so a value of 1 (001) will give a narrow phase acceptance or lock window of approximately ±(45º to 90º).	000 001 010 011 100 101 110 111	Do not use. Indicates phase loss continuously. Small phase window for phase lock indication. Recommended value.))) Larger phase window for phase lock indication.))

Address (hex): 74

Register Name	*cnfg_phase_loss_coarse_limit*	Description	(R/W) Register to configure some of the parameters of the T0 DPLL phase detector.	Default Value	1000 0101		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
coarse_lim-phaseloss_en	*wide_range_en*	*multi_ph_resp*		*phase_loss_coarse_limit*			

Bit No.	Description	Bit Value	Value Description
7	*coarse_lim_phaseloss_en* Register bit to enable the coarse phase detector, whose range is determined by *phase_loss_coarse_limit* Bits [3:0]. This register sets the limit in the number of input clock cycles (UI) that the input phase can move by before the DPLL indicates phase lost.	0 1	Phase loss not triggered by the coarse phase lock detector. Phase loss triggered when phase error exceeds the limit programmed in *phase_loss_coarse_limit*, Bits [3:0].

Address (hex): 74 (cont...)

Register Name	*cnfg_phase_loss_coarse_limit*	Description	(R/W) Register to configure some of the parameters of the T0 DPLL phase detector.	Default Value	1000 0101		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
coarse_lim-phaseloss_en	*wide_range_en*	*multi_ph_resp*		*phase_loss_coarse_limit*			

Bit No.	Description	Bit Value	Value Description
6	*wide_range_en* To enable the device to be tolerant to large amounts of applied jitter and still do direct phase locking at the input frequency rate (up to 77.76 MHz), a wide range phase detector and phase lock detector is employed. This bit enables the wide range phase detector. This allows the device to be tolerant to, and therefore keep track of, drifts in input phase of many cycles (UI). The range of the phase detector is set by the same register used for the phase loss coarse limit (Bits [3:0]).	0 1	Wide range phase detector off. Wide range phase detector on.
5	*multi_ph_resp* Enables the phase result from the coarse phase detector to be used in the DPLL algorithm. Bit 6 should also be set when this is activated. The coarse phase detector can measure and keep track over many thousands of input cycles, thus allowing excellent jitter and wander tolerance. This bit enables that phase result to be used in the DPLL algorithm, so that a large phase measurement gives a faster pull-in of the DPLL. If this bit is not set then the phase measurement is limited to ±360º which can give a slower pull-in rate at higher input frequencies, but could also be used to give less overshoot. Setting this bit in direct locking mode, for example with a 19.44 MHz input, would give the same dynamic response as a 19.44 MHz input used with 8 k locking mode, where the input is divided down internally to 8 kHz first.	0 1	DPLL phase detector limited to ±360º (±1 UI). However it will still remember its original phase position over many thousands of UI if Bit 6 is set. DPLL phase detector also uses the full coarse phase detector result. It can now measure up to: ±360º X 8191 UI = ±2,948,760º.
4	Not used.	-	-

Address (hex): 74 (cont...)

Register Name	*cnfg_phase_loss_coarse_limit*	Description	(R/W) Register to configure some of the parameters of the T0 DPLL phase detector.	Default Value	1000 0101		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
coarse_lim-phaseloss_en	*wide_range_en*	*multi_ph_resp*		*phase_loss_coarse_limit*			

Bit No.	Description	Bit Value	Value Description
[3:0]	*phase_loss_coarse_limit* Sets the range of the coarse phase loss detector and the coarse phase detector. When locking to a high frequency signal, and jitter tolerance greater than 0.5 UI is required, then the DPLL can be configured to track phase errors over many input clock periods. This is particularly useful with very low bandwidths. This register configures how many UI over which the input phase can be tracked. It also sets the range of the coarse phase loss detector, which can be used with or without the multi-UI phase capture range capability. This register value is used by Bits 6 and 7.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100-1111	Input phase error tracked over ±1 UI. Input phase error tracked over ±3 UI. Input phase error tracked over ±7 UI. Input phase error tracked over ±15 UI. Input phase error tracked over ±31 UI. Input phase error tracked over ±63 UI. Input phase error tracked over ±127 UI. Input phase error tracked over ±255 UI. Input phase error tracked over ±511 UI. Input phase error tracked over ±1023 UI. Input phase error tracked over ±2047 UI. Input phase error tracked over ±4095 UI. Input phase error tracked over ±8191 UI.

Address (hex): 76

Register Name	*cnfg_phasemon*	Description	(R/W) Register to configure the noise rejection function for low frequency inputs.	Default Value	0000 0110		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ip_noise_ window							

Bit No.	Description	Bit Value	Value Description
7	*ip_noise_window* Register bit to enable a window of 5% tolerance around low-frequency inputs (2, 4 and 8 kHz). This feature ensures that any edge caused by noise outside the 5% window where the edge is expected will not be considered within the DPLL. This reduces any possible phase hit when a low-frequency connection is removed and contact bounce is possible.	0 1	DPLL considers all edges for phase locking. DPLL ignores input edges outside a 95% to 105% window.
[6:0]	Not used.	-	-

Address (hex): 77

Register Name	*sts_current_phase [7:0]*	Description	(RO) Bits [7:0] of the current phase register.	Default Value	0000 0000		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
current_phase[7:0]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*current_phase* Bits [7:0] of the current phase register. See Reg. 78 *sts_current_phase [15:8]* for details.	-	See Reg. 78 *sts_current_phase [15:8]* for details.

Address (hex): 78

Register Name	*sts_current_phase [15:8]*	Description	(RO) Bits [15:8] of the current phase register.	Default Value	0000 0000		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
current_phase[15:8]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*current_phase* Bits [15:8] of the current phase register. This register is used to read either from the phase detector of either the T0 DPLL or the T4 DPLL, according to Reg. 4B Bit 4 *T4_T0_select*. The value is averaged in the phase averager before being made available.	-	The value in this register should be concatenated with the value in Reg. 77 *sts_current_phase [7:0]*. This 16-bit value is a 2's complement signed integer. The value multiplied by 0.707 is the averaged value of the current phase error, in degrees, as measured at the DPLL's phase detector.

Address (hex): 79

Register Name	*cnfg_phase_alarm_timeout*	Description	(R/W) Register to configure how long before a phase alarm is raised on an input	Default Value	0011 0010		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		timeout_value					

Bit No.	Description	Bit Value	Value Description
[7:6]	Not used.	-	-

Address (hex): 79 (cont...)

Register Name	*cnfg_phase_alarm_timeout*	Description	(R/W) Register to configure how long before a phase alarm is raised on an input	Default Value	0011 0010		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		timeout_value					

Bit No.	Description	Bit Value	Value Description
[5:0]	*timeout_value* Phase alarms can only be raised on an input when the T0 DPLL is attempting to lock to it. Once an input has been rejected due to a phase alarm, there is no way to measure whether it is good again, because it is no longer selected by the DPLL. The phase alarms can either remain until reset by software, or time-out after 128 second, as selected in Reg. 34 Bit 6, *phalarm_timeout*	-	This 6-bit unsigned integer represents the length of time before a phase alarm will be raised on an input. The value multiplied by 2 gives the time in seconds. This time value is the time that the controlling state machine will spend in Pre-locked, Pre-locked2 or Phase-lost modes before setting the phase alarm on the selected input.

Address (hex): 7A

Register Name	*cnfg_sync_pulses*	Description	(R/W) Register to configure the Sync outputs available from TO10 and TO11 and select the source for the 2 kHz and 8 kHz outputs from T01 - TO7.	Default Value	0000 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
2k_8k_from_T4				*8k_invert*	*8k_pulse*	*2k_invert*	*2k_pulse*

Bit No.	Description	Bit Value	Value Description
7	*2k_8k_from_T4* Register to select the source (T0 or T4) for the 2 kHz and 8 kHz outputs available from TO1 to TO7.	0 1	2/8 kHz on TO1-TO7 generated from the T0 DPLL. 2/8 kHz on TO1-TO7 generated from the T4 DPLL.
[6:4]	Not used.	-	-
3	*8k_invert* Register bit to invert the 8 kHz output from TO10.	0 1	8 kHz TO10 output not inverted. 8 kHz TO10 output inverted.
2	*8k_pulse* Register bit to enable the 8 kHz output from TO10 to be either pulsed or 50:50 duty cycle. Output TO3 must be enabled to use "pulsed output" mode on output TO10, and then the pulse width on TO10 will be defined by the period of the output programmed on TO3.	0 1	8 kHz TO10 output not pulsed. 8 kHz TO10 output pulsed.
1	*2k_invert* Register bit to invert the 2 kHz output from TO11.	0 1	2 kHz TO11 output not inverted. 2 kHz TO11 output inverted.

Address (hex): 7A (cont...)

Register Name	*cnfg_sync_pulses*	Description	(R/W) Register to configure the Sync outputs available from TO10 and TO11 and select the source for the 2 kHz and 8 kHz outputs from T01 - TO7.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2k_8k_from_T4				*8k_invert*	*8k_pulse*	*2k_invert*	*2k_pulse*

Bit No.	Description	Bit Value	Value Description
0	*2k_pulse* Register bit to enable the 2 kHz output from TO11 to be either pulsed or 50:50 duty cycle. Output TO3 must be enabled to use "pulsed output" mode on output TO10, and then the pulse width on TO11 will be defined by the period of the output programmed on TO3.	0 1	2 kHz TO11 output not pulsed. 2 kHz TO11 output pulsed.

Address (hex): 7B

Register Name	*cnfg_sync_phase*	Description	(R/W) Register to configure the behavior of the synchronization for the external frame reference.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
indep_FrSync/ MFrSync	*Sync_OC-N_ rates*					*Sync_phase*	

Bit No.	Description	Bit Value	Value Description
7	*indep_FrSync/MFrSync* This allows the option of either maintaining alignment of FrSync and other clock outputs during synchronization from the SYNC2K input, or whether to not maintain alignment to all clocks and so not disturb any of the output clocks	0 1	MFrSync & FrSync outputs are always aligned with other output clocks. MFrSync & FrSync outputs are independent of other output clocks.
6	Sync_OC-N_rates This allows the SYNC2K input to synchronize the OC-3 derived clocks in order to maintain alignment between the FrSync output and output clocks and allow a finer sampling precision of the SYNC2K input of either 19.44 MHz or 38.88 MHz.	0 1	The OC-N rate clocks are not affected by the SYNC2K input. The SYNC2K input is sampled with a 6.48 MHz precision. 6.48MHz should be provided as the input reference clock. Allows the SYNC2K to operate with a 19.44 MHz or 38.88 MHz input clock reference. Input sampling and output alignment to 19.44 MHz is used when the current clock input is 19.44 MHz, otherwise 38.88 MHz sampling precision is used.
[5:2]	Not used.		

Address (hex): 7B (cont...)

Register Name	*cnfg_sync_phase*	Description	(R/W) Register to configure the behavior of the synchronization for the external frame reference.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
indep_FrSync/ MFrSync	*Sync_OC-N_ rates*					*Sync_phase*	

Bit No.	Description	Bit Value	Value Description
[1:0]	*Sync_phase* Register to control the sampling of the external Sync input. Nominally the falling edge of the input is aligned with the falling edge of the reference clock. The margin is ±0.5 U.I. (Unit Interval).	00 01 10 11	On target. 0.5 U.I. early 1 U.I. late 0.5 U.I. late.

Address (hex): 7C

Register Name	*cnfg_sync_monitor*	Description	(R/W) Register to configure the external Sync input monitor. It also has a bit to control the phase offset automatic ramping feature.	Default Value	0010 1011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ph_offset_ramp	*Sync_monitor_limit*			*Sync_reference_source*			

Bit No.	Description	Bit Value	Value Description
7	*ph_offset_ramp* Register bit to force an internal phase offset calibration, see Reg. 71, *Cnfg_Phase_Offset.* The calibration routine is transparent to the outside and puts the device in holdover while it internally ramps the phase offset to zero, resets all internal output and feedback dividers and then ramps the phase offset to the current programmed value from Reg. 70 or 71., holdover is then turned off. All this is transparent to the outside with no change in output phase offset visible.	0 1	Phase offset automatically ramped from the old value to the new value when there is a change in Reg. 70 or 71. Start phase offset internal calibration routine. This bit is reset to 0 when this is complete.
[6:4]	*Sync_monitor_limit* An alternative to allowing the external Sync input to synchronize the outputs, is to use the Sync monitor block to alarm when the external Sync input does not align with the output within a certain number of input clock cycles. This register defines the limit in UI of the selected reference source. If the alignment does not occur within this limit, then Sync alarm will be raised, see Reg. 09 Bit 7.	000 001 010 011 100 101 110 111	Sync alarm raised beyond ±1 UI. Sync alarm raised beyond ±2 UI. Sync alarm raised beyond ±3 UI. Sync alarm raised beyond ±4 UI. Sync alarm raised beyond ±5 UI. Sync alarm raised beyond ±6 UI. Sync alarm raised beyond ±7 UI. Sync alarm raised beyond ±8 UI.

Address (hex): 7C (cont...)

Register Name	*cnfg_sync_monitor*	Description	(R/W) Register to configure the external Sync input monitor. It also has a bit to control the phase offset automatic ramping feature.	Default Value	0010 1011		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
ph_offset_ramp	*Sync_monitor_limit*			*Sync_reference_source*			

Bit No.	Description	Bit Value	Value Description
[3:0]	*Sync_reference_source* The external Sync reference can only be associated with a particular input reference. When automatic external Sync enabling is selected in Reg. 34 Bit 7, the external Sync input will only be enabled when locked to the selected source. This can be used to associate the Frame Sync reference with a reference clock for Master/Slave operation.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Not used. External Sync associated with input I1. External Sync associated with input I2. External Sync associated with input I3. External Sync associated with input I4. External Sync associated with input I5. External Sync associated with input I6. External Sync associated with input I7. External Sync associated with input I8. External Sync associated with input I9. External Sync associated with input I10. External Sync associated with input I11. External Sync associated with input I12. External Sync associated with input I13. External Sync associated with input I14. Not used.

Address (hex): 7D

Register Name	*cnfg_interrupt*	Description	(R/W) Register to configure interrupt output.	Default Value	0000 0010		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
					GPO_en	*tristate_en*	*int_polarity*

Bit No.	Description	Bit Value	Value Description
[7:3]	Not used.	-	-
2	*GPO_en* (Interrupt General Purpose Output). If the interrupt output pin is not required, then setting this bit will allow the pin to be used as a general purpose output. The pin will be driven to the state of the polarity control bit, *int_polarity*.	0 1	Interrupt output pin used for interrupts. Interrupt output pin used for GPO purpose.
1	*tristate_en* The interrupt can be configured to be either connected directly to a processor, or wired together with other sources.	0 1	Interrupt pin always driven when inactive. Interrupt pin only driven when active, High-impedance when inactive.

Address (hex): 7D (cont...)

Register Name	*cnfg_interrupt*		Description	(R/W) Register to configure interrupt output.		Default Value	0000 0010
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
					GPO_en	*tristate_en*	*int_polarity*

Bit No.	Description	Bit Value	Value Description
0	*int_polarity* The interrupt pin can be configured to be active *High* or *Low*.	0 1	Active *Low* - pin driven *Low* to indicate active interrupt. Active *High* - pin driven *High* to indicate active interrupt.

Address (hex): 7E

Register Name	*cnfg_protection*		Description	(R/W) Protection register to protect against erroneous software writes.		Default Value	1000 0101
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
protection_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*protection_value* This register can be used to ensure that the software writes a specific value to this register, before being able to modify any other register in the device. Three modes of protection are offered, (i) protected (ii) fully unprotected (iii) single unprotected. When protected, no other register in the device can be written to. When fully unprotected, any writeable register in the device can be written to. When single unprotected, only one register can be written before the device automatically re-protects itself.	0000 0000 – 1000 0100 1000 0101 1000 0110 1000 0111 – 1111 1111	Protected mode. Fully unprotected. Single unprotected. Protected mode.

Address (hex): 7F

Register Name	*cnfg_uPsel*	Description	(R/W)* Register reflecting the value on the UPSEL device pins following reset, and writeable in EPROM mode.	Default Value	0000 0000**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					upsel_value		

Bit No.	Description	Bit Value	Value Description
[7:3]	Not used.	-	-
[2:0]	*upsel_value* This register defaults to reflecting the value present on the UPSEL pins of the device at reset. At reset this is used to set the mode of the microprocessor interface. Following power-up, these pins have no further effect on the microprocessor interface. *In order that the device can be "booted" from an EPROM and subsequently communicate with a processor, this register is programmable in EPROM mode. The value programmed in location 7F of the EPROM will be the value loaded into this register. **The default of this register is entirely dependent on the value of the pins at reset.	000 001 010 011 100 101 110 111 (value at reset)	Not used. Interface in EPROM boot mode. Interface in Multiplexed mode. Interface in Intel mode. Interface in Motorola mode. Interface in Serial mode. Not used. Not used.

JTAG

The JTAG connections on the ACS8520 allow a full boundary scan to be made. The JTAG implementation is fully compliant to IEEE 1149.1[5], with the following minor exceptions, and the user should refer to the standard for further information.

1. The output boundary scan cells do not capture data from the core, and so do not support INTEST. However this does not affect board testing.
2. In common with some other manufacturers, pin TRST is internally pulled *Low* to disable JTAG by default. The standard is to pull *High*. The polarity of TRST is as the standard: TRST *High* to enable JTAG boundary scan mode, TRST *Low* for normal operation.

The JTAG timing diagram is shown in Figure 22.

Over-voltage Protection

The ACS8520 may require Over-Voltage Protection on input reference clock ports according to ITU recommendation K.41[16]. Semtech protection devices are recommended for this purpose (see separate Semtech data book).

ESD Protection

Suitable precautions should be taken to protect against electrostatic damage during handling and assembly. This device incorporates ESD protection structures that protect the device against ESD damage at ESD input levels up to at least ±2 kV using the Human Body Model (HBD) MIL-STD-883D Method 3015.7, for all pins except pins 24, 25, 26 and 27 (AMI I/Os) which are protected up to at least ±1 kV.

Latchup Protection

This device is protected against latchup for input current pulses of magnitude up to at least ±100 mA to JEDEC Standard No. 78 August 1997.

Figure 22 JTAG Timing

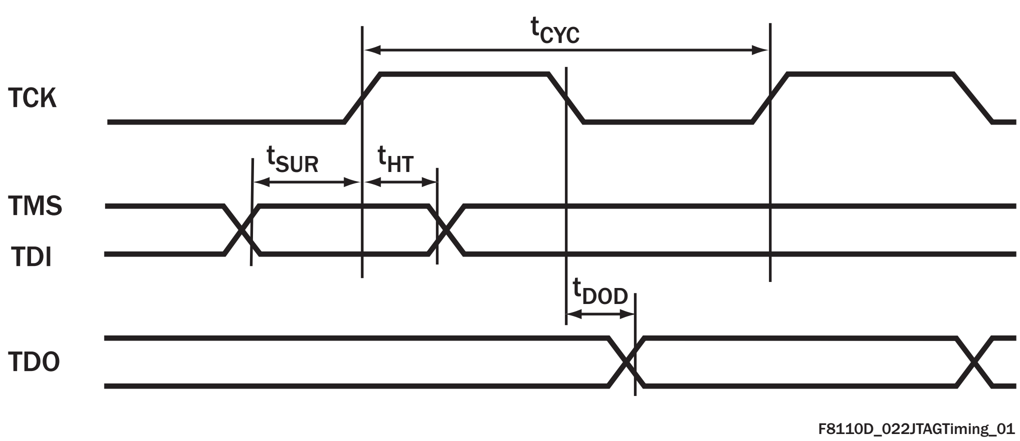


Table 31 JTAG Timing (for use with Figure 22)

Parameter	Symbol	Minimum	Typical	Maximum	Units
Cycle Time	t_{CYC}	50	-	-	ns
TMS/TDI to TCK rising edge time	t_{SUR}	3	-	-	ns
TCK rising to TMS/TDI hold time	t_{HT}	23	-	-	ns
TCK falling to TDO valid	t_{DOD}	-	-	5	ns

Maximum Ratings

Important Note: The Absolute Maximum Ratings, Table 32, are stress ratings only, and functional operation of the device at conditions other than those indicated in the Operating Conditions sections of this specification are not implied. Exposure to the absolute maximum ratings for an extended period may reduce the reliability or useful lifetime of the product.

Table 32 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage VDDa, VDDb, VDDc, VDDd, VD1+, VD2+, VD3+, VA1+, VA2+, VA3+, VAMI+, VDD_DIFFa, VDD_DIFFb	V_{DD}	-0.5	3.6	V
Power Supply (DC voltage) VDD5	V_{DD5}	-	5.5	V
Input Voltage (non-supply pins)	V_{IN}	-	5.5	V
Output Voltage (non-supply pins)	V_{OUT}	-	5.5	V
Ambient Operating Temperature Range	T_A	-40	+85	^oC
Storage Temperature	T_{STOR}	-50	+150	^oC

Operating Conditions

Table 33 Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supply (dc voltage) VDDa, VDDb, VDDc, VDDd, VD1+, VD2+, VD3+, VA1+, VA2+, VA3+, VAMI+, VDD_DIFFa, VDD_DIFFb	V_{DD}	3.0	3.3	3.6	V
Power Supply (DC voltage) VDD5	V_{DD5}	3.0	3.3/5.0	5.5	V
Ambient Temperature Range	T_A	-40	-	+85	^oC
Supply Current (Typical - one 19 MHz output)	I_{DD}	-	130	222	mA
Total Power Dissipation	P_{TOT}	-	430	800	mW

DC Characteristics

Table 34 DC Characteristics: TTL Input Port

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{IN} *High*	V_{IH}	2	-	-	V
V_{IN} *Low*	V_{IL}	-	-	0.8	V
Input Current	I_{IN}	-	-	10	µA

Table 35 DC Characteristics: TTL Input Port with Internal Pull-up

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{IN} *High*	V_{IH}	2	-	-	V
V_{IN} *Low*	V_{IL}	-	-	0.8	V
Pull-up Resistor	PU	25	-	90	kΩ
Input Current	I_{IN}	-	-	120	μA

Table 36 DC Characteristics: TTL Input Port with Internal Pull-down

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{IN} *High*	V_{IH}	2	-	-	V
V_{IN} *Low*	V_{IL}	-	-	0.8	V
Pull-down Resistor	PD	25	-	90	kΩ
Input Current	I_{IN}	-	-	120	μA

Table 37 DC Characteristics: TTL Output Port

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{OUT} *Low* (I_{OL} = 4mA)	V_{OL}	0	-	0.4	V
V_{OUT} *High* (I_{OH} = 4mA)	V_{OH}	2.4	-	-	V
Drive Current	I_D	-	-	4	mA

Table 38 DC Characteristics: PECL Input/Output Port

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
PECL Input *Low* Voltage Differential Inputs (Note ii)	V_{ILPECL}	V_{DD}-2.5	-	V_{DD}-0.5	V
PECL Input *High* Voltage Differential Inputs (Note ii)	V_{IHPECL}	V_{DD}-2.4	-	V_{DD}-0.4	V
Input Differential Voltage	V_{IDPECL}	0.1	-	1.4	V
PECL Input *Low* Voltage Single-ended Input (Note iii)	V_{ILPECL_S}	V_{DD}-2.4	-	V_{DD}-1.5	V

Table 38 DC Characteristics: PECL Input/Output Port (cont...)

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
PECL Input *High* Voltage Single-ended Input (Note iii)	V_{ILPECL_S}	V_{DD}-1.3	-	V_{DD}-0.5	V
Input *High* Current Input Differential Voltage V_{ID} = 1.4V	I_{IHPECL}	-10	-	+10	µA
Input *Low* Current Input Differential Voltage V_{ID} = 1.4V	I_{ILPECL}	-10	-	+10	µA
PECL Output *Low* Voltage (Note iv)	V_{OLPECL}	V_{DD}-2.10	-	V_{DD}-1.62	V
PECL Output *High* Voltage (Note iv)	V_{OHPECL}	V_{DD}-1.25	-	V_{DD}-0.88	V
PECL Output Differential Voltage (Note iv)	V_{ODPECL}	580	-	900	mV

Notes: (i) *Unused differential input ports should be left floating and set in LVDS mode, or the positive and negative inputs tied to V_{DD} and GND respectively.*

(ii) *Assuming a differential input voltage of at least 100 mV.*

(iii) *Unused differential input terminated to V_{DD} -1.4 V.*

(iv) *With 50 Ω load on each pin to V_{DD} -2 V, i.e. 82 Ω to GND and 130 Ω to V_{DD}.*

Figure 23 Recommended Line Termination for PECL Input/Output Ports

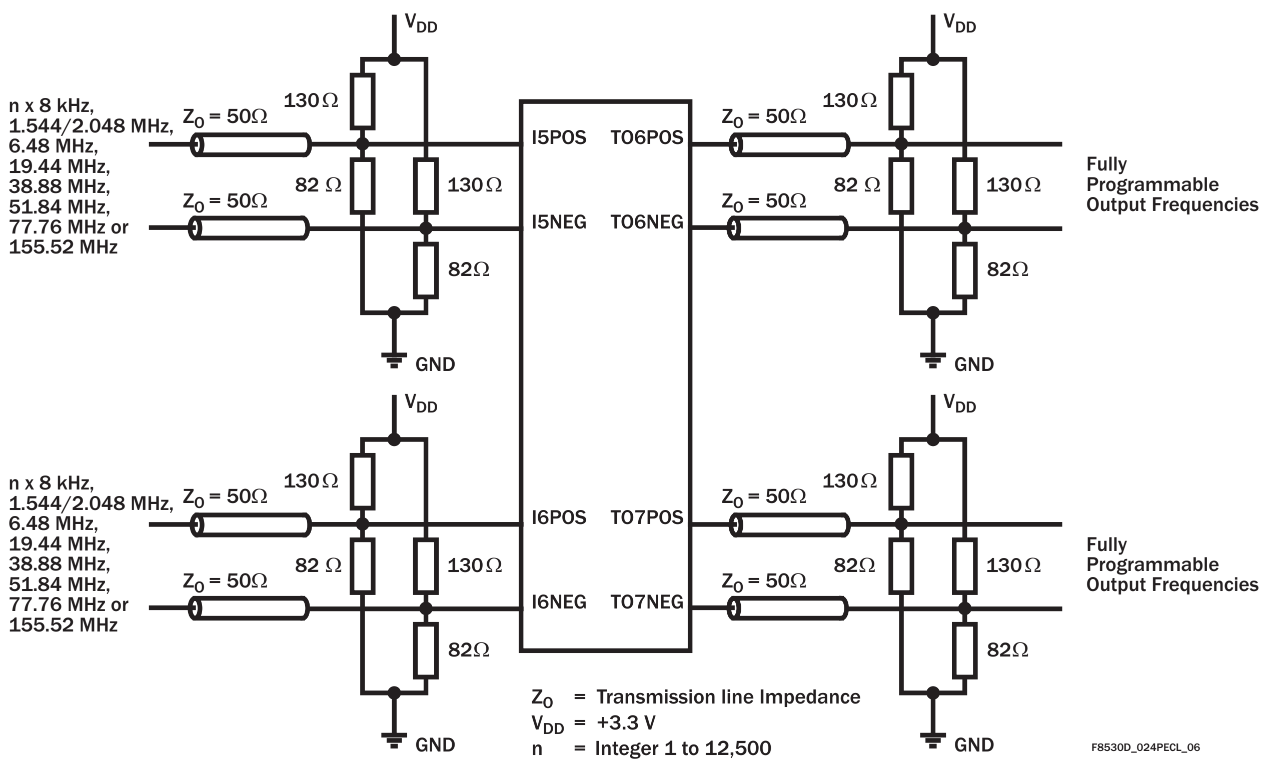


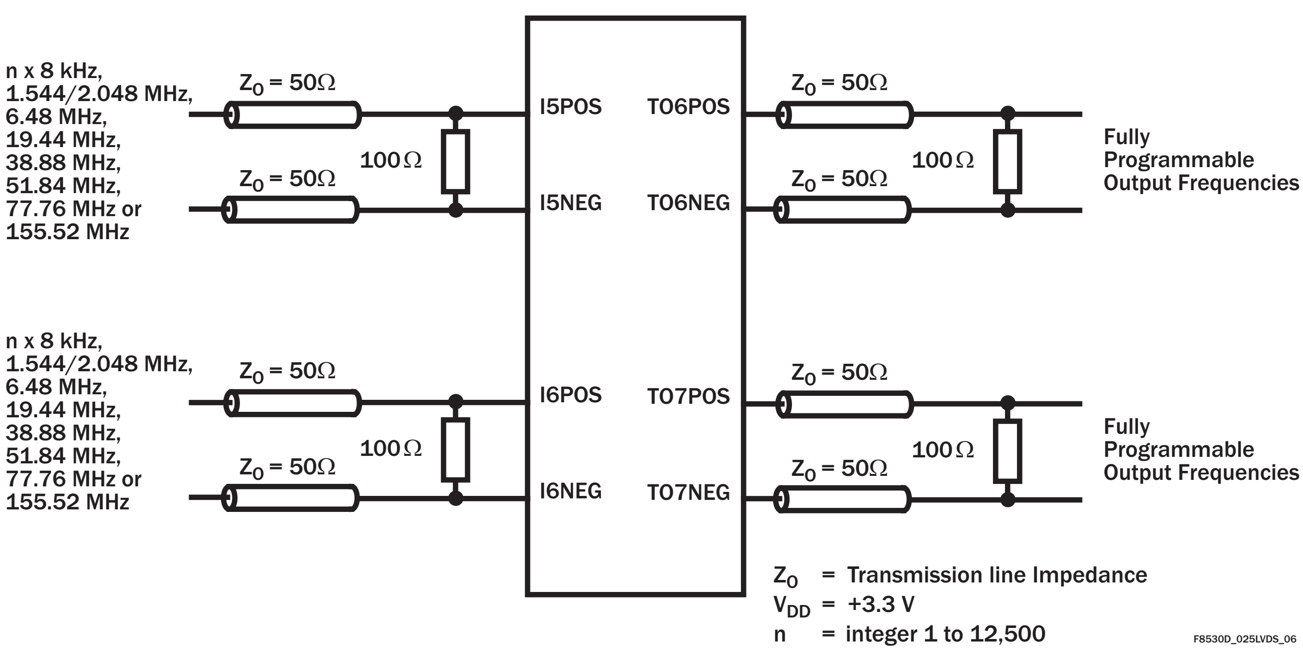
Table 39 DC Characteristics: LVDS Input/Output Port

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
LVDS Input Voltage Range Differential Input Voltage = 100 mV	V_{VRLVDS}	0	-	2.40	V
LVDS Differential Input Threshold	V_{DITH}	-100	-	+100	mV
LVDS Input Differential Voltage	$V_{IDLVTSDS}$	0.1	-	1.4	V
LVDS Input Termination Resistance Must be placed externally across the LVDS ± input pins of ACS8520. Resistor should be 100 Ω with 5% tolerance	R_{TERM}	95	100	105	Ω
LVDS Output *High* Voltage (Note (i))	V_{OHLVDS}	-	-	1.585	V
LVDS Output *Low* Voltage (Note (i))	V_{OLLVDS}	0.885	-	-	V
LVDS Differential Output Voltage	V_{ODLVDS}	250	-	450	mV
LVDS Change in Magnitude of Differential Output Voltage for complementary States (Note (i))	$V_{DOSLVDS}$	-	-	25	mV
LVDS Output Offset Voltage Temperature = 25°C (Note (i))	V_{OSLVDS}	1.125	-	1.275	V

Note: (i) *With 100 Ω load between the differential outputs.*

Figure 24 Recommended Line Termination for LVDS Input/Output Ports



DC Characteristics: AMI Input/Output Port

(Across all operating Conditions, unless otherwise stated.)

The Alternate Mark Inversion (AMI) signal is DC balanced and consists of positive and negative pulses with a peak-to-peak voltage of 2.0 ±0.2 V.

The electrical specifications are taken from option a) of Table 2/G.703 - Digital 64 kbit/s centralized clock interface, from ITU G.703[6].

The electrical characteristics of the 64 kbit/s interface are as follows:

Nominal bit rate: 64 kbit/s. The tolerance is determined by the network clock stability.

There should be a symmetrical pair carrying the composite timing signal (64 kHz and 8 kHz). The use of transformers is recommended.

Over-voltage protection requirement: refer to Recommendation K.41[16]

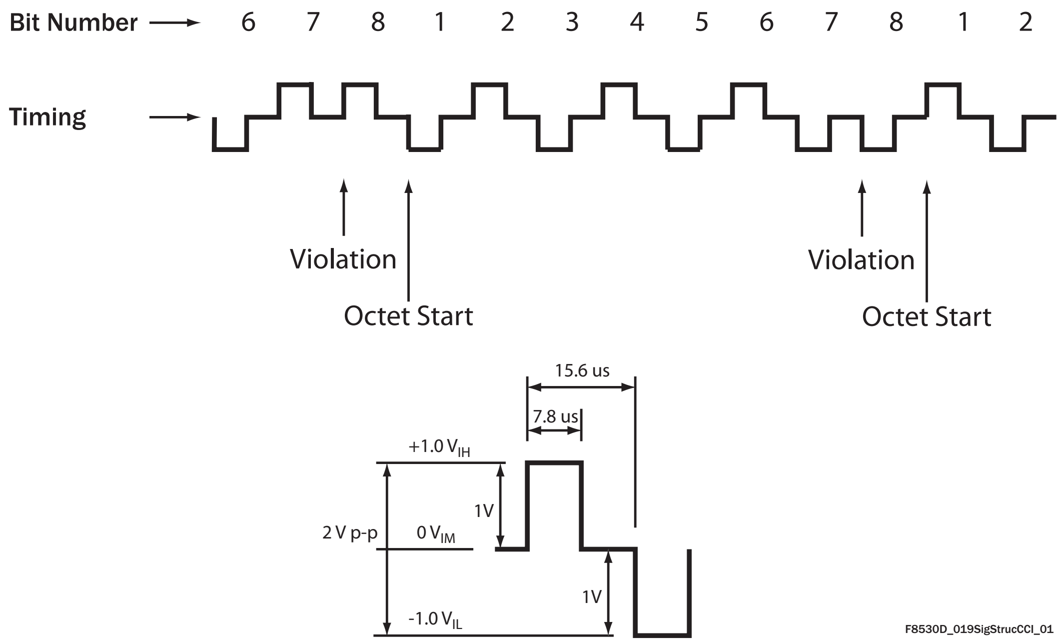
Code conversion rules:
The data signals are coded in AMI code with 100% duty cycle. The composite clock timing signals convey the 64 kHz bit-timing information using AMI coding with a 50% to 70% duty ratio and the 8 kHz octet phase information by introducing violations in the code rule. The structure of the signals and voltage level are shown in Figure 25, Figure 26 and Figure 27.

Table 40 DC Characteristics: AMI Input/Output Port

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Pulse Width	t_{PW}	1.56	7.8	14.04	µs
Input Pulse Rise/Fall Time	$t_{R/F}$	-	-	5	µs
AMI Input Voltage *High*	$V_{IH\ AMI}$	2.5	-	V_{DD} + 0.3	V
AMI Input Voltage *Middle*	$V_{VIM\ AMI}$	1.5	1.65	1.8	V
AMI Input Voltage *Low*	$V_{VIL\ AMI}$	0	-	1.4	V
AMI Output Current Drive	I_{AMIOUT}	-	-	20	mA
AMI Output *High* Voltage Output Current = 20mA	$V_{OH\ AMI}$	V_{DD} - 0.16	-	-	V
AMI Output *Low* Voltage Output Current = 20mA	$V_{OL\ AMI}$	-	-	0.16	V
Nominal Test Load Impedance	R_{TEST}	-	110	-	Ω
“Mark” Amplitude After Transformer	V_{MARK}	0.9	1.0	1.1	V
“Space” Amplitude After Transformer	V_{SPACE}	- 0.1	0	0.1	V

Figure 25 Signal Structure of 64 kHz/8 kHz Central Clock Interface)



Note...after suitable input/output transformer (also see G.703[6]).

Figure 26 AMI Input and Output Signal Levels

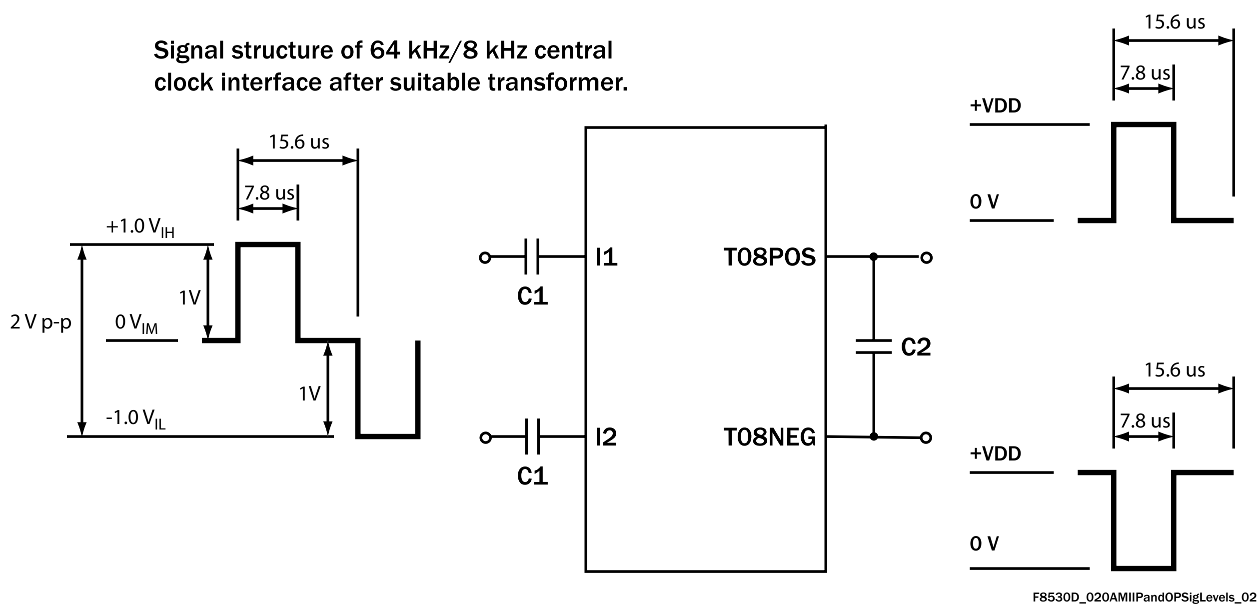
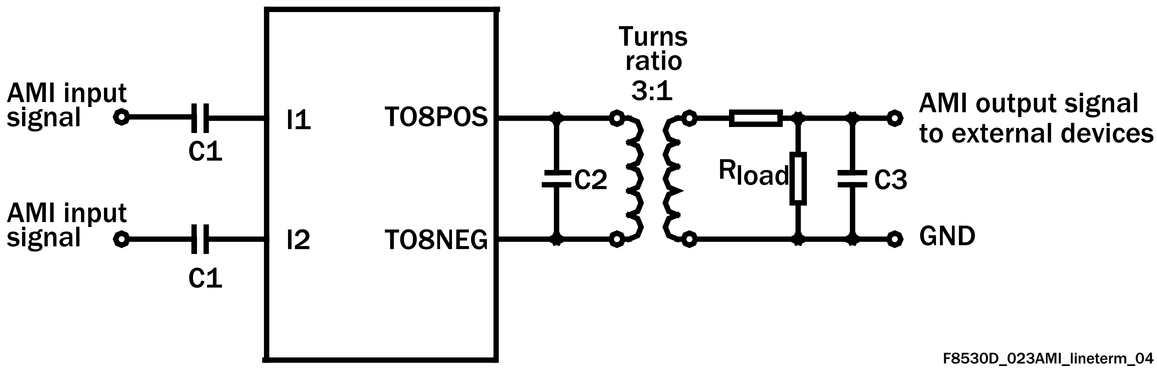


Figure 27 Recommended Line Termination for AMI Output/Output Ports



Note...The AMI inputs I1 and I2 should be connected to the external AMI clock source by 470 nF coupling capacitor C1.

The AMI differential output T08POS/T08NEG should be coupled to a line transformer with a turns ratio of 3:1. Components C2 = 470 pF and C3 = 2 nF. If a transformer with a turns ratio of 1:1 is used, a 3:1 ratio potential divider R_{load} must be used to achieve the required 1 V p-p voltage level for the positive and negative pulses.

Jitter Performance

Output jitter generation measured over 60 second interval, UI p-p max measured using C-MAC E2747 12.800 MHz TCXO on ICT Flexacom tester.

Table 41 Output Jitter Generation

Test Definition		Conditions			Jitter Spec	ACS8520 Jitter
Specification	Filter	Bandwidth	I/P Freq	Lock Mode	UI	UI (TYP)
G813[11] for 155 MHz o/p option 1	65 kHz - 1.3 MHz	4 Hz	19 MHz	Direct lock	0.1 p-p	0.067 p-p
				8k lock		0.065 p-p
G813[11] & G812[10] for 2.048 MHz option 1	20 Hz - 100 kHz	4 Hz	2.048 MHz	8k lock	0.05 p-p	0.012 p-p
G813[11] for 155 MHz o/p option 2	12 kHz - 1.3 MHz	18 Hz	19 MHz	Direct lock/ 8k lock	0.1 p-p	0.072 p-p
	12 kHz - 1.3 MHz	8 Hz	19 MHz	Direct lock/ 8k lock	0.1 p-p	0.072 p-p
	12 kHz - 1.3 MHz	4 Hz	19 MHz	Direct lock/ 8k lock	0.1 p-p	0.078 p-p
	12 kHz - 1.3 MHz	2.5 Hz	19 MHz	Direct lock/ 8k lock	0.1 p-p	0.078 p-p
	12 kHz - 1.3 MHz	1.2 Hz	19 MHz	Direct lock/ 8k lock	0.1 p-p	0.078 p-p
	12 kHz - 1.3 MHz	0.6 Hz	19 MHz	Direct lock/ 8k lock	0.1 p-p	0.076 p-p
G812[10] for 1.544 MHz o/p	10 Hz - 40 kHz	4 Hz	1.544 MHz	8k lock	0.05 p-p	0.006 p-p

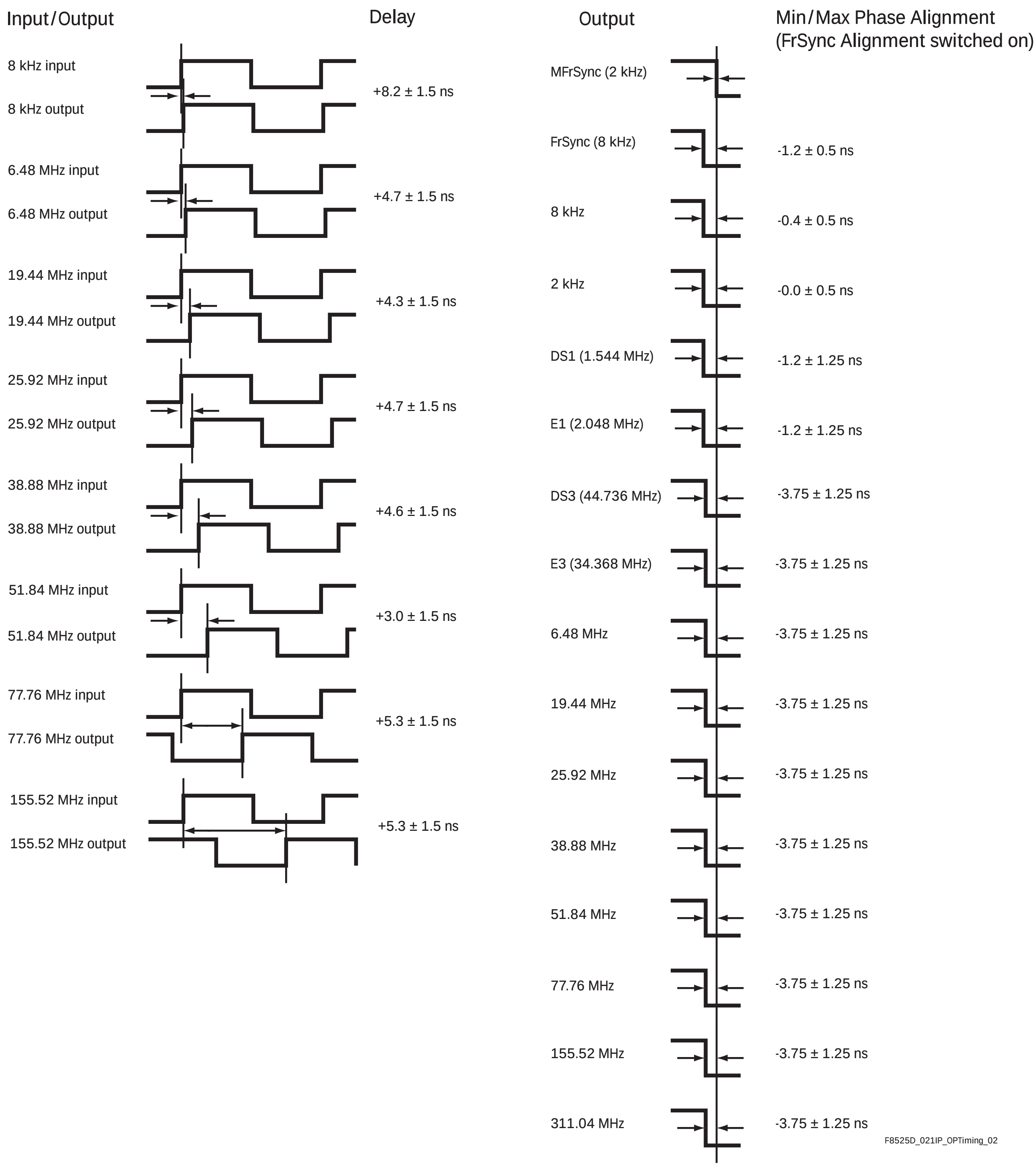
Table 41 Output Jitter Generation

Test Definition		Conditions			Jitter Spec	ACS8520 Jitter
Specification	Filter	Bandwidth	I/P Freq	Lock Mode	UI	UI (TYP)
G812[10] for 155 MHz electrical	500 Hz - 1.3 MHz	4 Hz	19 MHz	8k lock	0.5 p-p	0.118 p-p
G812[10] for 155 MHz electrical	65 kHz - 1.3 MHz	4 Hz	19 MHz	8k lock	0.075 p-p	0.065 p-p
ETS-300-462-3[3] for 2.048 MHz SEC o/p	20 Hz - 100 kHz	4 Hz	2.048 MHz	8k lock	0.5 p-p	0.012 p-p
ETS-300-462-3[3] for 2.048 MHz SEC o/p	49 Hz - 100 kHz	4 Hz	2.048 MHz	8k lock	0.2 p-p	0.012 p-p
ETS-300-462-3[3] for 2.048 MHz SSU o/p	20 Hz - 100 kHz	4 Hz	2.048 MHz	8k lock	0.05 p-p	0.012 p-p
ETS-300-462-5[4] for 155 MHz o/p	500 Hz - 1.3 MHz	4 Hz	19 MHz	8k lock	0.5 p-p	0.118 p-p
ETS-300-462-5[4] for 155 MHz o/p	65 kHz - 1.3 MHz	4 Hz	19 MHz	8k lock	0.1 p-p	0.067 p-p
GR-253-CORE[17] net i/f, 51.84 MHz o/p	100 Hz - 0.4 MHz	4 Hz	19 MHz	8k lock	1.5 p-p	0.027 p-p
GR-253-CORE[17] net i/f, 51.84 MHz o/p	20 kHz to 0.4 MHz	4 Hz	19 MHz	8k lock	0.15 p-p	0.017 p-p
GR-253-CORE[17] net i/f, 155 MHz o/p	500 Hz - 1.3 MHz	4 Hz	19 MHz	8k lock	1.5 p-p	0.118 p-p
GR-253-CORE[17] net i/f, 155 MHz o/p	65 kHz - 1.3 MHz	4 Hz	19 MHz	8k lock	0.15 p-p	0.067 p-p
GR-253-CORE[17]cat II elect i/f, 155 MHz	12 kHz - 1.3 MHz	4 Hz	19 MHz	8k lock	0.1 p-p	0.076 p-p
					0.01 rms	0.006 rms
GR-253-CORE[17] cat II elect i/f, 51.84 MHz	12 kHz - 400 kHz	4 Hz	19 MHz	8k lock	0.1 p-p	0.018 p-p
					0.01 rms	0.003 rms
GR-253-CORE[17] DS1 i/f, 1.544 MHz	10 Hz - 40 kHz	4 Hz	1.544 MHz	8k lock	0.1 p-p	0.001 p-p
					0.01 rms	<0.001 rms
AT&T 62411[2] for 1.544 MHz	10 Hz - 8 kHz	4 Hz	1.544 MHz	8k lock	0.02 rms	<0.001 rms
AT&T 62411[2] for 1.544 MHz	8 Hz - 40 kHz	4 Hz	1.544 MHz	8k lock	0.025 rms	<0.001 rms
AT&T 62411[2] for 1.544 MHz	10 Hz - 40 kHz	4 Hz	1.544 MHz	8k lock	0.025 rms	<0.001 rms
AT&T 62411[2] for 1.544 MHz	Broadband	4 Hz	1.544 MHz	8k lock	0.05 rms	<0.001 rms
G-742[8] for 2.048 MHz	DC - 100 kHz	4 Hz	2.048 MHz	8k lock	0.25 rms	0.012 rms
G-742[8] for 2.048MHz	18 kHz - 100 kHz	4 Hz	2.048 MHz	8k lock	0.05 p-p	0.012 p-p
G-736[7] for 2.048MHz	20 Hz - 100 kHz	4 Hz	2.048 MHz	8k lock	0.05 p-p	0.012 p-p
GR-499-CORE[18] & G824[14] for 1.544 MHz	10 Hz - 40kHz	4 Hz	1.544 MHz	8k lock	5.0 p-p	0.006 p-p
GR-499-CORE[18] & G824[14] for 1.544 MHz	8 kHz - 40kHz	4 Hz	1.544 MHz	8k lock	0.1 p-p	0.006 p-p
GR-1244-CORE[19] for 1.544 MHz	> 10 Hz	4 Hz	1.544 MHz	8k lock	0.05 p-p	0.006 p-p

Note...This table is only for comparing the ACS8520 output jitter performance against values and quoted in various specifications for given conditions. It should not be used to infer compliance to any other aspects of these specifications.

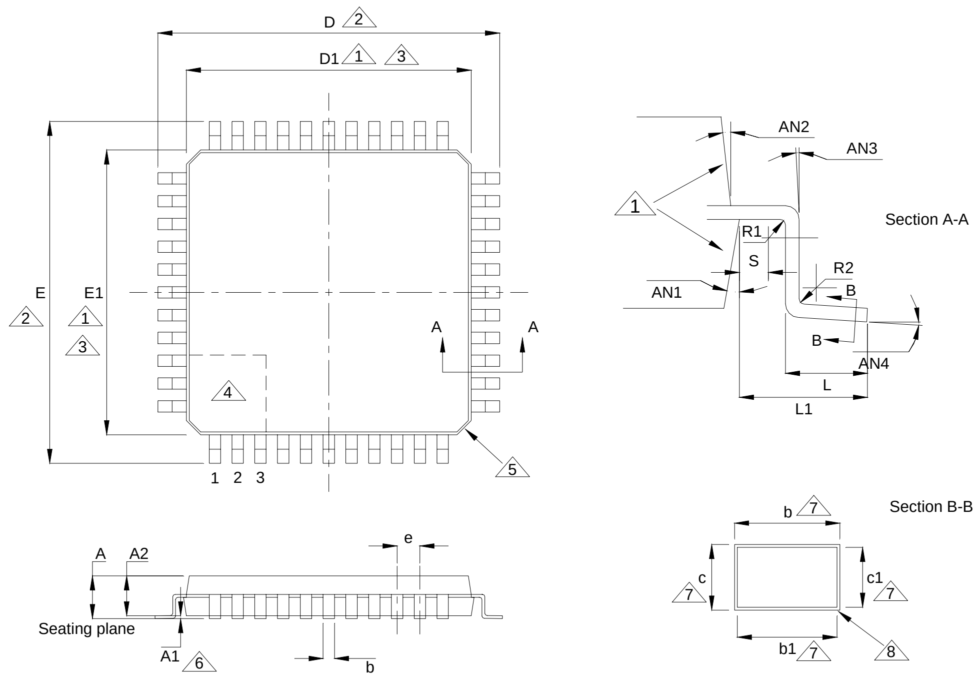
Input/Output Timing

Figure 28 Input/Output Timing with Phase Build-out Off



Package Information

Figure 29 LQFP Package



Notes

1. The top package body may be smaller than the bottom package body by as much as 0.15 mm.
2. To be determined at seating plane.
3. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Details of pin 1 identifier are optional but will be located within the zone indicated.
5. Exact shape of corners can vary.
6. A1 is defined as the distance from the seating plane to the lowest point of the package body.
7. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
8. Shows plating.

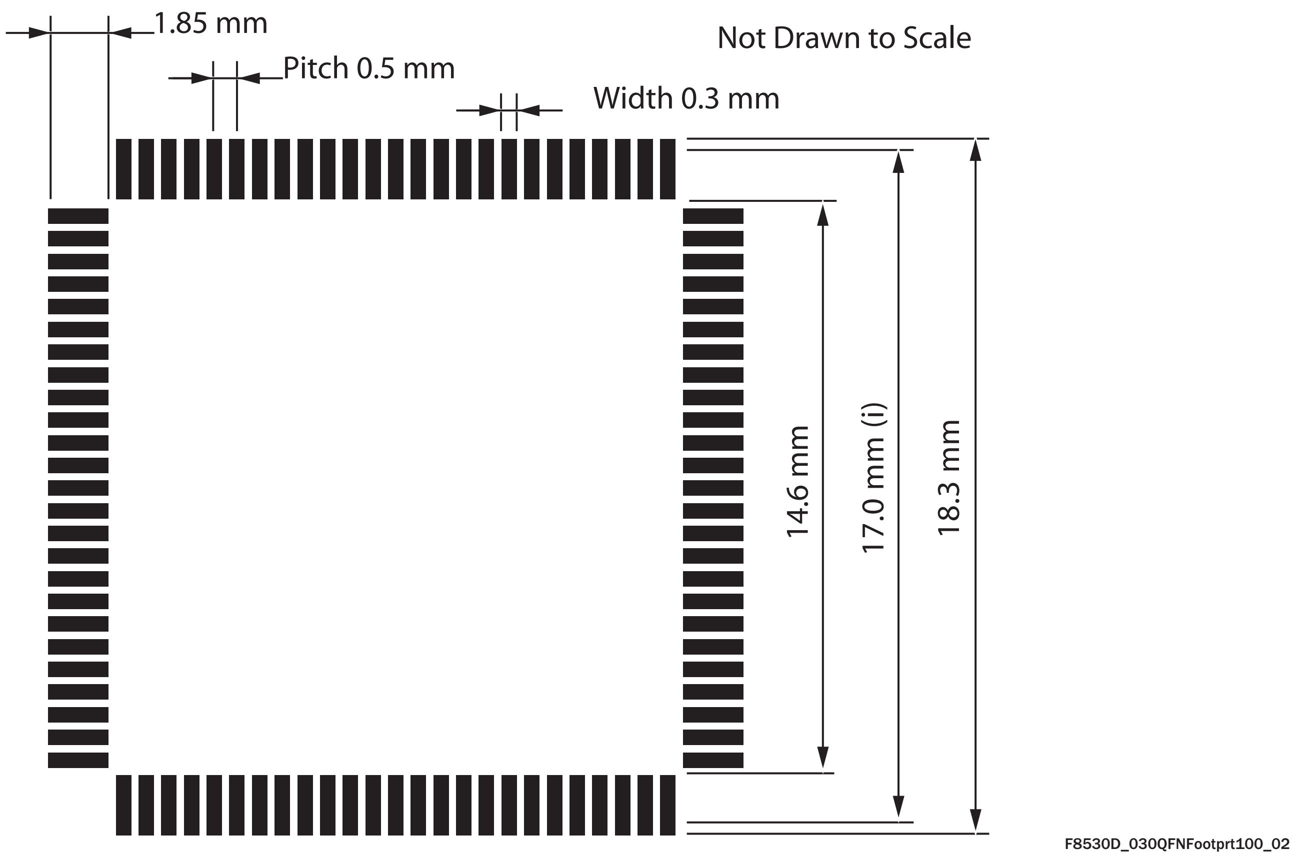
Table 42 100 Pin LQFP Package Dimension Data (for use with Figure 29)

100 LQFP Package Dimensions in mm	D/E	D1/ E1	A	A1	A2	e	AN1	AN2	AN3	AN4	R1	R2	L	L1	S	b	b1	c	c1
Min.	-	-	1.40	0.05	1.35	-	11^{o}	11^{o}	0^{o}	0^{o}	0.08	0.08	0.45	-	0.20	0.17	0.17	0.09	0.09
Nom.	16.00	14.00	1.50	0.10	1.40	0.50	12^{o}	12^{o}	-	3.5^{o}	-	-	0.60	1.00 (ref)	-	0.22	0.20	-	-
Max.	-	-	1.60	0.15	1.45	-	13^{o}	13^{o}	-	7^{o}	-	0.20	0.75	-	-	0.27	0.23	0.20	0.16

Thermal Conditions

The device is rated for full temperature range when this package is used with a 4 layer or more PCB. Copper coverage must exceed 50%. All pins must be soldered to the PCB. Maximum operating temperature must be reduced when the device is used with a PCB with less than these requirements.

Figure 30 Typical 100 Pin LQFP Footprint

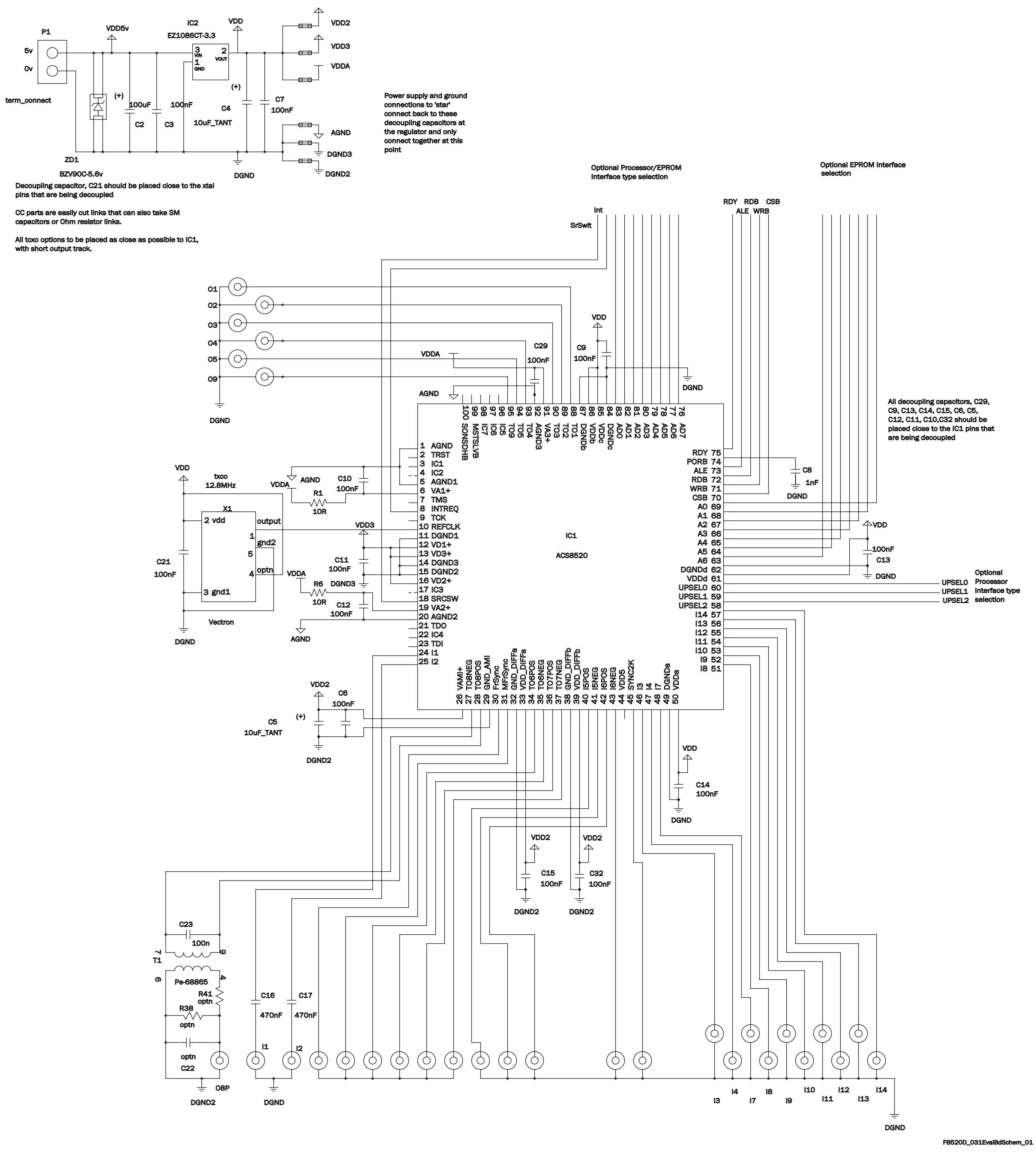


Notes: (i) Solderable to this limit.

(ii) Square package - dimensions apply in both X and Y directions.

(iii) Typical example. The user is responsible for ensuring compatibility with PCB manufacturing process, etc.

Figure 31 Simplified Application Schematic



Abbreviations

AMI	Alternate Mark Inversion
APLL	Analogue Phase Locked Loop
BITS	Building Integrated Timing Supply
DFS	Digital Frequency Synthesis
DPLL	Digital Phase Locked Loop
DS1	1544 kbit/s interface rate
DTO	Discrete Time Oscillator
E1	2048 kbit/s interface rate
I/O	Input - Output
LOF	Loss of Frame Alignment
LOS	Loss Of Signal
LQFP	Low profile Quad Flat Pack
LVDS	Low Voltage Differential Signal
MTIE	Maximum Time Interval Error
NE	Network Element
OCXO	Oven Controlled Crystal Oscillator
PBO	Phase Build-out
PDH	Plesiochronous Digital Hierarchy
PECL	Positive Emitter Coupled Logic
PFD	Phase and Frequency Detector
PLL	Phase Locked Loop
POR	Power-On Reset
ppb	parts per billion
ppm	parts per million
p-p	peak-to-peak
R/W	Read/Write
rms	root-mean-square
RO	Read Only
RoHS	Restrictive Use of Certain Hazardous Substances (directive)
SDH	Synchronous Digital Hierarchy
SEC	SDH/SONET Equipment Clock
SETS	Synchronous Equipment Timing source
SONET	Synchronous Optical Network
SSU	Synchronization Supply Unit
STM	Synchronous Transport Module
TDEV	Time Deviation
TCXO	Temperature Compensated Crystal Oscillator
UI	Unit Interval
WEEE	Waste Electrical and Electronic Equipment (directive)

References

[1] ANSI T1.101-1999 (1999)
Synchronization Interface Standard

[2] AT & T 62411 (12/1990)
ACCUNET® T1.5 Service description and Interface Specification

[3] ETSI ETS 300 462-3, (01/1997)
Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 3: The control of jitter and wander within synchronization networks

[4] ETSI ETS 300 462-5 (09/1996)
Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 5: Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) equipment

[5] IEEE 1149.1 (1990)
Standard Test Access Port and Boundary-Scan Architecture

[6] ITU-T G.703 (10/1998)
Physical/electrical characteristics of hierarchical digital interfaces

[7] ITU-T G.736 (03/1993)
Characteristics of a synchronous digital multiplex equipment operating at 2048 kbit/s

[8] ITU-T G.742 (1988)
Second order digital multiplex equipment operating at 8448 kbit/s, and using positive justification

[9] ITU-T G.783 (10/2000)
Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks

[10] ITU-T G.812 (06/1998)
Timing requirements of slave clocks suitable for use as node clocks in synchronization networks

[11] ITU-T G.813 (08/1996)
Timing characteristics of SDH equipment slave clocks (SEC)

[12] ITU-T G.822 (11/1988)
Controlled slip rate objectives on an international digital connection

[13] ITU-T G.823 (03/2000)
The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy

[14] ITU-T G.824 (03/2000)
The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy

[15] ITU-T G.825 (03/2000)
The control of jitter and wander within digital networks which are based on the Synchronous Digital Hierarchy (SDH)

[16] ITU-T K.41 (05/1998)
Resistibility of internal interfaces of telecommunication centres to surge overvoltages

[17] Telcordia GR-253-CORE, Issue 3 (09/ 2000)
Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria

[18] Telcordia GR-499-CORE, Issue 2 (12/1998)
Transport Systems Generic Requirements (TSGR) Common requirements

[19] Telcordia GR-1244-CORE, Issue 2 (12/2000)
Clocks for the Synchronized Network: Common Generic Criteria

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This is a FINAL release (Revision 3.02) of the ACS8520 datasheet. Changes made for this document revision are given in Table 43, together with a brief summary of previous revisions. For specific changes between earlier revisions, refer (where available) to those earlier revisions. Always use the current version of the datasheet.

Table 43 Revision History

Revision	Reference	Description of changes
1.00/February 2002	See particular revision	Initial datasheet and minor releases at Preliminary status. Refer to particular release for the changes made for that release.
1.01/February 2002		
1.02/April 2002		
1.03/April 2002		
1.04/May 2002		
1.05/September 2002		
1.06/September 2002		
2.00/January 2003		Major revision. First release at FINAL status and completely revised.
3.00/September 2003		Major revision.
3.01/October 2003		Minor revision
3.02/October 2005	Regs: 1D, 3C, 3D, 63, 64, 65 and 79	Register description updated.
	Figures 23 and 24	Figures updated.
	Page 21	“patent -pending” reference updated to “patented”.
	Figure 5	Title change and note added to Figure.
	Figure 30	Redrawn Figure.
	Table 32	New row added for VDD5.
	Figure 19 and pin 68 (Table 2)	References added such that A(1) = CLKE in serial mode.
	Back page	Former US mailing address removed. (Mail now delivered to main address).
	Trademark Acknowledgements and Revision Status/History	Sections updated.
	Front page bullets, back page Ordering Information and Abbreviations sections	References to availability of a lead (Pb)-free packaged version (ACS8520T) added.

Notes

Ordering Information

Table 44 Parts List

Part Number	Description
ACS8520	SETS Synchronous Equipment Timing Source for Stratum 3/4E/4 and SMC Systems
ACS8520T	Lead (Pb)-free packaged version of ACS8520; RoHS and WEEE compliant.

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