

# Programmable Duty Cycle Controller

## FEATURES

- 10- to 200-V Input Range
- Current-Mode Control
- Internal Start-Up Circuit
- Buffer Slope Compensation Voltage
- Soft-Start
- 2.7-MHz Error Amp
- 500-mA Output Drive Current
- Light Load Frequency Fold-Back
- Low Quiescent Current
- Programmable Maximum Duty Cycle, with 80% as Default

## DESCRIPTION

The Si9118/Si9119 are a BiC/DMOS current-mode pulse width modulation (PWM) controller ICs for high-frequency dc/dc converters. Single-ended topologies (forward and flyback) can be implemented at frequencies up to 1 MHz. The controller operates in constant frequency mode during the full load and automatically switches to pulse skipping mode under light load to maintain high efficiency throughout the full load range. The maximum duty cycle is easily programmed with a resistor divider for optimum control.

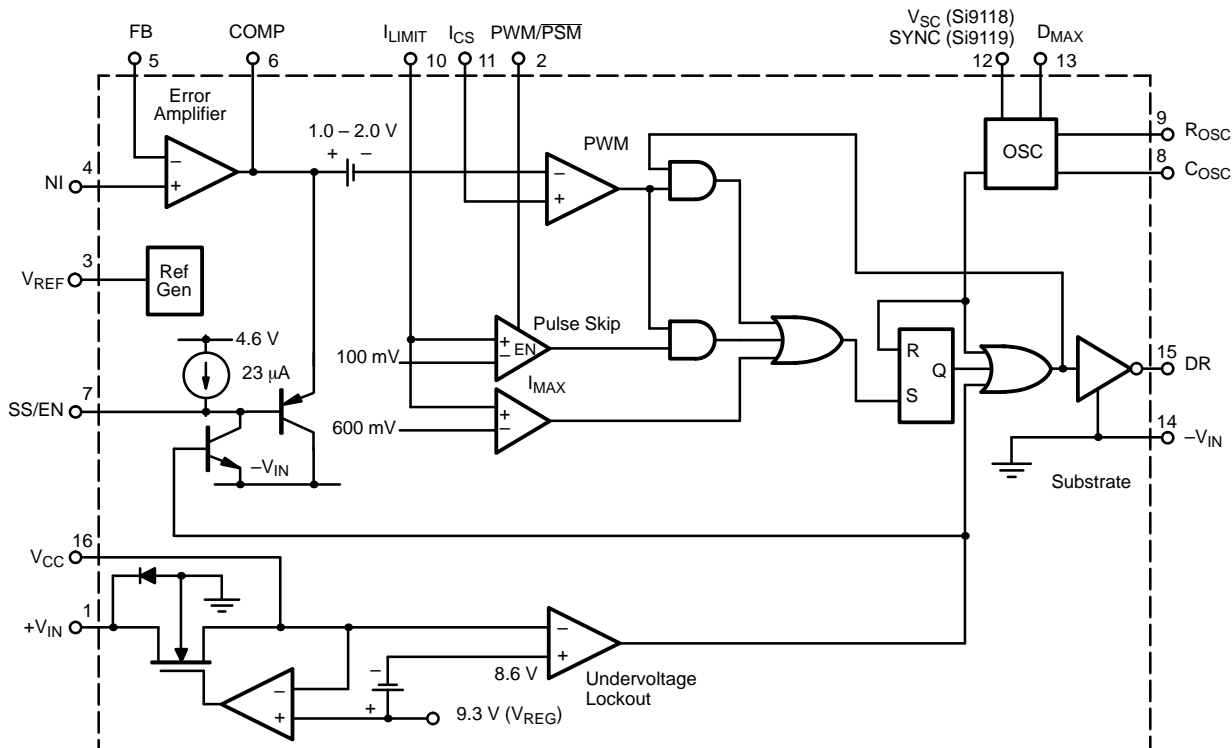
stage is almost eliminated to minimize quiescent supply current.

The high-voltage DMOS transistor permits direct operation from bus voltages of up to 200 V. Other features include a 1.5% accurate voltage reference, 2.7-MHz bandwidth error amplifier, standby mode, soft-start and undervoltage lockout circuits.

The push-pull output driver provides high-speed switching to external MOSPOWER devices large enough to supply 50 W of output power. Shoot-through current for internal push-pull

The Si9118/Si9119 are available in a 16-pin SOIC package and is specified over the industrial, D suffix (−40°C to 85°C) temperature range.

## FUNCTIONAL BLOCK DIAGRAM





### ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$	
$V_{CC}$ .....	18 V
$+V_{IN}$ (Note: $V_{CC} < +V_{IN} + 0.3$ V) .....	200 V
Logic Input (SYNC) .....	$-0.3$ V to $V_{CC} + 0.3$ V
Linear Inputs	
(FB, $I_{CS}$ , $I_{LIMIT}$ , SS/EN) .....	$-0.3$ V to $V_{CC} + 0.3$ V
HV Pre-Regulator Input Current (continuous) .....	5 mA
Storage Temperature .....	$-65$ to $150^{\circ}\text{C}$
Operating Temperature .....	$-40$ to $85^{\circ}\text{C}$

$D_{MAX}$ .....	3.2 V
Junction Temperature ( $T_J$ ) .....	$150^{\circ}\text{C}$
Power Dissipation (Package) <sup>a</sup>	
16-Pin SOIC (Y Suffix) <sup>b</sup> .....	900 mW
Thermal Impedance ( $\Theta_{JA}$ )	
16-Pin SOIC .....	$140^{\circ}\text{C/W}$

#### Notes

- Device mounted with all leads soldered or welded to PC board.
- Derate  $7.2$  mW/ $^{\circ}\text{C}$  above  $25^{\circ}\text{C}$ .

\* . Exposure to Absolute Maximum rating conditions for extended periods may affect device reliability. Stresses above Absolute Maximum rating may cause permanent damage. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

### RECOMMENDED OPERATING RANGE

Voltages Referenced to $-V_{IN}$	
$V_{CC}$ .....	10 V to 16.5 V
$+V_{IN}$ .....	10 V to 200 V
$f_{OSC}$ .....	40 kHz to 1 MHz

$R_{OSC}$ .....	56 k $\Omega$ to 1 M $\Omega$
$C_{OSC}$ .....	47 pF to 200 pF
Linear Inputs .....	0 to $V_{CC} - 4$ V
Digital Inputs .....	0 to $V_{CC}$

SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Specified Oscillator Disabled $-V_{IN} = 0$ V, $V_{CC} = 10$ V	Limits D Suffix $-40$ to $85^{\circ}\text{C}$				Unit
			Temp <sup>a</sup>	Min	Typ <sup>b</sup>	Max	
<b>Reference</b>							
Output Voltage	$V_{REF}$	OSC Disabled, $T_A = 25^{\circ}\text{C}$	Room	3.94	4.0	4.06	V
		OSC Disabled, Over Voltage and Temperature Ranges <sup>c</sup>	Full	3.88	4.0	4.12	
Short Circuit Current	$I_{SREF}$	$V_{REF} = -V_{IN}$			-30	-5	mA
Load Regulation	$\Delta V_R / \Delta I_R$	$I_{REF} = 0$ to $-1$ mA			10	40	mV
<b>Oscillator</b>							
Initial Accuracy <sup>d</sup>	$f_{OSC}$	$R_{OSC} = 374$ k $\Omega$ , $C_{OSC} = 200$ pF		90	100	110	kHz
	$f_{OSC}^c$	$R_{OSC} = 70$ k $\Omega$ , $C_{OSC} = 200$ pF		450	500	550	
Voltage Stability <sup>c</sup>	$\Delta f/f$	$R_{OSC} = 70$ k $\Omega$ , $C_{OSC} = 200$ pF $\Delta f/f = [(f(16.5 \text{ V}) - f(9.5 \text{ V})) / f(9.5 \text{ V})]$			1	2	%
Temperature Coefficient <sup>c</sup>	OSC TC	$-40 \leq T_A \leq 85^{\circ}\text{C}$ , $f_{OSC} = 100$ kHz			200	500	ppm/ $^{\circ}\text{C}$
Sync High Pulse Width (Si9119)				200			ns
Sync Low Pulse Width (Si9119)				200			
Sync Rise/Fall Time (Si9119)						200	
Sync Logic Low (Si9119)	$V_{IL}$					0.8	V
Sync Logic High (Si9119)	$V_{IH}$			4			
Sync Range <sup>c</sup> (Si9119)	$f_{EXT}$			$1.05 \times f_{OSC}$			kHz
<b>PWM/PSM</b>							
PWM/PSM Logic High	$V_{IH}$			4			V
PWM/PSM Logic Low	$V_{IL}$					0.8	
<b>D<sub>MAX</sub></b>							
Accuracy		$f_{OSC} = 100$ kHz with 1% Resistor			$\pm 10$		%



SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Specified Oscillator Disabled -V <sub>IN</sub> = 0 V, V <sub>CC</sub> = 10 V	Limits D Suffix -40 to 85°C				Unit
			Temp <sup>a</sup>	Min	Typ <sup>b</sup>	Max	
<b>Error Amplifier (OSC Disabled)</b>							
Input BIAS Current	I <sub>FB</sub>	V <sub>FB</sub> = 5 V, NI = V <sub>REF</sub>		< 1.0	± 200		nA
Input OFFSET Voltage	V <sub>OS2</sub>			± 5	± 25		mV
Open Loop Voltage Gain <sup>c</sup>	A <sub>VOL</sub>		65	80			dB
Unity Gain Bandwidth <sup>c</sup>	BW		1.8	2.7			MHz
Output Current	I <sub>OUT</sub>	Source (V <sub>FB</sub> = 3.5 V, NI = V <sub>REF</sub> )	-1.0	-2.7			mA
		Sink (V <sub>FB</sub> = 4.5 V, NI = V <sub>REF</sub> )	1.0	2.4			
Power Supply Rejection	PSRR	10 V ≤ V <sub>CC</sub> ≤ 16.5 V	50	80			dB
<b>Pre-Regulator/Start-up</b>							
Input Voltage <sup>c</sup>	+V <sub>IN</sub>	I <sub>IN</sub> = 10 μA	Room	200			V
Input Leakage Current	+I <sub>IN</sub>	V <sub>CC</sub> ≥ 10 V	Room			10	μA
Pre-Regulator Start-Up Current	I <sub>START</sub>	Pulse Width ≤ 300 μs V <sub>CC</sub> = V <sub>UVLO</sub>	Room	8	15		mA
V <sub>CC</sub> Pre-Regulator Turn-Off Threshold Voltage	V <sub>REG</sub>	I <sub>PRE-REGULATOR</sub> = 15 μA	Room	8.7	9.3	9.8	V
Undervoltage Lockout	V <sub>UVLO</sub>		Room	8.0	8.6	9.3	
V <sub>REG</sub> - V <sub>UVLO</sub>	V <sub>DELTA</sub>		Room	0.3	0.7		
<b>Supply</b>							
Supply Current	I <sub>CC</sub>	C <sub>LOAD</sub> ≤ 50 pF, f <sub>OSC</sub> = 100 kHz			1.9	2.5	mA
<b>Protection</b>							
Current Limit Threshold Voltage	V <sub>I(Limit)</sub>	V <sub>FB</sub> = 0 V, NI = V <sub>REF</sub>		0.5	0.6	0.7	V
Current Limit Delay to Output <sup>c</sup>	t <sub>d</sub>	V <sub>SENSE</sub> = 0.85 V, See Figure 1			77	100	ns
Soft-Start Current	I <sub>SS</sub>			-12	-23	-30	μA
Output Inhibit Voltage	V <sub>SS(off)</sub>	Soft-Start Voltage to Disable Driver Output		0.5	1.26		V
Pulse Skipping Threshold Voltage	V <sub>PS</sub>			80	100	120	mV
<b>Mosfet Driver</b>							
Output High Voltage	V <sub>OH</sub>	I <sub>OUT</sub> = -10 mA	Room Full	V <sub>CC</sub> - 0.3 V <sub>CC</sub> - 0.5			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OUT</sub> = 10 mA	Room Full			0.3 0.5	
Output Resistance <sup>c</sup>	R <sub>OUT</sub>	I <sub>OUT</sub> = 10 mA, Source or Sink	Room Full		20 25	30 50	Ω
Rise Time <sup>c</sup>	t <sub>r</sub>	C <sub>L</sub> = 500 pF	Room		40	75	ns
Fall Time <sup>c</sup>	t <sub>f</sub>		Room		40	75	

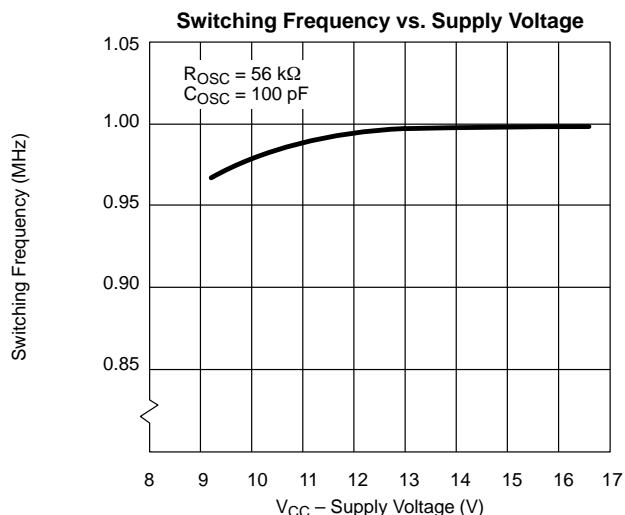
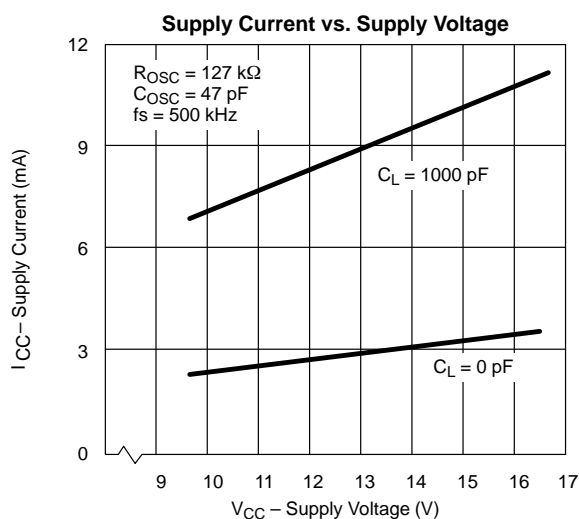
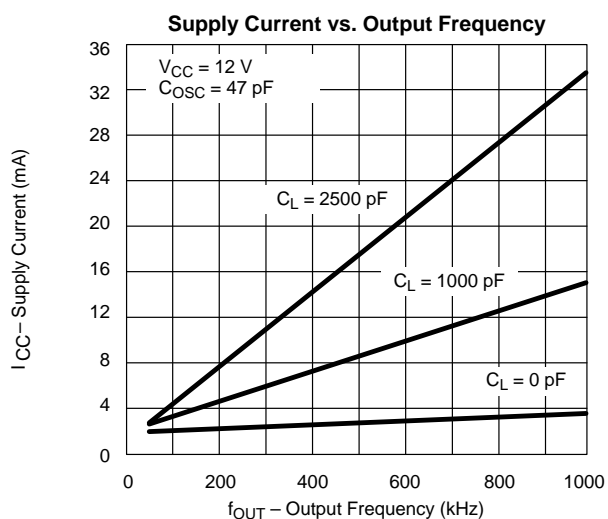
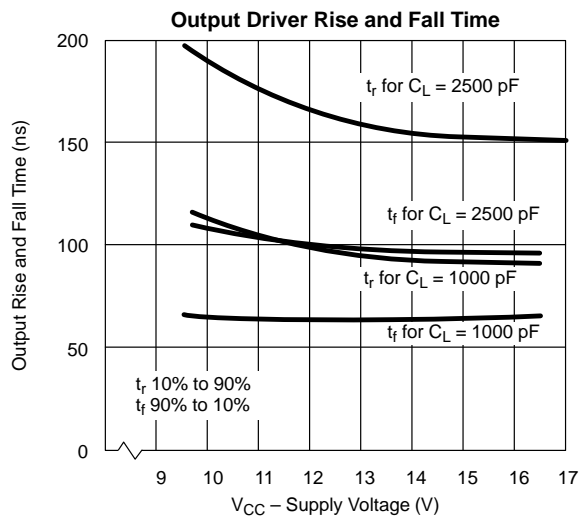
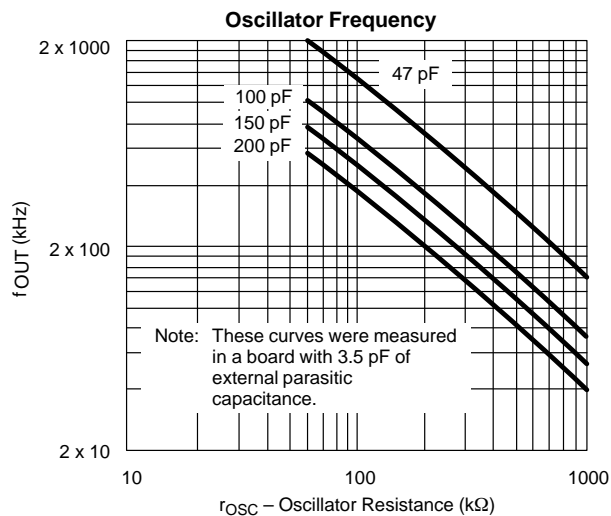
Notes

- a. Room = 25°C, Full = as determined by the operating temperature suffix.
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- c. Guaranteed by design, not subject to production test.
- d. C<sub>STRAY</sub> ≤ 5 pF on C<sub>OSC</sub>.



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

**MOSFET**



**TIMING WAVEFORMS**

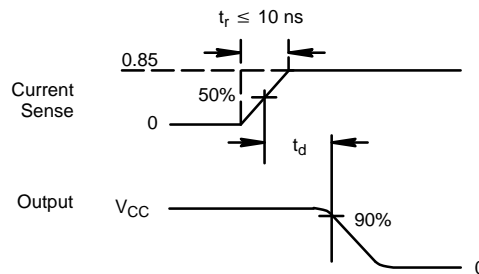
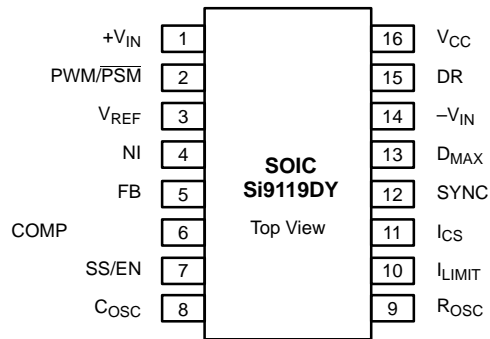
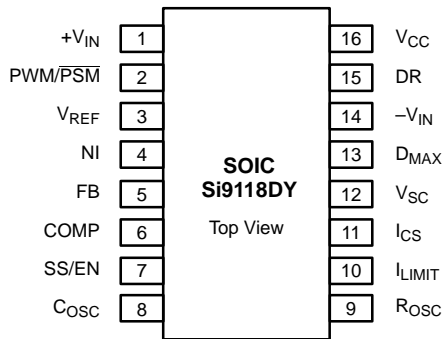


FIGURE 1.

**PIN CONFIGURATIONS**



Order Number  
SOIC: Si9118DY  
Si9119DY

PIN DESCRIPTION		
Pin Number	Symbol	Description
1	+VIN	Input bus voltage ranging from 10 V to 200 V.
2	PWM/PSM	Connected to VREF forces the converter into PWM mode. Connected to -VIN forces the converter into PSM mode.
3	VREF	4-V reference voltage. Decouple with 0.1-μF ceramic capacitor.
4	NI	Non-inverting input of an error amplifier.
5	FB	Inverting input of an error amplifier.
6	COMP	Error amplifier output for external compensation network.
7	SS/EN	Programmable soft-start with external capacitor or externally controlled disable mode.
8	COSC	External capacitor to determine the switching frequency.
9	ROSC	External resistor to determine the switching frequency.
10	ILIMIT	Pulse by pulse peak current limiting pin. When the current sense voltage exceeds the current limit threshold, the gate drive signal is terminated. ILIMIT is also used to sense the current in pulse skipping mode.
11	ICS	Current sense input to control feedback response.
12	SYNC or VSC	Si9118: slope compensation pin. Si9119: clock synchronization pin. Logic high to low transition from external signal synchronizes the internal clock frequency.
13	DMAX	Sets the maximum duty cycle. Internally, the maximum duty cycle is clamped to 80%.
14	-VIN	Single point ground.
15	DR	Gate drive for the external MOSFET switch.
16	VCC	Supply voltage for the IC after the startup transition.

#### STANDARD APPLICATION CIRCUITS

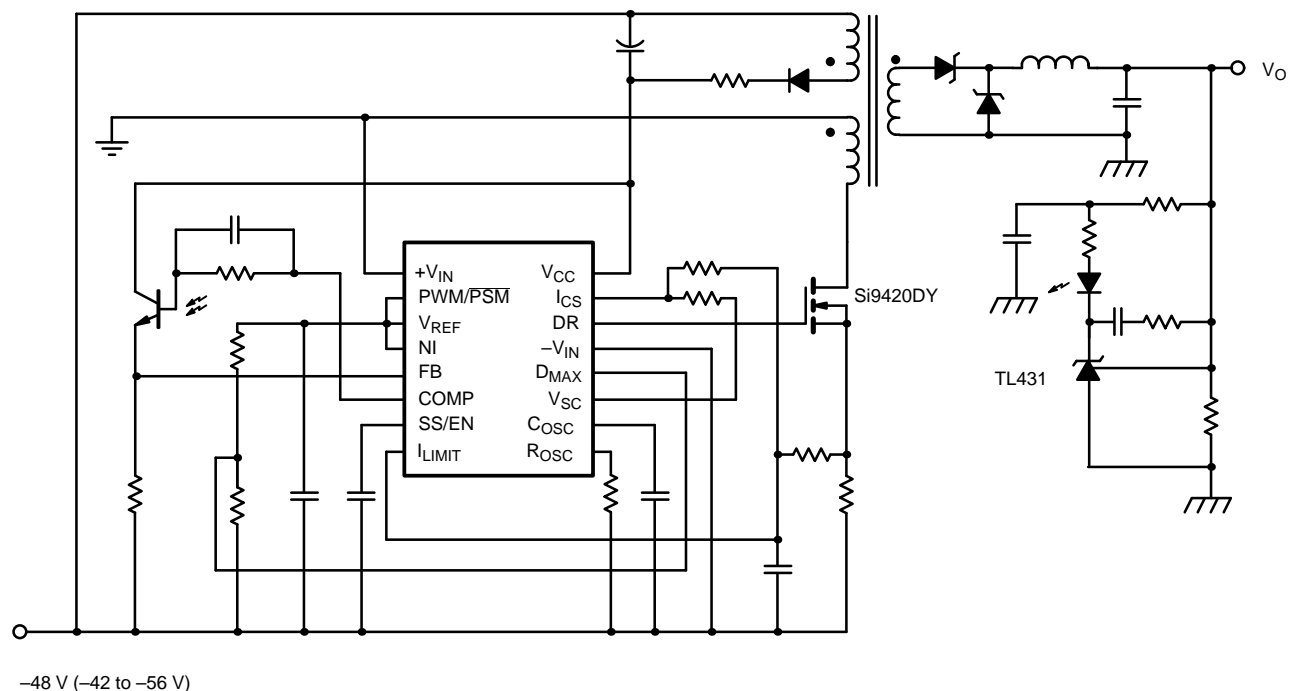


FIGURE 2. Si9118 15-W Forward Converter Schematic

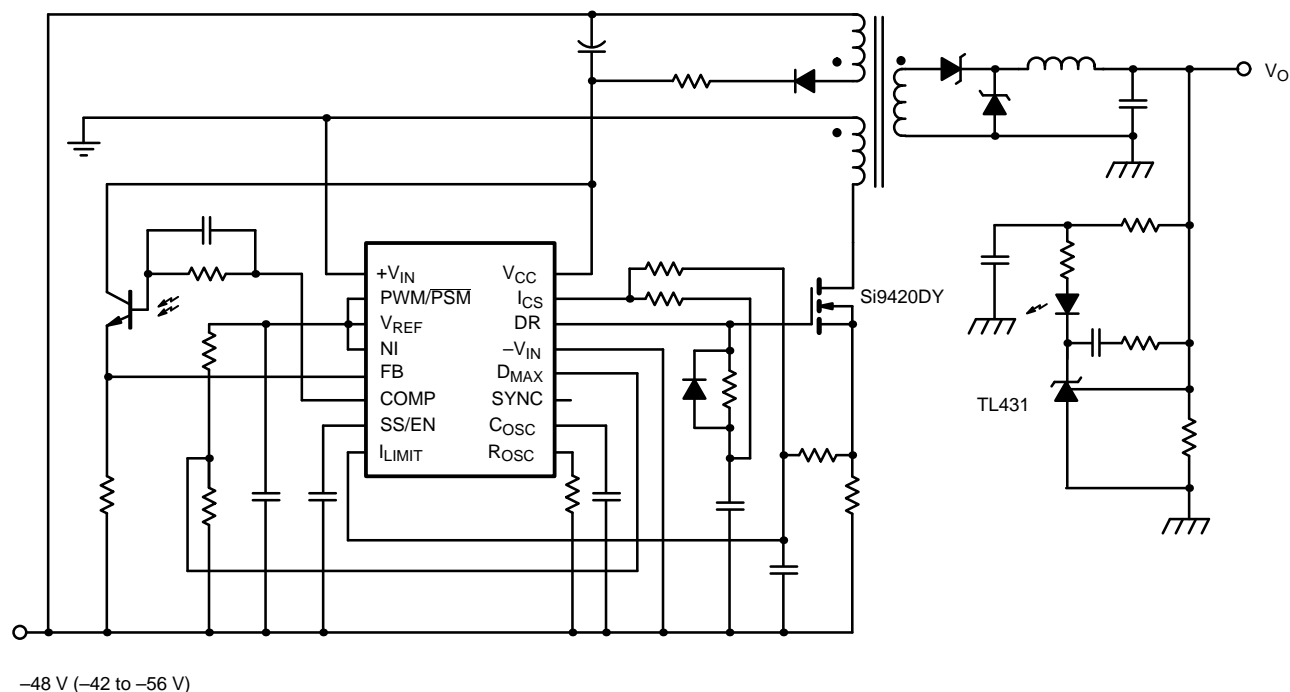


FIGURE 3. Si9119 Forward Converter With External Slope Compensation



## DETAILED OPERATIONAL DESCRIPTION

### Start-Up

Si9118/Si9119 are designed with internal depletion mode MOSFET capable of powering directly from the high input bus voltage. This feature eliminates the typical external start-up circuit saving valuable space and cost. But, most of all, this feature improves the converter efficiency during full load and has an even greater impact on light load. With an input bus voltage applied to the  $+V_{IN}$  pin, the  $V_{CC}$  voltage is regulated to 9.3 V. The UVLO circuit prevents the controller output driver section from turning on, until  $V_{CC}$  voltage exceeds 8.7 V. In order to maximize converter efficiency, the designer should provide an external bootstrap winding to override the internal  $V_{CC}$  regulator. If external  $V_{CC}$  voltage is greater than 9.3 V, the internal depletion mode MOSFET regulator is disabled and power is derived from the external  $V_{CC}$  supply. The  $V_{CC}$  supply provides power to the internal circuitry as well as providing supply voltage to the gate drive circuit.

### Soft-Start/Enable

The soft-start time is externally programmable with capacitor connected to the SS/EN pin. A constant current source provides the current to the SS/EN pin to generate a linear start-up time versus the capacitance value. The SS/EN pin clamps the error amplifier output voltage, limiting the rate of increase in duty cycle. By controlling the rate of rise in duty cycle gradually, the output voltage rises gradually preventing the output voltage from overshooting. The SS/EN pin can also be used to enable or disable the output driver section with an external logic signal.

### Synchronization

The synchronization to external clock is easily accomplished by connecting the external clock into the SYNC pin (Si9119 only). The logic high to low transition synchronizes the clock. The external clock frequency must be at least 5% faster than the internal clock frequency.

### Reference Voltage

The reference voltage for the Si9118/Si9119 are set at 4.0 V. The reference voltage is not connected to the non-inverting inputs of the error amplifier, therefore, the minimum output voltage is not limited to reference voltage. The  $V_{REF}$  pin requires a 0.1- $\mu$ F decoupling capacitor.

### Error Amplifier

The error amplifier gain-bandwidth product is critical parameter which determines the transient response of converter. The transient response is function of both small and large signal responses. The small signal response is determined by the feedback compensation network while the large signal response is determined by the inductor di/dt slew rate. Besides the

inductance value, the error amplifier gain-bandwidth determines the converter response time. In order to minimize the response time, Si9118/Si9119 is designed with a 2.7-MHz error amplifier gain-bandwidth product to provide the widest converter bandwidth possible.

### PWM Mode

The converter operates in PWM mode if the PWM/ $\overline{PSM}$  pin is connected to  $V_{REF}$  pin or logic high. As the load current and line voltage vary, the Si9118/Si9119 maintain constant switching frequency until they reach minimum duty cycle. Once the output voltage regulation is exceeded with minimum duty cycle, the switching frequency will continue to decrease until regulation is achieved. The switching frequency is controlled by the external  $R_{OSC}$  and  $C_{OSC}$  as shown by the typical oscillator frequency curve. In PWM mode, output ripple noise is constant reducing EMI concerns as well as simplifying the filter to minimize the system noise.

### Pulse Skipping Mode

If the PWM/ $\overline{PSM}$  pin is connected to  $-V_{IN}$  pin (logic low), the converter can operate in either PWM or PSM mode depending on the load current. The converter automatically transitions from PWM to PSM or vice versa to maintain output voltage regulation. In PSM mode, the MOSFET switch is turned on until the peak current sensed voltage reaches 100 mV and the output voltage meets or exceeds its regulation voltage. The converter is operating in pulse skipping mode because each pulse delivers excess energy into the output capacitor forcing the output voltage to exceed its regulation voltage. By forcing the output voltage to exceed the regulation voltage, succeeding pulses are skipped until the output voltage drops below the regulation point. Therefore, switching frequency will continue to reduce during PSM control as the demand for output current decreases. The pulse skipping mode cuts down the switching losses, the dominant power consumed during low output current, thereby maintaining high efficiency throughout the entire load range. With PWM/ $\overline{PSM}$  pin in logic low state, the converter transitions back into PWM mode, if the peak current sensed voltage of 100 mV does not generate the required output voltage. In the region between pulse skipping mode and PWM mode, the controller may transition between the two modes, delivering spurts of pulses. This may cause the current waveform to look irregular, but this will not overly affect the ripple voltage. Even in this transitional mode, efficiency remains high.

### Programmable Duty Cycle Control

The maximum duty cycle limit is controlled by the voltage on  $D_{MAX}$  pin. A  $D_{MAX}$  voltage of 3.2 V generates 80% duty cycle while 0.0 V generates 0% duty cycle. The 80% duty cycle is maximum default condition at 1-MHz switching frequency. The  $D_{MAX}$  voltage can be easily generated using resistor divider from the reference voltage.



## DETAILED OPERATIONAL DESCRIPTION (CONT'D)

The maximum duty cycle limitation will be different when the converter is synchronized by an external frequency. If the internal free running frequency is much slower than the external SYNC signal (SYNC signal causes the internal clock to reset before the  $C_{OSC}$  voltage ramps to 3.2 V), duty cycle is determined by the one shot discharge time of the oscillator capacitor (100 ns). Therefore, with 1-MHz SYNC signal, maximum duty cycle of 90% can be achieved (100 ns is 10% of 1 MHz). If the internal free running frequency is very close to the external SYNC frequency (SYNC signal causes the internal clock to reset somewhere between 3.2 V to 4 V), duty cycle is determined by the ratio of  $C_{OSC}$  voltage at the SYNC point and the 3.2 V. At this condition, the maximum duty cycle can be greater than 90%. Therefore,  $D_{MAX}$  voltage must be modified in order to maintain desired maximum duty cycle.

### Slope Compensation

Slope compensation is necessary for duty cycles greater than 50% to stabilize the inner current loop and maintain overall loop stability. In order to simplify the slope compensation circuitry, the Si9118 provides the buffered oscillator ramp signal,  $V_{SC}$  to be used for external slope compensation.  $V_{SC}$  is only available when DR is high. The  $V_{SC}$  signal super-imposed with actual current sense signal should be used by the PWM comparator to determine the duty cycle. The summation of this signal should be fed into  $I_{CS}$  pin. For optimum performance, proper slope compensation is required. The amount of slope compensation is determined by

the resistors connected to the  $I_{CS}$  pin. The amplitude of the  $V_{SC}$  signal is same as the  $C_{OSC}$  pin voltage ( $\approx 4$  V). For designs which use with SYNC pin, instead of  $V_{SC}$  pin, the converter can still operate at duty cycles greater than 50% by generating an external slope compensation ramp using a simple RC circuit from the MOSFET driver output pin as shown on the application circuit.

### Over Current Protection

Si9118/Si9119 are designed with a pulse-to-pulse peak current limiting protection circuit to protect itself, and the load in case of a failure. The voltage across the sense resistor is monitored continuously and if the voltage reaches its trigger level, the duty cycle is terminated. This limits the maximum current delivered to the load. In order to improve the accuracy of over current protection from traditional controllers, Si9118/Si9119 are designed with separate  $I_{LIMIT}$  and  $I_{CS}$  pins. Voltage on the  $I_{LIMIT}$  pin does not sum in the traditional slope compensation voltage, which adds error into the detection level.  $I_{CS}$  pin is used to sum the current sense signal and the slope compensation for loop stability.

### Output Driver Stage

The DR pin is designed to drive a low-side n-channel MOSFET. The driver stage is sized to sink and source peak currents up to 500 mA with  $V_{CC} = 12$  V. This provides ample drive capability for 50 W of output power.