LM158W-LM258W-LM358W

Low power dual operational amplifiers

Features

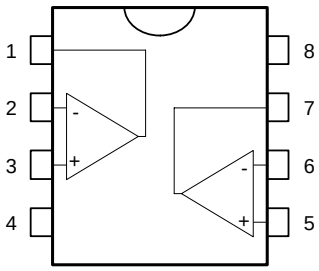
- Internally frequency compensated
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 1.1 MHz (temperature compensated)
- Very low supply current per operator essentially independent of supply voltage
- Low input bias current: 20 nA (temperature compensated)
- Low input offset voltage: 2 mV
- Low input offset current: 2 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V to (V_{CC} - 1.5 V)
- ESD internal protection: 2 kV

N
DIP-8
(Plastic package)

D & S
SO-8 & miniSO-8
(Plastic micropackage)

P
TSSOP8
(Thin shrink small outline package)

Pin connections
(top view)



1 - Output 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

Description

These circuits consist of two independent, high-gain, internally frequency-compensated which were designed specifically to operate from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage.

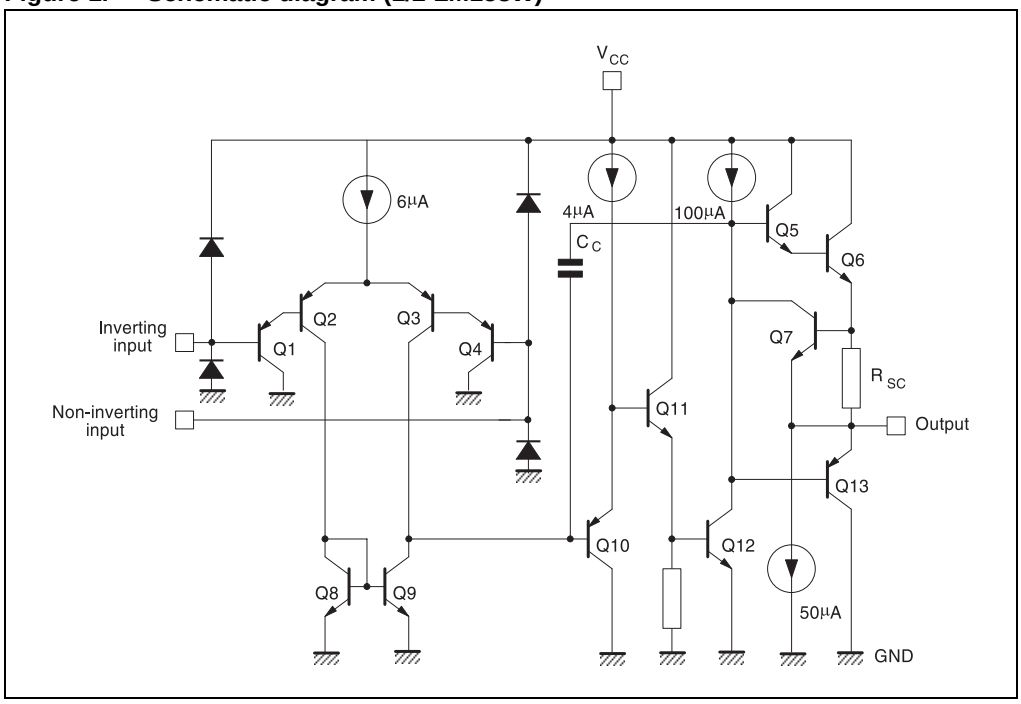
Application areas include transducer amplifiers, DC gain blocks and all the conventional op-amp circuits which now can be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with the standard +5 V which is used in logic systems and will easily provide the required interface electronics without requiring any additional power supply.

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

Contents

1 Schematic diagram

Figure 1. Schematic diagram (1/2 LM158W)



2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	LM158W/AW	LM258W/AW	LM358W/AW	Unit
V_{CC}	Supply voltage	+32			V
Vi	Input voltage	-0.3 to V_{CC} +0.3			V
V_{id}	Differential input voltage	-0.3 to V_{CC} +0.3			V
P_{tot}	Power dissipation (1)	500			mW
	Output short-circuit duration (2)	Infinite			
I_{in}	Input current (3)	50			mA
T_{oper}	Operating free-air temperature range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage temperature range	-65 to +150			°C
R_{thja}	Thermal resistance junction to ambient(4) (5)				°C/W
	SO-8	125			
	MiniSO-8	190			
	TSSOP8	120			
	DIP-8	85			
R_{thjc}	Thermal resistance junction to case				°C/W
	SO-8	40			
	MiniSO-8	39			
	TSSOP8	37			
	DIP-8	41			
ESD	HBM: human body model(6)	2			kV
	MM: machine model(7)	200			V
	CDM: charged device model(8)	1.5			kV

1. Power dissipation must be considered to ensure maximum junction temperature (T_j) is not exceeded.
2. Short-circuits from the output to V_{CC} can cause excessive heating if V_{CC} > 15V. The maximum output current is approximately 40 mA independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
3. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time during which an input is driven negative. This is not destructive and normal output will be restored for input voltage higher than -0.3 V.
4. Short-circuits can cause excessive heating and destructive dissipation.
5. R_{th} are typical values.
6. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
7. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
8. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	3 to 32	V
V_{icm}	Common mode input voltage range T_{amb} = +25° C	V_{DD} -0.3 to V_{CC} -1.5	V
T_{oper}	Operating free air temperature range LM158W LM258W LM358W LM258WY-LM358WY	 -55 - +125 -40 - +105 0 - +70 -40 - +125	°C

3 Electrical characteristics

Table 3. V_{CC}^+ = +5 V, V_{CC}^- = Ground, V_o = 1.4 V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	LM158AW-LM258AW LM358AW			LM158W-LM258W LM358W			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input offset voltage (1) T_{amb} = +25° C - except LM158AW/358W T_{amb} = +25° C - LM158AW/358W		 1 1	 3 2		 2 2	 5 7	mV
	$T_{min} \le T_{amb} \le T_{max}$ - except LM358W $T_{min} \le T_{amb} \le T_{max}$ - LM358W			4			7 9	mV
I_{io}	Input offset current T_{amb} = +25° C $T_{min} \le T_{amb} \le T_{max}$		2	 10 30		2	 30 40	nA
I_{ib}	Input bias current (2) T_{amb} = +25 °C $T_{min} \le T_{amb} \le T_{max}$		20	 50 100		20	 150 200	nA
A_{vd}	Large signal voltage gain: V_{CC} = +15 V, R_L = 2 kΩ, V_o = 1.4 V to 11.4 V T_{amb} = +25 °C $T_{min} \le T_{amb} \le T_{max}$	 50 25	 100		 50 25	 100		V/mV
SVR	Supply voltage rejection ratio ($R_s \le$10 kΩ) V_{CC}^+ = 5 V to 30 V T_{amb} = +25° C $T_{min} \le T_{amb} \le T_{max}$	 65 65	 100		 65 65	 100		dB
I_{CC}	Supply current, all amp, no load $T_{min} \le T_{amb} \le T_{max}$, V_{CC} = +5 V $T_{min} \le T_{amb} \le T_{max}$, V_{CC} = +30 V		0.7	1.2 2		0.7	1.2 2	mA
V_{icm}	Input common mode voltage range V_{CC} = +30 V (3) T_{amb} = +25° C $T_{min} \le T_{amb} \le T_{max}$	 0 0		 V_{CC}^+ -1.5 V_{CC}^+ -2	 0 0		 V_{CC}^+ -1.5 V_{CC}^+ -2	V
CMR	Common mode rejection ratio ($R_s \le$10kΩ) T_{amb} = +25° C $T_{min} \le T_{amb} \le T_{max}$	70 60	85		70 60	85		dB
I_{source}	Output current source V_{CC} = +15 V, V_o = +2 V, V_{id} = +1 V	20	40	60	20	40	60	mA
I_{sink}	Output sink current (V_{id} = -1 V) V_{CC} = +15V, V_o = +2V V_{CC} = +15V, V_o = +0.2V	10 12	20 50		10 12	20 50		mA µA

Table 3. V_{CC}^+ = +5 V, V_{CC}^-= Ground, V_o = 1.4 V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	LM158AW-LM258AW LM358AW			LM158W-LM258W LM358W			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OPP}	Output voltage swing (R_L = 2kΩ) T_{amb} = +25° C $T_{min} \le T_{amb} \le T_{max}$	0 0		V_{CC}^+ -1.5 V_{CC}^+ -2	0 0		V_{CC}^+ -1.5 V_{CC}^+ -2	V
V_{OH}	High level output voltage (V_{CC}^+ = 30 V) T_{amb} = +25°C, R_L = 2 kΩ $T_{min} \le T_{amb} \le T_{max}$ T_{amb} = +25° C, R_L = 10 kΩ $T_{min} \le T_{amb} \le T_{max}$	26 26 27 27	27 28 		26 26 27 27	27 28 		V
V_{OL}	Low level output voltage (R_L = 10 kΩ) T_{amb} = +25° C $T_{min} \le T_{amb} \le T_{max}$		5	20 20		5	20 20	mV
SR	Slew rate V_{CC} = 15 V, V_i = 0.5 to 3 V, R_L = 2 kΩ, C_L = 100 pF, unity Gain	0.3	0.6		0.3	0.6		V/µs
GBP	Gain bandwidth product V_{CC} = 30 V, f =100 kHz, V_{in} =10 mV, R_L=2 kΩ, C_L = 100 pF	0.7	1.1		0.7	1.1		MHz
THD	Total harmonic distortion f = 1 kHz, A_v = 20 dB, R_L = 2 kΩ, V_o = 2 V_{pp}, C_L = 100 pF, V_O = 2 V_{pp}		0.02			0.02		%
e_n	Equivalent input noise voltage f = 1 kHz, R_s = 100 Ω, V_{CC} = 30 V		55			55		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input offset voltage drift		7	15		7	30	µV/°C
DI_{io}	Input offset current drift		10	200		10	300	pA/°C
V_{o1}/V_{o2}	Channel separation (4) 1 kHz ≤ f ≤ 20 kHz		120			120		dB

1. V_o = 1.4 V, R_s = 0 Ω, 5 V < V_{CC}^+ < 30 V, 0 < V_{ic} < V_{CC}^+ - 1.5 V
2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so there is no load change on the input lines.
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC}^+ - 1.5 V, but either or both inputs can go to +32 V without damage.
4. Due to the proximity of external components ensure that there is no coupling originating via stray capacitance between these external parts. Typically, this can be detected at higher frequencies because then this type of capacitance increases.

Figure 2. Open loop frequency response

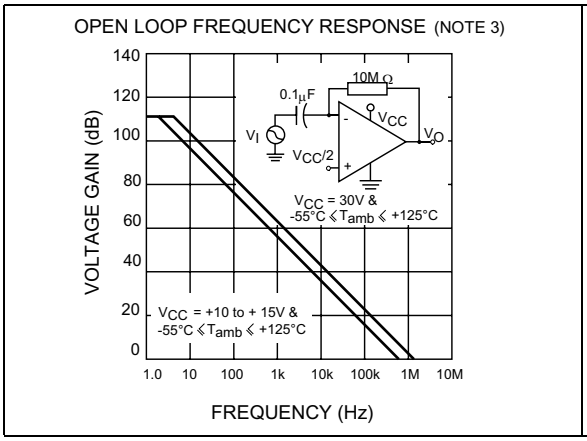


Figure 3. Large signal frequency response

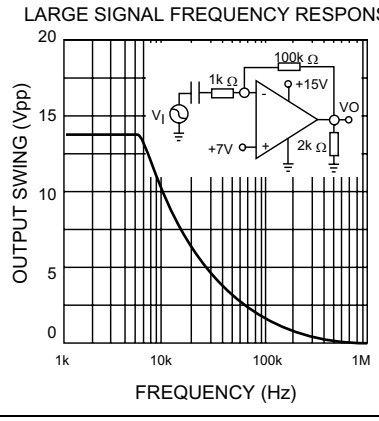


Figure 4. Voltage follower pulse response

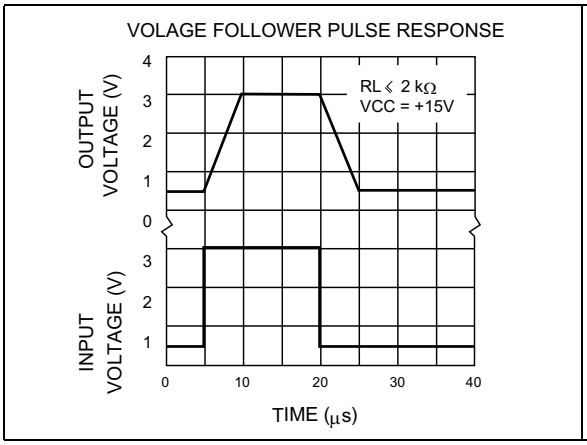


Figure 5. Voltage follower pulse response

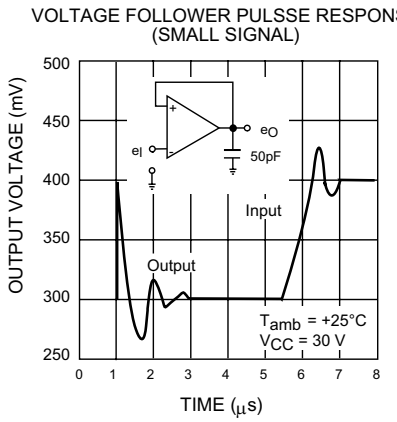


Figure 6. Input current

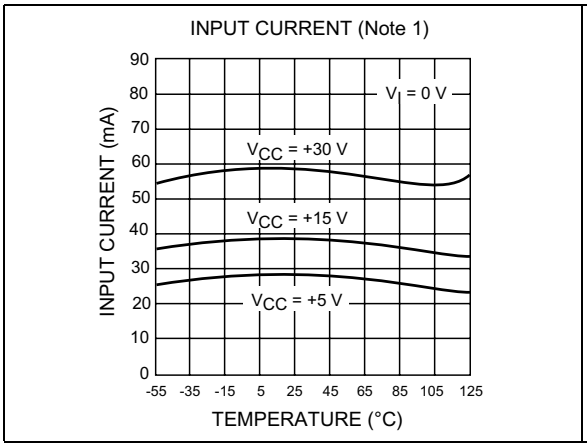


Figure 7. Output characteristics

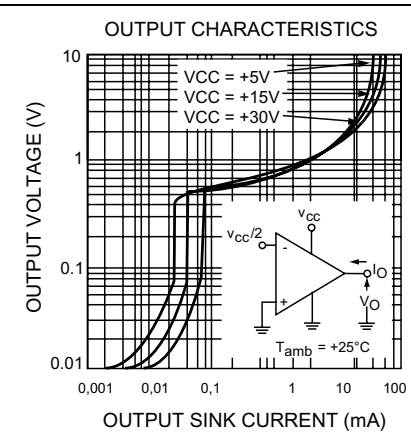


Figure 8. Output characteristics

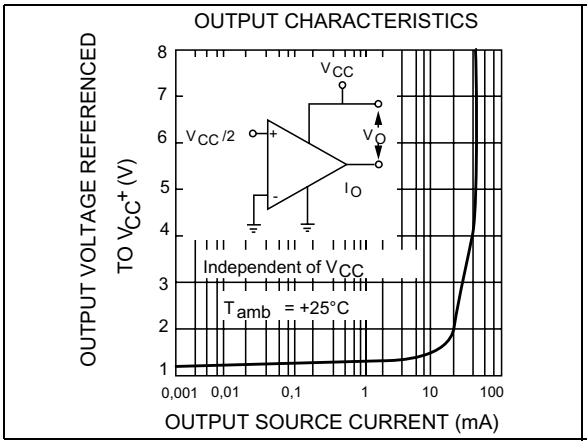


Figure 9. Current limiting

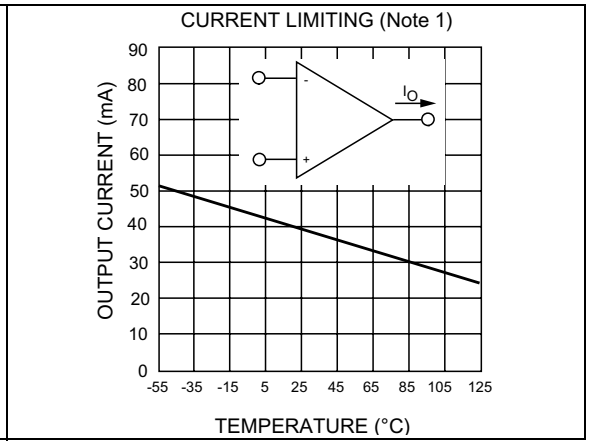


Figure 10. Input voltage range

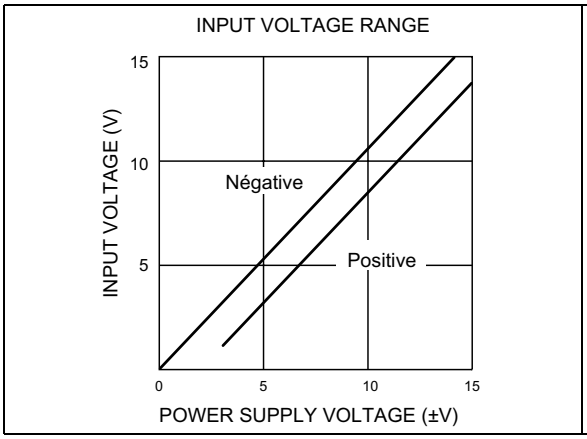


Figure 11. Positive supply voltage

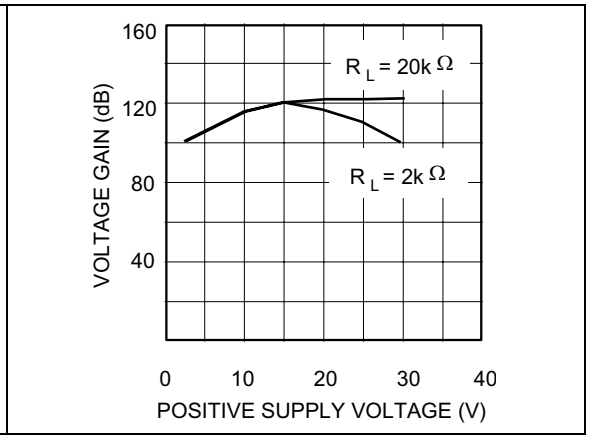


Figure 12. Input voltage range

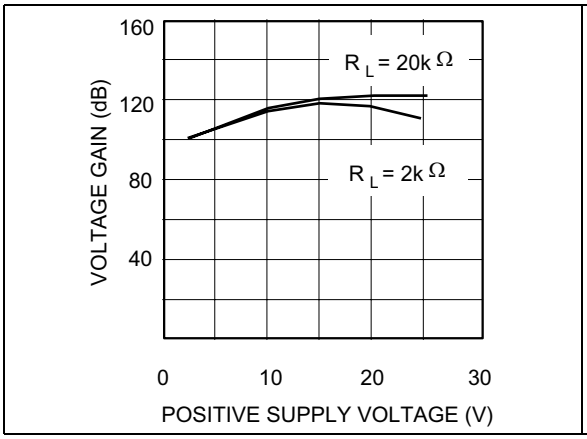


Figure 13. Supply current

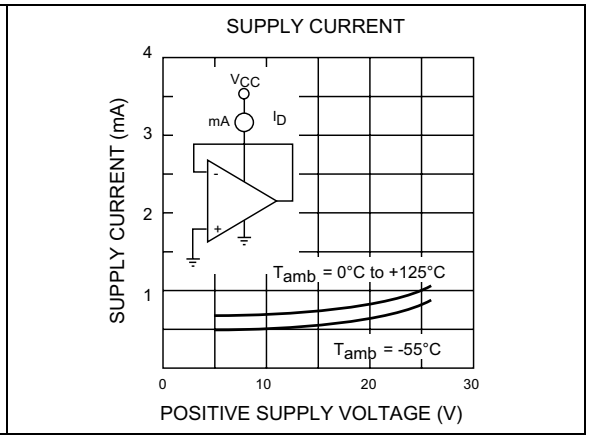


Figure 14. Input current

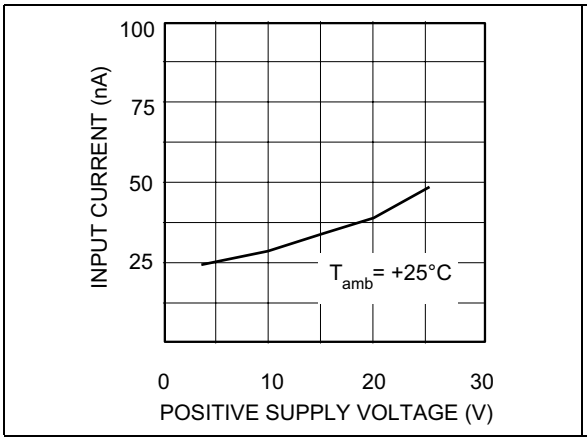


Figure 15. Gain bandwidth product

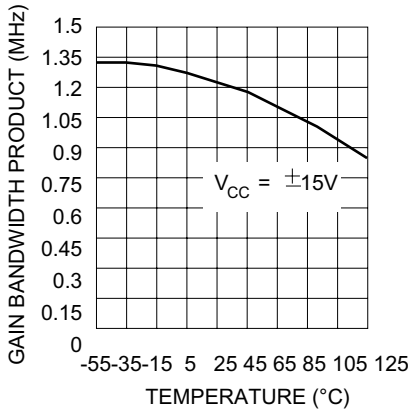


Figure 16. Power supply rejection ratio

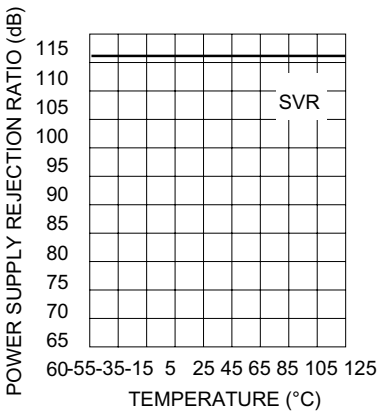


Figure 17. Common mode rejection ratio

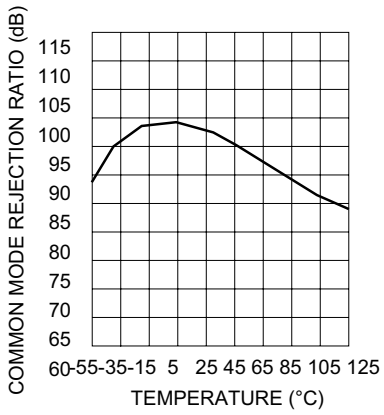
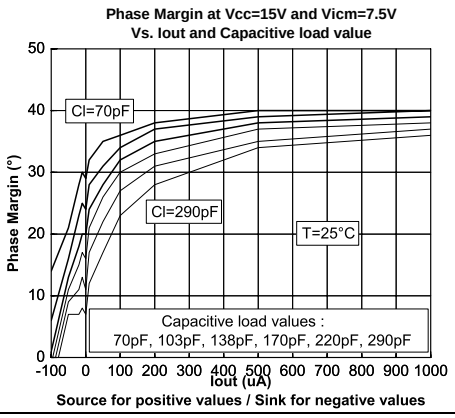


Figure 18. Phase margin vs capacitive load



4 Typical applications

Single supply voltage V_{CC} = +5 V_{DC}

Figure 19. AC coupled inverting amplifier

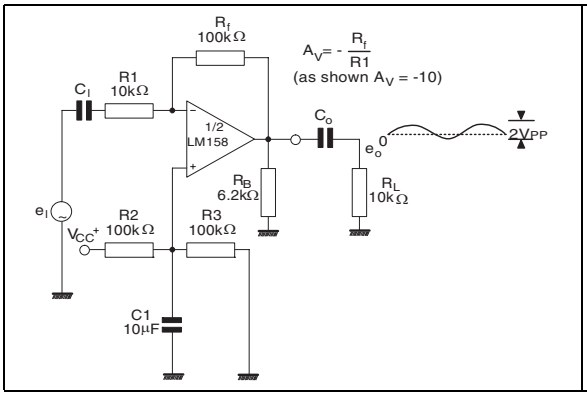


Figure 20. Non-inverting DC amplifier

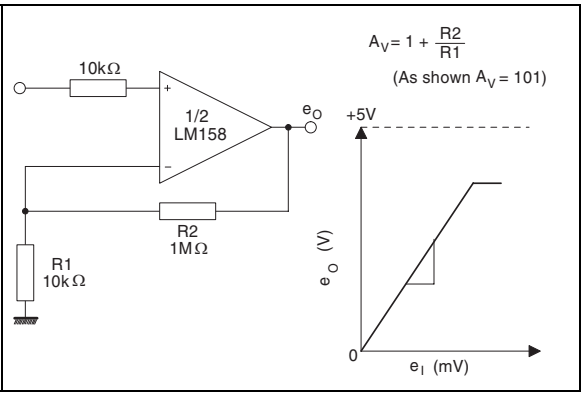


Figure 21. AC coupled non-inverting amplifier

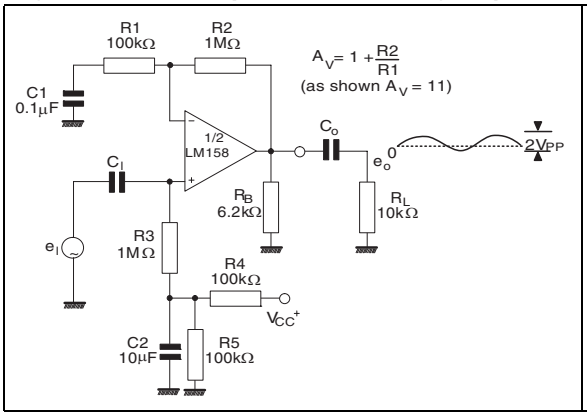
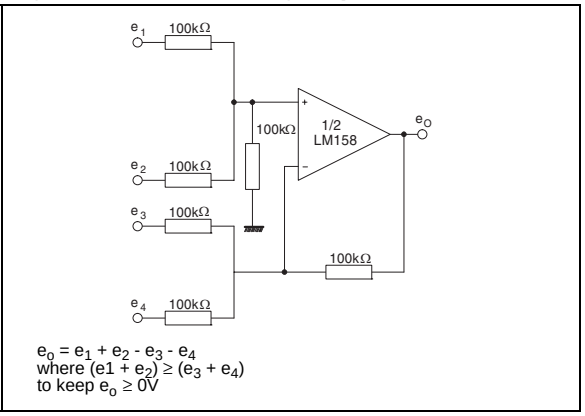
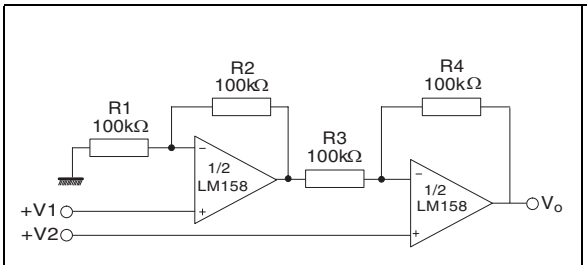


Figure 22. DC summing amplifier



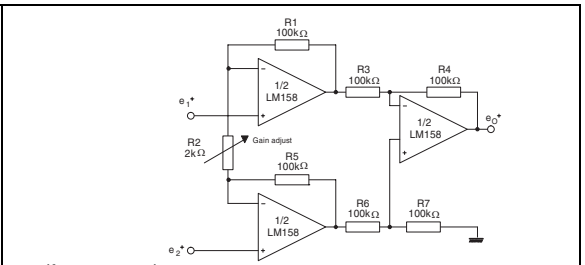
$e_o = e_1 + e_2 - e_3 - e_4$
where $(e1 + e_2) \geq (e_3 + e_4)$
to keep $e_o \geq 0V$

Figure 23. High input Z, DC differential amplifier



if R1 = R5 and R3 = R4 = R6 = R7
$e_o = [1 + \frac{2R1}{R2}] ((e_2 + e_1)$
As shown $e_o = 101 (e_2 + e_1)$

Figure 24. High input Z adjustable gain DC instrumentation amplifier



if R1 = R5 and
R3 = R4 = R6 = R7
$e_o = [1 + \frac{2R1}{R2}] ((e_2 + e_1)$

As shown $e_o = 101 (e_2 + e_1)$

Figure 25. Using symmetrical amplifiers to reduce input current

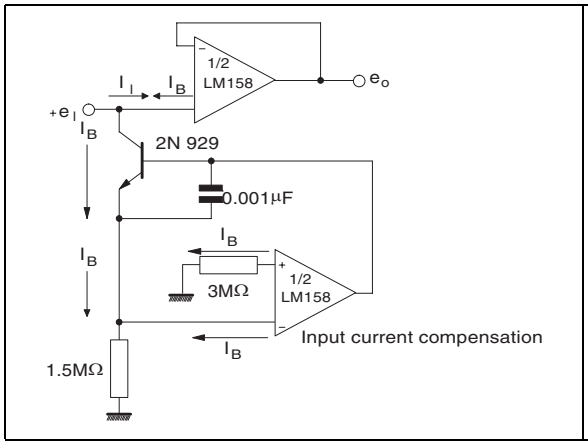


Figure 26. Low drift peak detector

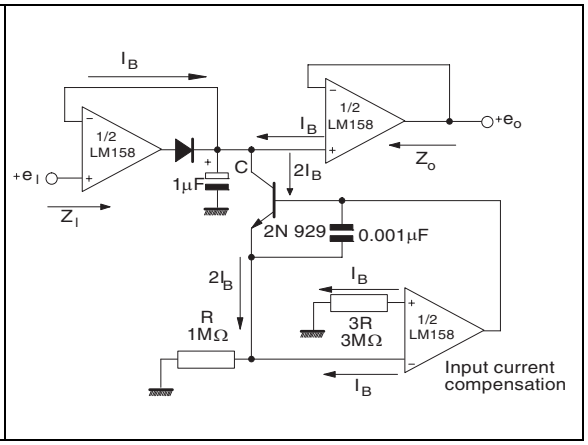
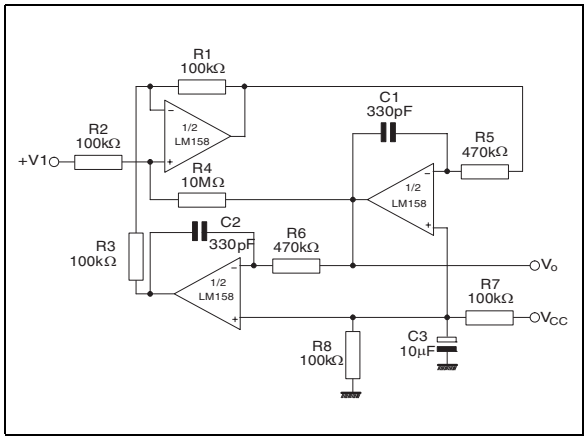


Figure 27. Active band-pass filter

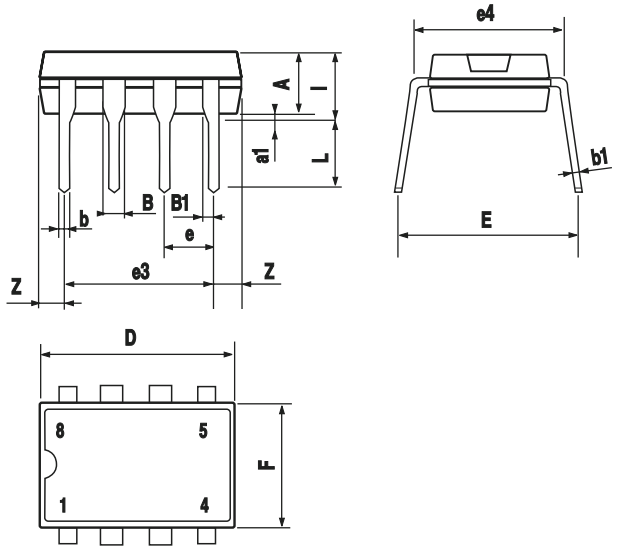


5 Package mechanical data

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

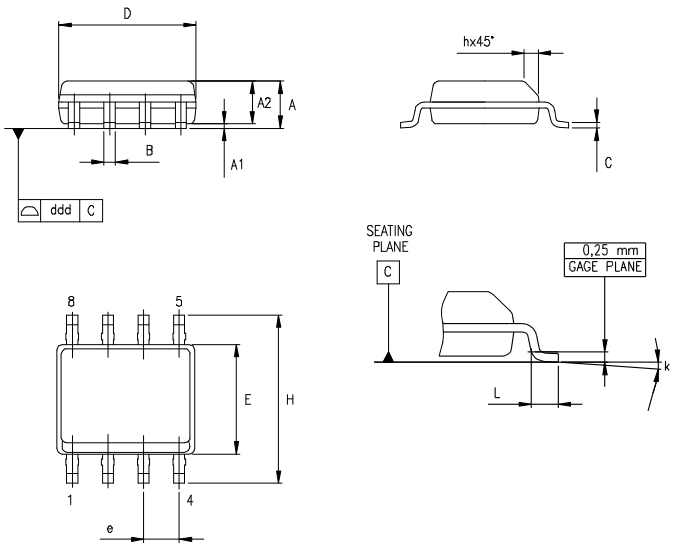
5.1 DIP8 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.3			0.130	
a1	0.7			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
I			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063



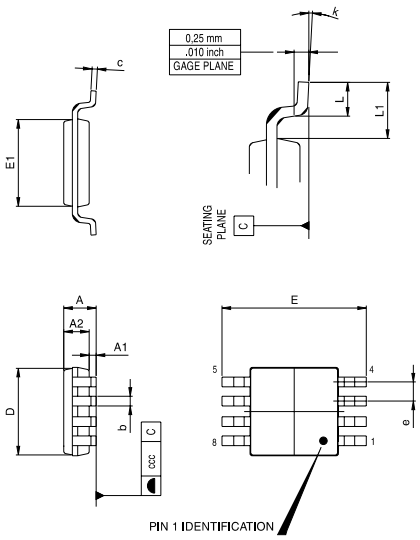
5.2 SO-8 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



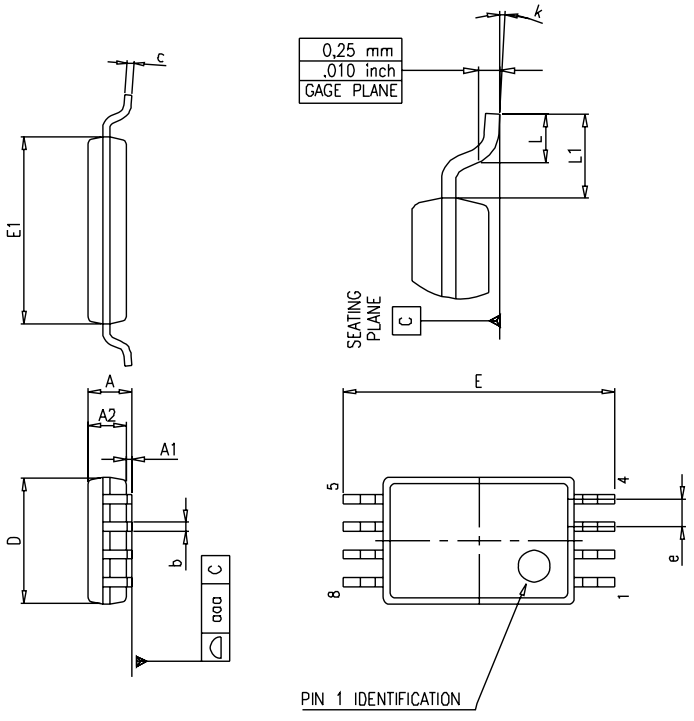
5.3 MiniSO-8 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.034	0.037
b	0.25	0.33	0.40	0.010	0.13	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	0.114	0.118	0.122
e		0.65			0.026	
K	0°		6°	0°		6°
L	0.40	0.55	0.70	0.016	0.022	0.028
L1			0.10			0.004



5.4 TSSOP8 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	



6 Ordering information

Part number	Temperature range	Package	Packaging	Marking
LM158WN	-55°C, +125°C	DIP-8	Tube	LM158WN
LM158WD LM158WDT		SO-8	Tube or tape & reel	158W
LM258WAN	-40°C, +105°C	DIP-8	Tube	LM258WA
LM258WAD LM258WADT		SO-8	Tube or tape & reel	258WA
LM258WN		DIP-8	Tube	LM258WN
LM258WD LM258WDT		SO-8	Tube or tape & reel	258W
LM358WN	0°C, +70°C	DIP-8	Tube	LM358WN
LM358WD LM358WDT		SO-8	Tube or tape & reel	358W
LM358AWD LM358AWDT				358AW
LM258WYPT (automotive grade)(1)	40°C, +125°C	TSSOP-8	Tape & reel	K411
LM258AWYPT (automotive grade)(1)		TSSOP-8	Tape & reel	K410
LM258WYD LM258WYDT (automotive grade)(1)		SO-8	Tube or tape & reel	258WY
LM258AWYD LM258AWYDT (automotive grade)(1)		SO-8	Tube or tape & reel	258AWY
LM358WYD LM358WYDT (automotive grade)(1)		SO-8	Tube or tape & reel	358WY
LM358AWYD LM358AWYDT (automotive grade)(1)		SO-8	Tube or tape & reel	358AWY
LM358WYPT (automotive grade)(1)		TSSOP-8	Tape & reel	K412
LM358AWYPT (automotive grade)(1)		TSSOP-8	Tape & reel	K413

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.

7 Revision history

Date	Revision	Changes
1-Nov-2002	1	First release.
1-Jul-2005	2	ESD protection inserted in *Table 1: Absolute maximum ratings on page 4*.
6-Oct-2006	3	ESD tolerance for model HBM improved to 2kV (*Table 1: Absolute maximum ratings on page 4*). R_{thja} and R_{thjc} typical values added in *Table 1: Absolute maximum ratings on page 4*. Added *Figure 18: Phase margin vs capacitive load on page 10*.
2-Jan-2007	4	Order codes added (automotive grade level) to *Section 6: Ordering information*.
15-Mar-2007	5	Previously called revision 4. Footnote for automotive grade order codes added to *Section 6: Ordering information*.
25-Apr-2007	6	Added missing Revision 4 of January 2007 in revision history. Corrected revision number of March 2007 to Revision 5.

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