National Semiconductor

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LM2524D/LM3524D Regulating Pulse Width Modulator

General Description

The LM3524D family is an improved version of the industry standard LM3524. It has improved specifications and additional features yet is pin for pin compatible with existing 3524 families. New features reduce the need for additional external circuitry often required in the original version.

The LM3524D has a ±1% precision 5V reference. The current carrying capability of the output drive transistors has been raised to 200 mA while reducing V_{CEsat} and increasing V_{CE} breakdown to 60V. The common mode voltage range of the error-amp has been raised to 5.5V to eliminate the need for a resistive divider from the 5V reference.

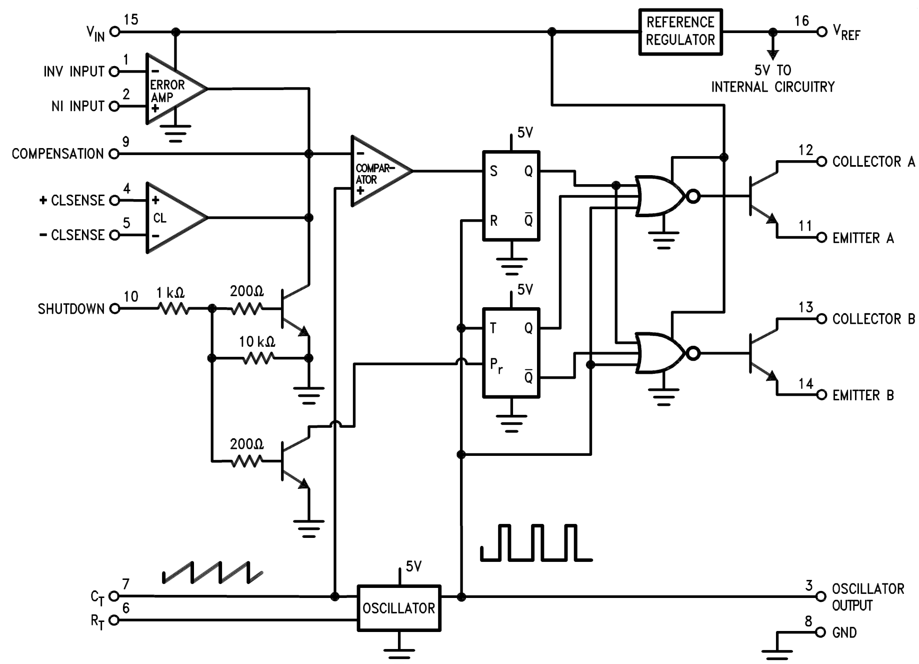
In the LM3524D the circuit bias line has been isolated from the shut-down pin. This prevents the oscillator pulse amplitude and frequency from being disturbed by shut-down. Also at high frequencies (≅300 kHz) the max. duty cycle per output has been improved to 44% compared to 35% max. duty cycle in other 3524s.

In addition, the LM3524D can now be synchronized externally, through pin 3. Also a latch has been added to insure one pulse per period even in noisy environments. The LM3524D includes double pulse suppression logic that insures when a shut-down condition is removed the state of the T-flip-flop will change only after the first clock pulse has arrived. This feature prevents the same output from being pulsed twice in a row, thus reducing the possibility of core saturation in push-pull designs.

Features

- Fully interchangeable with standard LM3524 family
- ±1% precision 5V reference with thermal shut-down
- Output current to 200 mA DC
- 60V output capability
- Wide common mode input range for error-amp
- One pulse per period (noise suppression)
- Improved max. duty cycle at high frequencies
- Double pulse suppression
- Synchronize through pin 3

Block Diagram



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Absolute Maximum Ratings (Note 5)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	40V
Collector Supply Voltage	
(LM2524D)	55V
(LM3524D)	40V
Output Current DC (each)	200 mA
Oscillator Charging Current (Pin 7)	5 mA
Internal Power Dissipation	1W
Operating Junction Temperature	
Range (Note 2)	
LM2524D	−40˚C to +125˚C
LM3524D	0˚C to +125˚C
Maximum Junction Temperature	150˚
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (Soldering 4 sec.)	
M, N Pkg.	260˚C

Electrical Characteristics

(Note 1)

Symbol	Parameter	Conditions	LM2524D Typ	LM2524D Tested Limit (Note 3)	LM2524D Design Limit (Note 4)	LM3524D Typ	LM3524D Tested Limit (Note 3)	LM3524D Design Limit (Note 4)	Units
REFERENCE SECTION									
V_{REF}	Output Voltage		5	4.85	**4.80**	5	4.75		V_{Min}
				5.15	**5.20**		5.25		V_{Max}
V_{RLine}	Line Regulation	V_{IN} = 8V to 40V	10	15	**30**	10	25	50	mV_{Max}
V_{RLoad}	Load Regulation	I_L = 0 mA to 20 mA	10	15	**25**	10	25	50	mV_{Max}
$\frac{\Delta V_{IN}}{\Delta V_{REF}}$	Ripple Rejection	f = 120 Hz	66			66			dB
I_{OS}	Short Circuit Current	V_{REF} = 0	50	25		50	25		mA Min
				180			200		mA Max
N_O	Output Noise	10 Hz ≤ f ≤ 10 kHz	40		100	40		100	$\mu V_{rms\ Max}$
	Long Term Stability	T_A = 125˚C	20			20			mV/kHr
OSCILLATOR SECTION									
f_{OSC}	Max. Freq.	R_T = 1k, C_T = 0.001 µF (Note 7)	550		500	350			kHz_{Min}
f_{OSC}	Initial Accuracy	R_T = 5.6k, C_T = 0.01 µF (Note 7)	20	17.5		20	17.5		kHz_{Min}
				22.5			22.5		kHz_{Max}
		R_T = 2.7k, C_T = 0.01 µF (Note 7)	38	34		38	30		kHz_{Min}
				42			46		kHz_{Max}
Δf_{OSC}	Freq. Change with V_{IN}	V_{IN} = 8 to 40V	0.5	1		0.5	1.0		$\%_{Max}$
Δf_{OSC}	Freq. Change with Temp.	T_A = −55˚C to +125˚C at 20 kHz R_T = 5.6k, C_T = 0.01 µF	5			5			%
V_{OSC}	Output Amplitude (Pin 3) (Note 8)	R_T = 5.6k, C_T = 0.01 µF	3	2.4		3	2.4		V_{Min}
t_{PW}	Output Pulse Width (Pin 3)	R_T = 5.6k, C_T = 0.01 µF	0.5	1.5		0.5	1.5		μs_{Max}
	Sawtooth Peak Voltage	R_T = 5.6k, C_T = 0.01 µF	3.4	3.6	**3.8**		3.8		V_{Max}
	Sawtooth Valley Voltage	R_T = 5.6k, C_T = 0.01 µF	1.1	0.8	**0.6**		0.6		V_{Min}
ERROR-AMP SECTION									
V_{IO}	Input Offset Voltage	V_{CM} = 2.5V	2	8	**10**	2	10		mV_{Max}
I_{IB}	Input Bias	V_{CM} = 2.5V	1	8	**10**	1	10		μA_{Max}

Electrical Characteristics (Continued)

(Note 1)

Symbol	Parameter	Conditions	LM2524D			LM3524D			Units
			Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
ERROR-AMP SECTION									
	Current								
I_{IO}	Input Offset Current	V_{CM} = 2.5V	0.5	1.0	**1**	0.5	1		μA_{Max}
I_{COSI}	Compensation Current (Sink)	$V_{IN(I)} - V_{IN(NI)}$ = 150 mV	95	65 125		95	65 125		μA_{Min} μA_{Max}
I_{COSO}	Compensation Current (Source)	$V_{IN(NI)} - V_{IN(I)}$ = 150 mV	−95	−125 −65		−95	−125 −65		μA_{Min} μA_{Max}
A_{VOL}	Open Loop Gain	$R_L = \infty$, V_{CM} = 2.5 V	80	74	**60**	80	70	60	dB_{Min}
VCMR	Common Mode Input Voltage Range			1.5 5.5	**1.4** **5.4**		1.5 5.5		V_{Min} V_{Max}
CMRR	Common Mode Rejection Ratio		90	80		90	80		dB_{Min}
G_{BW}	Unity Gain Bandwidth	A_{VOL} = 0 dB, V_{CM} = 2.5V	3			2			MHz
V_O	Output Voltage Swing	$R_L = \infty$		0.5 5.5			0.5 5.5		V_{Min} V_{Max}
PSRR	Power Supply Rejection Ratio	V_{IN} = 8 to 40V	80		70	80	65		db_{Min}
COMPARATOR SECTION									
$\frac{t_{ON}}{t_{OSC}}$	Minimum Duty Cycle	Pin 9 = 0.8V, [R_T = 5.6k, C_T = 0.01 µF]	0	0		0	0		$\%_{Max}$
$\frac{t_{ON}}{t_{OSC}}$	Maximum Duty Cycle	Pin 9 = 3.9V, [R_T = 5.6k, C_T = 0.01 µF]	49	45		49	45		$\%_{Min}$
$\frac{t_{ON}}{t_{OSC}}$	Maximum Duty Cycle	Pin 9 = 3.9V, [R_T = 1k, C_T = 0.001 µF]	44	35		44	35		$\%_{Min}$
V_{COMPZ}	Input Threshold (Pin 9)	Zero Duty Cycle	1			1			V
V_{COMPM}	Input Threshold (Pin 9)	Maximum Duty Cycle	3.5			3.5			V
I_{IB}	Input Bias Current		−1			−1			µA
CURRENT LIMIT SECTION									
V_{SEN}	Sense Voltage	$V_{(Pin\ 2)} - V_{(Pin\ 1)} \geq$ 150 mV	200	180 220		200	180 220		mV_{Min} mV_{Max}
TC-V_{sense}	Sense Voltage T.C.		0.2			0.2			mV/°C
	Common Mode Voltage Range	$V_5 - V_4$ = 300 mV	−0.7 1			−0.7 1			V_{Min} V_{Max}
SHUT DOWN SECTION									
V_{SD}	High Input Voltage	$V_{(Pin\ 2)} - V_{(Pin\ 1)} \geq$ 150 mV	1	0.5 1.5		1	0.5 1.5		V_{Min} V_{Max}
I_{SD}	High Input Current	$I_{(pin\ 10)}$	1			1			mA
OUTPUT SECTION (EACH OUTPUT)									
V_{CES}	Collector Emitter Voltage Breakdown	$I_C \leq$ 100 µA		55			40		V_{Min}

Electrical Characteristics (Continued)

(Note 1)

Symbol	Parameter	Conditions	LM2524D			LM3524D			Units
			Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
OUTPUT SECTION (EACH OUTPUT)									
I_{CES}	Collector Leakage Current	V_{CE} = 60V							
		V_{CE} = 55V	0.1	50					μA_{Max}
		V_{CE} = 40V				0.1	50		
V_{CESAT}	Saturation Voltage	I_E = 20 mA	0.2	0.5		0.2	0.7		V_{Max}
		I_E = 200 mA	1.5	2.2		1.5	2.5		
V_{EO}	Emitter Output Voltage	I_E = 50 mA	18	17		18	17		V_{Min}
t_R	Rise Time	V_{IN} = 20V, I_E = −250 µA R_C = 2k	200			200			ns
t_F	Fall Time	R_C = 2k	100			100			ns
SUPPLY CHARACTERISTICS SECTION									
V_{IN}	Input Voltage Range	After Turn-on		8 40			8 40		V_{Min} V_{Max}
T	Thermal Shutdown Temp.	(Note 2)	160			160			˚C
I_{IN}	Stand By Current	V_{IN} = 40V (Note 6)	5	10		5	10		mA

Note 1: Unless otherwise stated, these specifications apply for $T_A = T_J$ = 25˚C. Boldface numbers apply over the rated temperature range: LM2524D is −40˚ to 85˚C and LM3524D is 0˚C to 70˚C. V_{IN} = 20V and f_{OSC} = 20 kHz.

Note 2: For operation at elevated temperatures, devices in the N package must be derated based on a thermal resistance of 86˚C/W, junction to ambient. Devices in the M package must be derated at 125˚C/W, junction to ambient.

Note 3: Tested limits are guaranteed and 100% tested in production.

Note 4: Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage range. These limits are not used to calculate outgoing quality level.

Note 5: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

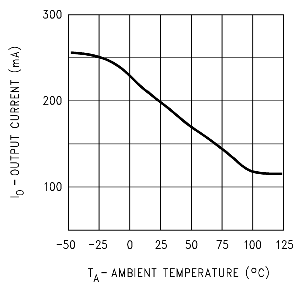
Note 6: Pins 1, 4, 7, 8, 11, and 14 are grounded; Pin 2 = 2V. All other inputs and outputs open.

Note 7: The value of a C_t capacitor can vary with frequency. Careful selection of this capacitor must be made for high frequency operation. Polystyrene was used in this test. NPO ceramic or polypropylene can also be used.

Note 8: OSC amplitude is measured open circuit. Available current is limited to 1 mA so care must be exercised to limit capacitive loading of fast pulses.

Typical Performance Characteristics

Switching Transistor Peak Output Current vs Temperature



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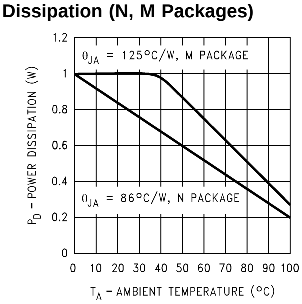
Maximum Average Power Dissipation (N, M Packages)



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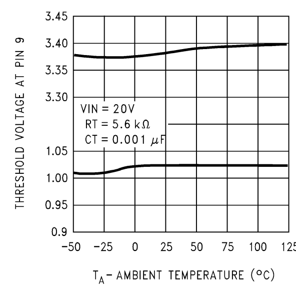
Maximum & Minimum Duty Cycle Threshold Voltage



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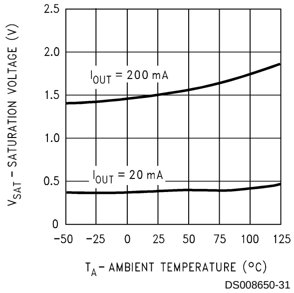
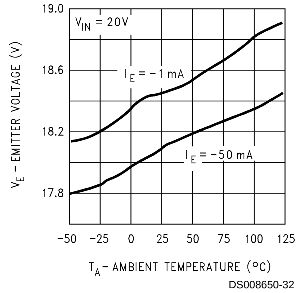
Typical Performance Characteristics (Continued)

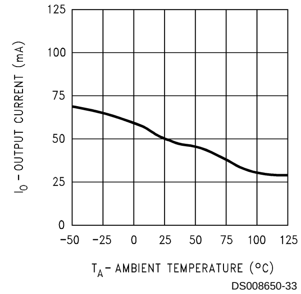
Output Transistor Saturation Voltage



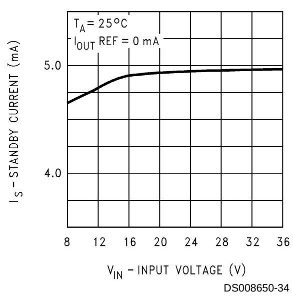
Output Transistor Emitter Voltage



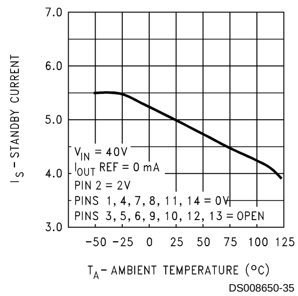
Reference Transistor Peak Output Current



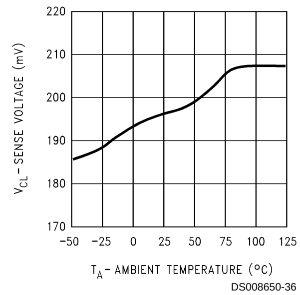
Standby Current vs Voltage



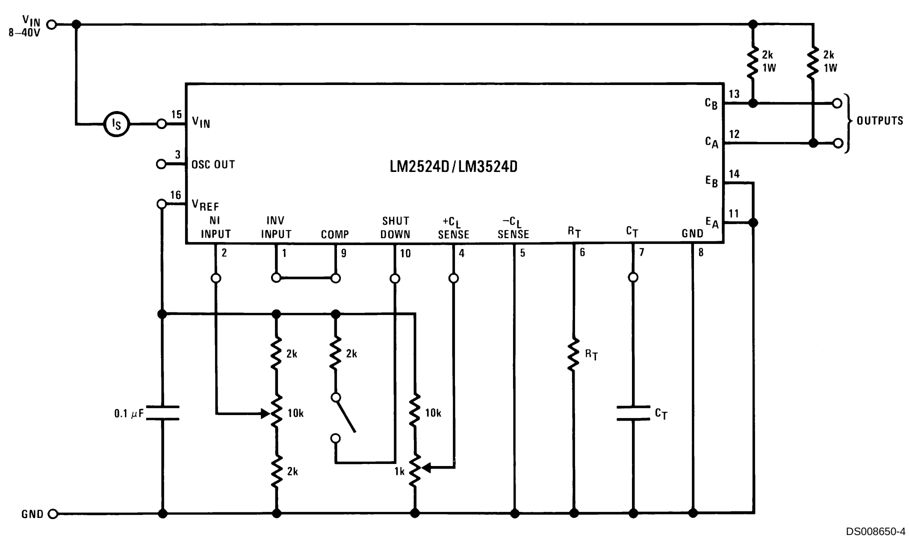
Standby Current vs Temperature



Current Limit Sense Voltage



Test Circuit

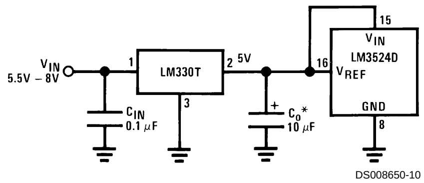


Functional Description

INTERNAL VOLTAGE REGULATOR

The LM3524D has an on-chip 5V, 50 mA, short circuit protected voltage regulator. This voltage regulator provides a supply for all internal circuitry of the device and can be used as an external reference.

For input voltages of less than 8V the 5V output should be shorted to pin 15, V_{IN}, which disables the 5V regulator. With these pins shorted the input voltage must be limited to a maximum of 6V. If input voltages of 6V–8V are to be used, a pre-regulator, as shown in *Figure 1*, must be added.



*Minimum C_O of 10 µF required for stability.

FIGURE 1.

OSCILLATOR

The LM3524D provides a stable on-board oscillator. Its frequency is set by an external resistor, R_T and capacitor, C_T. A graph of R_T, C_T vs oscillator frequency is shown is *Figure 2*. The oscillator's output provides the signals for triggering an internal flip-flop, which directs the PWM information to the outputs, and a blanking pulse to turn off both outputs during transitions to ensure that cross conduction does not occur. The width of the blanking pulse, or dead time, is controlled by the value of C_T, as shown in *Figure 3*. The recommended values of R_T are 1.8 kΩ to 100 kΩ, and for C_T, 0.001 µF to 0.1 µF.

If two or more LM3524D's must be synchronized together, the easiest method is to interconnect all pin 3 terminals, tie all pin 7's (together) to a single C_T, and leave all pin 6's open except one which is connected to a single R_T. This method works well unless the LM3524D's are more than 6" apart.

A second synchronization method is appropriate for any circuit layout. One LM3524D, designated as master, must have its R_TC_T set for the correct period. The other slave LM3524D(s) should each have an R_TC_T set for a 10% longer period. All pin 3's must then be interconnected to allow the master to properly reset the slave units.

The oscillator may be synchronized to an external clock source by setting the internal free-running oscillator frequency 10% slower than the external clock and driving pin 3 with a pulse train (approx. 3V) from the clock. Pulse width should be greater than 50 ns to insure full synchronization.

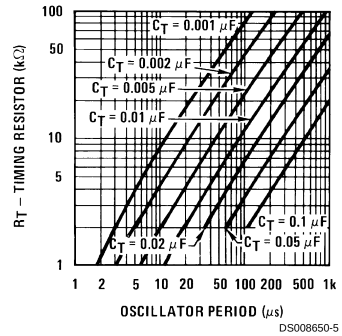


FIGURE 2.

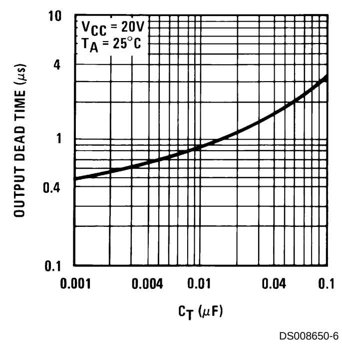


FIGURE 3.

ERROR AMPLIFIER

The error amplifier is a differential input, transconductance amplifier. Its gain, nominally 86 dB, is set by either feedback or output loading. This output loading can be done with either purely resistive or a combination of resistive and reactive components. A graph of the amplifier's gain vs output load resistance is shown in *Figure 4*.

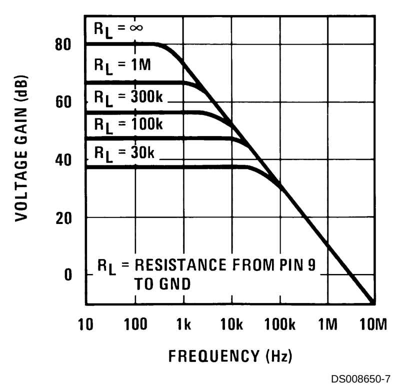


FIGURE 4.

The output of the amplifier, or input to the pulse width modulator, can be overridden easily as its output impedance is very high ($Z_O \cong 5$ MΩ). For this reason a DC voltage can be

Functional Description (Continued)

applied to pin 9 which will override the error amplifier and force a particular duty cycle to the outputs. An example of this could be a non-regulating motor speed control where a variable voltage was applied to pin 9 to control motor speed. A graph of the output duty cycle vs the voltage on pin 9 is shown in *Figure 5*.

The duty cycle is calculated as the percentage ratio of each output's ON-time to the oscillator period. Paralleling the outputs doubles the observed duty cycle.

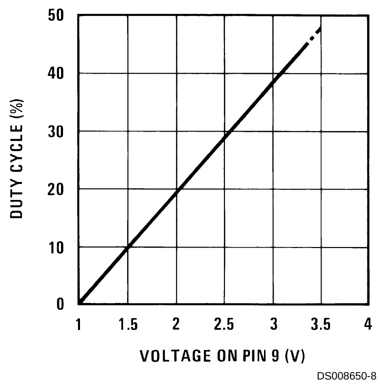


FIGURE 5.

The amplifier's inputs have a common-mode input range of 1.5V–5.5V. The on board regulator is useful for biasing the inputs to within this range.

CURRENT LIMITING

The function of the current limit amplifier is to override the error amplifier's output and take control of the pulse width. The output duty cycle drops to about 25% when a current limit sense voltage of 200 mV is applied between the $+C_L$ and $-C_L$ sense terminals. Increasing the sense voltage approximately 5% results in a 0% output duty cycle. Care should be taken to ensure the −0.7V to +1.0V input common-mode range is not exceeded.

In most applications, the current limit sense voltage is produced by a current through a sense resistor. The accuracy of this measurement is limited by the accuracy of the sense resistor, and by a small offset current, typically 100 µA, flowing from +CL to −CL.

OUTPUT STAGES

The outputs of the LM3524D are NPN transistors, capable of a maximum current of 200 mA. These transistors are driven 180° out of phase and have non-committed open collectors and emitters as shown in *Figure 6*.

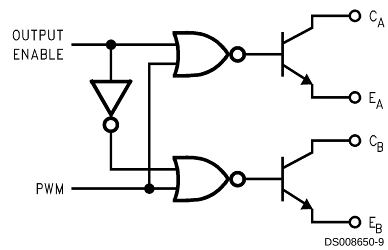
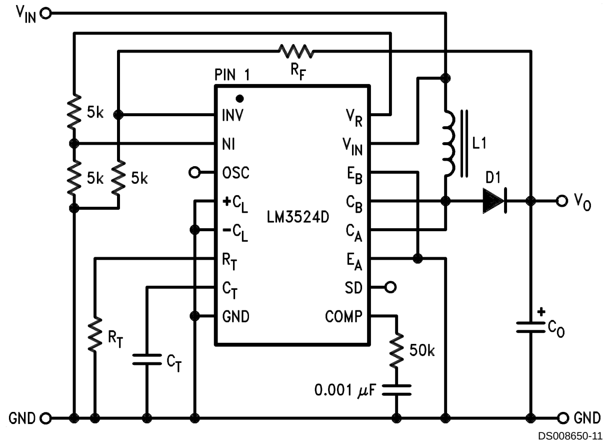


FIGURE 6.

Typical Applications



Design Equations

$$R_F = 5k\left(\frac{V_o}{2.5} - 1\right)$$

$$f_{OSC} \cong \frac{1}{R_T C_T}$$

$$L1 = \frac{2.5 V_{IN}^2 (V_o - V_{IN})}{f_{OSC} I_o V_o^2}$$

$$C_o = \frac{I_o (V_o - V_{IN})}{f_{OSC} \Delta V_o V_o}$$

$$I_{o(MAX)} = I_{IN} \frac{V_{IN}}{V_o}$$

FIGURE 7. Positive Regulator, Step-Up Basic Configuration ($I_{IN(MAX)}$ = 80 mA)

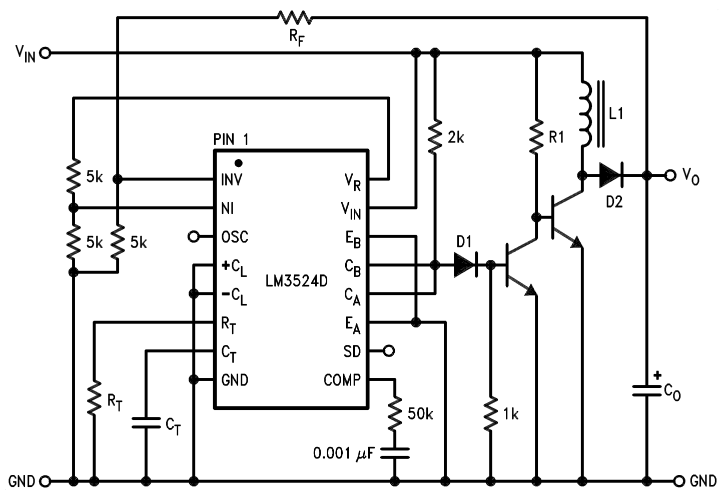
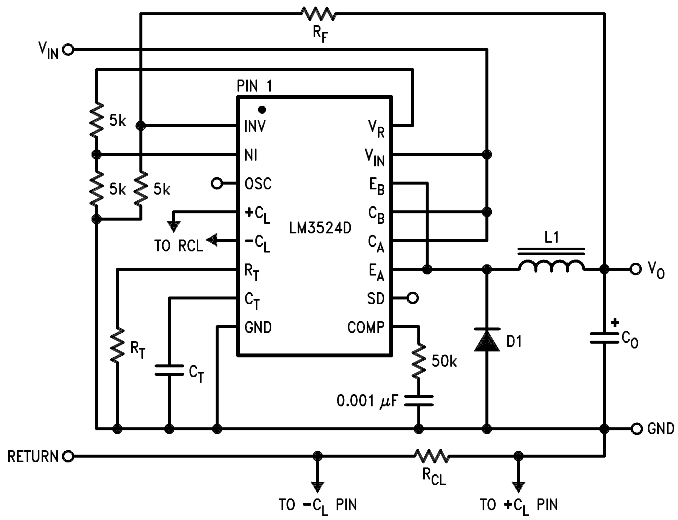


FIGURE 8. Positive Regulator, Step-Up Boosted Current Configuration

Typical Applications (Continued)



Design Equations

$R_F = 5\ k\Omega \left(\frac{V_o}{2.5} - 1\right)$

$R_{CL} = \frac{\text{Current Limit Sense Volt}}{I_{o(MAX)}}$

$f_{OSC} \cong \frac{1}{R_T C_T}$

$L1 = \frac{2.5 V_o (V_{IN} - V_o)}{I_o V_{IN} f_{OSC}}$

$C_o = \frac{(V_{IN} - V_o) V_o T^2}{8\ \Delta V_o V_{IN} L1}$

$I_{o(MAX)} = I_{IN} \frac{V_{IN}}{V_o}$

FIGURE 9. Positive Regulator, Step-Down Basic Configuration ($I_{IN(MAX)}$ = 80 mA)

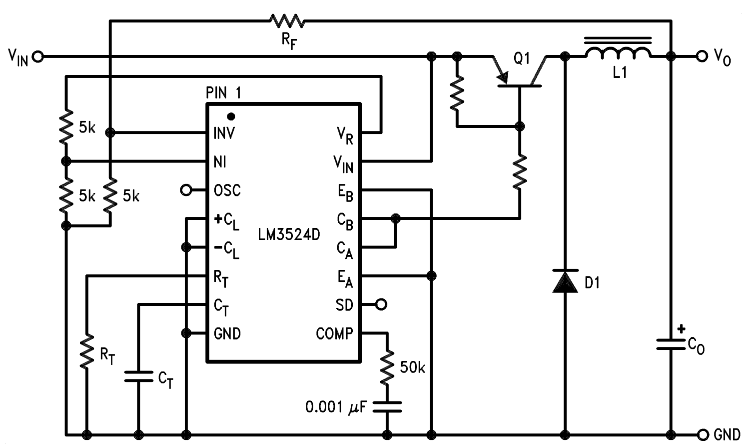
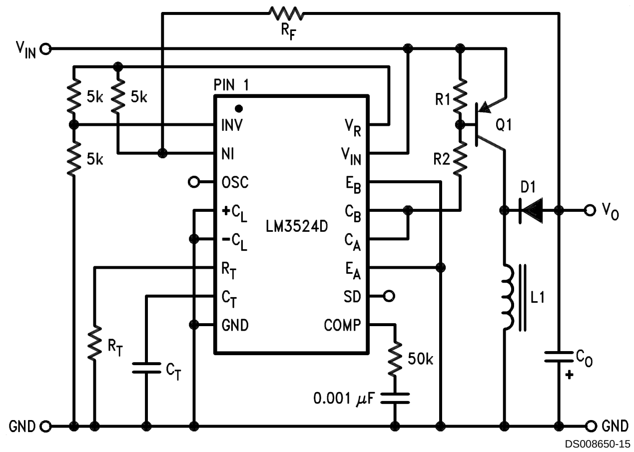


FIGURE 10. Positive Regulator, Step-Down Boosted Current Configuration



Design Equations

$$R_F = 5k \left(1 - \frac{V_o}{2.5}\right)$$

$$f_{OSC} \cong \frac{1}{R_T C_T}$$

$$L1 = \frac{2.5 V_{IN} V_o}{f_{OSC} (V_o + V_{IN}) I_o}$$

$$C_o = \frac{I_o V_o}{\Delta V_o \, f_{OSC} (V_o + V_{IN})}$$

FIGURE 11. Boosted Current Polarity Inverter

BASIC SWITCHING REGULATOR THEORY AND APPLICATIONS

The basic circuit of a step-down switching regulator circuit is shown in *Figure 12*, along with a practical circuit design using the LM3524D in *Figure 15*.

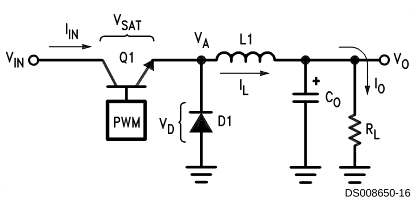


FIGURE 12. Basic Step-Down Switching Regulator

The circuit works as follows: Q1 is used as a switch, which has ON and OFF times controlled by the pulse width modulator. When Q1 is ON, power is drawn from V_{IN} and supplied to the load through L1; V_A is at approximately V_{IN}, D1 is reverse biased, and C_o is charging. When Q1 turns OFF the inductor L1 will force V_A negative to keep the current flowing in it, D1 will start conducting and the load current will flow through D1 and L1. The voltage at V_A is smoothed by the L1, C_o filter giving a clean DC output. The current flowing through L1 is equal to the nominal DC load current plus some ΔI_L which is due to the changing voltage across it. *A good rule of thumb is to set* $\Delta I_{LP-P} \cong 40\% \times I_o$.

Typical Applications (Continued)

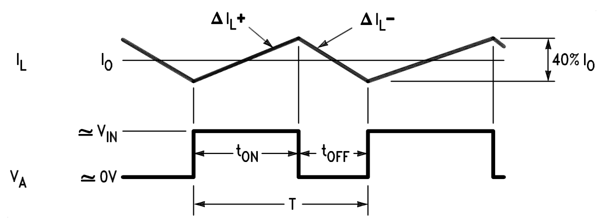


FIGURE 13. Relation of Switch Timing to Inductor Current in Step-Down Regulator

From the relation $V_L = L\frac{d_i}{d_t}$, $\Delta I_L \cong \frac{V_L T}{L1}$

$$\Delta I_L{}^+ = \frac{(V_{IN} - V_o)\,t_{ON}}{L1};\ \Delta I_L{}^- = \frac{V_o\,t_{OFF}}{L1}$$

Neglecting V_{SAT}, V_D, and settling $\Delta I_L{}^+ = \Delta I_L{}^-$;

$$\boxed{V_o \cong V_{IN}\left(\frac{t_{ON}}{t_{OFF} + t_{ON}}\right)} = V_{IN}\left(\frac{t_{ON}}{T}\right);$$

where T = Total Period

The above shows the relation between V_{IN}, V_o and duty cycle.

$$I_{IN(DC)} = I_{OUT(DC)}\left(\frac{t_{ON}}{t_{ON} + t_{OFF}}\right),$$

as Q1 only conducts during t_{ON}.

$$P_{IN} = I_{IN(DC)}\,V_{IN} = (I_{o(DC)})\left(\frac{t_{ON}}{t_{ON} + t_{OFF}}\right)V_{IN}$$

$$P_o = I_oV_o$$

The efficiency, η, of the circuit is:

$$\eta MAX = \frac{P_o}{P_{IN}} = \frac{I_oV_o}{I_o\frac{(t_{ON})}{T}V_{IN} + \frac{(V_{SAT}\,t_{ON} + V_{D1}t_{OFF})}{T}I_o}$$

$$= \boxed{\frac{V_o}{V_o + 1}}\ \text{for } V_{SAT} = V_{D1} = 1V.$$

ηMAX will be further decreased due to switching losses in Q1. For this reason Q1 should be selected to have the maximum possible f_T, which implies very fast rise and fall times.

CALCULATING INDUCTOR L1

$$t_{ON} \cong \frac{(\Delta I_L{}^+) \times L1}{(V_{IN} - V_o)},\ t_{OFF} = \frac{(\Delta I_L{}^-) \times L1}{V_o}$$

$$t_{ON} + t_{OFF} = T = \frac{(\Delta I_L{}^+) \times L1}{(V_{IN} - V_Q)} + \frac{(\Delta I_L{}^-) \times L1}{V_o}$$

$$= \frac{0.4I_oL1}{(V_{IN} - V_o)} + \frac{0.4I_oL1}{V_o}$$

Since $\Delta I_L{}^+ = \Delta I_L{}^- = 0.4I_o$

Solving the above for L1

$$\boxed{L1 = \frac{2.5\,V_o\,(V_{IN} - V_o)}{I_o\,V_{IN}\,f}}$$

where: L1 is in Henrys

f is switching frequency in Hz

Also, see LM1578 data sheet for graphical methods of inductor selection.

CALCULATING OUTPUT FILTER CAPACITOR C_o:

Figure 13 shows L1's current with respect to Q1's t_{ON} and t_{OFF} times (V_A is at the collector of Q1). This curent must flow to the load and C_o. C_o's current will then be the difference between I_L, and I_o.

$$Ic_o = I_L - I_o$$

From *Figure 13* it can be seen that current will be flowing into C_o for the second half of t_{ON} through the first half of t_{OFF}, or a time, $t_{ON}/2 + t_{OFF}/2$. The current flowing for this time is $\Delta I_L/4$. The resulting ΔV_c or ΔV_o is described by:

$$\Delta V_{op\text{-}p} = \frac{1}{C} \times \frac{\Delta I_L}{4} \times \left(\frac{t_{ON}}{2} + \frac{t_{OFF}}{2}\right)$$

$$= \frac{\Delta I_L}{4C}\left(\frac{t_{ON} + t_{OFF}}{2}\right)$$

Since $\Delta I_L = \frac{V_o(T - t_{ON})}{L1}$ and $t_{ON} = \frac{V_oT}{V_{IN}}$

$$\Delta V_{op\text{-}p} = \frac{V_o\left(T - \frac{V_oT}{V_{IN}}\right)}{4C\,L1}\left(\frac{T}{2}\right) = \frac{(V_{IN} - V_o)\,V_oT^2}{8V_{IN}C_oL1}\ \text{or}$$

$$\boxed{C_o = \frac{(V_{IN} - V_o)\,V_o\,T^2}{8\Delta V_oV_{IN}L1}}$$

where: C is in farads, T is $\frac{1}{\text{switching frequency}}$

ΔV_o is p-p output ripple

For best regulation, the inductor's current cannot be allowed to fall to zero. Some minimum load current I_o, and thus inductor current, is required as shown below:

$$I_{o(MIN)} = \frac{(V_{IN} - V_o)\,t_{ON}}{2L1} = \boxed{\frac{(V_{IN} - V_o)\,V_o}{2fV_{IN}L1}}$$

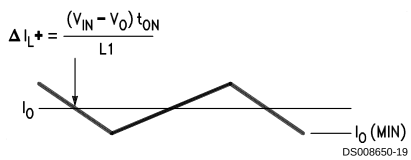


FIGURE 14. Inductor Current Slope in Step-Down Regulator

A complete step-down switching regulator schematic, using the LM3524D, is illustrated in *Figure 15*. Transistors Q1 and Q2 have been added to boost the output to 1A. The 5V regulator of the LM3524D has been divided in half to bias the error amplifier's non-inverting input to within its common-mode range. Since each output transistor is on for half the period, actually 45%, they have been paralleled to allow longer possible duty cycle, up to 90%. This makes a lower possible input voltage. The output voltage is set by:

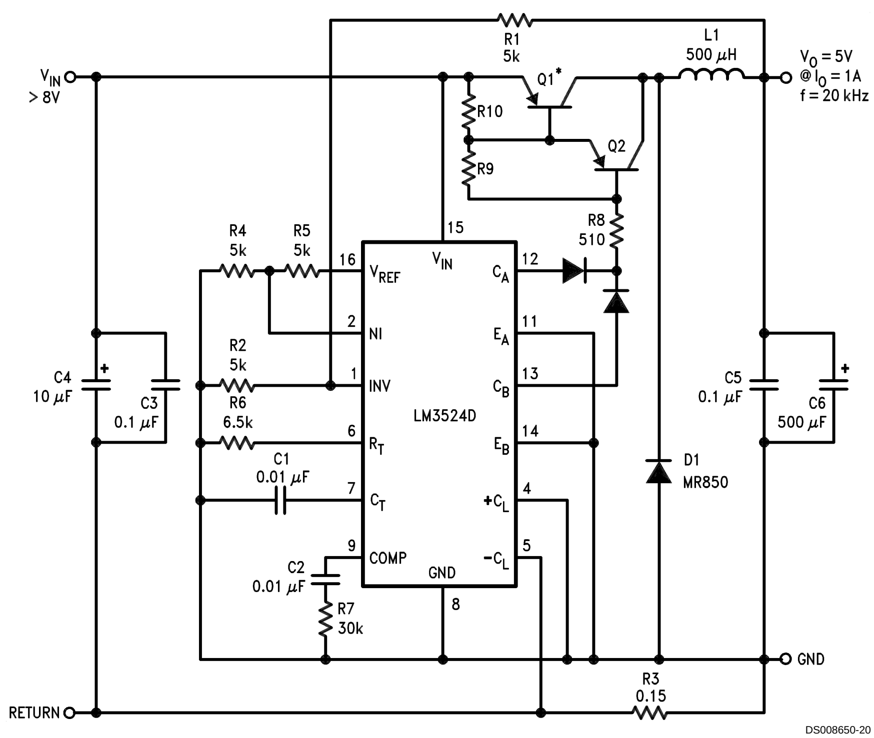
$$V_o = V_{NI}\left(1 + \frac{R1}{R2}\right),$$

where V_{NI} is the voltage at the error amplifier's non-inverting input.

Resistor R3 sets the current limit to:

$$\frac{200\ \text{mV}}{R3} = \frac{200\ \text{mV}}{0.15} = 1.3\text{A}.$$

Figures 16, 17 and show a PC board layout and stuffing diagram for the 5V, 1A regulator of *Figure 15*. The regulator's performance is listed in *Table 1*.



*Mounted to Staver Heatsink No. V5-1.
Q1 = BD344
Q2 = 2N5023
L1 = >40 turns No. 22 wire on Ferroxcube No. K300502 Torroid core.

FIGURE 15. 5V, 1 Amp Step-Down Switching Regulator

Typical Applications (Continued)

TABLE 1.

Parameter	Conditions	Typical Characteristics
Output Voltage	V_{IN} = 10V, I_o = 1A	5V
Switching Frequency	V_{IN} = 10V, I_o = 1A	20 kHz
Short Circuit Current Limit	V_{IN} = 10V	1.3A
Load Regulation	V_{IN} = 10V I_o = 0.2 − 1A	3 mV
Line Regulation	ΔV_{IN} = 10 − 20V, I_o = 1A	6 mV
Efficiency	V_{IN} = 10V, I_o = 1A	80%
Output Ripple	V_{IN} = 10V, I_o = 1A	10 mVp-p

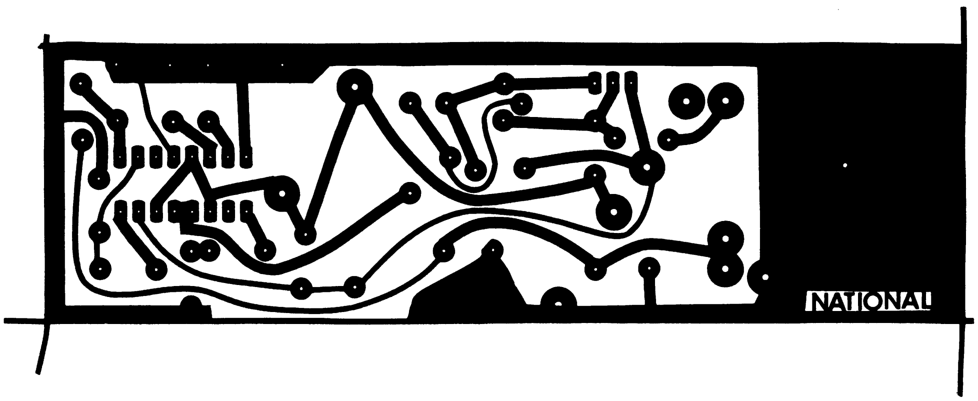


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FIGURE 16. 5V, 1 Amp Switching Regulator, Foil Side

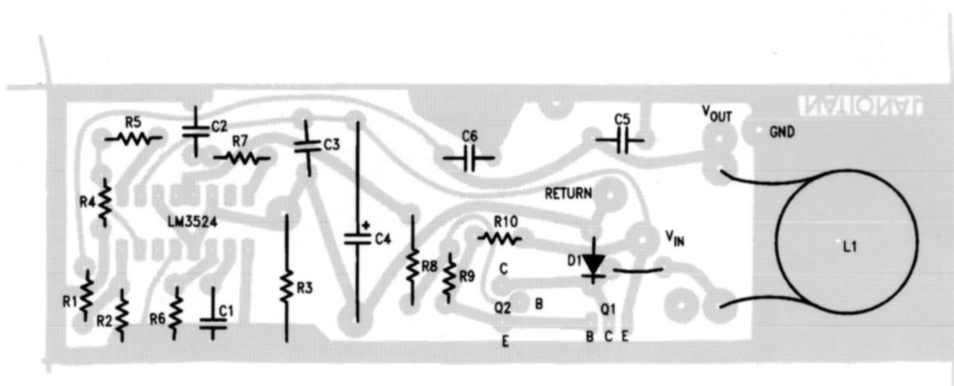

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FIGURE 17. Stuffing Diagram, Component Side

Typical Applications (Continued)

THE STEP-UP SWITCHING REGULATOR

Figure 18 shows the basic circuit for a step-up switching regulator. In this circuit Q1 is used as a switch to alternately apply V_{IN} across inductor L1. During the time, t_{ON}, Q1 is ON and energy is drawn from V_{IN} and stored in L1; D1 is reverse biased and I_o is supplied from the charge stored in C_o. When Q1 opens, t_{OFF}, voltage V1 will rise positively to the point where D1 turns ON. The output current is now supplied through L1, D1 to the load and any charge lost from C_o during t_{ON} is replenished. Here also, as in the step-down regulator, the current through L1 has a DC component plus some ΔI_L. ΔI_L is again selected to be approximately 40% of I_L. *Figure 19* shows the inductor's current in relation to Q1's ON and OFF times.

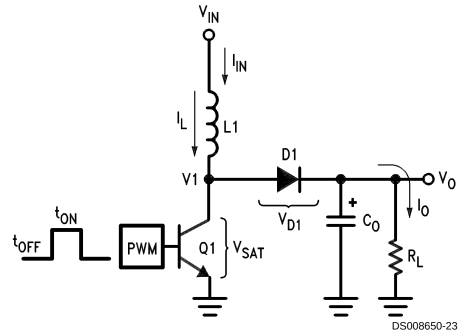


FIGURE 18. Basic Step-Up Switching Regulator

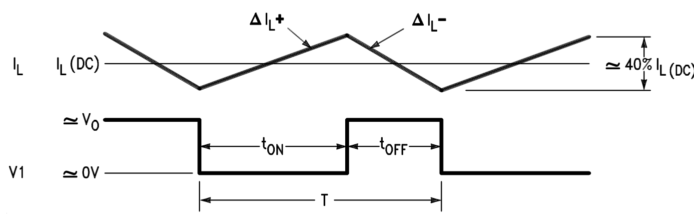


FIGURE 19. Relation of Switch Timing to Inductor Current in Step-Up Regulator

$$\text{From } \Delta I_L = \frac{V_L T}{L},\ \Delta I_L{}^{+} \cong \frac{V_{IN} t_{ON}}{L1}$$

$$\text{and } \Delta I_L{}^{-} \cong \frac{(V_o - V_{IN})\, t_{OFF}}{L1}$$

Since $\Delta I_L{+} = \Delta I_L{-}$, $V_{IN} t_{ON} = V_o t_{OFF} - V_{IN} t_{OFF}$, and neglecting V_{SAT} and V_{D1}

$$\boxed{V_o \cong V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right)}$$

The above equation shows the relationship between V_{IN}, V_o and duty cycle.

In calculating input current $I_{IN(DC)}$, which equals the inductor's DC current, assume first 100% efficiency:

$$P_{IN} = I_{IN(DC)}\, V_{IN}$$

$$P_{OUT} = I_o V_o = I_o\, V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right)$$

for η = 100%, $P_{OUT} = P_{IN}$

$$I_o\, V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right) = I_{IN(DC)}\, V_{IN}$$

$$I_{IN(DC)} = I_o\left(1 + \frac{t_{ON}}{t_{OFF}}\right)$$

This equation shows that the input, or inductor, current is larger than the output current by the factor $(1 + t_{ON}/t_{OFF})$. Since this factor is the same as the relation between V_o and V_{IN}, $I_{IN(DC)}$ can also be expressed as:

$$\boxed{I_{IN(DC)} = I_o\left(\frac{V_o}{V_{IN}}\right)}$$

So far it is assumed η = 100%, where the actual efficiency or η_{MAX} will be somewhat less due to the saturation voltage of Q1 and forward on voltage of D1. The internal power loss due to these voltages is the average I_L current flowing, or I_{IN}, through either V_{SAT} or V_{D1}. For $V_{SAT} = V_{D1}$ = 1V this power loss becomes $I_{IN(DC)}$ (1V). η_{MAX} is then:

$$\eta_{MAX} = \frac{P_O}{P_{IN}} = \frac{V_O I_O}{V_O I_O + I_{IN}\,(1V)} = \frac{V_O I_O}{V_O I_O + I_O\left(1 + \frac{t_{ON}}{t_{OFF}}\right)}$$

$$\text{From } V_o = V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right)$$

$$\boxed{\eta_{max} = \frac{V_{IN}}{V_{IN} + 1}}$$

This equation assumes only DC losses, however η_{MAX} is further decreased because of the switching time of Q1 and D1.

Typical Applications (Continued)

In calculating the output capacitor C_o it can be seen that C_o supplies I_o during t_{ON}. The voltage change on C_o during this time will be some $\Delta V_c = \Delta V_o$ or the output ripple of the regulator. Calculation of C_o is:

$$\Delta V_o = \frac{I_o t_{ON}}{C_o} \text{ or } C_o = \frac{I_o t_{ON}}{\Delta V_o}$$

$$\text{From } V_o = V_{IN}\left(\frac{T}{t_{OFF}}\right);\ t_{OFF} = \frac{V_{IN}}{V_o}T$$

$$\text{where } T = t_{ON} + t_{OFF} = \frac{1}{f}$$

$$t_{ON} = T - \frac{V_{IN}}{V_o}T = T\left(\frac{V_o - V_{IN}}{V_o}\right) \text{ therefore:}$$

$$C_o = \frac{I_o T\left(\frac{V_o - V_{IN}}{V_o}\right)}{\Delta V_o} = \boxed{\frac{I_o (V_o - V_{IN})}{f \Delta V_o V_o}}$$

where: C_o is in farads, f is the switching frequency,
ΔV_o is the p-p output ripple

Calculation of inductor L1 is as follows:

$$L1 = \frac{V_{IN} t_{ON}}{\Delta I_L +}, \text{ since during } t_{ON},$$

V_{IN} is applied across L1

$$\Delta I_{Lp\text{-}p} = 0.4\, I_L = 0.41\, I_{IN} = 0.4\, I_o\left(\frac{V_o}{V_{IN}}\right), \text{ therefore:}$$

$$L1 = \frac{V_{IN} t_{ON}}{0.4\, I_o\left(\frac{V_o}{V_{IN}}\right)} \text{ and since } t_{ON} = \frac{T(V_o - V_{IN})}{V_o}$$

$$\boxed{L1 = \frac{2.5\, V_{IN}^2 (V_o - V_{IN})}{f\, I_o V_o^2}}$$

where: L1 is in henrys, f is the switching frequency in Hz

To apply the above theory, a complete step-up switching regulator is shown in *Figure 20*. Since V_{IN} is 5V, V_{REF} is tied to V_{IN}. The input voltage is divided by 2 to bias the error amplifier's inverting input. The output voltage is:

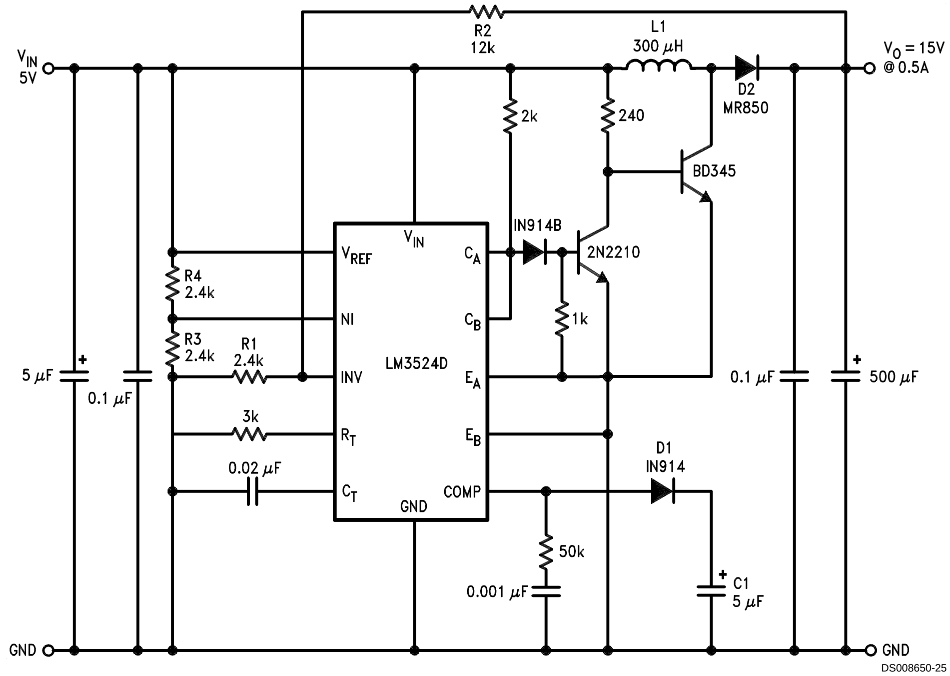
$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) \times V_{INV} = 2.5 \times \left(1 + \frac{R2}{R1}\right)$$

The network D1, C1 forms a slow start circuit.

This holds the output of the error amplifier initially low thus reducing the duty-cycle to a minimum. Without the slow start circuit the inductor may saturate at turn-on because it has to supply high peak currents to charge the output capacitor from 0V. It should also be noted that this circuit has no supply rejection. By adding a reference voltage at the non-inverting input to the error amplifier, see *Figure 21*, the input voltage variations are rejected.

The LM3524D can also be used in inductorless switching regulators. *Figure 22* shows a polarity inverter which if connected to *Figure 20* provides a −15V unregulated output.

Typical Applications (Continued)



L1 = > 25 turns No. 24 wire on Ferroxcube No. K300502 Toroid core.

FIGURE 20. 15V, 0.5A Step-Up Switching Regulator

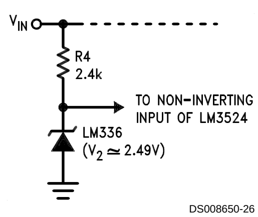


FIGURE 21. Replacing R3/R4 Divider in *Figure 20* with Reference Circuit Improves Line Regulation

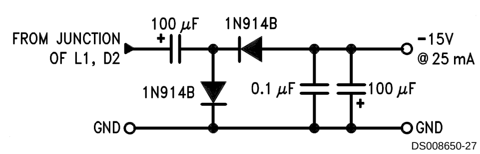
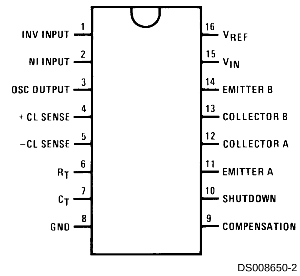


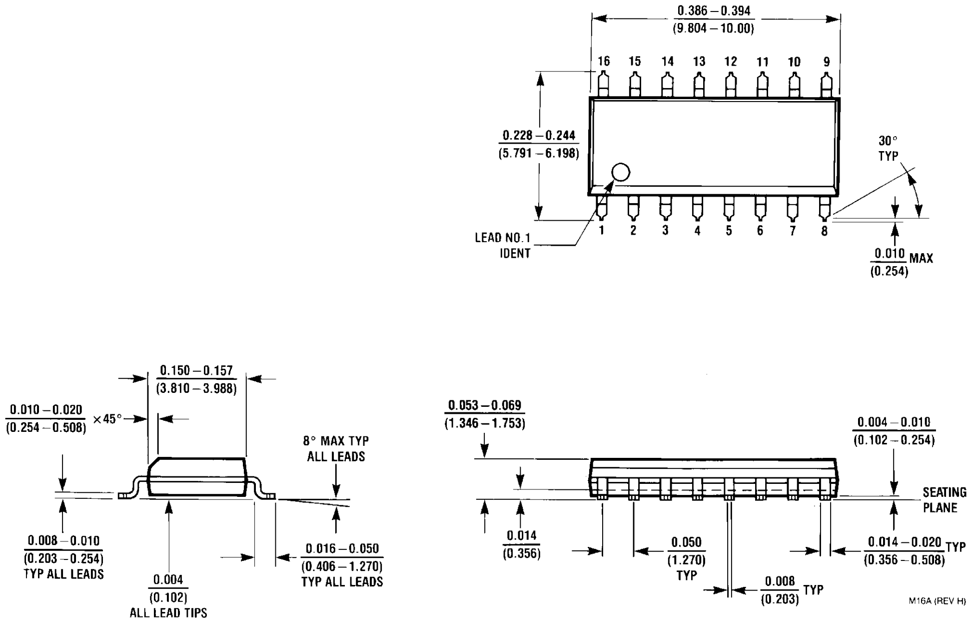
FIGURE 22. Polarity Inverter Provides Auxiliary −15V Unregulated Output from Circuit of *Figure 20*

Connection Diagram



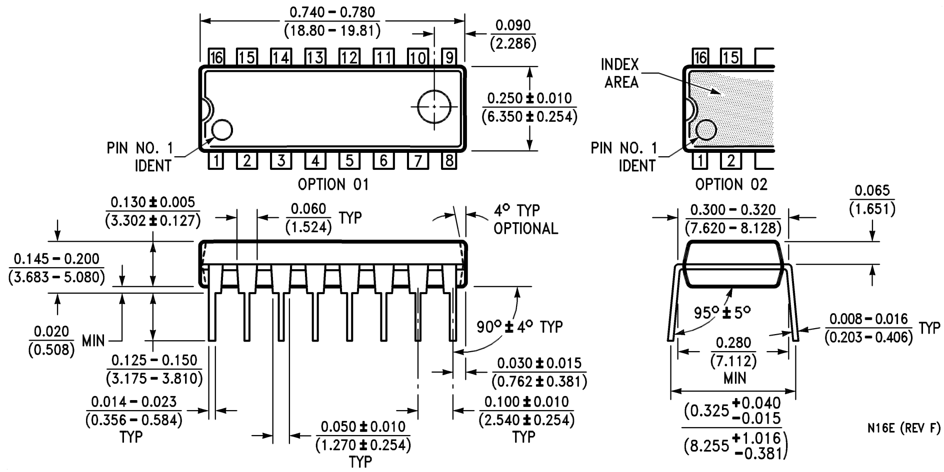
Top View
Order Number LM2524DN or LM3524DN
See NS Package Number N16E
Order Number LM3524DM
See NS Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Surface-Mount Package (M)
Order Number LM3524DM
NS Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
Order Number LM2524DN or LM3524DN
NS Package Number N16E

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