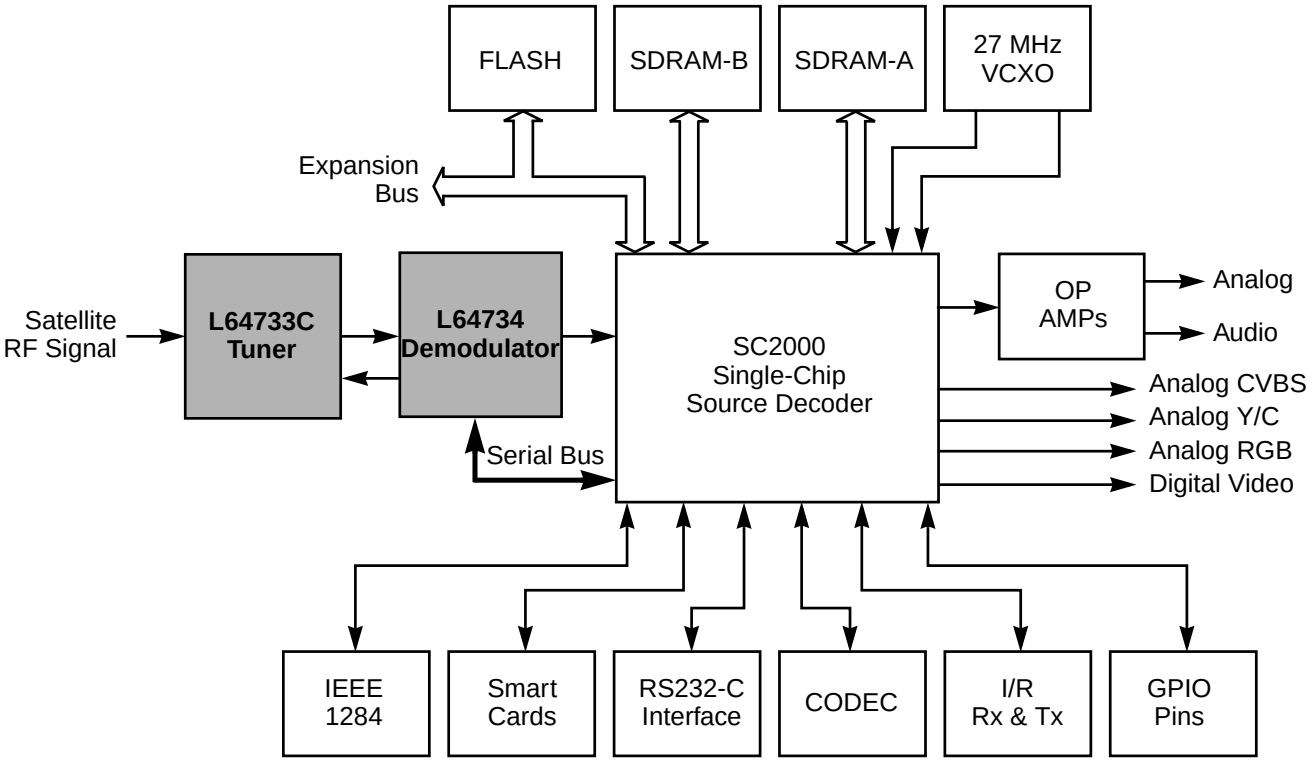
L64733C/L64734 Tuner and Satellite Receiver Chipset

Datasheet

The L64733C/734 chipset is designed for satellite broadcast digital TV. It is compliant with the European digital video broadcast (DVB-S) standard, as well as the technical specifications for DSS systems. The L64733C/734 chipset forms a complete “L-band-to-bits” system.

A typical application of the L64733C/734 chipset is satellite digital TV reception in accordance with the ETS 300 421 standard. Figure 1 shows the L64733C/734 chipset satellite receiver implemented in a typical satellite receiver set-top decoder.

Figure 1 Set-Top Box Block Diagram



The L64733C Tuner IC directly down-converts the satellite signal from L-band to baseband; it includes an on-chip synthesizer. Using frequency information programmed into its configuration registers, the L64734 Satellite Receiver generates control signals for the L64733C synthesizer. The L64734 also controls the programming of the low-pass filters on the

L64733C and generates dual automatic gain control (AGC) voltages for the two-stage automatic gain control on the L64733C. A simplified chipset block diagram is shown in Figure 2.

Figure 2 L64733C/734 Simplified Block Diagram

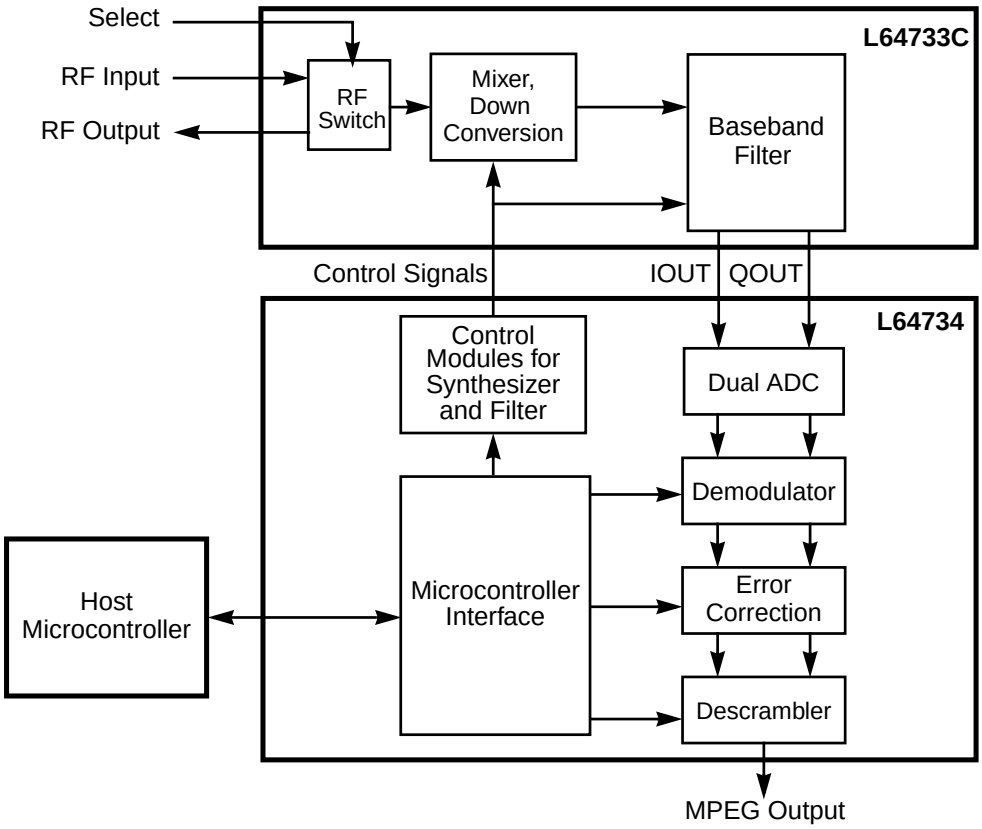
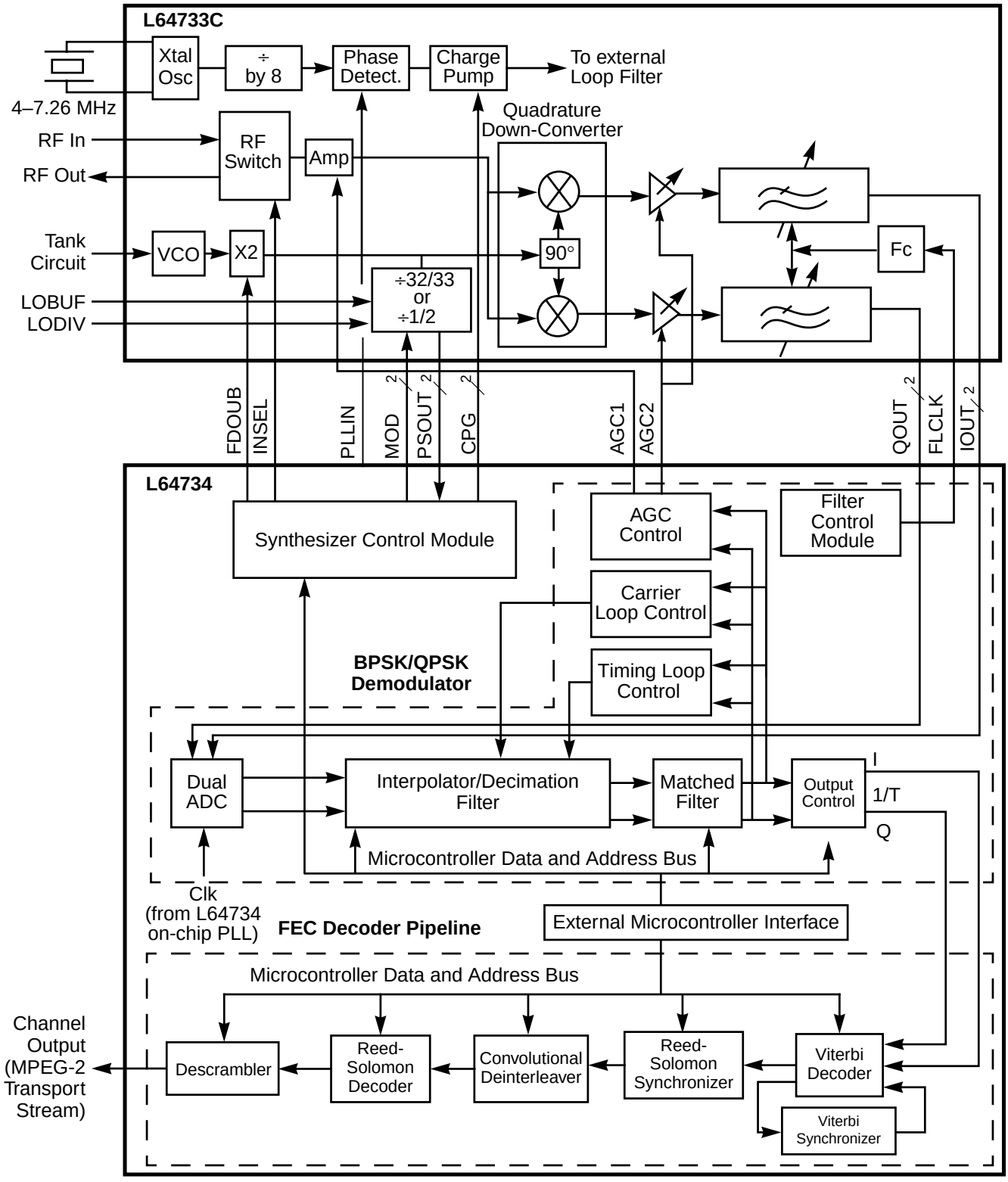


Figure 3 shows a more detailed chipset block diagram.

The L64733C accepts the RF In L-Band signal input from the satellite low noise block (LNB) feed. The L64733C handles a fully loaded raster of transponder signals from 925 MHz to 2175 MHz. RF In is internally matched to 75 Ω; it requires no matching network between the cable connector and the L64733C input pins, except for a DC-blocking capacitor. The L64733C uses the L64734 INSEL signal to select the appropriate RF function (Normal or Loop-Through Mode).

Figure 3 Detailed Chipset Block Diagram



The RF signal is sent to a variable gain stage controlled by the L64734 AGC1 signal. The L64734 adjusts AGC1 in conjunction with AGC2 to maximize the SNR of the RF In signal while maintaining proper levels at the baseband outputs (IOUT and QOUT). The signal then is fed to two mixers in the quadrature demodulator. The mixers are fed with local oscillator signals that are offset by 90 degrees from one another. The quadrature demodulator converts the frequency of the RF In signal directly to baseband while splitting the signal into quadrature I and Q signal paths.

The baseband signals pass through a pair of variable gain amplifiers, controlled through the AGC2 pin by the L64734. The signals then pass through a pair of seventh-order filters for antialiasing. The filter shape is seventh-order Butterworth, followed by a single-pole delay equalizer. The L64734 FLCLK signal controls the filter cutoff frequency, which is related to the baud rate. The filtered baseband output signals are fed to differential output stages at IOUTp, IOUTn, QOUTp, and QOUTn.

The baseband outputs of the L64733C are sent to the L64734 to be digitized by the analog-to-digital converter (ADC). Then, they are sent to a BPSK/QPSK demodulator, filtered, and sent to the L64734 forward error correction (FEC) decoder pipeline, which outputs an MPEG-2 transport stream.

The frequency synthesizer functionality is split between the L64733C and L64734. The Synthesizer Control Module resides on the L64734 and generates control signals for the L64733C Tuner IC frequency synthesizer. The Synthesizer Control Module also contains programmable counters for the synthesizer feedback loop.

The L64733C provides analog functions for the frequency synthesizer, the RF local oscillator, and the crystal reference oscillator. Tuning oscillator signals are generated for the mixers in the 925–2175 MHz range, with a 0.625 MHz step size when using a 5 MHz crystal reference. The on-chip VCO tuning frequency is 543–1088 MHz. To tune channels from 925–1086 MHz, the L64734 disables the frequency doubler (X2 block) on the L64733C. To tune channels from 1086–2175 MHz, the L64734 enables the frequency doubler.

The L64733C can improve half-harmonic rejection. It requires special programming of the frequency doubler control pin (FDOUB), which now

has 3-state operation (see the “Synthesizer Control Interface” section on page 20).

The VCO requires an external resonant tank circuit, which includes varactor diodes to vary the frequency of oscillation.

The VCO signal is fed to the Prescaler block before being passed deferentially through the PSOUTp and PSOUTn pins to the L64734. The L64734 MODp and MODn differential signals control the divider ratio for the Prescaler block. The L64734 dynamically changes the divide ratio to ensure that the tuning step size is not affected by the divider. The L64734 contains programmable counters to further divide the signal frequency before it is fed back to the L64733C through the PLLINp and PLLINn pins. The crystal reference oscillator frequency is divided by eight and fed to the phase detector. The phase detector generates a current signal proportional to the difference in phase between PLLINp, PLLINn, and the divided crystal frequency. A charge pump circuit generates current that controls pins CP and FB, and an external transistor to buffer the L64733C against the tuning voltage (28 V). The current is passed through a discrete loop filter and is converted to a tuning voltage that drives the external varactor diodes for the VCO tank circuit. A frequency controlled loop is formed. Changing the frequency divider ratios in the L64734 registers varies the VCO frequency. See Figure 7, on page 23, for more details regarding the external circuitry for the VCO, crystal oscillator, charge pump, tank circuitry, and frequency-controlled loop.

The chipset provides maximum integration and flexibility for system designers at a minimum cost. The number of external components required to build a system is minimal because the synthesizer, variable rate filters, and clock and carrier loops are integrated into the two devices.

Features and Benefits

The following subsections provide a list of system and chipset features.

System Features

- Direct down-conversion
- Integrated programmable cut-off low-pass filters for variable-rate operation
- Dual AGC for optimizing performance with respect to intermodulation and noise
- Integrated synthesizer
- Integrated quadrature amplitude and phase imbalance compensation
- RF Loop-Through

Chipset Features

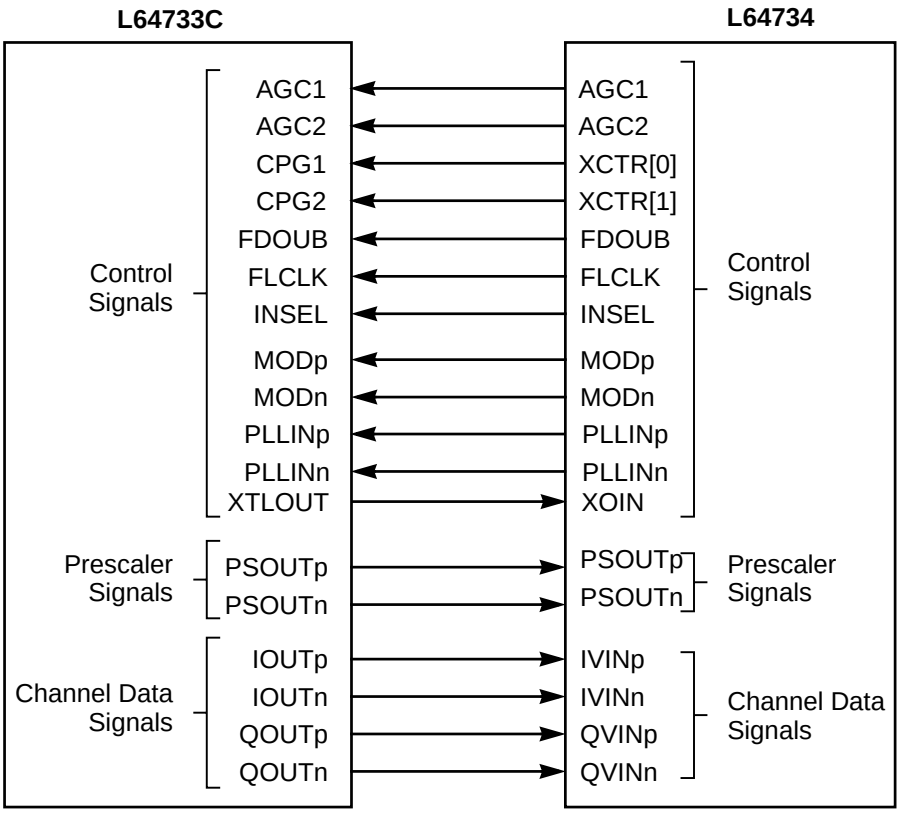
- DVB and DSS system specifications support
- BPSK/QPSK demodulation rates from 1 to 45 Mbaud
- Matched filter (square root raised cosine filter with roll off factor of 20% or 35%)
- Antialiasing filters for operation from 1 to 45 MBaud without switching external SAW filters or the need for low-pass filters
- On-chip digital clock synchronization
- On-chip digital carrier synchronization, featuring a frequency sweep capability for signal acquisition
- Autoacquisition demodulator mode and tuner control through an on-chip microcontroller
- Integrated Phase-Locked Loop (PLL) for clock synthesis, allowing the use of a fundamental mode crystal
- Fast channel switching mode
- Power estimation for AGC
- Programmable Viterbi decoder module for rates 1/2, 2/3, 3/4, 5/6, 6/7, and 7/8

- (204/188), (146/130) Reed-Solomon decoder
- Autosynchronization for Viterbi decoder
- Programmable synchronization for deinterleaver, Reed-Solomon decoder, and descrambler
- Bit error monitoring for channel performance measurements
- Deinterleaver (DVB and DSS)
- Serial host interface compatible with the LSI Logic Serial Control bus interface
- Power-down mode
- On-chip dual differential 6-bit ADCs
- Supports Synchronous Parallel Interface protocol for FEC data output

Chipset Interconnections

Figure 4 illustrates the signals between the L64733C and L64734.

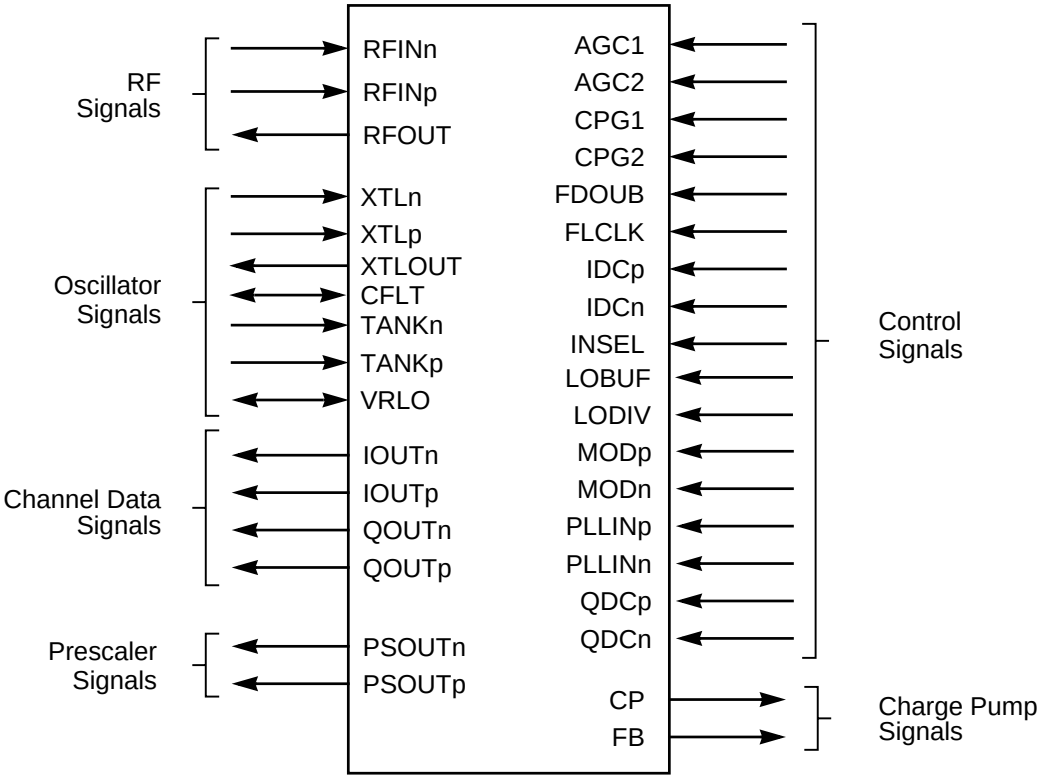
Figure 4 Chipset Interconnection Diagram



L64733C Signal Descriptions

This section describes the L64733C signals. Figure 5 shows the interface diagram of the L64733C. An “n” suffix (for example, ERROROUTn) designates an active LOW signal. Names of differential signals are designated with a “p” suffix for the noninverting side (for example, QOUTp), and with an “n” suffix for the inverting side (for example, QOUTn).

Figure 5 L64733C Interface Diagram



As shown in Figure 5, the L64733C has the following major interfaces:

- RF
- Oscillator
- Channel Data
- Prescaler
- Control
- Charge Pump

The following signal descriptions are listed according to the major interface groups.

RF Signals

The L64733C can accept an RF input signal and loop it to RFOUT, as determined by an on-chip RF switch.

RFINp, RFINn **RF Input** **Input**

The RFIN differential signals form the 75 Ω input. Connect the RFINp signal through a series 100 pF capacitor to a 75 Ω F video connector and the RFINn signal through a series 75 Ω resistor and 100 pF capacitor to ground.

RFOUT **RF Output** **Output**

The RFOUT signal is a 75 Ω output that is active when the INSEL input is deasserted. When active, the signal at RFOUT is a copy of the RFIN signal.

Oscillator Signals

The L64733C has two internal oscillators, a crystal oscillator and a tank oscillator.

CFLT **Bias Voltage Bypass** **Bidirectional**

Connect the CFLT pin as shown in Figure 7 on page 23.

TANKp, TANKn

Oscillator Tank Port **Input**

Connect the TANKp and TANKn pins as shown in Figure 7 on page 23.

VRLO **Local Oscillator Regulator Bypass** **Bidirectional**

Connect the VRLO pin as shown in Figure 7 on page 23.

XTLp, XTLn **Crystal Oscillator Port** **Input**

Connect the XTLp and XTLn pins as shown in Figure 7 on page 23.

XTLOUT **Crystal Out** **Output**

This signal provides a buffered clock reference frequency for driving the L64734 XOIN pin.

Channel Data Signals

The following signals are the channel data signals from the L64733C to the L64734.

IOUTp, IOUTn **I Channel Baseband Data** **Output**

The IOUT differential signals form the in-phase data provided to the L64734.

QOUTp, QOUTn

Q Channel Baseband Data **Output**

The QOUT differential signals form the quadrature-phase data provided to the L64734.

Prescaler Signals

The following signals are the prescaler outputs from the L64733C to the L64734.

PSOUTp, **PSOUTn**

Prescaler **Output**

When the LOBUF signal is LOW, the PSOUT differential signals are the L64733C prescaler outputs.

When LOBUF is HIGH, the Local Oscillator (LO) buffer (50 Ω) feeds the PSOUT differential signals.

The programmable counters on the L64734 are clocked on the rising edge of the PSOUT signal.

Control Signals

The following signals, some of which are generated by the L64734 IC, control the mode of operation of the L64733C IC.

AGC1 **Automatic Gain Control 1** **Input**

The AGC1 signal is a high-impedance input from the L64734 that controls RF AGC circuitry. The AGC1 voltage has a range of 0.5 V to 4.8 V.

AGC2 **Automatic Gain Control 2** **Input**

The AGC2 signal is a high-impedance input from the L64734 that controls RF AGC circuitry.

CPG[2:1] **Charge Pump Gain** **Input**

The CPG[2:1] signals set the charge pump gain according to the table below.

		Charge Pump Current (typ), mA	
CPG1	**CPG2**	**FB HIGH**	**FB LOW**
0	0	0.1	–0.1
0	1	0.3	–0.3
1	0	0.6	–0.6
1	1	1.8	–1.8

FDOUB **Frequency Doubler** **Input**

When FDOUB is asserted, the L64733C local oscillator frequency is internally doubled and fed to the mixers. When FDOUB is deasserted, the oscillator frequency is not doubled before being fed to the mixers.

Bit 6 of register 79, group 4 (APR 79), controls the L64734 FDOUB output pin, which enables or disables the frequency doubler on the L64733C.

The FDOUB pin is set as shown in the table below, where F_{switch} is the frequency at which the frequency doubler is enabled or disabled.

Frequency	FDOUB APR 79[6]	TRI APR 79[2]	FDOUB Pin
925 MHz–F_{switch}	0	0	LOW
F_{switch}–1680 MHz	1	1	3-state
1680–2175 MHz	1	0	HIGH

This method of control preserves the compatibility with the L64733B, which is not affected by 3-stating the FDOUB pin.

FLCLK **Filter Clock** **Input**

The FLCLK signal is a low amplitude, self-biased clock input. The frequency of the FLCLK signal multiplied by 16 is the baseband filter's –3 dB frequency.

IDCp, IDCn **I-Channel DC Offset Correction** **Input**

Connect a 0.1 µF or larger capacitor between the IDCp and IDCn signals.

INSEL **RF Port Input Select** **Input**

When the INSEL signal is asserted, the L64733C is in normal mode. When the INSEL signal is deasserted, the L64733C is in Loop-Through mode. In this mode, the RFIN signal is looped through out to the RFOUT signal and the L64733C local oscillator is shut off.

LOBUF **Local Oscillator Buffer Select** **Input**

Asserting LOBUF causes the external PLL mode to be in effect, the local oscillator (LO) buffer to be enabled, and the LO signal to be sent out to the PSOUT pins according to the division ratio selected with the LODIV signal. When

LOBUF is deasserted, the internal PLL mode is in effect, and the PSOUT pins are driven from the 32/33 prescaler.

LODIV **Local Oscillator Buffer Division Ratio** **Input**
When the LODIV signal is asserted, the local oscillator (LO) buffer division ratio is set to 1; when it is deasserted, the ratio is set to 2.

MODp, MODn **Prescaler Modulus** **Input**
The MOD differential signals form a Positive Emitter Coupled Logic (PECL) input that sets the prescaler modulus. When the MODp signal is positive with respect to the MODn signal, the prescaler modulus is set to 32 (divide by 32). When the MODn signal is positive with respect to the MODp signal, the prescaler modulus is set to 33 (divide by 33).

PLLINp, PLLINn
Phase Detector **Input**
The PLLIN differential signals form the phase detector input and are connected to the L64734 PLLINp and PLLINn output signals. See the L64734 PLLINp and PLLINn descriptions in the “Synthesizer Control Interface” section.

QDCp, QDCn **Q-Channel DC Offset Correction** **Input**
Connect a 0.1 µF or larger capacitor between the QDCp and QDCn signals.

Charge Pump Signals

The following signals are outputs from the L64733C charge pump.

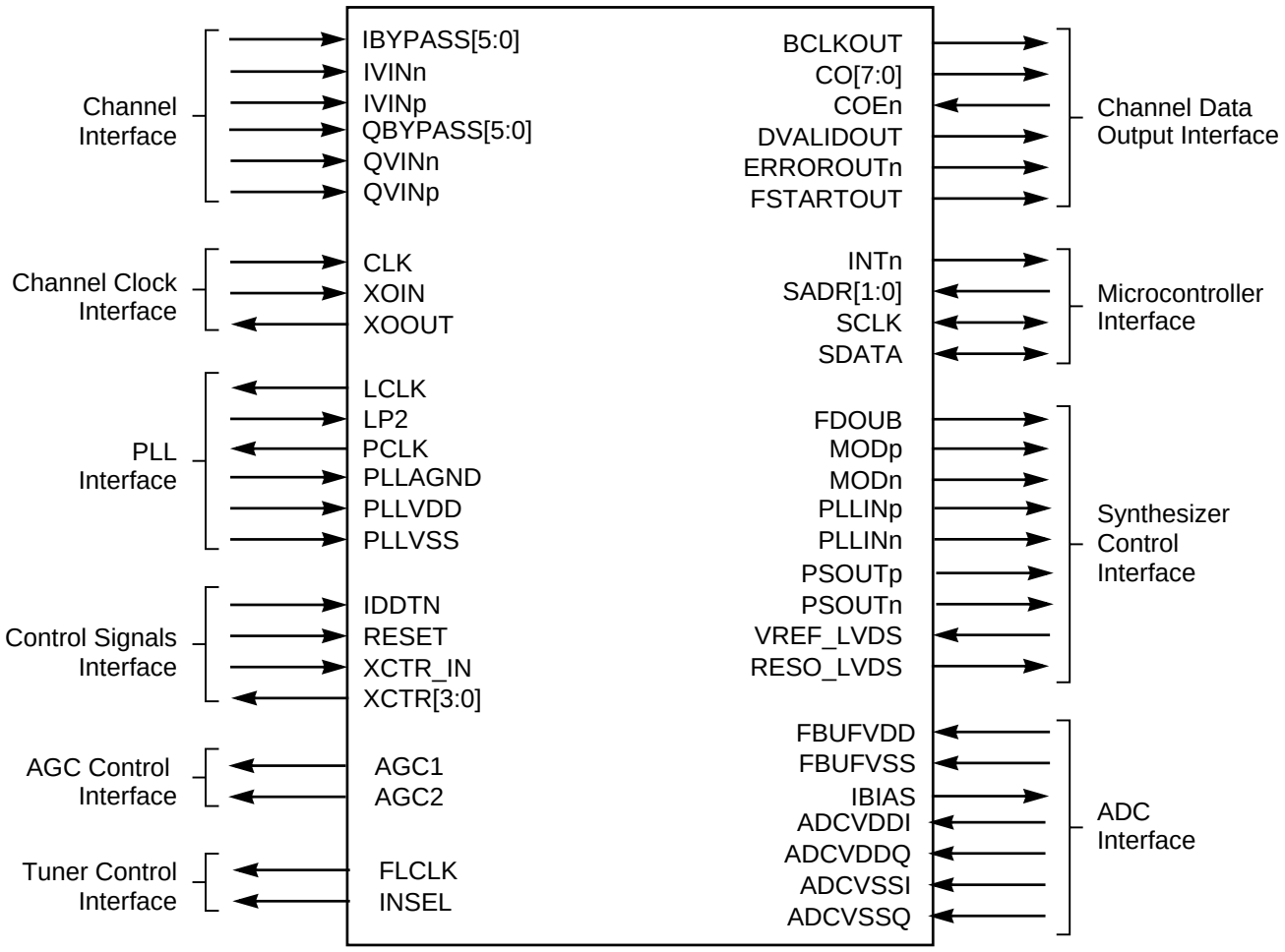
CP **Charge Pump** **Output**
Connect the CP signal as shown in Figure 7, on page 23.

FB **Feedback**
Charge Pump Transistor Drive **Output**
Connect the FB signal as shown in Figure 7, on page 23.

L64734 Signal Descriptions

This section describes the L64734 signals. Figure 6 shows the interface diagram of the L64734.

Figure 6 L64734 Interface Diagram



As shown in Figure 6, the L64734 has the following major interfaces:

- Channel
- Channel Clock
- PLL
- Control Signals
- ADC
- AGC Control
- Channel Data Output
- Microcontroller
- Synthesizer Control
- Tuner Control

The following signal descriptions are listed according to the major interface groups.

Channel Interface

The Channel Interface is the input path to the L64734 satellite receiver. The two signals IVIN and QVIN are the I and Q streams from the satellite tuner circuit. The CLK signal strobes in the data signals.

IBYPASS[5:0] **I Channel Data** **Input**

The IBYPASS[5:0] signals form the digital received I channel data input bus, which supplies the I Stream to the L64734 when the ADC is bypassed. The setting of particular register bits in the L64734 controls the bypass.

IVINp, IVINn **I Channel Data** **Input**

The IVINp and IVINn differential signals form the analog received I channel data input bus, which supplies the I stream to the L64734.

QBYPASS[5:0]

Q Channel Data **Input**

The QBYPASS[5:0] signals form the digital received Q channel data input bus, which supplies the Q Stream to the L64734 when the ADC is bypassed. The setting of particular register bits in the L64734 controls the bypass.

QVINp, QVINn

Q Channel Data **Input**

The QVINp and QVINn differential signals form the analog received Q channel data input bus, which supplies the Q stream to the L64734.

Channel Clock Interface

The Channel Clock Interface consists of the clock and crystal oscillator signals.

CLK **IVIN/QVIN Input Clock** **Input**

CLK is a positive, edge-triggered clock that strobes input data to the L64734.

XOIN **Crystal Oscillator In** **Input**
The XOIN pin provides a crystal oscillator or external reference clock input. Normally, a 15 MHz crystal is connected to the XOIN pin.

XOOUT **Crystal Oscillator Out** **Output**
The XOOUT pin is the crystal oscillator output pin.

Phase-Locked Loop (PLL) Interface

The internal PLL generates the signals to operate the ADC, Demodulator, and FEC modules.

LCLK **Decimated Clock Output** **Output**
The L64734 internal clock generation module generates the LCLK signal. LCLK is derived from CLK by dividing by the value of the CLK_DIV2 register parameter.

LP2 **Input to VCO** **Input**
The LP2 signal is the input to the internal voltage-controlled oscillator. Normally, it is connected to the output of an external RC filter circuit.

PCLK **PLL Clock Output** **Output**
The L64734 internal PLL clock synthesis module generates the PCLK signal. The reference crystal connected between the XOIN and XOOUT pins drives the PLL. The PLL clock synthesis module can be configured to generate a PCLK rate that is appropriate for all data rates.

PLLAGND **PLL Analog Ground** **Input**
PLLAGND is the analog ground pin for the PLL module and normally is connected to the system ground plane.

PLLVDD **PLL Power** **Input**
PLLVDD is the power supply pin for the PLL module and normally is connected to the system power (V_{DD}) plane.

PLLVSS **PLL Ground** **Input**
PLLVSS is the ground pin for the PLL module and normally is connected to the system ground plane.

Control Signals Interface

The Control Signals Interface controls the operation of the L64734 and is not associated with any particular interface.

IDDTN **Test** **Input**
The IDDTN pin is an LSI Logic internal test pin. Tie the IDDTN pin LOW for normal operation.

RESET **Reset** **Input**
This active-HIGH signal resets all internal data paths. Reset timing is asynchronous to the device clocks. Reset does not affect the configuration registers.

XCTR_IN **Control Input** **Input**
The XCTR_IN pin is an external input control pin. It is sensed by reading the XCTR_IN register bit.

XCTR[3] **Control Output/Sync Status Flag** **Output**
The XCTR[3] signal indicates the synchronization status for one of three synchronization modules in the L64734 or the XCTR[3] field in Group 4, APR 55. The three modules are the Viterbi Decoder, Reed-Solomon Deinterleaver (DI/RS), and Descrambler. For each of the three synchronization outputs, the asserted XCTR[3] signal indicates that synchronization is achieved for the sync module chosen using the SSS[1:0] register bits. When deasserted, the signal indicates an out-of-synchronization condition.

XCTR[2:0] **Output Control** **Output**
The XCTR[2:0] pins are external output control pins. They are set by programming particular register bits. XCTR[2] is mapped to CPG1 and XCTR[0] is multiplexed with CPG2 when used with the L64733C Tuner IC. When the on-chip serializer generates a serial 2- or 3-wire protocol on the XCTR[2:0] pins, the mapping is XCTR[2] = EN, XCTR[1] = SCL, and XCTR[0] = SDA.

Analog-to-Digital Converter (ADC) Interface

The ADC module converts the incoming IVIN and QVIN signals into an internal 6-bit digital representation for processing. The following pins support the ADC module.

ADCVDDI/Q **ADC Power** **Input**
ADCVDDI/Q are the analog power supply pins for the ADC module and normally are connected to the system power (V_{DD}) plane.

ADCVSSI/Q **ADC Analog Ground** **Input**
ADCVSSI/Q are the analog ground pins for the ADC module and normally are connected to the system ground plane.

FBUFVDD **Analog Supply** **Input**
FBUFVDD is the analog supply pin for the on-chip reference voltage generator. This pin normally is connected to the system power (V_{DD}) plane.

FBUFVSS **Analog Ground** **Input**
FBUFVSS is the analog ground pin for the on-chip reference voltage generator. This pin normally is connected to the system ground (V_{SS}) plane.

IBIAS **ADC Bias Current** **Output**
This is the bias current for the ADC module. Connect this output to a 39 kΩ resistor, and connect the other side of the resistor to ground.

AGC Control Interface

The AGC Control Interface contains signals used for power control.

AGC1, AGC2 **Power Control** **Output**
The AGC1 and AGC2 signals are the positive ΣΔ modulated output used for power control. These signals can each drive an external passive RC filter that feeds a gain control stage for dual-stage AGC. For a single stage AGC, AGC1 can be used, and has the same functionality as the PWRP pin on the L64724.

Channel Data Output Interface

The Channel Data Output Interface is the output path from the L64734. It typically is connected to the input of the transport demultiplexer in a set-top decoder application.

BCLKOUT **Byte Clock Out** **Output**

The BCLKOUT output signal is a strobe that indicates valid data bytes on the CO[7:0] bus when the L64734 is in Parallel Channel Output mode. The BCLKOUT signal cycles once every valid output data byte and is used by the transport demultiplexer to latch output data from the L64734 at the BCLKOUT rate. The BCLKOUT signal must be disregarded in Serial Channel Output mode.

CO[7:0] **Channel Data Out** **Output**

The CO[7:0] signals form the decoded output data port. When the OF bit is 1 (Group 4, APR17), the L64734 operates in the Parallel Channel Output mode. In this mode, the L64734 outputs the channel data as 8-bit wide parallel data on the CO[7:0] signals. In Serial Channel Output mode (OF = 0), the L64734 outputs the channel data as serial data on CO[0]. The data is latched on each bit clock cycle. The chronological ordering in Serial Channel output mode is MSB oldest, LSB newest.

COEn **Channel Output Enable** **Input**

When asserted, the COEn signal enables the ERROROUTn, CO[7:0], DVALIDOUT, BCLKOUT, and FSTARTOUT signals. Operation of the receiver continues regardless of the state of the COEn signal.

DVALIDOUT **Valid Data Out** **Output**

The DVALIDOUT signal indicates that the CO[7:0] signals contain the corrected channel data. New data is valid on the CO[7:0] signals when the DVALIDOUT signal is asserted. DVALIDOUT is not asserted during the propagated check and GAP bytes. The DVALIDOUT signal is deasserted after the FEC_RST register bit (Group 4, APR 55) is set to one.

ERROROUTn **Error Detection Flag** **Output**

The L64734 asserts the ERROROUTn signal at the beginning of each frame that contains an uncorrectable error, and deasserts it at the end of the frame if the error condition is removed. The ERROROUTn signal is aligned with the output data stream and is asserted after the FEC_RST register bit is set.

FSTARTOUT **Frame Start Output** **Output**

The L64734 asserts the FSTARTOUT signal during the first bit of every frame with valid data in Serial Channel Output mode and during the first byte in Parallel Channel Output mode. FSTARTOUT is valid only when the DVALIDOUT signal is asserted. The FSTARTOUT signal is deasserted after the FEC_RST register bit is set.

Microcontroller Interface

The Microcontroller Interface connects the L64734 to an external microcontroller.

INTn **Interrupt** **Output**

The L64734 asserts INTn when an internal unmasked interrupt flag is set. The INTn signal remains asserted during the interrupt condition, and the interrupt flag is not masked.

SADR[1:0] **Serial Address** **Input**

The SADR[1:0] signals are the two programmable bits of the serial address for the L64734.

SCLK **Serial Clock** **Bidirectional**

SCLK is the serial clock pin for a two-wire serial protocol.

SDATA **Serial Data** **Bidirectional**

SDATA is the serial data pin for a two-wire serial protocol.

Synthesizer Control Interface

The Synthesizer Control Interface allows the L64734 to control the L64733C frequency synthesizer.

FDOUB **Frequency Doubler** **Output, 3-State**

Bit 6 of register Group 4, APR 79 controls the L64734 FDOUB output pin, which enables or disables the frequency doubler on the L64733C.

The FDOUB pin is set as shown below; F_{switch} is the frequency that disables or enables the frequency doubler.

Frequency	FDOUB APR 79[6]	TRI APR 79[2]	FDOUB Pin
925 MHz–F_{switch}	0	0	LOW
F_{switch}–1680 MHz	1	1	3-state
1680–2175 MHz	1	0	HIGH

MODp, MODn **Modulus Selector** **Output**

The MODp and MODn signals are low-voltage differential signals from the L64734 of modulus selector programmable counter (A). PSOUT clocks these signals. When the MODp signal is positive with respect to the MODn signal, divide-by-32 is selected at the dual modulus prescaler on the L64733C Tuner IC. When MODp is negative with respect to MODn, divide-by-33 is selected. The counter A can be programmed to count down from a particular value by register bit programming.

PLLINp, PLLINn

PLL Differential Counter M **Output**

The PLLINp and PLLINn signals are low-voltage differential signals from the L64734 programmable synthesizer counter (M). PSOUT clocks these signals. PLLINp is positive with respect to PLLINn for one PSOUT cycle. The repetition rate is 0.5 MHz for a 4 MHz reference crystal. The counter M can be programmed to count down from a particular value by register bit programming.

PSOUTp, PSOUTn

Prescaler Output **Output**

The PSOUTp and PSOUTn signals are differential signals to the L64734 from the L64733C. The programmable counters on the L64734 are clocked on the rising edge of the PSOUT signal.

In the external PLL mode (LOBUF = HIGH), these signals come from the LO buffer, for which the LODIV signal sets the divider ratio.

RESO_LVDS **LVDS Buffers Precision Resistor** **Output**

The RESO_LVDS output must be connected to a resistor (6.8 kΩ, which controls the swing of the LVDSOUT

buffers used to drive the differential signals MODp, MODn, and PLLINp, PLLINn. Connect the other side of the resistor to ground.

VREF_LVDS **LVDS Buffers Reference Voltage** **Input**
The VREF_LVDS input is a 1.2 V ± 10% voltage level that controls the common mode voltage of the LVDSOUT buffers used to drive the differential signals MODp, MODn, and PLLINp, PLLINn.

Tuner Control Interface

The Tuner Control Interface contains signals that control the L64733C Tuner IC.

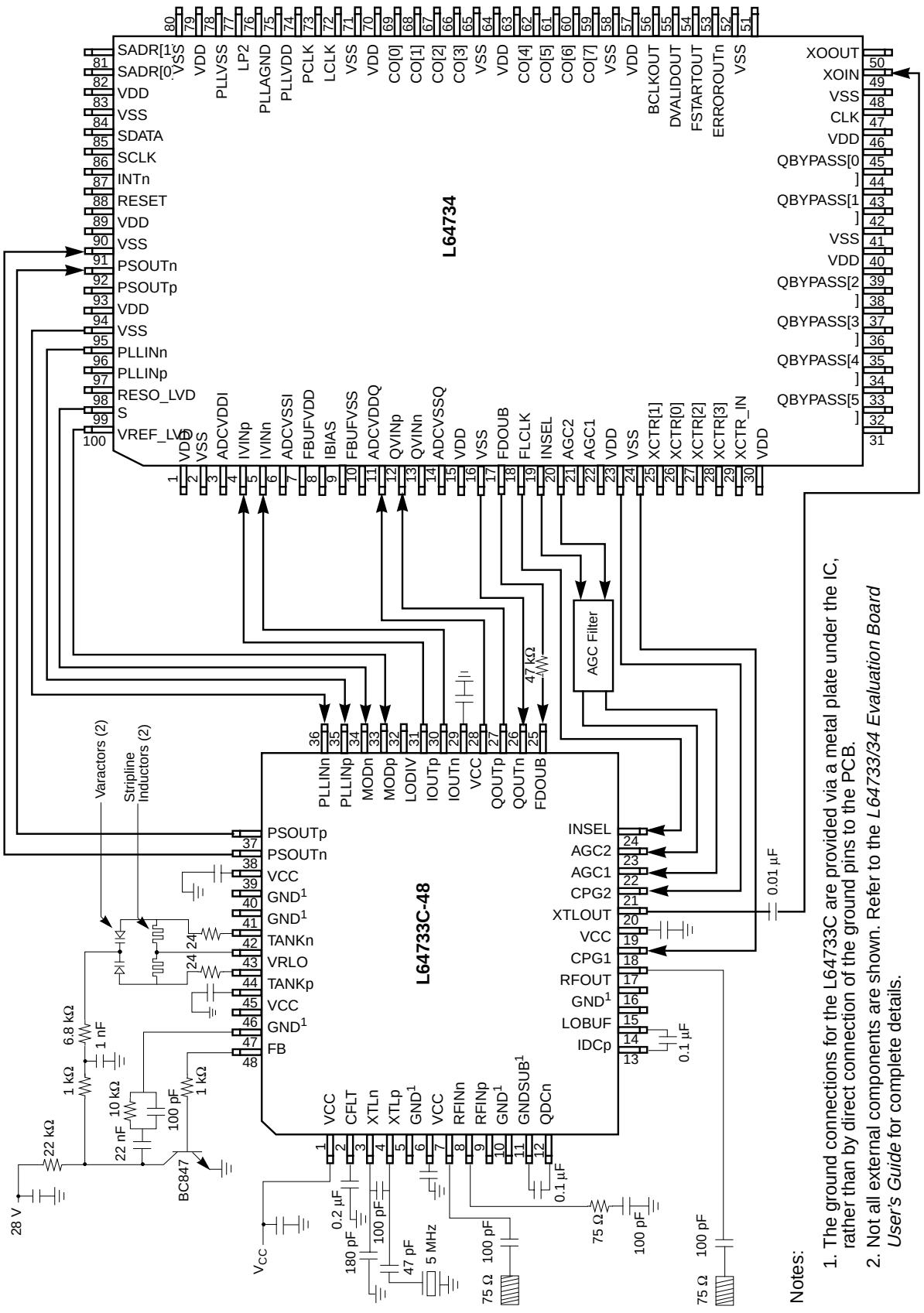
FLCLK **Filter Control Clock** **Output**
This is the output of a programmable integer value divider clocked by PCLK (the demodulator sampling clock). The division ratio can be programmed with register bits. The FLCLK frequency multiplied by 16 is the 3 dB cutoff of the programmable low pass filters on the L64733C.

INSEL **RF Input Select** **Output**
When INSEL is asserted, the L64733C tuner selects the normal mode. When INSEL is deasserted, the L64733C selects the Loop-Through mode.

Typical Operating Circuit

Figure 7 is a diagram of a typical operating circuit for the chipset, implemented with the L64733C-48 (48-pin package), including external components. Not all external components are shown. See the *L64733/34 Evaluation Board User's Guide* for complete schematic details.

Figure 7 Typical Operating Circuit



Notes:

1. The ground connections for the L64733C are provided via a metal plate under the IC, rather than by direct connection of the ground pins to the PCB.
2. Not all external components are shown. Refer to the *L64733/34 Evaluation Board User's Guide* for complete details.

Specifications

This section contains the electrical, timing, and mechanical specifications for the L64733C/734 chipset.

L64733C Electrical Specifications

Table 1 lists the absolute maximum values. Exceeding the values listed can cause damage to the L64733C. Table 2 gives the recommended operating supply voltage and temperature. Table 3 gives the DC characteristics; Table 4 gives the AC characteristics; and Table 5 and Table 6 summarize the pins for the 48- and 44-pin packages, respectively.

Table 1 L64733C Absolute Maximum Rating (Referenced to V_{SS})

Symbol	Parameter	Limits[1]	Units
V_{CC}	DC supply voltage	–0.5 to +7.0	V
–	Continuous power dissipation up to +70 °C	1.8	W
–	Derating above +70 °C	27	mW/°C
–	Operating temperature	0 to +70	°C
–	Junction temperature	+150	°C
–	Storage Temperature	–65 to +165	°C
–	Lead temperature (soldering 10 sec)	+300	°C

1. Note that the ratings in this table are those beyond which permanent device damage is likely to occur. Do not use these values as the limits for normal device operation.

Table 2 Recommended Operating Conditions

Symbol	Parameter	Limits[1]	Units
V_{DD}	DC Supply Voltage	5 ± 5%	V
T_A	Operating Ambient Temperature Range (Commercial)	70	°C

1. For normal device operation, adhere to the limits in this table. Sustained operation of a device at conditions exceeding these values, even if they are within the absolute maximum rating limits, can result in permanent device damage or impaired device reliability. Device functionality to stated DC and AC limits is not guaranteed if recommended operating conditions are exceeded.

Table 3 DC Characteristics of the L64733C

Parameter	Condition	Min	Typ	Max	Units
Power Supply					
Power Supply Voltage	All DC specs met	4.75	5.0	5.25	V
Power Supply Current		–	195	275	mA
Digital Control Inputs - CPG1, CPG2, INSEL, FDOUB, LOBUF, LODIV					
Input Logic Level High		2.4	–	–	V
Input Logic Level Low		0	–	0.5	V
Input Bias Current	Pin at 2.4 V	–15	–	10	µA
Slew-Limited Digital Clock Inputs - FLCLK					
FLCLK Input Level Low		–	–	1.45	V
FLCLK Input Level High		1.85	–	–	V
FLCLK Input Resistance/Leakage Current	50 kΩ series resistor between L64734 and FLCLK pin. L64734 generates normal CMOS levels	–1	–	1	µA
Fast Digital Clock Inputs - MODp, MODn, PLLINp, PLLINn					
MODp, MODn, PLLINp, PLLINn Common Mode Input Range (VCM)		1.08	1.2	1.32	V
MODp, MODn, PLLINp, PLLINn Input Voltage Low	MODp, MODn, or PLLINp, PLLINn differential swing around VCM. Need external 100-Ω termination.	–	–	–100	mV
MODp, MODn, PLLINp, PLLINn Input Voltage High	MODp, MODn, or PLLINp, PLLINn differential swing around VCM. Need external 100-Ω termination	100	–	–	mV
MODp, MODn, PLLINp, PLLINn Input Current	MODp, MODn, PLLINp, PLLINn	–5	–	+5	µA
Digital Clock Outputs - PSOUTp, PSOUTn					
PSOUTp, PSOUTn Common Mode Output Range (VCM)		2.16	2.4	2.64	V
PSOUTp, PSOUTn Output Voltage Low	PSOUTp, PSOUTn differential swing around VCM. Driving LSI PECL Load (±10 µA), LOBUF = 0	–	–215	–150	mV

(Sheet 1 of 3)

Table 3 DC Characteristics of the L64733C (Cont.)

Parameter	Condition	Min	Typ	Max	Units
PSOUTp, PSOUTn Output Voltage High	PSOUTp, PSOUTn differential swing around VCM. Driving LSI PECL Load (±10 µA), LOBUF = 0	150	215	–	mV
PSOUTp, PSOUTn Output Voltage Low	PSOUTp, PSOUTn differential swing around VCM, driving 100 Ω differential LOBUF = 1	–	–140	–100	mV
PSOUTp, PSOUTn Output Voltage High	PSOUTp, PSOUTn differential swing around VCM, driving 100 Ω differential. LOBUF is asserted.	100	140	–	mV
Synthesizer/Local Oscillator Buffer					
Prescaler Ratio	MOD = High	32	–	32	–
	MOD = Low	33	–	33	–
LO Buffer Division Ratio	LOBUF = High, LODIV = Low	2			–
	LOBUF = High, LODIV = High	1			–
Reference Divider Ratio		8	–	8	–
Charge Pump Output High Current (at FB)	CPG1, CPG2 = 0, 0	0.08	0.1	0.12	mA
	CPG1, CPG2 = 0, 1	0.24	0.3	0.36	mA
	CPG1, CPG2 = 1, 0	0.48	0.6	0.72	mA
	CPG1, CPG2 = 1, 1	1.44	1.8	2.16	mA
Charge Pump Output Low Current (at FB)	CPG1, CPG2 = 0, 0	–0.12	-0.1	–0.08	mA
	CPG1, CPG2 = 0, 1	–0.36	-0.3	–0.24	mA
	CPG1, CPG2 = 1, 0	–0.72	-0.6	–0.48	mA
	CPG1, CPG2 = 1, 1	–2.16	-1.8	–1.44	mA
Charge Pump Output Leakage Current		–25	–	25	nA
Charge Pump Positive-to-Negative Current Matching	FB self-biased.	–5	–	5	%
Charge Pump Output Transistor Base Current Drive		100	–	–	µA

(Sheet 2 of 3)

Table 3 DC Characteristics of the L64733C (Cont.)

Parameter	Condition	Min	Typ	Max	Units
Analog Control Inputs - AGC1, AGC2					
Input Bias Current	1 V < Pin < 4 V	–50	—	50	µA
Baseband Outputs - IOUTp, IOUTn, QOUTp, QOUTn					
Output Swing	Loaded with 2 kΩ differential across IOUTp, IOUTn, and QOUTp, QOUTn	1	—	—	V_{PP}
IOUTp, IOUTn, QOUTp, QOUTn Common Mode Voltage		0.65	—	0.85	V
IOUTp, IOUTn, QOUTp, QOUTn DC Offset Voltage		–50	—	50	mV
(Sheet 3 of 3)					

Table 4 AC Characteristics of the L64733C

Parameter	Condition		Min	Typ	Max	Units
RF Front End						
RFIN Input Freq. Range	Meets all following AC specs		925	–	2175	MHz
RFIN Single-Carrier Input Power[1]	RF level needed to produce 0.59 V_{PP}		–68	–	–25	dBm
AGC1 Range	1 V < AGC1 < 4 V		50	–	–	dB
AGC2 Range	1 V < AGC2 < 4 V		19	–	–	dB
RFIN referred IP3 (front-end contributions)	AGC1 gain set for –25 dBm input level (0.59 V_{PP} output), and AGC2 set to maximum gain (V_{AGC2} = 1 V). Two signals at FLO + 32 MHz, FLO + 72 MHz	@2175 MHz @1550MHz @925 MHz	– – –	10.5 11.5 10.5	– – –	dBm dBm dBm
Baseband 1 dB Compression Point	IOUTp, IOUTn, QOUTp, QOUTn have one signal within filter bandwidth		2	–	–	V_{PP}
RFIN Referred IP2	PRFIN = -25 dBm, F_{LO} = 951 MHz		–	15.5	–	dBm
(Sheet 1 of 3)						

Table 4 AC Characteristics of the L64733C (Cont.)

Parameter	Condition		Min	Typ	Max	Units
Noise Figure	At maximum gain AGC1, AGC2, 2150 MHz		–	10.8	–	dB
RFIN Return Loss	Complex “75 Ω source” subject to board, connector parasitics.		–	11	–	dB
LO Leakage Power at RFIN	950 MHz to 2150 MHz, subject to board layout		–	-65	–	dBm
Second Harmonic Rejection	Due to LO-generated 2nd harmonic		–	44	–	dB
Half-Harmonic Rejection and x 1.5 Harmonic Rejection[2]	Due to RFIN-generated 2nd harmonic		–	40	–	dB
Loop Through						
Gain		@2175 MHz @1550MHz @925 MHz	–	2.0 1.0 0.5	–	dB
RFIN referred IP3 (when Loop-Through enabled)	At PRFIN = –25 dBm	@2175 MHz @1550MHz @925 MHz	–	5.4 7.7 9.5	–	dBm
Noise Figure			–	12.0	–	dB
Return Loss	Subject to board and connector parasitics		–	8	–	dB
Baseband						
IOUTp, IOUTn, QOUTp, QOUTn Differential Output Voltage Swing	2 kΩ differential load, IOUTp, IOUTn, QOUTp, QOUTn. Expect 20 pF from each pin to GND		1	–	–	V_{PP}
IOUTp, IOUTn, QOUTp, QOUTn Output Impedance	Per side, IOUTp, IOUTn, QOUTp, QOUTn. To 200 MHz		–	–	50	Ω
Baseband Highpass –3 dB Point	0.22 µF caps connected from IDCp to IDCn, and QDCp to QDCn.		–	–	750	Hz
LPF Nominal Cutoff Frequency Range	Fc is –3 dB point of filter		8	–	33	MHz
LPF Nominal Fc			–	$14.5 \cdot F_{FLCLK} + 1$	–	–

(Sheet 2 of 3)

Table 4 AC Characteristics of the L64733C (Cont.)

Parameter	Condition		Min	Typ	Max	Units
Baseband Frequency Response	Deviation from ideal 7th-order Butterworth, measure to F – 3 dB x 0.7. Include front-end tilt effects		–0.5	–	0.5	dB
LPF Cutoff Frequency Accuracy	Measured –3 dB point.	@8 MHz @31.4 MHz	–5.5 –10	– –	5.5 10	% %
Quadrature Gain Error	Includes effects from baseband filters		–	–	1.2	dB
Quadrature Phase Error	Measure at 125 kHz		–	–	4	Deg
Synthesizer						
Crystal Frequency Range			4	–	7.26	MHz
XTLOUT Voltage Levels	Measured on 10 pF in parallel with 1 MΩ		0.75	1.0	1.5	Vpp
XTLOUT DC Level			–	2.0	–	V
MODp, MODn Delay	Must assert MOD level within this time period to ensure that the next PSOUT period gives correct count. Delay is with respect to rising edge of PSOUT (previous count).		–	–	7	nsec
PLLINp, PLLINn and MODp, MODn Hold Time	With respect to rising edge of PSOUT. This means that PSOUT need not continue to be asserted after MOD has given correct count.		0	–	–	nsec
Local Oscillator						
LO Tuning Range			543	–	1180	MHz
LO Phase Noise, Including Doubler. Subject to LC tank implementation.	1 kHz offset. Depends on PLL loop gain.		–	–55	–	dBc/Hz
	10 kHz offset. Depends on PLL loop gain.		–	–75	–	dBc/Hz
	100 kHz offset		–	–95	–	dBc/Hz
LO Buffer Frequency Range when overdriven by external LO	FDOUB = low		925	–	2175	MHz

(Sheet 3 of 3)

1. For symbol rates below 15 MS/s, the maximum input power might be subject to shifting down by roughly 10 * log(15/Rs[MS/s]) dB due to channel bandwidth reduction.
2. x 1.5 harmonic rejection for F_{LO} = 725 MHz.

Table 5 L64733C-48 Pin Description Summary

Mnemonic	Description	Type
AGC1	Automatic Gain Control 1	Input
AGC2	Automatic Gain Control 2	Input
CFLT	Bias Voltage Bypass	Bidirectional
CP	Charge Pump	Output
CPG[2:1]	Charge Pump Gain	Input
FB	Feedback Charge Pump Transistor Drive	Output
FDOUB	Frequency Doubler	Input
FLCLK	Filter Clock	Input
GND	Ground (seven pins total)	Input
IDCp	I-Channel DC Offset Correction (noninverting)	Input
IDCn	I-Channel DC Offset Correction (inverting)	Input
INSEL	RF Port Input Select	Input
IOUTp	I-Channel Baseband Data (noninverting)	Output
IOUTn	I-Channel Baseband Data (inverting)	Output
LOBUF	Local Oscillator Buffer Select	Input
LODIV	Local Oscillator Buffer Division Ratio Select	Input
MODp	Prescaler Modulus (noninverting)	Input
MODn	Prescaler Modulus (inverting)	Input
PLLINp	Phase Detector (noninverting)	Input
PLLINn	Phase Detector (inverting)	Input
PSOUTp	Prescaler (noninverting)	Output
PSOUTn	Prescaler (inverting)	Output
QDCp	Q-Channel DC Offset Correction (noninverting)	Input

(Sheet 1 of 2)

Table 5 L64733C-48 Pin Description Summary (Cont.)

Mnemonic	Description	Type
QDCn	Q-Channel DC Offset Correction (inverting)	Input
QOUTp	Q-Channel Baseband Data (noninverting)	Output
QOUTn	Q-Channel Baseband Data (inverting)	Output
RFINp	RF Input (noninverting)	Input
RFINn	RF Input (inverting)	Input
RFOUT	RF Output (Loop-Through)	Output
TANKp	Oscillator Tank Port (noninverting)	Input
TANKn	Oscillator Tank Port (inverting)	Input
VCC	Power (six pins total)	Input
VRLO	Local Oscillator Regulator Bypass	Bidirectional
XTLp	Crystal Oscillator Port (noninverting)	Input
XTLn	Crystal Oscillator Port (inverting)	Input
XTLOUT	Crystal Out	Output
(Sheet 2 of 2)		

Table 6 L64733C-44 Pin Description Summary

Mnemonic	Description	Type
AGC1	Automatic Gain Control 1	Input
AGC2	Automatic Gain Control 2	Input
CFLT	Bias Voltage Bypass	Bidirectional
CP	Charge Pump	Output
CPG[2:1]	Charge Pump Gain	Input
FB	Feedback Charge Pump Transistor Drive	Output
FDOUB	Frequency Doubler	Input
FLCLK	Filter Clock	Input
GND	Ground (three pins total)	Input
IDCp	I-Channel DC Offset Correction (noninverting)	Input
IDCn	I-Channel DC Offset Correction (inverting)	Input
INSEL	RF Port Input Select	Input
IOUTp	I-Channel Baseband Data (noninverting)	Output
IOUTn	I-Channel Baseband Data (inverting)	Output
LOBUF	Local Oscillator Buffer Select	Input
LODIV	Local Oscillator Buffer Division Ratio Select	Input
MODp	Prescaler Modulus (noninverting)	Input
MODn	Prescaler Modulus (inverting)	Input
PLLINp	Phase Detector (noninverting)	Input
PLLINn	Phase Detector (inverting)	Input
PSOUTp	Prescaler (noninverting)	Output
PSOUTn	Prescaler (inverting)	Output
QDCp	Q-Channel DC Offset Correction (noninverting)	Input

(Sheet 1 of 2)

Table 6 L64733C-44 Pin Description Summary (Cont.)

Mnemonic	Description	Type
QDCn	Q-Channel DC Offset Correction (inverting)	Input
QOUTp	Q-Channel Baseband Data (noninverting)	Output
QOUTn	Q-Channel Baseband Data (inverting)	Output
RFINp	RF Input (noninverting)	Input
RFINn	RF Input (inverting)	Input
RFOUT	RF Output (Loop-Through)	Output
TANKp	Oscillator Tank Port (noninverting)	Input
TANKn	Oscillator Tank Port (inverting)	Input
VCC	Power (six pins total)	Input
VRLO	Local Oscillator Regulator Bypass	Bidirectional
XTLp	Crystal Oscillator Port (noninverting)	Input
XTLn	Crystal Oscillator Port (inverting)	Input
XTLOUT	Crystal Out	Output
(Sheet 2 of 2)		

L64734 Electrical Specifications

This section contains the electrical parameters for the L64734. Table 7 lists the absolute maximum values. Exceeding the values listed can cause damage to the L64734. Table 8 gives the recommended operating supply voltage and temperature conditions. Table 9 shows the pin capacitance, Table 10 gives the DC characteristics, and Table 11 summarizes the pins.

Table 7 L64734 Absolute Maximum Rating (Referenced to V_{SS})

Symbol	Parameter	Limits[1]	Units
V_{DD}	DC Supply Voltage	–0.3 to + 3.9	V
V_{IN}	LVTTL Input Voltage	–1.0 to V_{DD} + 0.3	V
V_{IN}	5 V Compatible Input Voltage	–1.0 to 6.5	V
I_{IN}	DC Input Current	±10	mA
T_{STG}	Storage Temperature Range (Plastic)	–40 to +125	°C

1. Note that the ratings in this table are those beyond which permanent device damage is likely to occur. Do not use these values as the limits for normal device operation.

Table 8 L64734 Recommended Operating Conditions

Symbol	Parameter	Limits[1]	Units
V_{DD}	DC Supply Voltage	+3.14 to 3.47	V
T_A	Operating Ambient Temperature Range (Commercial)	0 to +70	°C
T_j	Junction Temperature	+125	°C
Θ_{jc}	Junction to Case Thermal Resistance[2]	7	°C/watt

1. For normal device operation, adhere to the limits in this table. Sustained operation of a device at conditions exceeding these values, even if they are within the absolute maximum rating limits, can result in permanent device damage or impaired device reliability. Device functionality to stated DC and AC limits is not guaranteed if recommended operating conditions are exceeded.
2. The junction to case thermal resistance is valid for measurements in an isothermal environment including the board and package.

Table 9 L64734 Capacitance

Symbol	Parameter[1]	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF

1. Measurement conditions are V_{IN} = 3.3 V, T_A = 25 ˚C, and clock frequency = 1 MHz.

Table 10 DC Characteristics of the L64734

Symbol	Parameter	Condition[1]	Min	Typ	Max	Units
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
V_{IL}	Input Voltage LOW		V_{SS} – 0.5	–	0.8	V
V_{IH}	Input Voltage HIGH	LVTTL Com/Ind/Mil Temp Range	2.0	–	V_{DD} + 0.3	V
		5 V compatible	2.0	–	5.5	V
V_T	Switching Threshold		–	1.4	2.0	V
I_{IL}	Input Current Leakage	V_{DD} = Max, V_{IN} = V_{DD} or V_{SS}	–10	±1	10	µA
I_{IPU}	Input Current Leakage with Pull-up	V_{IN} = V_{SS}	–62	–215	–384	µA
I_{IPD}	Input Current Leakage with Pull-down	V_{IN} = V_{DD}	–62	–215	–384	µA
V_{OH}	Output Voltage HIGH	I_{OH} = –1.0, –2.0, –4.0, –6.0, –8.0, –12.0 mA	2.4	–	V_{DD}	V
V_{OL}	Output Voltage LOW	I_{OH} = 1.0, 2.0, 4.0, 6.0, 8.0, 12.0 mA	—	0.2	0.4	V
I_{OZ}	3-State Output Leakage Current	V_{DD} = Max, V_{OUT} = V_{SS} or 3.5 V	-10	±1	10	µA
I_{DD}	Quiescent Supply Current	V_{IN} = V_{DD} or V_{SS}	–		2	mA
I_{CC}	Dynamic Supply Current	f = MHz, V_{DD} = Max	–	290	–	mA
V_{CM}	Midpoint of PSOUTp, PSOUTn inputs		–	2.4	–	V
V_{IH_PECL}	Input Voltage High Level (DC)	PSOUTp – PSOUTn = 50 mV	V_{CM} + 50 mV	–	–	V

(Sheet 1 of 2)

Table 10 DC Characteristics of the L64734 (Cont.)

Symbol	Parameter	Condition[1]	Min	Typ	Max	Units
V_{IL_PECL}	Input Voltage Low Level (DC)	PSOUTp – PSOUTn = 50 mV	–	–	V_{CM} – 50 mV	V
I_{IL_PECL}	Input Low Current	$V_{IN} = V_{SS}$	–10	–	–	µA
I_{IH_PECL}	Input High Current	$V_{IN} = V_{DD}$	–	–	+10	µA
V_{RESO_LVDS}	Output Voltage on pin RESO_LVDS		–	1.2	–	V
V_{OH_LVDS}	Output Voltage High Level (DC)	On PLLINp/PLLINn, MODp/MODn signals	1.253	1.373	1.437	V
V_{OL_LVDS}	Output Voltage Low Level (DC)	On PLLINp/PLLINn, MODp/MODn signals	1.030	1.032	1.059	V
(Sheet 2 of 2)						

1. Specified at V_{DD} = 3.3 V ± 5% at ambient temperature over the specified range.

Table 11 L64734 Pin Description Summary

Mnemonic	Description	Type
ADCVDDI/Q	ADC Power	Input
ADCVSSI/Q	ADC Analog Ground	Input
AGC1, AGC2	Power Control	Outputs
BCLKOUT	Byte Clock Out	Output
CLK	IVIN/QVIN Input Clock	Input
CO[7:0]	Channel Data Out	Output
COEn	Channel Output Enable	Input
DVALIDOUT	Valid Data Out	Output
ERROROUTn	Error Detection Flag	Output
FBUFVDD	Analog Supply	Input
FBUFVSS	Analog Ground	Input
(Sheet 1 of 3)		

Table 11 L64734 Pin Description Summary (Cont.)

Mnemonic	Description	Type
FDOUB	Frequency Doubler	Output, 3-State
FLCLK	Filter Control Clock	Output
FSTARTOUT	Frame Start Output	Output
IBIAS	ADC Bias Current	Output
IBYPASS[5:0]	I Channel Data (ADC bypassed)	Inputs
IDDTN	Test	Input
INSEL	RF Input Select	Output
INTn	Interrupt	Output
IVINn, IVINp	I Channel Data	Input
LCLK	Decimated Clock Output	Output
LP2	Input to VCO	Input
MODp, MODn	Modulus Selector	Outputs
PCLK	PLL Clock Output	Output
PLLAGND	PLL Analog Ground	Input
PLLINn, PLLINp	PLL Differential Counter M	Outputs
PLLVDD	PLL Power	Input
PLLVSS	PLL Ground	Input
PSOUTp, PSOUTn	Prescaler Output	Outputs
QBYPASS[5:0]	Q Channel Data (ADC bypassed)	Input
QVINn, QVINp	Q Channel Data	Input
RESET	Reset	Input
RESO_LVDS	LVDS Buffers Precision Resistor	Output
SADR[1:0]	Serial Address	Input
SCLK	Serial Clock	Bidirectional

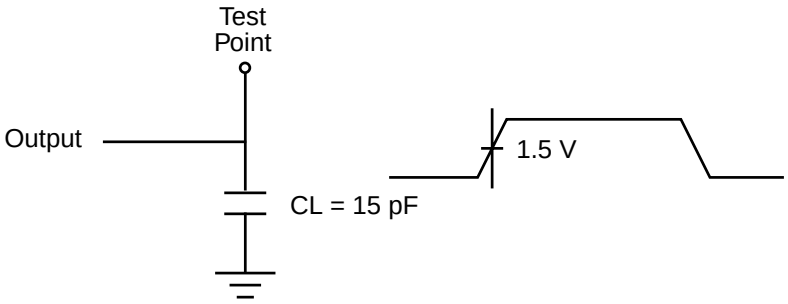
(Sheet 2 of 3)

Table 11 L64734 Pin Description Summary (Cont.)

Mnemonic	Description	Type
SDATA	Serial Data	Bidirectional
VREF_LVDS	LVDS Buffers Reference Voltage	Input
XCTR_IN	Control Input	Input
XCTR[3:0]	Control Output/Sync Status Flag	Output
XOIN	Crystal Oscillator In	Input
XOOUT	Crystal Oscillator Out	Output
(Sheet 3 of 3)		

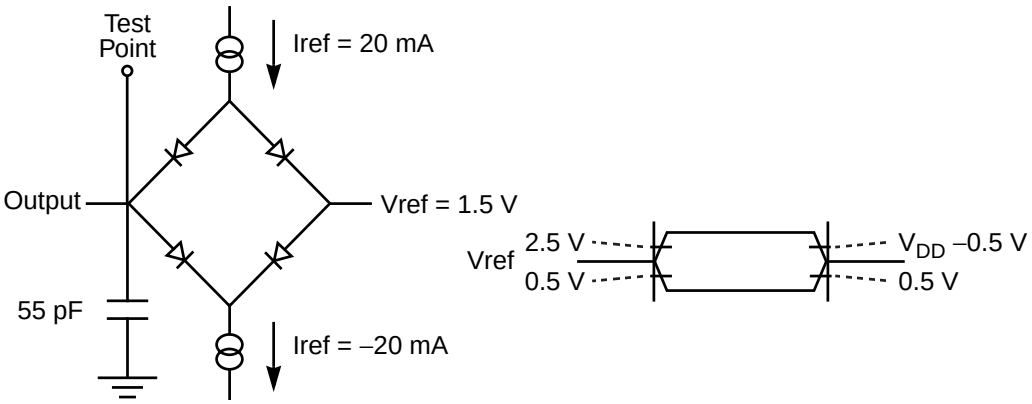
This section includes AC timing information for the L64734. During AC testing, HIGH inputs are driven to 3.0 V and LOW inputs are driven to 0 V. For transitions between HIGH, LOW, and invalid states, timing measurements are made at 1.5 V, as shown in Figure 8.

Figure 8 AC Test Load and Waveform for Standard Outputs



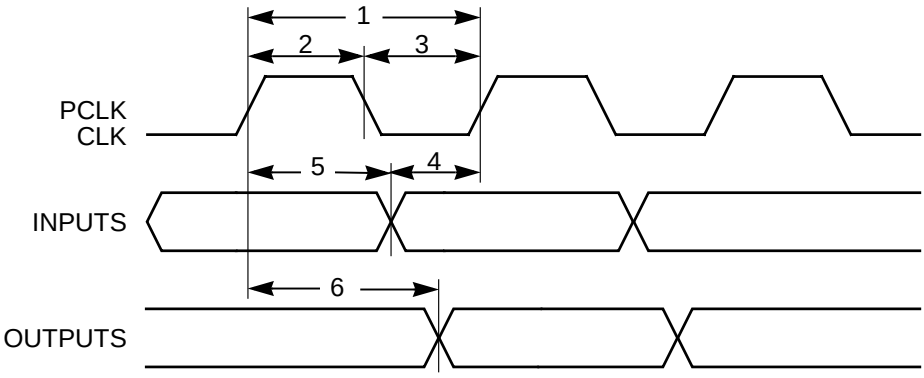
For 3-state outputs, timing measurements are made from the point at which the output turns ON or OFF. An output is ON when its voltage is greater than 2.5 V or less than 0.5 V. An output is OFF when its voltage is less than V_{DD} – 0.5 V or greater than 0.5 V, as shown in Figure 9.

Figure 9 AC Test Load and Waveforms for 3-State Outputs



Synchronous timing is shown in Figure 10. Synchronous inputs must have a setup and hold relationship with respect to the clock signal that samples them. Synchronous outputs have a delay from the clock edge that asserts them.

Figure 10 L64734 Synchronous AC Timing



The reset pulse requirements are shown in Figure 11.

Figure 11 L64734 RESET Timing Diagram

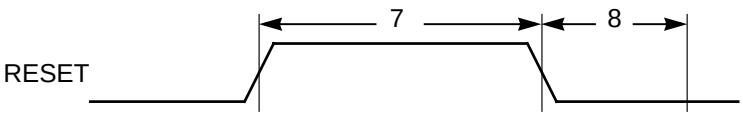


Figure 12 shows the relationship of the L64734 3-state signals to the COEn signal.

Figure 12 L64734 Bus 3-State Delay Timing

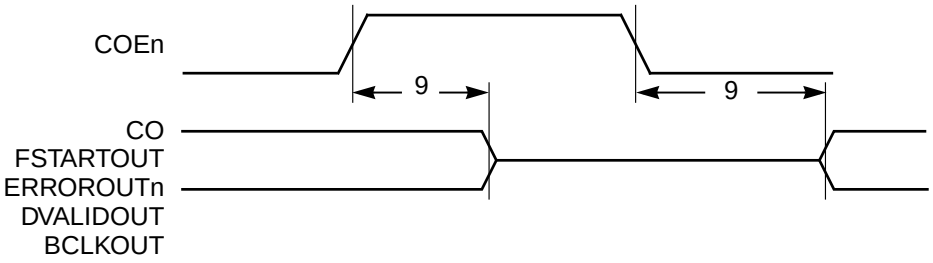
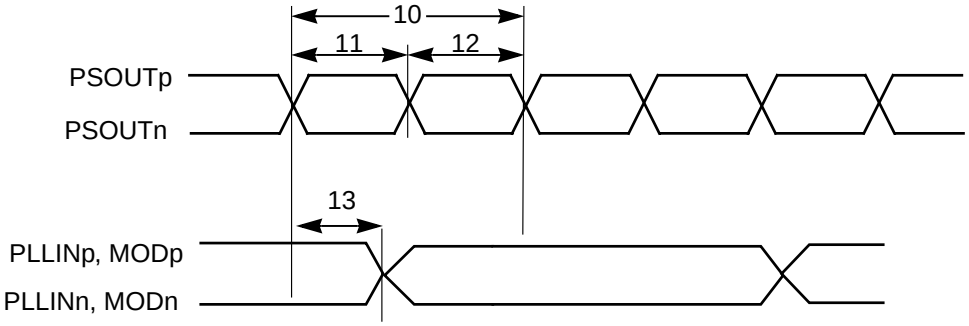


Figure 13 shows the relationship of the L64733C PSOUTp and PSOUTn prescaler signals to the signals fed back to the L64733C from the L64734 to control the synthesizer.

Figure 13 L64734 Synchronous AC Timing - Synthesizer Control



The numbers in the first column of Table 12 refer to the timing parameters shown in the preceding figures. All parameters in the timing tables apply for T_A = 0 °C to 70 °C and a capacitive load of 15 pF.

Table 12 L64734 AC Timing Parameters

Parameter		Description	90 MHz		Units
			Min	Max	
1	t_{CYCLE}	Clock Cycle for PCLK	11.1	33.3[1]	ns
2	t_{PWH}	Clock Pulse Width HIGH	6	–	ns
3	t_{PWL}	Clock Pulse Width LOW	5	–	ns
4	t_S	Input Setup Time to CLK	4	–	ns
5	t_H	Input Hold to CLK	4	–	ns
6	t_{ODS}	Output Delay from PCLK, serial mode	3	8	ns
6	t_{ODP}	Output Delay from BCLKOUT, parallel mode	3	–	PCLK cycles
7	t_{RWH}	Reset Pulse Width HIGH	3	–	CLK cycles
8	t_{WK}	Wake-Up Time	280	–	CLK cycles
9	T_{DLY}	Delay from COEn	–	6	ns
10	t_{CYCLE_PS}	Clock Cycle for PSOUTp, PSOUTn clock	14	35	ns
11	t_{PWH_PS}	PSOUT Clock Pulse Width HIGH	6	–	ns
12	t_{PWL_PS}	PSOUT Clock Pulse Width LOW	6	–	ns

1. Minimum Fs (sampling clock = 30 MHz).

L64733C/734 Chipset Ordering Information

The L64733C-48 is available in a 48-pin TQFP package, the L64733C-44 is available in a 44-pin MLF2 package, and the L64734 is available in a 100-pin PQFP package. They are ordered as a set. Table 13 gives ordering information for the chipset.

Table 13 L64733C/734 Chipset Ordering Information

Order Number	Package Type	Operating Range
Kit 733x 734y x = 733 version y = 734 version	 48-pin TQFP (L64733C-48) 44-pin MLF2 (L64733C-44) 100-pin PQFP (L64734)	Commercial

The tables and figures that follow provide pinouts and mechanical drawings for each package in the chipset.

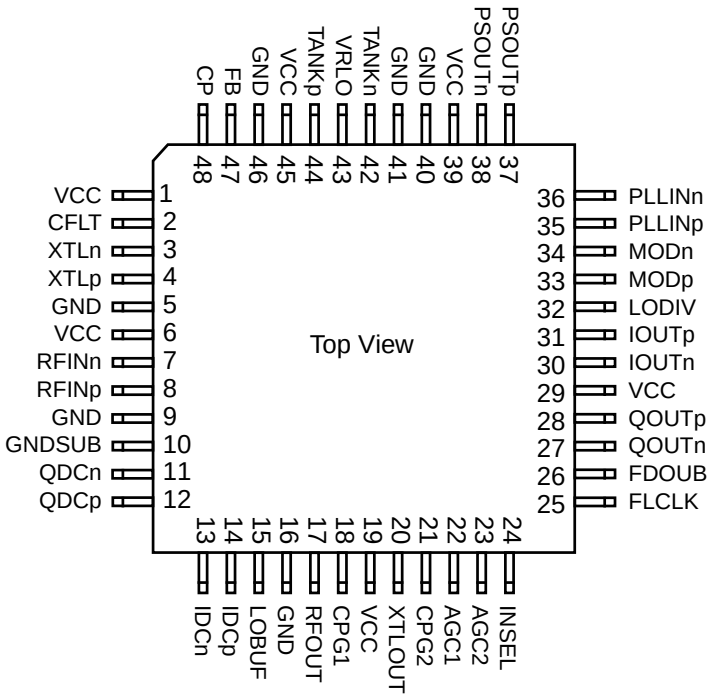
L64733C-48 Pinout and Packaging Information

The following subsections provide pinout and packaging information for the 48-pin L64733C chip.

L64733C-48 Pinouts

Figure 14 gives the pinout for the 48-pin TQFP L64733C-48 package.

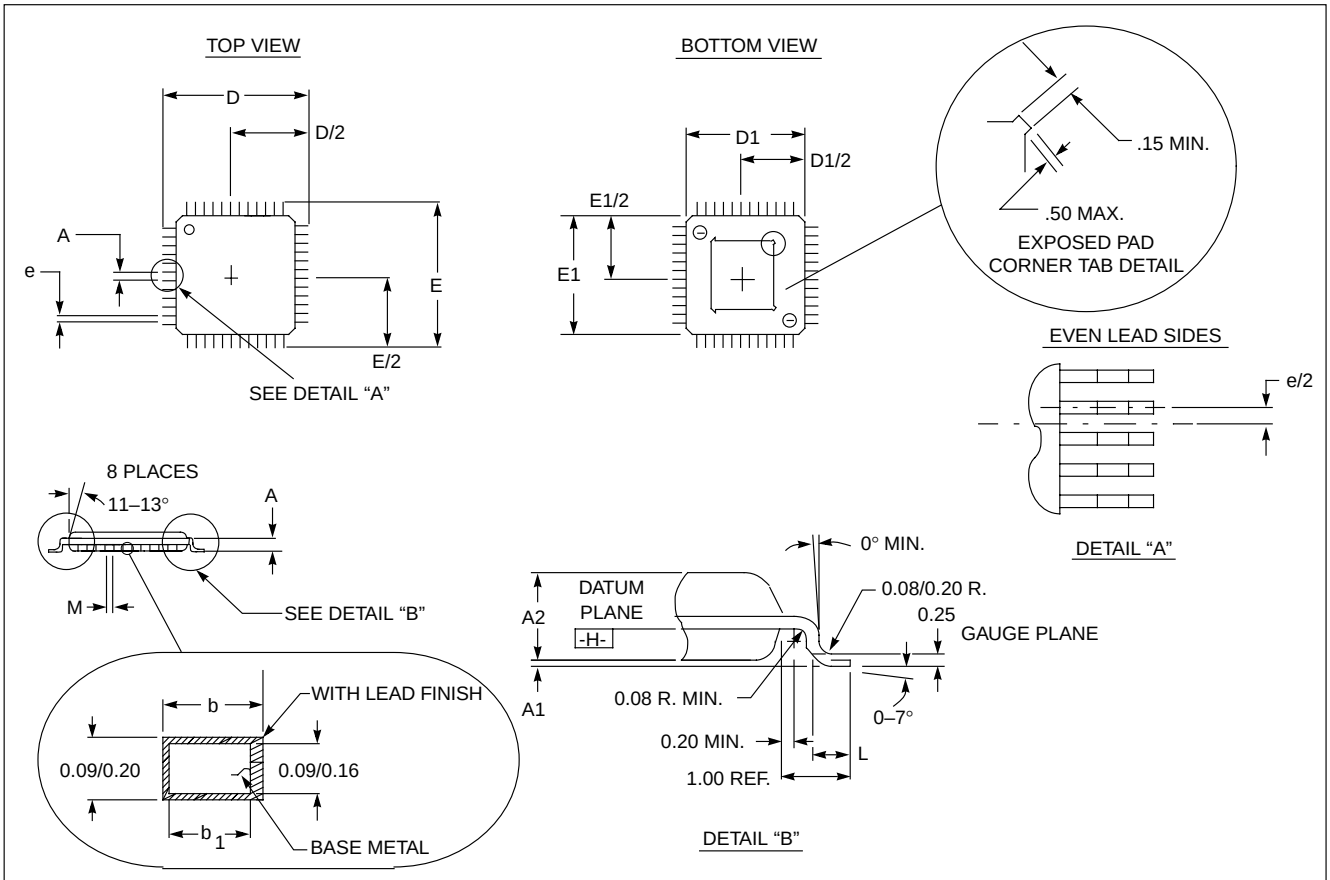
Figure 14 L64733C 48-Pin TQFP Pinout



L64733C-48 Mechanical Drawing

Figure 15 is a mechanical drawing for the 48-pin TQFP L64733C-48 package.

Figure 15 L64733C-48 48-pin TQFP Mechanical Drawing



Notes:
1. All dimensioning and tolerancing conform to Ansi Y14.5–1982.
2. Datum plane – H – is located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Dimensions D1 and E1 do not include mold protrusion. allowable mold protrusion is 0.254 mm on D1 and E1 dimensions.
4. The top of package is smaller than the bottom of package by 0.15 millimeters.
5. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the B dimension at maximum material condition.
6. Controlling dimension: millimeter.
7. Maximum allowable die thickness to be assembled in this package family is 0.30 millimeters.
8. This outline conforms to Jedec Publication 95 Registration MO–136, variations AC and AE.
9. Exposed die pad shall be coplanar with bottom of package within 2 mils (0.05 mm).
10. Metal area of exposed die pad shall be within 0.3 mm of the nominal die pad size.

SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
	AE		
	MIN.	NOM.	MAX.
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
D		9.00 BSC.	
D1		7.00 BSC.	
E		9.00 BSC.	
E1		7.00 BSC.	
L	0.45	0.60	0.75
M	0.14		
N		48	
e		0.5 BSC.	
b	0.17	0.22	0.27
b1	0.17	0.20	0.23

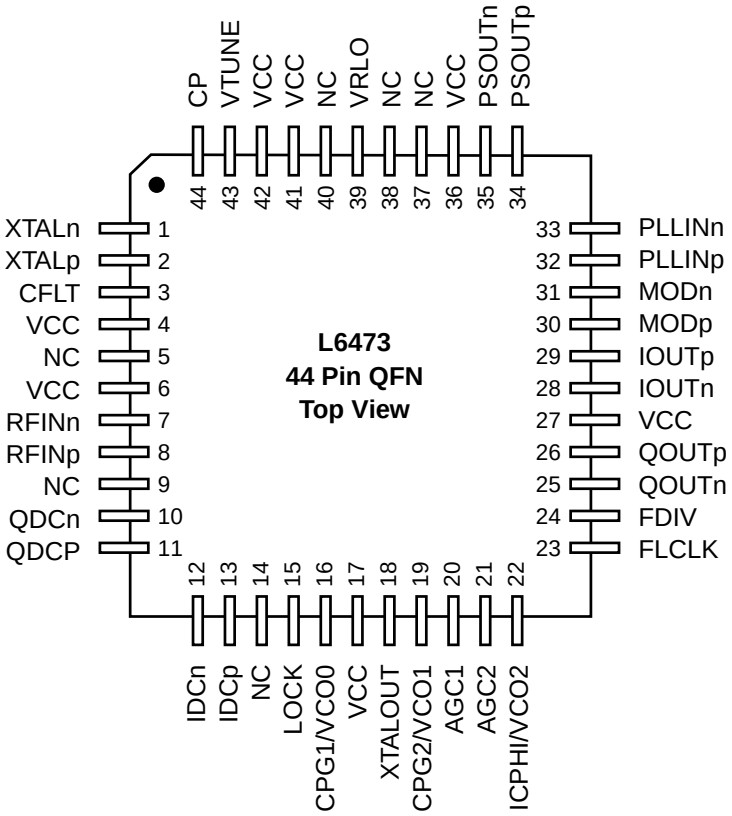
L64733C-44 Pinout and Packaging Information

The following subsections provide pinout and packaging information for the 44-pin L64733C chip.

L6433C-44 Pinout

Figure 16 gives the pinout for the 44-pin QFN L64733-44 package.

Figure 16 L64733 44-Pin QFN Pinout



L64733C-44 Mechanical Drawings

Figure 17 is a mechanical drawing for the 44-pin QFN L64733-44 package.

Figure 17 L64733C-44 44-pin QFN Mechanical Drawing

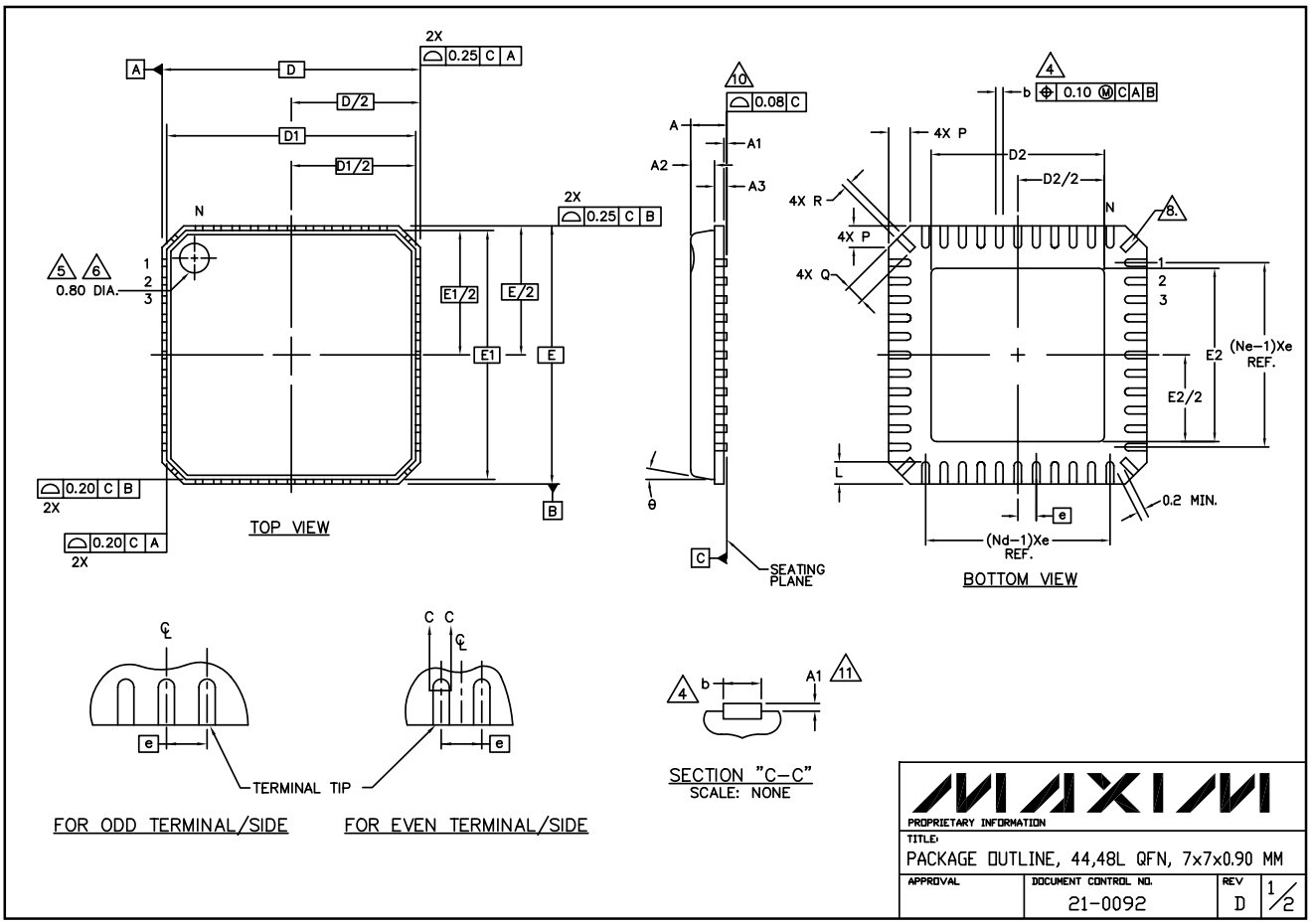


Figure 17 L64753-44 44-pin QFN Mechanical Drawing (Cont.)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.08mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
    EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.
12. MEETS JEDEC MO220.

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.90	1.00	
A1	0.00	0.01	0.05	11
A2	–	0.65	0.80	
A3		0.20 REF.		
D		7.00 BSC		
D1		6.75 BSC		
E		7.00 BSC		
E1		6.75 BSC		
θ			12°	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	

SYMBOL	PITCH VARIATION C			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		44		3
Nd		11		3
Ne		11		3
L	0.50	0.60	0.75	
b	0.18	0.23	0.30	4
Q	0.30	0.40	0.65	
D2	SEE EXPOSED PAD VARIATION: A,B,D			
E2	SEE EXPOSED PAD VARIATION: A,B,D			

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		48		3
Nd		12		3
Ne		12		3
L	0.30	0.40	0.45	
b	0.18	0.23	0.30	4
Q	0.00	0.20	0.45	
D2	SEE EXPOSED PAD VARIATION: C			
E2	SEE EXPOSED PAD VARIATION: C			

SYMBOLS		D2			E2			NOTE
		MIN	NOM	MAX	MIN	NOM	MAX	
EXPOSED PAD VARIATIONS	A	4.55	4.70	4.85	4.55	4.70	4.85	
	B	3.15	3.30	3.45	3.15	3.30	3.45	
	C	4.95	5.10	5.25	4.95	5.10	5.25	
	D	3.65	3.80	3.95	3.65	3.80	3.95	

EXAMPLE: WE CAN CALL VARIATION "CA" FOR 44 TERMINAL QFN WITH 4.70x4.70 mm NOMINAL EXPOSED PAD DIMENSION. THE FORMER ONE IN VARIATION IS FOR PITCH VARIATION AND THE LATTER ONE IS FOR EXPOSED PAD VARIATION.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 44,48L QFN, 7x7x0.90 MM

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0092	D	2/2

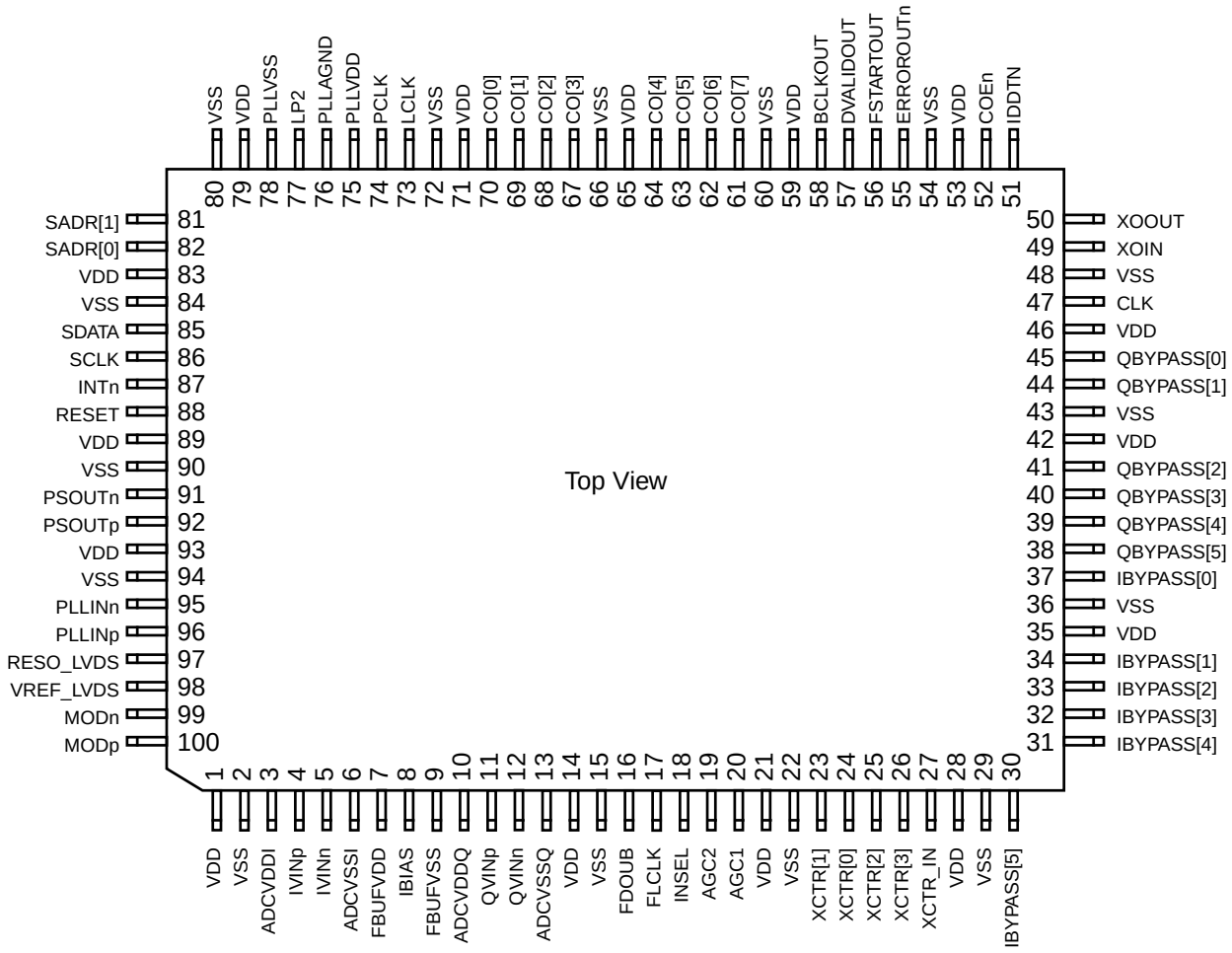
L64734 Pinout and Packaging Information

The following subsections provide pinout and packaging information for the L64734.

L64734 Pinouts

Figure 18 gives the pinout for the 100-pin PQFP L64734 package.

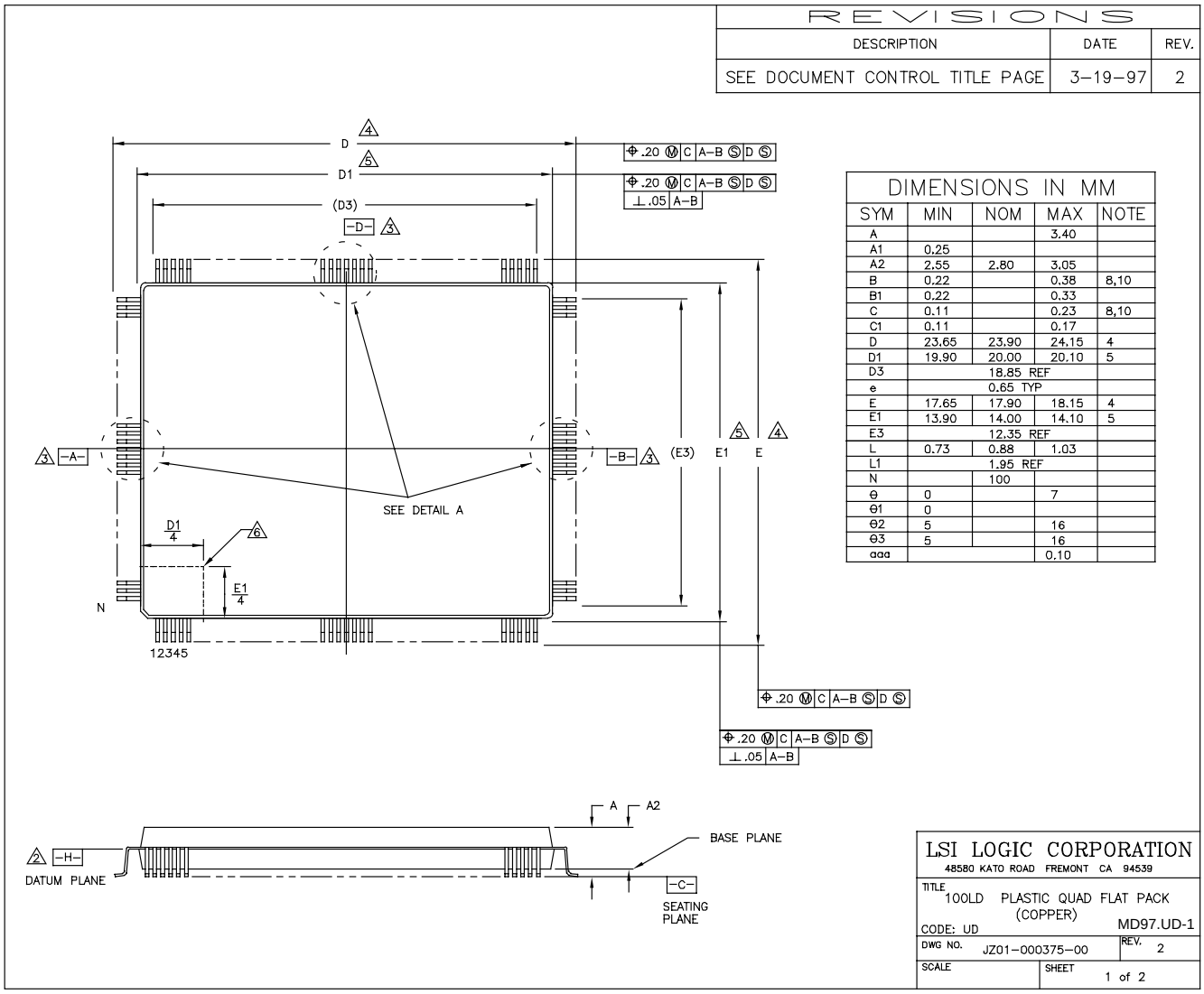
Figure 18 L64734 100-Pin PQFP Pinout



L64734 Mechanical Drawings

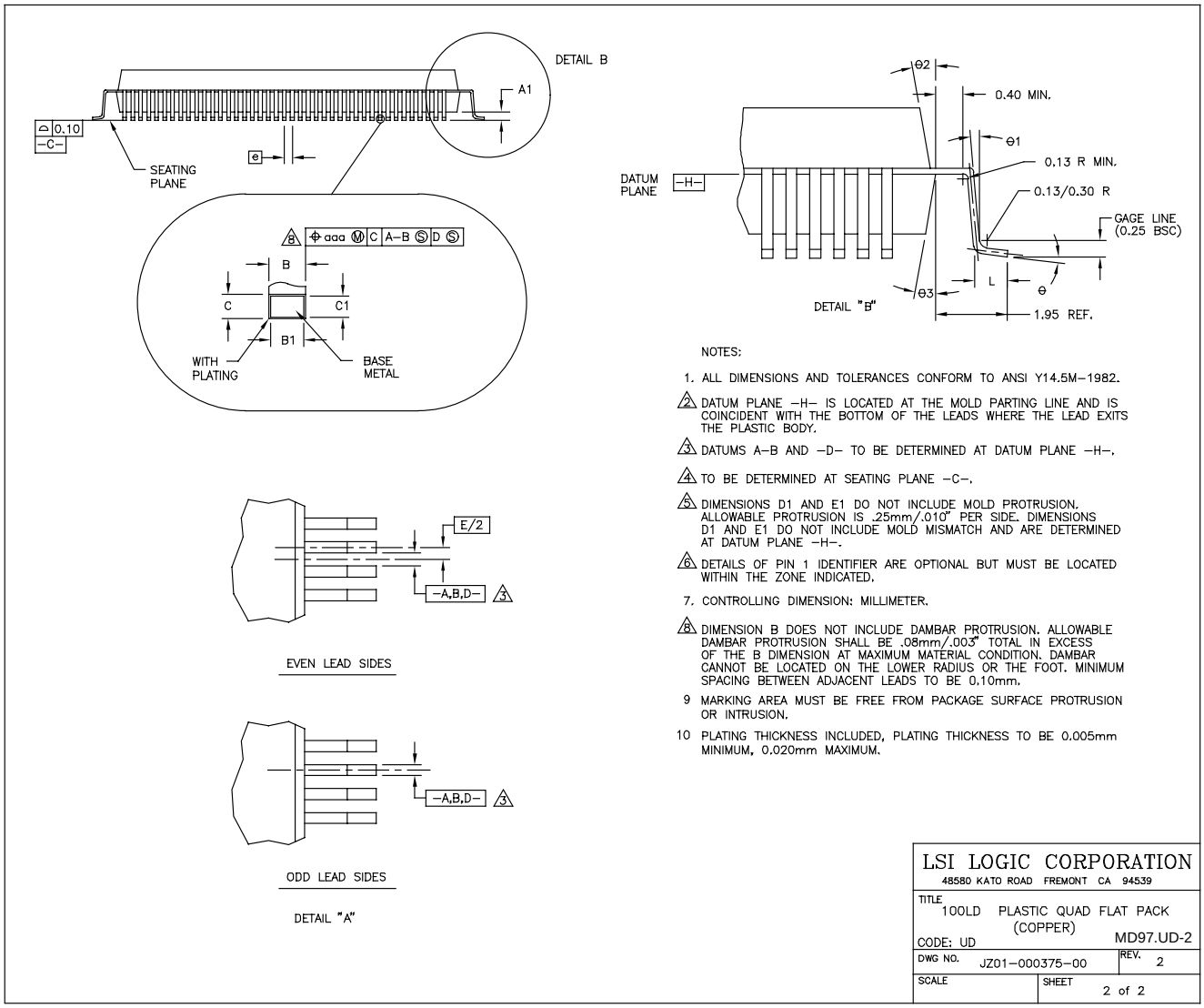
Figure 19 and Figure 20 show the mechanical drawings for the 100-pin PQFP L64734 package.

Figure 19 100-pin PQFP (UD) Mechanical Drawing



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative.**

Figure 20 100-pin PQFP (UD) Mechanical Drawing (Cont.)



NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982.
2. DATUM PLANE –H– IS LOCATED AT THE MOLD PARTING LINE AND IS COINCIDENT WITH THE BOTTOM OF THE LEADS WHERE THE LEAD EXITS THE PLASTIC BODY.
3. DATUMS A–B AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
4. TO BE DETERMINED AT SEATING PLANE –C–.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .25mm/.010" PER SIDE. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. CONTROLLING DIMENSION: MILLIMETER.
8. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .08mm/.003" TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACING BETWEEN ADJACENT LEADS TO BE 0.10mm.
9. MARKING AREA MUST BE FREE FROM PACKAGE SURFACE PROTRUSION OR INTRUSION.
10. PLATING THICKNESS INCLUDED, PLATING THICKNESS TO BE 0.005mm MINIMUM, 0.020mm MAXIMUM.

LSI LOGIC CORPORATION 48580 KATO ROAD FREMONT CA 94539		
TITLE: 100LD PLASTIC QUAD FLAT PACK (COPPER)		
CODE: UD		MD97.UD-2
DWG NO. JZ01–000375–00	REV. 2	
SCALE	SHEET 2 of 2	

Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code UD.**

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