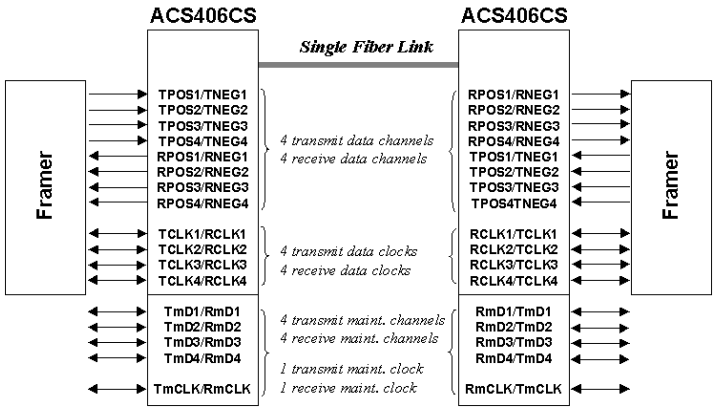
4000 SERIES

Acapella Optical Modem IC

ACS406CS Main Features

* Full duplex serial transmission through a single fiber-optic cable without the need for expensive WDM devices.
* E2 data-rates of 8.448Mbps or 4 * E1 at 2.048Mbps.
  T2 data rates of 6.312Mbps or 4 * T1 at 1.544Mbps.
* 4 clock domains for independent transmission of 4 * E1 or 4 * T1 data channels.
* Link lengths up to 25km (50km at reduced bandwidth).
* Single wavelength of light to transmit and receive data.
* Low power, zero cross talk between Rx and Tx channels.
* Incorporates up to 4 maintenance channel at 16kbps or 1 channel at 64kbps.
* Bit Error Rate (BER) of < 10^{-10}
* Typical latency of 0.75ms.



Single fiber full duplex system using ACS406CS chip set with a quad T1/E1 Framer IC.

General Description

The ACS406CS is a complete controller, driver and receiver chip-set, supporting full-duplex synchronous transmission up to 8.448/6.312Mbps over a single-optical fiber. The designer can share the available bandwidth over 1 to 8 main channels by selecting the appropriate combination on the DR input pins. In addition to the main channels, the ACS406CS provides either 1 x 64kbps or 4 x 16kbps auxilliary maintenance channels.

The internal machine cycle provides for link lengths up to 25/50km. On the electrical side HDB3/AMI/NRZ/B8ZS interfaces are selectable.

Communicating modems automatically maintain synchronisation with each other, such that the receive phase of one modem is lined-up with the transmit phase of the other, compensating for the propagation delay presented by the link. Link lengths from zero to maximum distance are catered for automatically.

The ACS406CS comprises a chip-set of two highly integrated devices, the ACS9010 and ACS4060. The ACS9010 is an analogue device and the ACS4060 is predominately a digital device.

The ACS9010 contains the Laser/LED driver as well as the PIN receiver circuitry. Since the device does not transmit and receive concurrently (ping-pong), there is no risk of noise generated by the transmitter interfering with the sensitive receive circuitry.

The ACS4060 comprises the logic necessary to time compress and decompress the data, plus all the logic associated with window synchronisation and locking.

For the purpose of this specification the chip-set will be referred to as the ACS406CS and the individual devices as the ACS9010 or ACS4060.

Inter-Modem Coding

The inter-IC coding between communication modems is 8B10B. Whilst transparent to the user, 8B10B encoding ensures that there is no DC component in the signal, and provides frequent data transitions, factors which ease the task of data recovery and clock extraction.

The coding rules are continuously checked to ensure the integrity of the link, and errors are indicated on the ERRL and ERRC pins *(see section headed ERRC and ERRL - Error Detection).*

The Transmit and Receiver Functions

Data presented at the near-end TPOS/TNEG is time-compressed, encoded in the 8B10B format and transmitted over the link in a high frequency burst. The optical interface is then configured as a receiver ready to accept data from the far-end. The received data is decoded, time decompressed and de-jittered and then presented to the RPOS/RNEG data output pins.

PORB

The Power On Reset (PORB) pin resets the device if forced low for 2ms or more. In normal operation PORB should be held High. It is recommended that PORB is connected to VD+ via a 100KΩ resistor and to GND via a 100nF capacitor.

PORB has a special function when used in conjunction with memory lock (see section headed *Diagnostic Modes*).

System Clock

The system clock on the ACS406CS may be derived from an external source or generated locally using the on-chip crystal oscillator.

The oscillator (XTO/I) requires the use of a fundamental parallel resonance crystal with appropriate padding capacitors. The input pin, SCEXT should be connected to GND. The crystal specification should be:

Calibration tolerance:	+/- 20ppm @ 25ºC
Temp. tolerance:	+/-20ppm @ -40 to +85ºC
Temperature range:	-40 to +85ºC
Load condition:	parallel load 15pF
Padding capacitor:	18-22pF (tune for desired tolerance)

If it is required to drive the device with an externally generated system clock source, then the clock source should be connected to input pin ECLK with SCEXT connected to VD+. It is often more convenient to drive boards containing multi ACS406CS chip-sets from a single system clock source.

The system clock frequency is determined by the choice of data rates and is tabulated in section headed, *Data Rate Selection.* For example, for E2 operation, the appropriate frequency is 33.792MHz and for T2 operation, 31.560MHz.

The system clock defines the burst frequency at which data is transmitted over the optical link via the optical interface. The receive circuitry within the ACS4060 recovers the clock from the received data at the Rxdat inputs and produces a clock that is synchronised to the incoming data stream. The system clock must have a maximum tolerance of +/-50ppm over the desired temperature range.

Optical Operational Modes

The ACS406CS has four optical operational modes controlled by the pins LASER, LASRX and PINRX on the ACS9010 device.

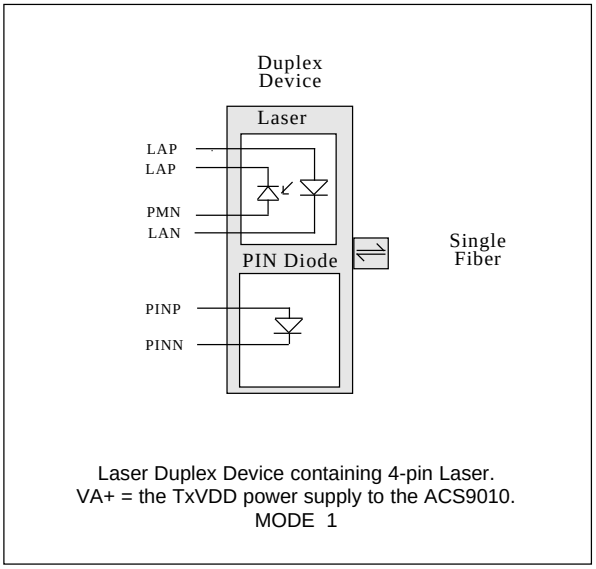
All of the duplex modes in Table 1 may be converted to dual fiber operation simply by interfacing to separate transmitting and receiving devices.

Mode	Optical Device
1	Laser Duplex using 4-pin Laser.
2	Laser Duplex using 3-pin Laser.
3	LED Duplex.
4	LED (ping-pong).

Table 1

Mode 1 - Laser Duplex using 4-pin Laser

In mode 1, the device is configured for use with a Laser duplex device containing a 4-pin laser. The diagram below shows the connections to the ACS9010 device. The operational control pins found on the ACS9010 are configured as follows:



Laser Duplex Device containing 4-pin Laser.
VA+ = the TxVDD power supply to the ACS9010.
MODE 1

LASER = VA+
LASRX = GND
PINRX = VA+

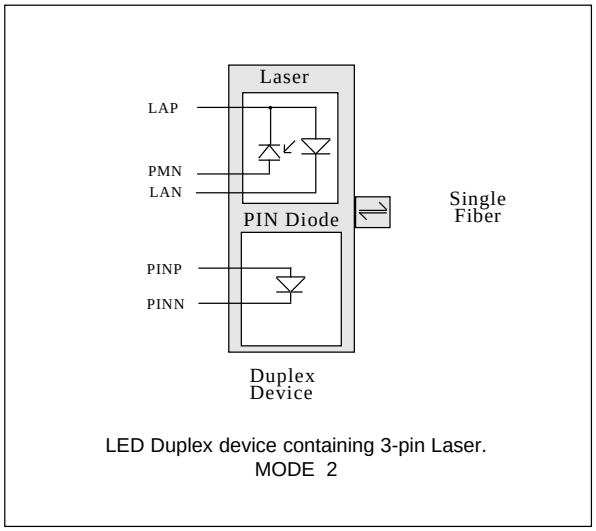
For the Bookham BKM 2101-A-02 transceiver module, the following connections should be made:

Monitor pd p side - pin2	=	PMN
Monitor pd n side - pin3	=	LAP
Laser diode n side - pin5	=	LAN
Laser diode p side - pin6	=	LAP
Receive pd p side - pin9	=	PINP
Receive pd n side - pin 10	=	PINN

pin 1, 4, 7, 8, 11, 14 should be tied to GND

Mode 2 - Laser Duplex using 3-pin Laser

In mode 2, the device is configured for use with a Laser duplex device containing a 3-pin laser. The diagram below shows the connections to the ACS9010 device. The operational control pins found on the ACS9010 are configured as follows:

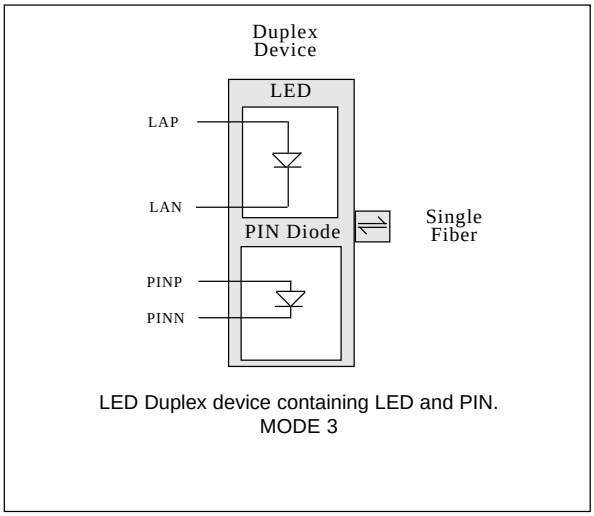


LED Duplex device containing 3-pin Laser.
MODE 2

LASER = VA+
LASRX = GND
PINRX = VA+

Mode 3 - LED Duplex Device

In mode 3, the device is configured for use with an LED duplex device. The diagram below shows the connections to the ACS9010 device. The operational control pins found on the ACS9010 are configured as follows:

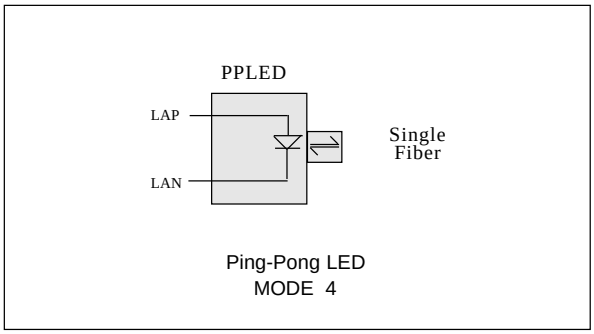


LED Duplex device containing LED and PIN.
MODE 3

LASER = GND
LASRX = GND
PINRX = VA+

Mode 4 - LED Ping Pong

In mode 4, the modem is configured for use with a ping-pong LED device (PPLED). The diagram below shows the connections to the ACS9010 device.
Ping-Pong LEDs are standard LEDs which exhibit good photo-detection (high responsivity, low capacitance) characteristics when reverse biased. Ping-Pong LEDs are available from several manufacturers as well as from Acapella.



Ping-Pong LED
MODE 4

LASER = GND
LASRX = VA+
PINRX = GND

Control of LED current

During the transmit cycle, the LED drive current is directly proportional to the programmed reference current. To minimise switching delay, a permanent bias current is maintained through the LED. The data modulation produces bursts of high light and low light to represent logic high and low levels respectively. The low light level is set by a current equal to 10% of the drive current generated for the high light level. Since LEDs have a linear relationship between current and optical output power, this results in a optical high power of 10 times the optical low power.

The optical power is controlled by a variable resistor (Rtset) connected between TSET and Ground (GND). The lower the value of Rtset the greater the current, for this reason the lower limit for Rtset should be 1KΩ, which equates to a nominal peak transmit current of 100mA. A practical maximum for Rtset is 50KΩ. Acapella, therefore recommends that Rtset should comprise a fixed resistor of 1KΩ in series with a logarithmic potentiometer of 50KΩ, thus, affording overload protection for the LED together with precise control of current.

$$I^{*}_{LED\ (High)} = 100 / Rtset$$

$$I^{*}_{LED\ (Low)} = 10 / Rtset$$

* where Rtset > 1KΩ, tolerance = +/- 20%.
I = Amps

Control of Laser Current

During the transmit cycle, the Laser drive current is controlled so as to maintain a constant optical output power from the Laser. The monitor-pin resident in the Laser converts the incident light power (from the Laser itself) to a monitor-current, which is directly compared to a preset programmed current (the current flowing through TSET). The Laser drive current is automatically adjusted to maintain the original preset light level over the recommended temperature and voltage range. The designer should be aware that whilst the control loop maintains the current generated by the monitor-pin within a tolerance of 2%, there is additional uncertainty attributed to the monitor-pin's temperature coefficient of responsivity. Data relating to the Laser characteristics should be acquired from the Laser supplier.

The monitor-pin current is set by a variable resistor (Rtset), connected between TSET and Ground (GND). Acapella recommends that Rtset should comprise a logarithmic potentiometer of value 50KΩ. It is important to ensure that the Rtset resistor is inserted and adjusted to its maximum resistance value of 50KΩ prior to applying power to the ACS9010 for the first time and prior to following the procedure detailed in section headed, *Laser Adjustment Procedure.*

$$I^{*}_{PIN\ (High)} = 2.0 / Rtset$$

* Tolerance = +/- 20%.
I = Amps

TxMN and TxFLG

TxMN is used to monitor the current delivered to the LED or Laser. TxMN is a current source that proportionally mirrors the current flow through the LED or Laser. By placing an appropriate resistor (Rtxmn) between TxMN and GND, the voltage developed (referenced to GND), will be proportional to the transmit current. During the Laser setup procedure TxMN should be monitored to ensure that the Laser manufacturer's maximum current specification is not exceeded (see section headed *Laser Adjustment Procedure*).

TxMN may also be employed during normal operation to continuously check the Laser current. The voltage developed across Rtxmn is compared within an internally generated reference voltage of 1.25V. In the event that the reference voltage is exceeded, the TxFLG is set high, otherwise it is set low.

The relationship between the transmit current and the TxMN current is :

$$I^{*}_{LASER\ (High)} = 100 * TxMN$$

* Tolerance = +/- 10%.
I = Amps
If Rtxmn = 1KΩ, then TxFLG = 1 when the Laser current exceeds 125mA.

Laser Adjustment Procedure

The output power from the Laser should be measured with a optical power meter during the setup procedure.

Select one of the Laser drive modes in accordance with section headed, *Operational Modes*. Start with the highest resistance for Rtset (at least 50KΩ is recommended). This defines the monitor-pin reference current. Select the Laser setup mode on the ACS4060 by asserting SETB low, this forces the Laser into a continuous transmit mode and applies dc-balanced data (equal number of ones and zeros) to the Txdat input of the ACS9010 device.

As Rtset is reduced in value, the current to the Laser will increase. The current to the Laser should be monitored at the TxMN in accordance with section headed, *TxMN and TxFLAG*.

The Laser current will be stable when the Laser starts to lase, and produces enough optical power for the PIN feedback current to equal the current flowing through Rtset.

The Rtset impedance should be decreased until the desired Laser output high-power is achieved. Once the setup procedure has been completed, the SETB

pin should then be set high to return the device to the operation mode. The preset Laser power will then be maintained over the recommended temperature and voltage range.

Receive Monitor

The ACS9010 incorporates a power meter which generates a current source which is proportional to the received optical current.

$$I^{*}_{RxMN} = 6 * I_{(PIN)}$$

* Tolerance = +/- 20%.
I = Amps
I_{RxMN} flows through a resistor, internal to the ACS9010, connected between RxMN and GND. The internal resistor has a value of 260KΩ +/- 20 %.

RxMN is compared with 1.25V. If RxMN exceeds 1.25V, then output RxFLG is set = 1, otherwise RxFLG is set = 0. With the internal resistor of 260KΩ, the default threshold for the RxFLG is a input current of 800nA +/- 25%. By adding an external parallel resistor between RxMN and GND, this threshold may be increased.

The voltage on RxMN will modulate with receive data bursts. It will settle to its correct value within 4us following the start of a receive burst, and will collapse to 0V after a burst ends.

Transmission Clock TCLK

There are four independent transmit clocks on the ACS406CS; TCLK1,TCLK2,TCLK3 and TCLK4. For the purpose of this specification, these signals will be referred to collectively as TCLK.

The ACS406CS gives a choice between internally and externally generated transmit clocks. When the CKC pin is held Low, the set of TCLK clocks are configured as outputs producing a clock at the frequency defined by DR(5:1).

When the CKC pin is held High, the set of TCLK clocks are configured as inputs, and will accept an externally produced transmission clock with a tolerance of up to 250ppm with respect to the transmission rate determined by DR(5:1).

The data appearing on TPOS/TNEG is valid on the rising or falling edge of the TCLK clock dependent on the setting of TRSEL *(see Figure 1. Timing diagrams)*. This is the case for both internally and externally generated transmission clocks.

Receive Clock RCLK

There are four independent receive clocks on the ACS406CS; RCLK1, RCLK2, RCLK3 and RCLK4. For the purpose of this specification, these signals will be referred to collectively as RCLK.

The data appearing on RPOS/RNEG is valid on the rising or falling edge of the RCLK clock dependent on the setting of RESEL *(see Figure 1. Timing diagrams)*. To ensure that the average receive frequency is the same as the transmitted frequency, RCLK is generated from a Digital Phase-Lock Loop (DPLL) system (except where master mode has been selected). The DPLL makes periodic corrections to the output RCLK clock by subtracting or adding a single crystal clock bit-period, so that the average frequency of the RCLK clock tracks the average frequency of the transmit clock of the far-end modem (or system master clock). This decompression/de-jittering function is covered in more detail in section headed, *Jitter Characteristics.*

Data Coding

The main synchronous channels may use any of the following coding methods; NRZ, AMI, HDB3, B8ZS. The desired mode is selected by POL1 and POL2 input pins, as shown in Table 2.

Data Coding	POL2	POL1
AMI	0	0
HDB3	0	1
B8ZS	1	0
NRZ	1	1

Table 2

For Non-Return-to-Zero (NRZ) coding, data is applied directly to TPOS inputs, and output data appears only on the RPOS output pins (except for 8-channel mode, see section headed, *Multi-Channel Operation).* When using NRZ code, unconnected TNEG input pins will automatically pull-up to VD+. In addition, the ACS406CS will assert a continuous Low on redundant RNEG output pins.

AMI, B8ZS and HDB3 coding is normally bipolar. However, it is possible to interface with the ACS406CS using two inputs and outputs rather than a single bipolar interface. Data equivalent to positive excursions of the bipolar AMI/B8ZS/HDB3 signal are applied as a logic High to TPOS, while data equivalent to negative excursions are applied as a logic High to TNEG. Similarly, AMI/B8ZS/HDB3 positive excursions will appear as a logic High on RPOS and negative excursions will appear as a logic High on RNEG.

It is anticipated that most users of the ACS406CS will interface directly with a E1/T1 framers. All the popular framers provide POS/NEG bipolar interfaces which will directly connect to the ACS4060.

If required, a detailed description of the AMI/HDB3 coding rules are available from Acapella.

Data Rate Selection

For the purpose of this specification TPN1 represents the set of signals TPOS1 and TNEG1, and RPN1 represents the set of signals RPOS1 and RNEG1. See section headed, *Data Coding* for a description of the coding types.

The maximum recommended crystal (XTAL) is 33.792MHz, this gives a maximum bandwidth of 8.448MHz (E2). This bandwidth can be utilised in various ways, it may be divided up over 1,2,4 or 8 channels. It is also possible to support 1,2 or 4 independent clocks. Single clock operation is known as TX1 mode and dual clock as TX2 and four independent clocks is known as TX4 mode. There is a fourth mode of operation known as HT mode (High Tolerance), which is more fully described later. For the purpose of this specification these transmission modes are known collectively as the Tmodes.

The data rate selection pins DR(5:1) determine the frequency of the TCLK clock, the number of channels and the transmission mode (TMode) in accordance with the Table 3.

DR Pins 5	4	3	2	1	TCLK freq	Nos. of channels	Tmode
1	1	1	1	1	XTAL/4	1	Tx1
1	1	1	1	0	XTAL/5	1	Tx1
1	1	1	0	1	XTAL/16	2	Tx2
1	1	1	0	0	XTAL/20	2	Tx2
1	1	0	1	1	XTAL/16	1	HT
1	1	0	1	0	XTAL/20	1	HT
1	1	0	0	1	XTAL/16	4	Tx1
1	1	0	0	0	XTAL/20	4	Tx1
1	0	1	1	1	XTAL/32	4	Tx2
1	0	1	1	0	XTAL/64	4	Tx2
1	0	1	0	1	XTAL/32	8	Tx1
1	0	1	0	0	XTAL/64	8	Tx2
1	0	0	1	1	XTAL/128	8	Tx2
1	0	0	1	0	XTAL/256	8	Tx2
1	0	0	0	1	XTAL/8	1	Tx1*
1	0	0	0	0	XTAL/10	1	Tx1*
0	1	1	1	1	XTAL/16	4	Tx4
0	1	1	1	0	XTAL/20	4	Tx4

* 50 Km modes

Table 3

Asymmetrical Data Rates

It is possible to configure the DR pins setting on each side of the link differently (with input Fhold) as long as identical crystal values are observed on the communicating devices. For example, the near-end ACS406CS may be configured to transmit 8 channels at 1Mbps and the far-end modem may be configured to transmit 1 channel at 8Mbps. For asymmetrical communication, set fhold = 0, this will lead to the receive circuitry reading the DR pins settings from the far-end ACS406CS rather than locally. It is important that the receive circuitry is aware of the configuration and formatting of the data so that it can correctly interpret it. Prior to lock (when DCD = 0), the receive circuitry will default to the local DR pin settings.

For symmetrical communication (with input Fhold = 1), DR pins setting sent over the link are ignored and the receive circuitry will always read the locally set DR pin values.

It is expected that for the vast majority of applications symmetrical communication will be employed. When asymmetrical mode is selected (Fhold = 0), the only valid DM settings are the Full Duplex modes. The other modes of Remote-Loop-back, Local-Loop-back, master and slave (as described in the sections headed *Configuration modes & Diagnostic modes)* are not available.

Multi-Channel Operation

There are four choices for multi-channel operation on the ACS406CS, selected by the DR(5:1) pins, namely, 1, 2, 4 or 8 channel operation.

1-Channel Operation

In 1-channel operation TPOS1/TNEG1 and RPOS1/RNEG1 is the only active channel. Data appearing on other TPN inputs is ignored. All other RPN outputs are forced to the zero state.

2-Channel Operation

In 2-channel operation channel mappings can be seen in Table 4. Data appearing on all other TPN inputs is ignored. All other RPN outputs are forced to the zero state.

Channel Nos.	Input	Output
1	TPOS1/TNEG1	RPOS1/RNEG1
2	TPOS2/TNEG2	RPOS2/RNEG2

Table 4

4-Channel Operation

In 4-channel operation the mappings can be seen in Table 5.

Channel Nos.	Input	Output
1	TPOS1/TNEG1	RPOS1/RNEG1
2	TPOS2/TNEG2	RPOS2/RNEG2
3	TPOS3/TNEG3	RPOS3/RNEG3
4	TPOS4/TNEG4	RPOS4/RNEG4

Table 5

8-Channel Operation

If one of the 8-channel modes is selected by the DR(5:1) inputs, then the ACS406CS must be configured to expect Non-Return-to-Zero (NRZ) transmission data using the POL1/2 settings. The otherwise redundant TNEG and RNEG pins are then available to carry 4 additional data channels. The mapping of transmission pins for 8-channel NRZ operation can be seen in Table 6.

Channel Nos.	Input	Output
1	TPOS1	RPOS1
2	TNEG1	RNEG1
3	TPOS2	RPOS2
4	TNEG2	RNEG2
5	TPOS3	RPOS3
6	TNEG3	RNEG3
7	TPOS4	RPOS4
8	TNEG4	RNEG4

Table 6

Transmission Modes (TMode)

There are three transmission modes available on the ACS406CS selected by the DR(5:1) pins, these are TX1, TX2, TX4 and HT modes.

TX1 mode

In TX1 mode all of the data channels (TPN/RPN) are related to the clocks TCLK1/RCLK1.

TX2 mode

In TX2 mode there are two system clocks, half the signals are aligned to the clock TCLK1/RCLK1 and the remaining half are aligned to the clock TCLK2/ RCLK2.

For dual channel operation, channel 1 is aligned to clock TCLK1/RCLK1 and channel 2 is aligned to clock TCLK2/RCLK2.

For four channel operation, channels 1-2 are aligned to clock TCLK1/RCLK1 and channels 3-4 are aligned to clock TCLK2/RCLK2.

For eight channel operation, channels 1-4 are aligned to clock TCLK1/RCLK1 and channels 5-8 are aligned to clock TCLK2/RCLK2.

TX4 mode

In TX4 mode there are four system clocks. TX4 mode operates only in conjunction with 4 channel operation. Channel 1 is aligned to TCLK1/RCLK1, channel 2 with TCLK2/RCLK2, channel 3 with TCLK3/RCLK3 and channel 4 with TCLK4/RCLK4.

HT mode

Acapella recognises that a large number of designers using the ACS406CS modem will be employing the device for single channel T1 or single channel E1 operation. In such cases, the available bandwidth far exceeds the bandwidth required. To exploit this otherwise redundant bandwidth, the ACS406CS incorporates a High Tolerant (HT) transmission mode. In HT mode, by virtue of on-chip error-correction, the device is extremely tolerant to data errors.

All modes in the ACS406CS generate regular unique Synchronisation Words (SWs) in order to re-enforce 8B10B word boundary synchronisation. This prevents single bit-errors causing an avalanche of errors due to word boundary slippage, often referred to as "error extension". In HT mode, SWs are interleaved with the data-words such that alternate words are SWs, ensuring that the effect of 8B10B word boundary errors will not propagate beyond one received data word.

In HT mode the single data channel is aligned to the TCLK1/RCLK1 clock.

50km long haul mode

Some customers will require a modem capable of supporting a longer distance than the standard 25km. To support this Acapella have implemented a 50km mode for a single E1 or T1 channel. This is achieved with an XTAL of value half of that used for the standard E1 or T1 for 25km modes in combination with the appropriate configuration of the DR(5:1) pins.

NOTE: The designer should be aware that the use of lower value crystal will proportionally increase the end-to-end data delay through the system in accordance with the formula found in section headed, *Data Delay (Latency).* Therefore, for the 50km mode the latency will double compared to the standard 25km modes.

Example Data Rate Selection

A set of example configurations follow:

E2 Selection

In order to select one E2 operation then set DR5 = DR4 = DR3 = DR2 = DR1 = 1, together with a crystal of 33.792MHz as shown in the Table 7.

DR5	DR4	DR3	DR2	DR1	XTAL Divide	TCLK (MHz)
1	1	1	1	1	4	8.448

crystal = 33.792 MHz — Table 7

T2 Selection

In order to select one T2 channel then set DR5 = DR4 = DR3 = DR2 = 1; DR1 = 0, together with a crystal of 31.560MHz as shown in the Table 8.

DR5	DR4	DR3	DR2	DR1	XTAL Divide	TCLK (MHz)
1	1	1	1	0	5	6.312

crystal = 31.560 MHz — Table 8

2 * E1 Channel Selection

In order to select two independent E1 channels in TX2 mode then set DR5 = DR4 = DR3 = DR1 = 1; DR2 = 0, together with a crystal of 32.768MHz as shown in the Table 9.

DR5	DR4	DR3	DR2	DR1	XTAL Divide	TCLK (MHz)
1	1	1	0	1	16	2.048

crystal = 32.768 MHz — Table 9

2 * T1 Channel Selection

In order to select two independent E1 channels in TX2 mode then set DR5 = DR4 = DR3 = 1; DR1 = DR2 = 0, together with a crystal of 30.88MHz as shown in the Table 10.

DR5	DR4	DR3	DR2	DR1	XTAL Divide	TCLK (MHz)
1	1	1	0	0	20	1.544

crystal = 30.88 MHz — Table 10

1 * E1 Channel Selection HT mode

In order to select one E1 channel operating in High Tolerance (HT) mode then set DR5 = DR4 = DR2 = DR1 = 1; DR3 = 0, together with a crystal of 32.768MHz as shown in the Table 11.

DR5	DR4	DR3	DR2	DR1	XTAL Divide	TCLK (MHz)
1	1	0	1	1	16	2.048

crystal = 32.768 MHz — Table 11

1 * E1 Channel Selection at 50km

In order to double the available transmission distance from 25km to 50km, the value of the crystal must be reduced by half. For a single E1 channel set DR5 = DR4 = DR3 = DR2 = 0; DR1 = 1, together with a crystal of 16.384MHz as shown in Table 12.

DR5	DR4	DR3	DR2	DR1	XTAL Divide	TCLK (MHz)
1	0	0	0	1	8	2.048

crystal = 16.384 MHz — Table 12

1 * T1 Channel Selection in HT mode

In order to set the device for one T1 channels operating in High Tolerance Mode (HT) then DR5 = DR4 = DR2 = 1; DR3 = DR = 0, together with a crystal of 30.88MHz as shown in the Table 13.

DR5	DR4	DR3	DR2	DR1	XTAL Divide	TCLK (MHz)
1	1	0	1	0	20	1.544

crystal = 30.88 MHz — Table 13

1 * T1 Channel Selection at 50km

In order to double the available transmission distance from 25km to 50km, the value of the crystal must be reduced by half. For a single T1 channel then set DR5 = 1; DR4 = DR3 = DR2 = DR1 = 0, together with a crystal of 15.44MHz as shown in Table 14.

DR5	DR4	DR3	DR2	DR1	XTAL Divide	TCLK (MHz)
1	0	0	0	0	20	1.544

crystal = 15.44 MHz — Table 14

4 * E1 Channel Selection in TX1 mode

In order to set the device for four E1 channels with a common TCLK clock then set DR5 = DR4 = DR1 = 1; DR3 = DR2 = 0, together with a crystal of 32.768MHz as shown in the Table 15.

DR5	DR4	DR3	DR2	DR1	XTAL Divide	TCLK (MHz)
1	1	0	0	1	16	2.048

crystal = 32.768 MHz **Table 15**

4 * T1 Channel Selection in TX1 mode

In order to set the device for four T1 channels with a common TCLK clock then set DR5 = DR4 = 1; DR3 = DR2 = DR1 = 0; together with a crystal of 30.88MHz as shown in the Table 16.

DR5	DR4	DR3	DR2	DR1	XTAL Divide	TCLK (MHz)
1	1	0	0	0	20	1.544

crystal = 30.88 MHz **Table 16**

4 * E1 Channel Selection in TX4 mode

In order to set the device for four E1 channels with an independent TCLK clock for each channel then set DR4 = DR3 = DR2 = DR1 = 1; DR5 = 0; together with a crystal of 32.786MHz as shown in the Table 17.

DR5	DR4	DR3	DR2	DR1	XTAL Divide	TCLK (MHz)
0	1	1	1	1	16	2.048

crystal = 32.768 MHz **Table 17**

4 * T1 Channel Selection in TX4 mode

In order to set the device for four T1 channels with a an independent TCLK clock for each channel then set DR5 = DR4 = 1; DR3 = DR2 = DR1 = 0; together with a crystal of 30.88MHz as shown in the Table 18.

DR5	DR4	DR3	DR2	DR1	XTAL Divide	TCLK (MHz)
0	1	1	1	0	20	1.544

crystal = 30.88 MHz **Table 18**

Other Transmission Data Rate

Other standard frequencies may be obtained by setting the appropriate DR(5:1) combination with a 32.768MHz crystal as shown in the Table 19.

DR5	DR4	DR3	DR2	DR1	Nos. of Chann.	XTAL Divide	TCLK (KHz)
1	0	1	1	1	4	32	1024
1	0	1	1	0	4	64	512
1	0	1	0	1	8	32	1024
1	0	1	0	0	8	64	512
1	0	0	1	1	8	128	256
1	0	0	1	0	8	256	128

crystal = 32.768 MHz **Table 19**

Asynchronous Communication

In order to propagate asynchronous data through the ACS406CS, the device should be configured with CKC = 0 so that the device produces a TCLK output clock. The TCLK clock asynchronously over-samples the data applied to TPOS at the rate defined by DR(5:1). The choice of TCLK frequency defines the sample rate of the input data and therefore the sampling-jitter appearing at RPOS of the far-end modem.

Example:
8 - asynchronous 115kbps channels.

XTAL	=	32.768MHz
DR5/4/3/2/1	=	1/0/1/0/1
CKC	=	0
TCLK clock	=	1.024MHz
TPOS/TNEG data rate	=	115kbps
Over-sample factor	=	8.9
Sampling Jitter (approx.')	=	11%.

Similar considerations apply to the maintenance channel, which may also be used to convey asynchronous data.

Support channels

There are up to four support channels on the ACS406CS: TmD1/RmD1, TmD2/RmD2 TmD3/ RmD3 and TmD4/RmD4. For the purpose of this specification these will be referred to collectively as TmD and RmD.

The number of support channels and the bandwidth available is dependent on the setting of the DR(5:1) input pins.

The support channels can be used in one of two ways selected by the input Frame. When Frame = 1, then the support channels are said to be in Frame Mode. When Frame = 0, then the support channels are in maintenance mode.

Maintenance channel mode with Frame = 0

When Frame = 0 then maintenance mode is selected.

One maintenance channel TmD1/RmD1 is available when TX1, TX2 and HT transmission modes are selected. Four maintenance channels TmD(4:1)/ RmD(4:1) are available when the TX4 transmission mode is selected.

In maintenance mode there is only one valid clock TmCLK/RmCLK. The set of four signals TmD(4:1) are collectively synchronised to the TmCLK clock and the set of signals RmD(4:1) are collectively synchronised with the RmCLK clock.

Input data appearing on the TmD inputs is latched into the device on either the rising or falling edge of the TmCLK clock depending on the setting of TRSEL. This data appears at the RmD outputs of the far-end modem on the rising or falling edge of the RmCLK clock depending on the setting of RESEL (*see Figure 1. Timing diagrams*). To ensure that the average receive frequency is the same as the transmitted frequency, RmCLK is generated from a Digital Phase-Lock Loop (DPLL) system.

The ACS406CS gives a choice between internally and externally generated TmCLK clocks. When the CKM pin is held Low, TmCLK is configured as an output producing a clock at 16, 32 or 64kHz. When the CKM pin is held High, TmCLK is configured as an input, and will accept an externally produced transmission clock at the data rate determined by DR(5:1).

Whilst the TmD/RmD maintenance channels have a fixed phase relationship with each other, they do not have a fixed phase relationship with the main TPOS/ TNEG data transmission channels.

DR5	DR4	DR3	DR2	DR1	XTAL (MHz)	XTAL DC	TmCLK (KHz)	Nos. of Channels
1	1	1	1	1	33.792	528	64	1*
1	1	1	1	0	31.560	493.125	64	1*
1	1	1	0	1	32.768	512	64	1*
1	1	1	0	0	30.88	482.5	64	1*
1	1	0	1	1	32.768	512	64	1*
1	1	0	1	0	30.88	482.5	64	1*
1	1	0	0	1	32.768	512	64	1*
1	1	0	0	0	30.88	482.5	64	1*
1	0	1	1	1	32.768	512	64	1*
1	0	1	1	0	32.768	512	64	1*
1	0	1	0	1	32.768	512	64	1*
1	0	1	0	0	32.768	512	64	1*
1	0	0	1	1	32.768	512	64	1*
1	0	0	1	0	32.768	512	64	1*
1	0	0	0	1	16.384	512	32	1*
1	0	0	0	0	15.440	482.5	32	1*
0	1	1	1	1	32.768	512	64	1*
0	1	1	1	0	30.88	482.5	64	1*

*For M4B = 1. For M4B = 0, 4 channels @ 1/4 TmCLK

Table 20

Each DR(5:1) mode is designed to achieve a particular communication frequency by the combination of the XTAL value and Divide Constant (DC) value. The recommended XTAL and the DC value for each DR(5:1) selection are shown in Table 20.

If the recommended XTALs are not employed, then the frequency of the TmCLK clock can be calculated by dividing the XTAL frequency by the DC value.

Frame channel mode with Frame = 1

Frame mode is selected when the input Frame = 1. In Frame mode the channels TmD/RmD become support channels to the main TPOS/TNEG data channels and are associated with the TCLK and RCLK clock rather than the TmCLK and RmCLK clocks employed in maintenance mode.

Frame mode is only available for a subset of the possible DR(5:1) settings; these are shown in Table 21. Where Table 21 denotes the number of Frame channels available as zero, then the status of the Frame input pin will be ignored and the support channels will function in maintenance mode.

DR5	DR4	DR3	DR2	DR1	XTAL (MHz)	TmD/TCLK transitions per period	Nos. of Frame Mode channels available
1	1	1	1	1	33.792	2/512	1
1	1	1	1	0	31.560	2/512	1
1	1	1	0	1	32.768	2/128	2
1	1	1	0	0	30.88	2/128	2
1	1	0	1	1	32.768	2/128	1
1	1	0	1	0	30.88	2/128	1
1	1	0	0	1	32.768	0	0
1	1	0	0	0	30.88	0	0
1	0	1	1	1	32.768	0	0
1	0	1	1	0	32.768	0	0
1	0	1	0	1	32.768	0	0
1	0	1	0	0	32.768	0	0
1	0	0	1	1	32.768	0	0
1	0	0	1	0	32.768	0	0
1	0	0	0	1	16.384	2/512	1
1	0	0	0	0	15.440	2/512	1
0	1	1	1	1	32.768	0	0
0	1	1	1	0	30.88	0	0

Table 21

Data appearing on inputs TmD1/2 is latched into the device on either the rising or falling edge of the TCLK depending on the setting of TRSEL for both internally and externally generated transmission clocks.

Output data appearing on RmD1/2 is valid on the rising or falling edge of the RCLK clock depending on the setting of RESEL *(see Figure 1. Timing diagrams)*.

For 1-channel operation in either TX1 or HT mode then TmD1/RmD1 will be available for transmission but data appearing on TmD2 will be ignored.

For 2-channel operation in TX2 mode then both TmD1/RmD1 and TmD2/RmD2 are available for transmission. TmD1 is associated with channel 1 and is clocked by TCLK1/RCLK1. TmD2 is associated with channel 2 and is clocked by TCLK2/RCLK2.

For TX4 mode and all other data formats, Frame mode is currently unavailable.

Although, the data applied to the TmD1/2 is clocked by TCLK with the same resolution as TCLK the number of transitions allowed on these inputs is restricted according to the rules below.

TX1 mode

A maximum of 2 transitions are permitted on TmD1 for each 512 TCLK1 clock period. If two transitions occur sequentially (on two successive TCLK cycles) then this may be counted as one transition.

TX2 mode

A maximum of 2 transitions may occur on both TmD1/2 for each 128 TCLK1/2 clock period. If two transitions occur sequentially (on two successive TCLK1/2 cycles) then this may be counted as one transition.

HT mode

A maximum of 2 transitions may occur on TmD1 for each 128 TCLK1 clock period. If two transitions occur sequentially (on two successive TCLK1 cycles) then this may be counted as one transition.

In frame mode, TPOS/TNEG and the associated TmD data are transmitted over the link in phase and will appear in phase at the RPOS/RNEG and RmD outputs at the far-end ACS406CS.

A typical application of frame mode follows:

In an E1 frame, only 30 of the available 32 symbols are available for data transmission, the remaining two symbols are deployed for frame synchronisation and signalling. In a proprietary system, it is possible to use the TmD1/2 support channels to mark the first bit or first word of each frame, thus freeing up extra bandwidth in the main data channel.

4 Support channel mode, M4B=0

The ACS406CS has provision for 1 or 4 maintenance channel mode. This is controlled by the signal M4B. When M4B =1, then the number of maintenance channels is set at 1 with a 32/64kHz TmCLK clock per channel, determined by DR(5:1). When M4B = 0, then the number of maintenance channels is increased to 4 with a reduced 8/16kHz TmCLK clock per channel, determined by DR(5:1). This mode is only available for Maintenance channel mode, Frame = 0.

Configuration Modes

The ACS406CS has six Configuration Modes controlled by CM(3:1) as shown in Table 22. It can be seen that the CM(3:1) settings also control the lock mode (*See section headed Lock Modes).*

Configuration Mode	Lock	CM3	CM2	CM1
Full-duplex	Drift	0	0	0
Full-duplex	Memory	0	0	1
Full-duplex	Random	0	1	1
Full-duplex slave	Active	1	0	1
Full-duplex master	Drift	1	1	0
Full-duplex	Active	1	1	1

Table 22

Full-Duplex

In the full-duplex configuration, the RCLK clock of both devices track the average frequency of the corresponding TCLK clock of the opposite end of the link. The receiving Digital-Phase-Lock Loop (DPLL) system makes periodic adjustments to the RCLK clock to ensure that the average frequency is exactly the same as the far-end TCLK clock. In summary, each TCLK is an independent master clock and each RCLK a slave of the far-end TCLK clock.

The relationship between TmCLK and RmCLK are treated similarly.

Full-Duplex Slave

In slave mode, the TCLK and RCLK clock is derived from the TCLK clock of the far-end modem, such that their average frequencies are identical. Clearly, it is essential that only one modem within a communicating pair is configured in slave mode. The CKC pin should be forced to GND, so that TCLK is always configured as an output. Since only one device in the modem pair may be configured in slave mode, the mode also selects active lock. See section headed, *Locking Modes*.

The relationship between TmCLK and RmCLK are treated similarly. The CKM pin should be forced to GND, so that TmCLK is always configured as an output.

Full-Duplex Master

In master mode, the local RCLK clock is internally generated from the local TCLK clock. The local TCLK clock may be internally or externally generated. Master mode is only valid if the far-end device is configured in slave mode or if the far-end TCLK clock is derived from the far-end RCLK clock. Only one modem within a communicating pair may be configured as a master.

The relationship between TmCLK and RmCLK are treated similarly.

Locking Modes

Drift Lock

Communicating modems attain a stable state when the “transmit window” of one modem coincides with the “receive window” of the other, allowing for delay through the optical link. Adjustments to machine cycles are made automatically during operation, to compensate for differences in XTAL frequencies which would otherwise cause loss of synchronisation.

When both modems are configured in drift lock, synchronisation described above depends on a difference in the XTAL or system clock frequencies at each end of the link, and the greater the difference the faster the locking. Therefore, if the difference between XTAL frequencies is very small (a few ppm), automatic locking may take tens of seconds or even minutes. For this reason, normally only one modem in the communication pair will be configured in drift lock mode.

Drift lock will not succeed if the two modems are driven by an external XTAL clock derived from a single source (i.e. tolerance of 0 ppm).

Active Lock Mode

Active lock mode may be used to accelerate synchronisation of a pair of communicating modems so that they achieve lock in less than 1 second. Active lock reduces the machine cycle of the device by 0.5 % ensuring that the receive window moves swiftly through the transmit window of the opposing modem. To effect active lock, one modem should be permanently configured in drift lock and the other in active lock. If this is not possible because the system mandates that all modems are peers (configured identically), then the same effect may be realised by temporarily invoking lock for a short time after power-up. This is achieved as follows: connect pins CM(3:1) together attaching the node to an RC arrangement, with the capacitor to VDD and the resistor to GND, to create a 5V to 0V ramp on power-up. The RC time-constant should be Ca. 5 seconds.

Active lock will succeed even when communicating devices are driven from clocks derived from a single source (0ppm).

Random Lock

This mode achieves moderate locking times (typically 2 seconds, worst case 3 seconds) with the advantage that the ACS406CS's are configured as peers. Communicating modems may be permanently configured in this mode (i.e. with hard-wired pins).

Random lock will succeed even when communicating devices are driven from clocks derived from a single source (0ppm). Random lock mode is compatible with drift lock and active lock.

Memory Lock

Following the assertion of a reset (PORB = 0) communicating devices will initiate an arbitration process where within 2 seconds (typically) the communicating modems will achieve synchronisation, one establishing itself as an active-lock modem and the other establishing itself as a drift-lock modem. On subsequent attempts to lock, synchronisation will be achieved within 1 second. It is only necessary to apply PORB to one device in the communicating pair to initiate an arbitration process.

Since memory lock status (Active or Drift) uses on-chip storage, loss of power to the IC will require a new reset (PORB = 0). Furthermore, should there be a need to synchronise with a third modem, a new reset will be required.

Mixing Lock Modes

It is possible to mix all combinations of locking modes once the modems are locked, however, prior to synchronisation two modems configured in active lock will not operate. The effect of mixing locking modes on locking speed can be seen in Table 23.

Device A Mode	Device B Mode	Locking Speed
Drift	Drift	Drift
Drift	Active	Active
Drift	Random	Random
Drift	Memory	Random
Active	Active	Not allowed
Active	Random	Random
Active	Memory	Random
Random	Random	Random
Random	Memory	Random
Memory	Memory	Active*

* Memory lock has random lock speed for the first synchronisation (arbitration).

Table 23

Diagnostic Modes

The ACS406CS offers independent diagnostic control of the data channels. The two diagnostic modes are described below; Local Loopback and Remote Loopback.

Local Loopback

In local loopback mode, TPN and TmD data is looped back inside the near-end modem and is output at its own RPN and RmD outputs.

Data received from the far-end device is ignored, except to maintain lock. If concurrent requests occur

for local and remote loopback, local loopback is selected.

The local loopback diagnostic mode is used to test data flow up to, and back from, the local ACS406CS and does not test the integrity of the link itself. Therefore, local loopback operates independently of synchronisation with a second modem (i.e. DCD may be High or Low).

Remote Loopback

In remote loopback mode, the near-end modem sends a request to the far-end modem to loopback its received data, thus returning the data so that it appears at the RPN and RmD of the initiating modem.

Both modems are exercised completely, as well as the Lasers/LEDs and the fiber optic link. The remote loopback test is normally used to check the integrity of the entire link from the near-end (initiating modem).

Whilst a device is responding to a request for remote loopback from the far-end, requests from the near-end to initiate remote loopback will be ignored.

Initiating Loopbacks

The data channels associated with each clock domain can be independently controlled on the ACS406CS in accordance with Table 24.

DM2C*X*	DM1C*X*	Diagnostic mode
0	0	Full Duplex
0	1	Full Duplex
1	0	Local Loopback
1	1	Remote Loopback

Where X in DM2CX and DM1CX both = 1,2,3 or 4.

Table 24

Therefore:

TCLK1/RCLK1 is controlled by DM2C1/DM1C1;

TCLK2/RCLK2 is controlled by DM2C2/DM1C2;

TCLK3/RCLK3 is controlled by DM2C3/DM1C3;

TCLK4/RCLK4 is controlled by DM2C4/DM1C4.

TX4 mode

In TX4 mode there are 4 clock domains each controlled by a pair of signals DM2CX / DM1CX, where X = the channels number = 1,2,3,4.

TX2 mode

In TX2 mode there are 2 clock domains those data signals associated with TCLK1/RCLK1 are controlled by DM2C1/DM1C1, and those data signals associated with TCLK2/RCLK2 are controlled by DM2C2/DM1C2.

TX1 and HT mode

In TX1 and HT mode there is only one clock domain , so all the data signals are associated with DM2C1/ DM1C1.

ERRC and ERRL - Error Detection

These signals can be used to give an indication of the quality of the optical link. Even when a DC signal is applied to the data, maintenance and TCLK inputs, the ACS406CS modem transmits approximately 11Mbps over the link in each direction. This control data is used to maintain the timing and the relative positioning of transmit and receive windows.

The transmit and control data is constantly monitored to make sure it is compatible with the 8B10B format. If a coding error is detected ERRL will go High and will remain High until reset. ERRL may be reset by asserting PORB, or by removing the fiber optic cable from one side of the link thereby forcing the device temporarily out of lock.

ERRC produces a pulse on detection of each coding error. These pulses may be accumulated by means of an external electronic counter.

Please note that ERRL and ERRC detect coding errors and not data errors, nevertheless because of the complexity of the coding rules employed on the ACS406CS, the absence of detected errors on these pins will give a good indication of a high quality link.

Laser/LED Considerations

Since LEDs or Lasers from different suppliers may emit different wavelengths, it is recommended that the Lasers/LEDs in a communicating pair of modems are obtained from the same supplier. Acapella will assist with contact names and addresses on request.

Power Supply Decoupling

The ACS9010 contains a highly sensitive amplifier, capable of responding to extremely low current levels. To exploit this sensitivity it is important to reduce external noise to a low level compared to the input signal from the Laser/LED. The modem should have an independent power trace to the point where power enters the board.

Figure 4, shows the recommended power supply decoupling. The Laser/LED should be sited very close to the PMN, PINP, PINN, LAN and LAP pins. A generous ground plane should be provided, especially surrounding the sensitive PINP and PINN tracks from the ACS9010 pins to the optical

component. The modem should be protected from EMI/RFI sources in the standard ways.

Link Budgets

The link budget is the difference between the power coupled to the fiber via the transmit Laser/LED and the power required to realise the minimum input-amplifier current via the receive PIN/LED. The link budget is normally specified in dB, and represents the maximum attenuation allowed between communicating Lasers/LEDs. The budget is utilised in terms of the cable length, cable connectors and splices. It usually includes an operating margin to allow for degradation in LASER/LED performance. The power coupled to the cable is a function of the efficiency of the Laser/LED, the current applied to the Laser/LED and the type of the fiber optic cable employed.

Digital Mode

The ACS4060 may be used as a controller and data compression/decompression engine, which allows the device to be used with in external circuitry for non-fiber applications. Check with Acapella for details.

LOSS (Loss Of Synchronisation)

There are two conditions that will make LOSS go to logic 1:

i) Loss of synchronisation - ping-pong windows incorrectly aligned i.e DCD = 0.

ii) 64 received symbols break the 8B10B encoding rules in a sequence of 256 symbols.

In order to return LOSS to the logic state 0 the following criteria must be met.

i) The devices must be synchronised - ping-pong windows correctly aligned i.e DCD = 1.

ii) There are no received symbols in a sequence of 256 symbols which break the 8B10B coding rules.

Data Delay (Latency)

Although the ACS406CS is a full-duplex modem, at the fiber level the device operates in a half-duplex manner. Typically, half-duplex systems allow bidirectional transmission by alternating the direction of data flow. This means that data must be stored until the link is configured in the appropriate direction. Storage inevitably leads to delay or latency. Acapella has designed the ACS406CS to minimise latency by very rapidly switching direction at the fiber level, minimising the need to store data.

The latency through the system applies to the main data TPOS/TNEG channels and the support channels TmD/RmD and is a function of the XTAL frequency.

For a given implementation, the latency has three components:

1) A Constant Delay (CD) set by the machine cycle and system clock at a frequency of 32.768MHz then CD = 0.7ms.

2) A Transmission Rate Delay (TRD) which is equal to 125 bit periods worst case (de-jittering buffer and internal registers).

3) Fiber length Dependent Delay (FDD) which is equal to 2 * (fiber delay).

The Latency formula is:

Latency =
$(0.7 * 10^{-3} * 32.768 * 10^{-6}/XTAL) + (125 * \text{transmit bit period}) + (2 * \text{fiber delay})$
where the fiber delay is typically 5us per km.

Example Latency calculation

Latency calculation:

Fiber length = 10km (~ 50us)
XTAL = 33.792MHz
DR mode = 4 * 2.048Mbps (transmit bit period = 488ns)

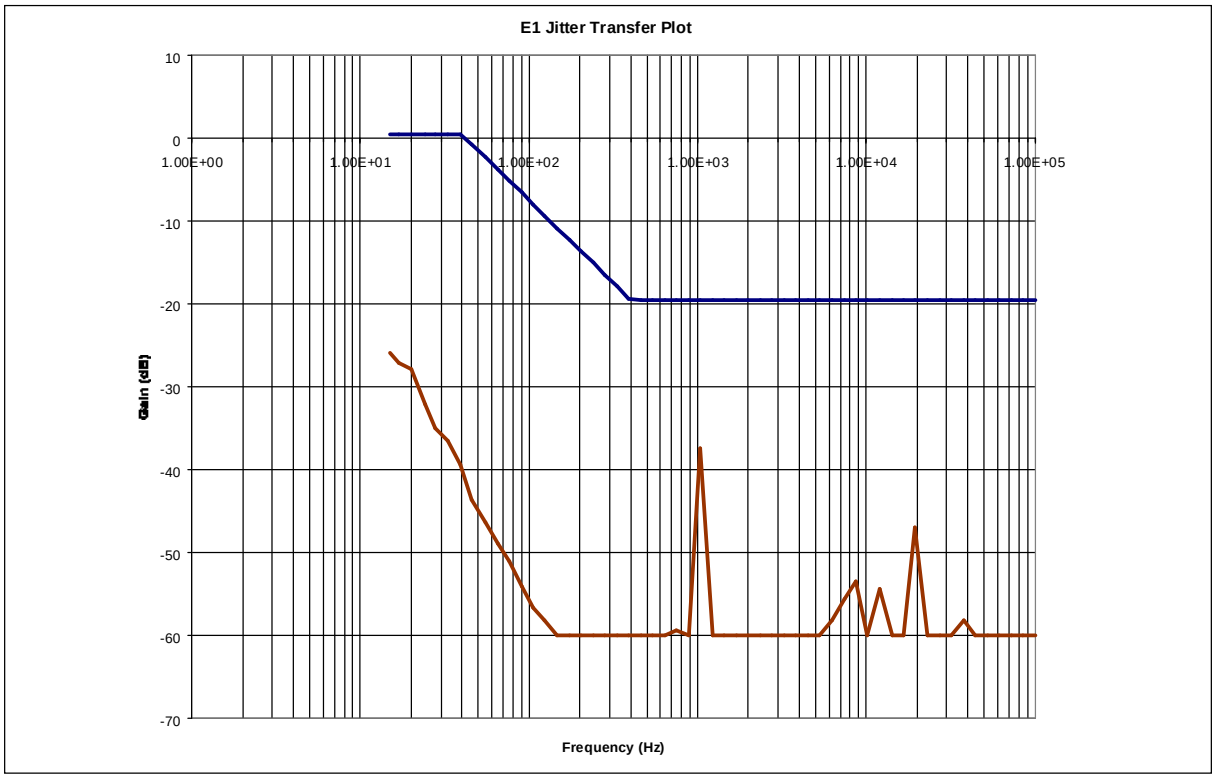
Latency = $((0.7 * 10^{-3} * 32.768 * 10^{-6}/33.792 * 10^{-6}) + (125 * 488 * 10^{-9}) + (2 * 50 * 10^{-6})) = 0.84ms$

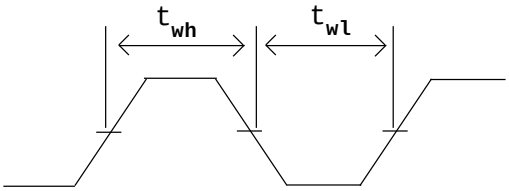
Jitter Characteristics

The transmit path contains a Transmit FIFO, which acts to attenuate high frequency input jitter components of the order 1kHz or greater.
The receive path contains a Digital Phase Locked Loop (D_PLL), which controls the output frequency of the receive clock in order to track the transmit clock frequency at the far end modem. The D_PLL also acts to:-

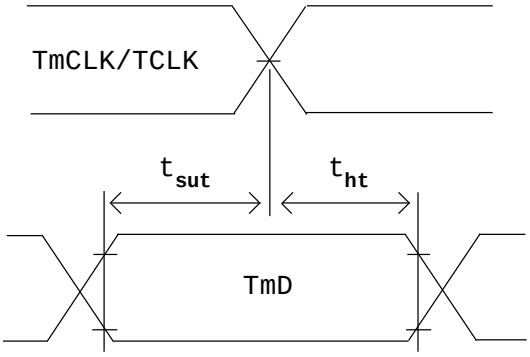
1) maintain the fill level in the receive FIFO, to ensure that the data latency stays within the specified limits.
2) ensure that Jitter Tolerance and Jitter Attenuation is within ITU G.823 and AT&T 62411 specifications.
3) accommodate any clock drift that may be present.

The performance boundary of the D_PLL is ±500 ppm. The ±500 ppm performance limit includes jitter attenuation and drift accommodation.
The oscillator controlled by the Digital Phase Locked Loop operates in steps of 8ppm, and therefore has a resolution down to +/- 4ppm. Due to the discrete nature of the frequency changes, the period of the receive clock can change by +/- one system clock cycle. In the absence of input jitter, output jitter generation for E1 remote loopback configuration is measured at 0.40UIpp over frequency range 20Hz to 100kHz, and 0.08UIpp over frequency range 18kHz to 100kHz.
The E1 Jitter Transfer plot is shown below, measured worst case, Remote Loopback.



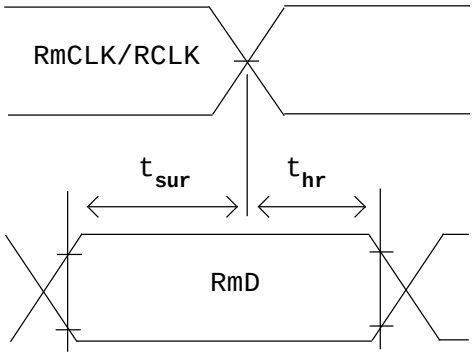


TmCLK and RmCLK clock pulse widths



Transmit set-up and hold times

The active TmCLK edge is defined by input TRSEL.



Receive set-up and hold times

The active RmCLK edge is defined by input RESEL.

Figure 1. Timing diagrams

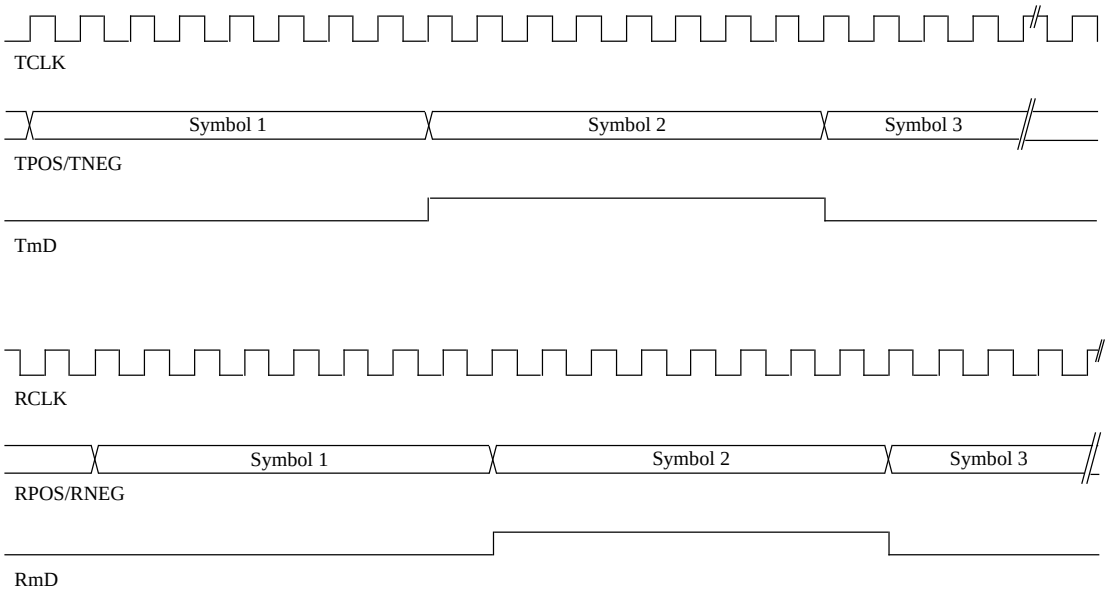
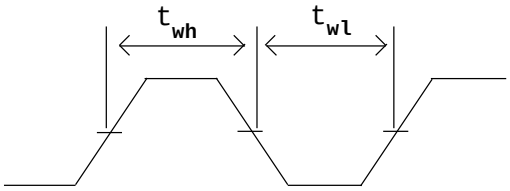
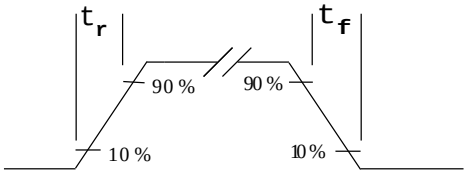


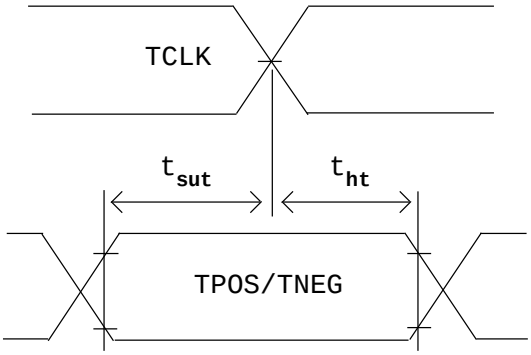
Figure 2. Use of support signals to identify symbols in E1/E2 frame



TCLK and RCLK clock pulse widths

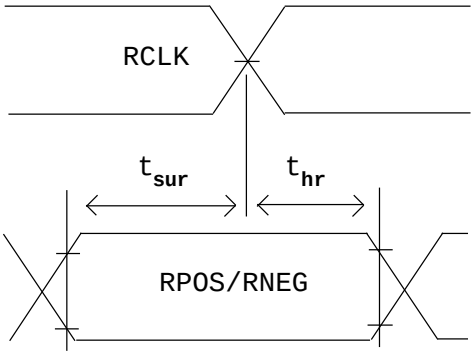


Digital outputs rise and fall times



Transmit set-up and hold times

The active TCLK edge is defined by input TRSEL.



Receive set-up and hold times

The active RCLK edge is defined by input RESEL.

Figure 3. Timing diagrams

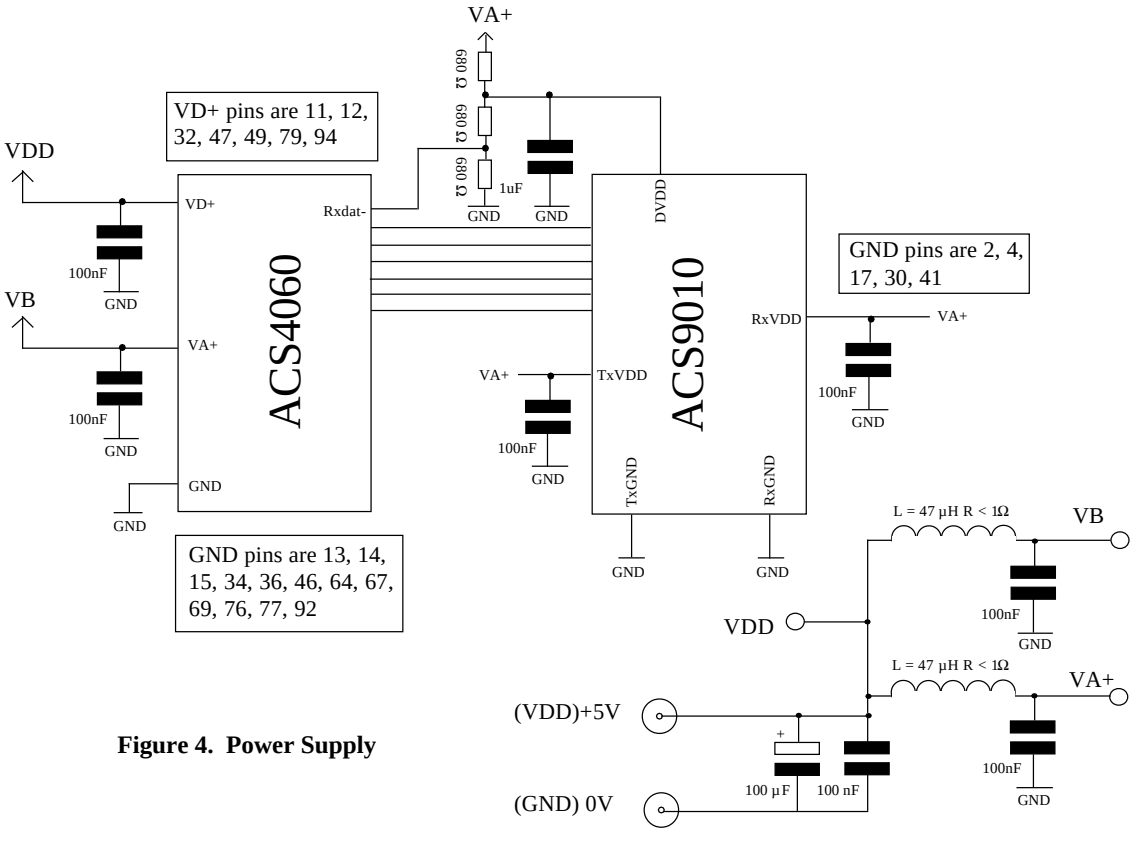
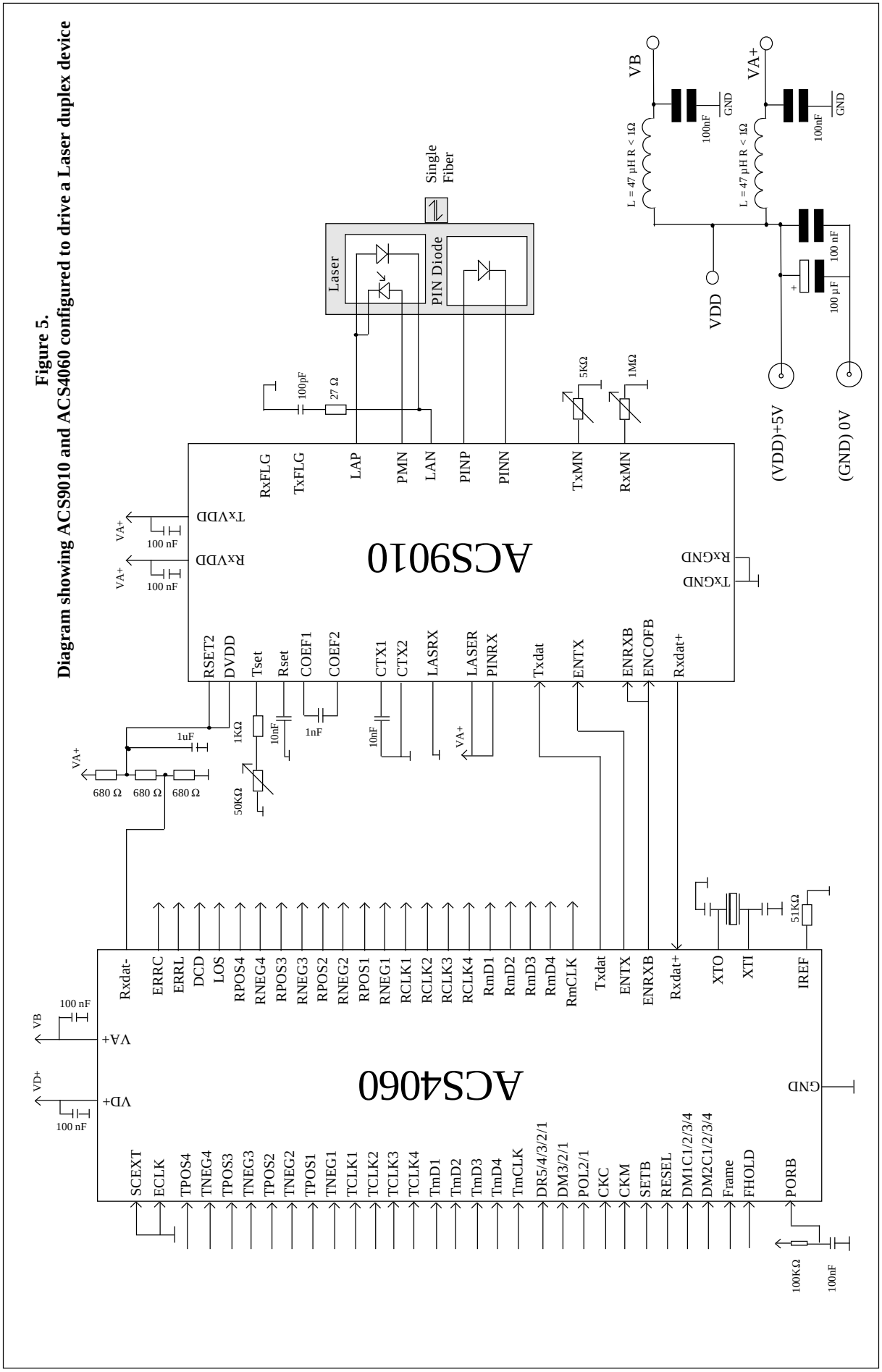


Figure 4. Power Supply

Figure 5.
Diagram showing ACS9010 and ACS4060 configured to drive a Laser duplex device



Single Fiber LED link

Link Budget Example (Rtset set so LED launch current = 100 mA peak)

Fiber type **Fiber size**	**Plastic** **1000 micron**	**Glass** **62.5micron**	**Glass** **50 micron**
Minimum transmit couple power to fiber (µW)	1000	100	50
Minimum LED responsivity (A/W)	0.01	0.1	0.12
Minimum ACS406CS sensitivity (nA)	1500	1500	1500
Minimum input power to ACS406CS amplifier (µW)	100	15	12.5
Link budget (dB)	10	8.24	6.0

Single Fiber LASER link

Link Budget Example (Rtset set so LASER launch current = 25 mA peak)

Fiber type **Fiber size**	**Glass (single mode)** **9 micron**
Minimum transmit couple power to fiber (µW)	1000
Minimum LASER & PIN responsivity (A/W)	0.25
Minimum ACS406CS sensitivity (nA)	1000
Minimum input power to ACS406CS amplifier (µW)	4
Link budget (dB) (single mode fiber attenuation = 0.3 dB/km)	24

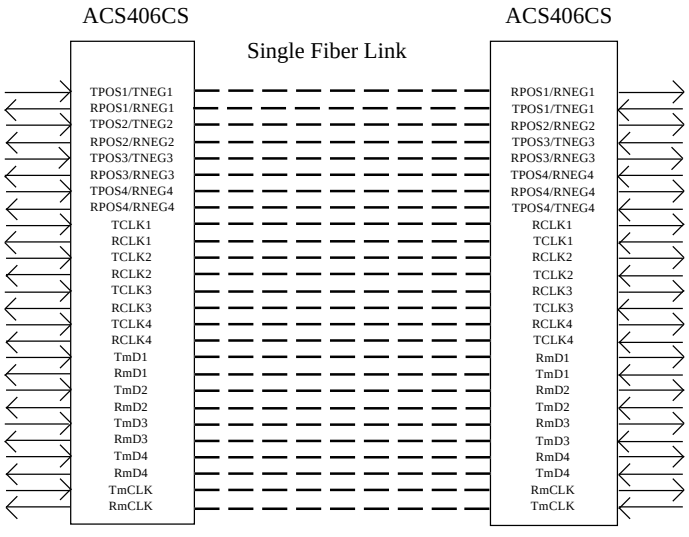


Figure 8. Shows the relationship between data channels

Pin Description ACS4060 part 1

Pin	Sym	IO	Name	Description
11,12 32,47 49,79 94	VD+	-	+ve power supply	Power supply, 4.75 - 5.25 Volts.
61	VA+	-	+ve power supply	Power supply for Clock Recovery PLL, 4.75 - 5.25 Volts.
13,14 15,34 36,46 64,67 69,76 77,92	GND	-	Ground	Power Supply
24 26 29 31	TPOS1 TPOS2 TPOS3 TPOS4	I	Transmit Data Pos	Transmit channel 1, corresponds to +ve in bipolar signal. Transmit channel 2, corresponds to +ve in bipolar signal. Transmit channel 3, corresponds to +ve in bipolar signal. Transmit channel 4, corresponds to +ve in bipolar signal.
22 25 27 30	TNEG1 TNEG2 TNEG3 TNEG4	I	Transmit Data Neg	Transmit channel 1, corresponds to -ve in bipolar signal. Transmit channel 2, corresponds to -ve in bipolar signal. Transmit channel 3, corresponds to -ve in bipolar signal. Transmit channel 4, corresponds to -ve in bipolar signal.
2 5 7 10	RPOS1 RPOS2 RPOS3 RPOS4	O	Receive Data Pos	Receive channel 1, corresponds to +ve in bipolar signal. Receive channel 2, corresponds to +ve in bipolar signal. Receive channel 3, corresponds to +ve in bipolar signal. Receive channel 4, corresponds to +ve in bipolar signal.
1 4 6 9	RNEG1 RNEG2 RNEG3 RNEG4	O	Receive Data Neg	Receive channel 1, corresponds to -ve in bipolar signal. Receive channel 2, corresponds to -ve in bipolar signal. Receive channel 3, corresponds to -ve in bipolar signal. Receive channel 4, corresponds to -ve in bipolar signal.
60 59	XTI/ XTO	-	System Clock Crystal	Connect fundamental parallel resonance crystal with appropriate padding capacitor to GND
80	DCD	O	Data Carrier Detect	When DCD = 1, then the communicating modems have synchronized, and are communicating.
82	PORB	I	Power On Reset	Will initialise the device when PORB= 0. PORB is normally connected to an RC circuit so that a POR is automatically invoked on power-up. PORB= 1 for normal operation.

Pin Description ACS4060 part 2

Pin	Sym	IO	Name	Description
16	TmCLK	I/O	Transmit maintenance CLK	Transmit maintenance Clock. samples TmD on falling edge when device is not in valid frame mode. See input 'FRAME'
19 17 18 23	TCLK1 TCLK2 TCLK3 TCLK4	I/O	Transmit clocks	Transmit Clock 1/2/3/4, samples TPOS/TNEG data on clock edge selected by input TRSEL.
95	RmCLK	O	Receive Clock (support channel)	Support channel receive clock With frame = '0' then nominal frequency = 64KHz
97 96 98 93	RCLK1 RCLK2 RCLK3 RCLK4	O	Receive clocks	Receive Clock, RPOS/RNEG data is valid on edge selected by input "RESEL".
50	RESEL	I	Receive Edge Select	When RESEL = 1, RPOS/RNEG and RmD data is valid on the rising edge of RCLK/RmCLK. When RESEL = 0, the data is valid on the falling edge of RCLK/RmCLK.
58	TRSEL	I	Transmit Edge Select	When TRSEL = 1, TPOS/TNEG and TmD data is latched on the falling edge of TCLK/TmCLK. When TRSEL = 0, the data is latched on the rising edge of TCLK/TmCLK.
20 21 28 33	TmD1 TmD2 TmD3 TmD4	I	Transmit maintenance Data	NRZ maintenance channel. TmD is sampled on the TmCLK clock edge defined by TRSEL (when the device is not in FRAME mode).
100 99 8 3	RmD1 RmD2 RmD3 RmD4	O	Receive maintenance Data	NRZ maintenance channel. Data is set-up with repect to RCLK clock when FRAME mode is valid else data is set-up with respect to RmCLK. Data is valid on the clock edge selected by RESEL.
42	M4B	I	Maintenance 4 channel mode	When M4B = 1, the number of maintenance channels is 1 When M4B = 0, the number of maintenance channels increases to 4, where the bandwidth of each channel is reduced by a factor of 4. See Table 20

Pin Description ACS4060 part 3

Pin	Sym	IO	Name	Description
57 56 55	CM1 CM2 CM3	I	Configuration Modes	CM1,CM2,CM3 select the Configuration Modes such as full duplex, master and slave mode.
85	ERRL	O	Error Latch	If errors are detected in the 8B10B coding rules ERRL will be forced high.. ERRL will be reset low if the device is forced out of synchronisation e.g. PORB = 0.
86	ERRC	O	Error count	ERRC will go high coincident with each error detected in the 8B10B coding rules. Errors may be accumulated by means of an external electronic counter.
91 90 89 87 88	DR1 DR2 DR3 DR4 DR5	I	Data Rate Select	The DR(5:1) input select the Data Rates and number of channels. See section headed *Data Rate Selection*.
44	CKC	I	Clock Select	When CKC = 0, TCLK1/2/3/4 is configured as an output. When CKC = 1, TCLK1/2/3/4 is configured as an input.
45	CKM	I	Clock Select	When CKM = 0, TmCLK1/2/3/4 is configured as an output. When CKM = 1, TmCLK1/2/3/4 is configured as an input
52	SETB	I	LASER set-up	SETB = 0, to adjust the LASER output power. SETB = 1, in operational mode.
81	LOSS	O	LOSS of Signal	When LOSS = 1, receive data is unreliable. When LOSS = 0, receive data is reliable.
54	Frame	I	Frame Mode	When Frame = '1' , Support channels are configured in frame mode.
51	Fhold	I	Format Hold	When Fhold = '0', the device is configured for asymmetrical data communication.The most common setting for this input is Fhold = '1' supporting symmetrical communications.

Pin Description ACS4060 part 4

Pin	Sym	IO	Name	Description
75 74	POL1 POL2	I	Polarity	Defines the polarity of input signal TPOS/TNEG. NRZ,HDB3, B8SZ or AMI.
71	SCEXT	I	Select Clock External	When SCEXT = '1' , then the system clock will be the external clock applied to input 'ECLK'. When SCEXT = '0' , then the system clock will be the crystal clock generated at XTI/XTO.
37	ECLK	I	External Clock	External system clock input. Only valid when SCEXT = '1'. Clock must have at least 40% High and 40% Low time.
63	IREF	I	Current reference	A 51KΩ 1% resistor should be placed between IREF and GND.
66	Rxdat-	I	Rxdat -ve input	This determines the slicing level for input Rxdat+. Should be set at DVDD/2. On the next generation of devices this is likely to be derived from the ACS9010 device . Backward compatibilty will be maintained.
38 43	DM1C1 DM2C1	I	Diag. mode 1 CLK1 Diag. mode 2 CLK1	Diagnostic mode selection pin for data channels associated with TxCLK1.
48 53	DM1C2 DM2C2	I	Diag. mode 1 CLK2 Diag. mode 2 CLK2	Diagnostic mode selection pin for data channels associated with TxCLK2.
83 78	DM1C3 DM2C3	I	Diag. mode 1 CLK3 Diag. mode 2 CLK3	Diagnostic mode selection pin for data channels associated with TxCLK3.
73 68	DM1C4 DM2C4	I	Diag. mode 1 CLK4 Diag. mode 2 CLK4	Diagnostic mode selection pin for data channels associated with TxCLK4.

Pin Description ACS9010 part 1

Pin	Sym	IO	Name	Description
3	RSET2	-	PLL frequency set	Tie to DVDD at all times.
6	LASER	I	LASER	LASER = 1, when interfacing to a LASER. LASER = 0, when interfacing to a LED.
7	RSET	-	Receive Bias Set	Internally sets the bias current for the analogue cells. Connect a 10nF capacitor between RSET and GND.
8	LASRX	I	LAP/LAN Receive	When LASRX = 1, LAP and LAN are connected to the receiver. Required for LED ping-pong applications.
13	PINRX	I	PINP/PINN Receive	When PINRX = 1, PINP and PINN are connected to the receiver.
14	RxFLG	O	Receive Power Flag	When RxFLG = 1, receiver power > RxMN threshold. When RxFLG = 0, receive power < RxMN threshold.
15	RxMN	O	Receive Monitor	Receive power monitor.
16	RxVDD	-	Receive Power Supply	Power supply, 4.75 - 5.25 Volts.
17	RxGND	-	Ground	Power supply.
18 19	COEF1 COEF2	-	Compensation Capacitor	Differential offset compensation capacitor. Connect a 1nF capacitor between pins 18,19.
24 25	PINP PINN	-	PIN Anode PIN Cathode	Connections for pin-diode receiver.
26	PMN	-	LASER mon-pin	Connection to Anode of LASER monitor-pin.
27	TxVDD	-	Transmit Power Supply	Power supply, 4.75 - 5.25 Volts.
28 29	LAP LAN	-	LASER Anode LASER Cathode	Connections to LASER OR LED.
30	TxGND	-	Ground	Power supply.
2 4 41	GND	-	Ground	Power supply.
31 35	CTX1 CTX2	-	Driver Smoothing Capacitor	<u>When using LEDs:</u> Place a 10 nF capacitor between CTX1 and GND. Place a 10 nF capacitor between CTX2 and GND. <u>When using LASERs:</u> Place a 10 nF capacitor between CTX1 and GND. Connect CTX2 directly to GND.

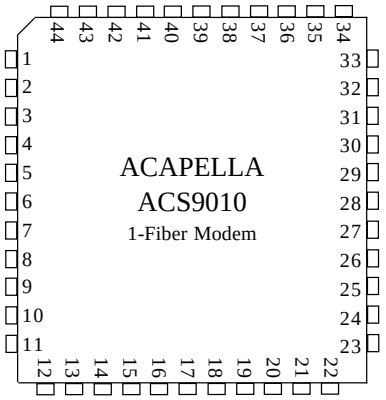
Pin Description ACS9010 part 2

Pin	Sym	IO	Name	Description
36	TxMN	-	Transmit Power Monitor	Monitors transmit output power.
37	TxFLG	O	Transmit Power Flag	When TxFLG = 1, transmit power > TxMN threshold. When TxFLG = 0, transmit power < TxMN threshold.
38	TSET	-	Transmit Power Setting	A 40KΩ resistor placed between TSET and GND will set the appropriate transmit power level.
42	DVDD	-	Rxdat Slicing level voltage	Provides the appropriate slicing level for Rxdat+. Use resistor arrangement seen in *fig 5* of this specification.

PIN Description of interface signals between ACS9010 and ACS4060.

Pin	Sym	IO	Name	Description
40 39	ENTX	O I	Enable Transmit	Transmit window active (ACS4060). Enable transmit (ACS9010).
39 9	ENRXB	O I	Enable Receive	Receive Window active (ACS4060). Enable receive (ACS9010).
20	ENCOFB	I	Enables DC Offset Compensation	Enables the DC offset compensation - ENCOFB is normally connected to ENRXB (ACS9010).
35 40	Txdat	O I	Transmit Burst Data.	Transmit burst data out (ACS4060). Transmit burst data in (ACS9010).
5 65	Rxdat+	O I	Receive Burst Data	Positive Differential receive burst data out (ACS9010). Positive Differential receive burst data in (ACS4060).

1	IC	IC	44
2	GND	RES	43
3	RSET2	DVDD	42
4	GND	GND	41
5	Rxdat+	Txdat	40
6	LASER	ENTX	39
7	RSET	TSET	38
8	LASRX	TxFLG	37
9	ENRXB	TxMN	36
10	RES	CTX2	35
11	RES	RES	34
12	RES	RES	33
13	PINRX	RES	32
14	RxFLG	CTX1	31
15	RxMN	TxGND	30
16	RxVDD	LAN	29
17	RxGND	LAP	28
18	COEF1	TxVDD	27
19	COEF2	PMN	26
20	ENCOFB	PINN	25
21	RES	PINP	24
22	RES	RES	23



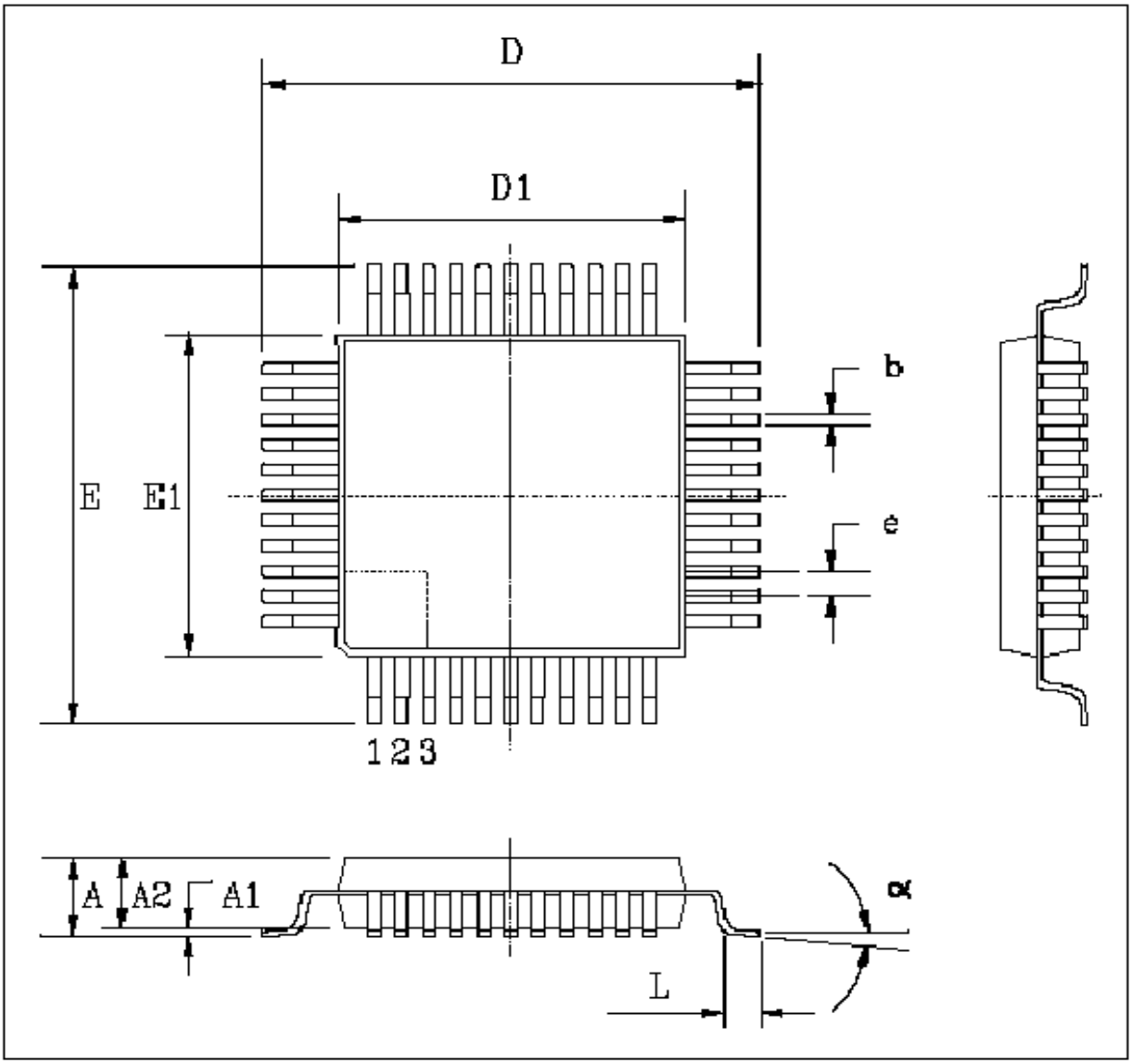
RES = Reserved, IC = Internally Connected

Figure 6. Top view of 44 pin TQFP package

1	RNEG1	RmD1	100
2	RPOS1	RmD2	99
3	RmD3	RCLK3	98
4	RNEG2	RCLK1	97
5	RPOS2	RCLK2	96
6	RNEG3	RmCLK	95
7	RPOS3	VD+	94
8	RmD4	RCLK4	93
9	RNEG4	GND	92
10	RPOS4	DR1	91
11	VD+	DR2	90
12	VD+	DR3	89
13	GND	DR5	88
14	GND	DR4	87
15	GND	ERRC	86
16	TmCLK	ERRL	85
17	TCLK2	IC	84
18	TCLK3	DM1C3	83
19	TCLK1	PORB	82
20	TmD1	LOSS	81
21	TmD2	DCD	80
22	TNEG1	VD+	79
23	TCLK4	DM2C3	78
24	TPOS1	GND	77
25	TNEG2	GND	76
26	TPOS2	POL1	75
27	TNEG3	POL2	74
28	TmD3	DM1C4	73
29	TPOS3	IC	72
30	TNEG4	SCEXT	71
31	TPOS4	IC	70
32	VD+	GND	69
33	TmD4	DM2C4	68
34	GND	GND	67
35	Txdat	Rxdat-	66
36	GND	Rxdat+	65
37	ECLK	GND	64
38	DM1C1	IREF	63
39	ENRXB	RES	62
40	ENTX	VA+	61
41	IC	XIN	60
42	M4B	XOUT	59
43	DM2C1	TRSEL	58
44	CKC	CM1	57
45	CKM	CM2	56
46	GND	CM3	55
47	VD+	FRAME	54
48	DM1C2	DM2C2	53
49	VD+	SETB	52
50	RESEL	FHOLD	51

Figure 7. Top view of 100 pin TQFP package

RES = Reserved, IC = Internally Connected



Thin Quad Flat Pack dimensions in mm	E1/D1	A	A1	A2	e	b	L	α	E/D	Copl.
	min		0.05	1.35		0.30	0.45	0°		
TQFP44	10.00				0.80				12.00	
	max	1.60	0.15	1.45		0.45	0.75	7°		0.10
	min		0.05	1.35		0.17	0.45	0°		
TQFP100	14.00				0.50				16.00	
	max	1.60	0.15	1.45		0.27	0.75	7°		0.10

Package information for the TQFP 44 and 100 pin packages

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Power supply VD+, VA+, RxVDD, TxVDD	VDD	-0.3	6.0	V
Input Voltage (non-supply pins)	Vin	GND-0.3	VDD+0.3	V
Input current (except LAN, LAP, PINN, PINP, PMN)	Iin	-	10.0	mA
Input current (LAN, LAP, PINN, PINP, PMN)	Iina	-	1.0	mA
Storage temperature	Tstor	-50	160	°C

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power supply VD+,VA+, TxVDD, RxVDD	VDD	4.75	5	5.25	V
Ambient temperature range	TA	-40	-	85	°C

Static Digital Input Conditions (for specified operating conditions)

For TLL Logic level input pins: TCLK1/2/3/4 (as input), TmCLK (as input), PORB, CKM, CKC, CM1/2/3, POL1/2, SETB, FRAME, FHOLD, SCEXT, ECLK.

Parameter	Symbol	Min	Typ	Max	Units
Vin High	Vih	2.0	-	-	V
Vin Low	Vil	-	-	0.8	V
Input current	Iin	-	-	10	µA

Static Digital Input Conditions (for specified operating conditions)

For input pins: Rxdat+(ACS4060), Rxdat-(ACS4060).

Parameter	Symbol	MIN	Typ	Max	Units
Vin High (Rxdat+) - (Rxdat-)	Vihdif	100	-	200	mV
Vin Low (Rxdat+) - (Rxdat-)	Vildif	-100	-	-200	mV
Input current	Iin	-	-	10	µA

Static Digital Input Conditions (for specified operating conditions)

For TTL logic level input pins with Pull Up: DR1/2/3/4/5, TPOS1/2/3/4, TNEG1/2/3/4, TmD1/2/3/4, DM1C1/2/3/4, DM2C1/2/3/4, TRSEL, RESEL, M4B.

Parameter	Symbol	Min	Typ	Max	Units
Vin High	Vih	2.0	-	-	V
Vin Low	Vil	-	-	0.8	V
Pull-up resistor	PU	18K	-	55K	Ω
Input current	Iin	-	-	277	µA

Static Digital Input Conditions (for specified operating conditions)

For CMOS logic level input pins: ENTX(ACS9010), ENRXB(ACS9010), Txdat(ACS9010), Rxdat+(ACS9010), LASER, LASRX, PINRX, ENCOFB(ACS9010).

Parameter	Symbol	Min	Typ	Max	Units
Vin High	Vih	65%VDD	-	-	V
Vin Low	Vil	-	-	35%VDD	V
Pull-up resistor	PU	75K	125K	175K	Ω
Input current	Iin	-	-	100	µA

Static Digital Output Conditions (for specified operating conditions)

For CMOS output pins: RPOS1/2/3/4, RNEG1/2/3/4, RCLK1/2/3/4, RmCLK, RmD1/2/3/4, DCD, ERRL, ERRC, LOS, ENRXB (ACS4060), ENTX(ACS4060), Txdat(ACS4060), RxFLG(ACS9010), Rxdat+(ACS9010), TxFLG(ACS9010), TCLK1/2/3/4 (as output), TmCLK (as output).

Parameter	Symbol	Min	Typ	Max	Units
Vout Low Iol = 4mA	Voh	0	-	0.5	V
Vout High Ioh = 4mA	Vol	VDD-0.5	-	VDD	V
Max load capacitance	Cl	-	-	50	pF

Dynamic Characteristics (for specified operating conditions)

Parameter	Symbol	Min	Typ	Max	Units
Crystal frequency XTI/XTO	XTAL	16	32.768	35	MHz
External System CLK (ECLK) High or Low time	fclp	40	-	60	%
TPOS/TNEG data rate	fclf	0	-	XTA-L/4	bps
RCLK and TCLK duty cycle (with TCLK= output)	twh twl	40	50	60	%
Frequency deviation at TCLK from selected value (with TCLK = input)	Fd	-250	-	+250	ppm
TPOS/TNEG to TCLK set-up time	tsut	20	-	-	ns
TPOS/TNEG to TCLK hold time	tht	10	-	-	ns
RPOS/RNEG to RCLK set-up time	tsur	0.4*1/R-CLK	0.5*1/R-CLK	0.6*1/R-CLK	ns
RPOS/RNEG to RCLK hold time	thr	0.4*1/R-CLK	0.5*1/R-CLK	0.6*1/R-CLK	ns
RmCLK and TmCLK duty cycle (with TmCLK= output)	twh twl	30	50	70	%
When frame = '0'; TmD1/2/3/4 data rate When frame = '1' ; special data transmission rules apply (see support channels).	fclmf	0	-	64K	bps
Frequency deviation at TmCLK from selected value (with TmCLK = input)	Fd	-400	-	+400	ppm
TmD1/2/3/4 to TmCLK set-up time	tsut	20	-	-	ns
TmD1/2/3/4 to TmCLK hold time	tht	10	-	-	ns
RmD1/2/3/4 to RmCLK set-up time	tsur	0.4*1/R-mCLK	0.5*1/R-mCLK	0.6*1/R-mCLK	ns
RmD1/2/3/4 to RmCLK hold time	thr	0.4*1/R-mCLK	0.5*1/R-mCLK	0.6*1/R-mCLK	ns
Digital output - fall time 50pF load	tf			10	ns
Digital output - rise time 50pF load	tr			10	ns
Power consumption with LASER/LED = 50 mA in operational mode. ACS9010 ACS4060	PC	- -	- -	150 125	mW

Matching Characteristics (for specified operating conditions)

Parameter	Symbol	Min	Typ	Max	Units
Crystal tolerance using fundamenal parallel resonance crystals	Ct	-50	-	+50	ppm
Minimum amplifier input current LED: LASER:	Irec	-	-	 1500 1000	nA
Maximum amplifier input current (see Acapella if this is restrictive)	Irmax	400	-	-	µA
Rtset placed between TSET and GND	Rtset	1K	-	40K	Ω
Maximum Monitor PIN current	Ipin	2.0			mA
LASER Current (LASER = 1) TxMN = 0.5mA Rtset < 40KΩ	Ilaser	45	50	55	mA
LASER Current limit (LASER = 1)	Ilaser	100	-	-	mA
LED Current (LASER = 0) Rtset = 1KΩ Rtset = 40KΩ	Iled	 75 2.0	 100 2.5	 125 3.0	mA
LED as receiver (ping-pong) reverse bias	vr	-	-	1.4	V
LED as receiver (ping-pong) capacitance (vr = 0)	Cled	-	-	50	pF
LED as receiver (ping-pong) leakage (vr = 1.4)	Cleak	-	-	150	nA
PIN Diode receiver reverse bias	Vrb	-	-	4	V
PIN Diode leakage current Vrb = 4.0V	Pleak	-	-	100	nA
DVDD Input Voltage	DVDDV	3.0	3.3	3.6	V
DVDD input current	DVDDI	-	-	500	µA
IREF resistor	RIFREF	49.5	51	51.5	KΩ

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