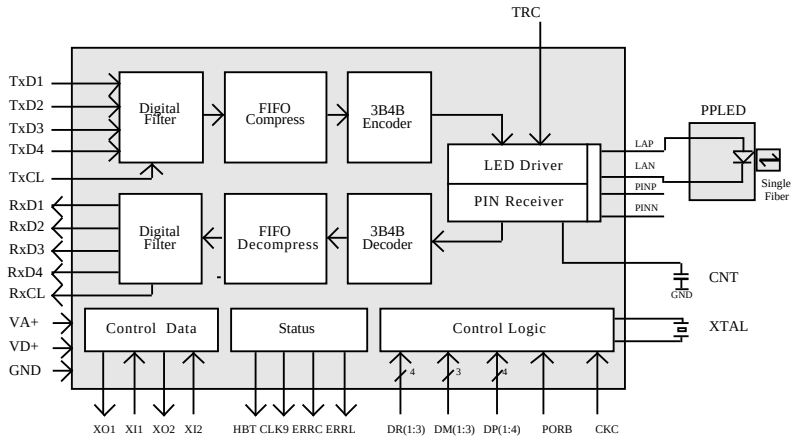
400 SERIES

Acapella Optical Modem IC

ACS401 Main Features:

* Enables up to four full-duplex serial transmission channels through a single fiber optic cable, providing eight virtual fiber paths.
* Two additional low speed handshake signals.
* Supports Ping Pong LED (PPLED) and LASER Duplex Devices (LDD) for single fiber applications or dual fiber applications using low cost LED/LASER emitters and PIN Diode receiver.
* Link lengths up to 95 km with appropriate Laser.
* Maximum data rate 128 kbps - optimised for talk-set applications.
* Typical 7 mA (average) current consumption, including LASER drive current.
* Digital mode, allowing the user to add an external amplifier. Also enables the ACS401 to be used in non-fiber applications.
* Bit Error Rate (BER) of 10^{-9}

Equivalent block diagram of ACS401.



General Description:

The ACS401 is a complete optical-modem controller/driver/receiver IC, supporting various user programmable, full-duplex, synchronous data rates to 128 kbps over a single fiber. Communicating modems automatically maintain synchronisation with each other such that the receive phase of one modem is lined up with the transmit phase of the other, compensating for the propagation delay presented by the link. Link lengths from zero to maximum distance, up to 95 km, are catered for automatically.

Acapella Optical Modem IC ACS401

128 kbps Optical Modem for Long Haul Transmission for Single/Dual Fiber applications

Inter-IC Encoding Technique

The 3B4B encoding method is used for communication between ACS401s, thus ensuring that there is no DC component in the signal. The encoding and decoding is transparent to the user.

Transmitter and Receiver Functions

Signals TxD and RxD in this specification refer to the set of signals TxD(1:4) and RxD(1:4) respectively.

The TxD input data of the transmitting modem is time compressed and encoded in 3B4B format. In the receiving modem, 3B4B encoding ensures easy extraction of the bit-clock. The received data is filtered, decoded, then stored in an output memory. The memory provides time expansion, de-jittering and frequency compensation. The data is finally directed to the RxD output pin.

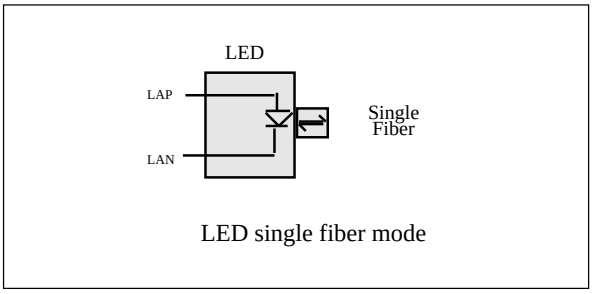
Operational Modes

The ACS401 has four operational modes controlled by DP(1:4). There are modes of operation to support PPLED and LASER duplex devices on single fiber. In addition, LED/PIN and LASER/PIN are supported on dual fiber.

Operational Mode	No. of Fibers	DP4	DP3	DP2	DP1
1. PPLED	Single	1	0	0	1
2. 4-pin Duplex	Single	1	0	0	0
3. LED & PIN	Dual	1	0	0	0
4. LASER & PIN	Dual	1	0	0	0

N.B. All LASERs must be 4-pin LASERS. DP(1:4) combinations not listed above are factory IC test modes, and should not be selected by the user. Damage to the PPLED/Duplex & LED/PIN components may result if these illegal modes are selected.

N.B. for all Operational modes 1, 2, 3, 4 SETB (Pin2) MUST be tied High.



LED single fiber mode

Mode 1 - LED single fiber mode

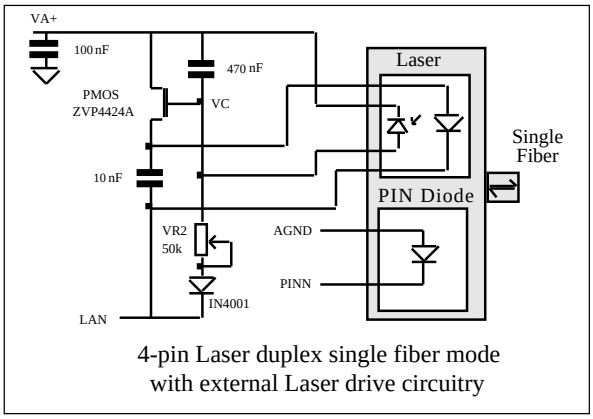
This is the operational mode for single fiber LED transmission, i.e. the LED is a 'ping-pong' type (PPLED) used for both transmit and receive. Connect PINP of ACS401 to GND and leave PINN floating.

Mode 2 4-pin Laser duplex single fiber mode

This is a single fiber mode where the Laser duplex device is employed. This duplex device comprises a 4-pin Laser for transmission and a PIN diode for reception in a single housing. The Duplex devices are driven by the ACS401 in a half-duplex manner, so potential cross-talk between the transmitter and receiver is of no consequence.

It is necessary to use a small number of external components (shown in the diagram) to support the power regulation technique. The method for setting the Laser power is described in section headed *Control of LASER current*.

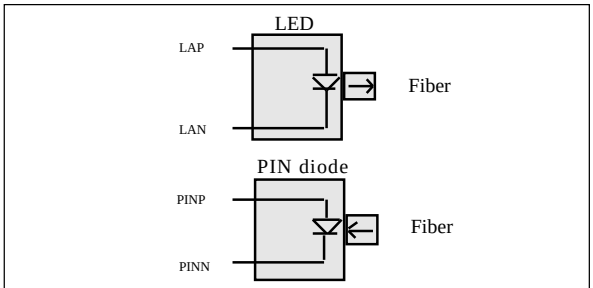
VA+ is the +5V supply used to power the analogue of the ACS401. AGND is analogue ground (pin 49 of the ACS401).The loop is stable when the average current from the monitor pin equals the current through variable resistor VR2. The voltage VC is stable at this point and sets the laser drive current.



4-pin Laser duplex single fiber mode with external Laser drive circuitry

Mode 3 - LED/PIN dual fiber mode

This is a dual fiber mode where the LED is used for transmission and a separate PIN diode is used for reception. This allows the use of low cost standard LEDs.



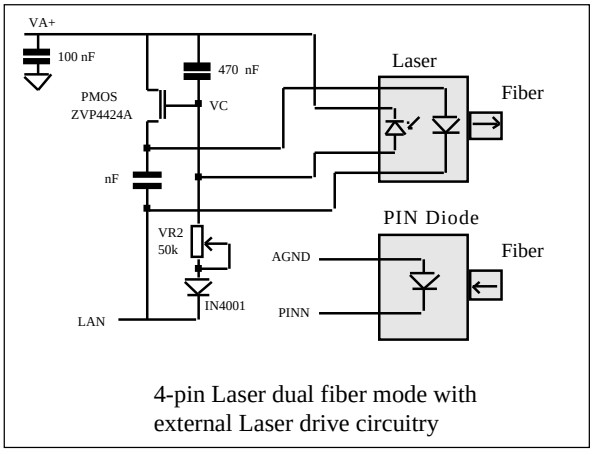
LED/PIN dual fiber mode

Mode 4 4-Pin LASER/PIN dual fiber mode

This is a dual fiber mode where the 4-pin laser is used for transmission and a separate PIN diode is used for reception.

It is necessary to use a small number of external components (shown in the diagram) to support the power regulation technique. The method for setting the Laser power is described in section headed *Control of LASER current*.

VA+ is the +5V supply used to power the analogue of the ACS401. AGND is analogue ground (pin 49 of the ACS401).The loop is stable when the average current from the monitor pin equals the current through variable resistor VR2. The voltage VC is stable at this point and sets the laser drive current.



4-pin Laser dual fiber mode with external Laser drive circuitry

Control of LASER current

The LASER output current must be set for each individual device in accordance with the manufacturer's recommendations. The maximum output current to the Laser is controlled by the resistor Rtrc connected between ground and TRC. The minimum value set on Rtrc to avoid damage to the ACS401 is 800Ω.

LASER(current max) = 100/Rtrc

tolerance +/- 25 %.

Whilst TRC sets the maximum current (to prevent damage to the laser during the adjustment procedure), the actual current to the Laser is determined by the external component VR2. The adjustment procedure is described in the following section.

Adjustment Procedure

Select the appropriate mode using the pins DP(1:4) (see section headed *Operational Modes*). Choose a value for the resistor Rtrc that delivers sufficient current to correctly drive the laser at the desired power, with sufficient power margin to compensate for temperature/voltage changes and potential laser degradation. In many applications the value of Rtrc will be set to the maximum current using a resistor value of 800 Ω.

The output power from the laser may be measured directly using an optical-power meter that is capable of detecting peak optical-power. If an average optical-power meter is employed then a correction factor of 16 must be used to obtain the peak value .

LASER(peak power) = Laser(average power) * 16.

The external component VR2 should have a range of 0 to 50 KΩ. As VR2 is decreased, output power will first be detected when the laser begins to lase. VR2 should be reduced further until the desired output power is achieved (within the limits of the manufacturer's specification).

LED current control

The LED transmit current is less critical though it is important not to exceed the LED manufacturer's recommendation for maximum current. The current is controlled by a resistor Rtrc connected between TRC and ground. The lower the value Rtrc, the greater the current. The lower limit for Rtrc is 800 Ω while a practical maximum is 40 kΩ.

The LED current is inversely proportional to Rtrc while Rtrc > 800Ω:

LED(current) = 100/Rtrc

tolerance +/- 25 %.

PORB

The Power-On Reset or PORB pin resets the device if forced Low for 100 ms or more. In normal operation PORB should be held High. Although the PORB pin has been included, e.g. for factory test, the modem has been designed to power up correctly without the aid of PORB.

PORB has a special function when used in conjunction with memory lock (see section headed *Diagnostic Modes*).

Crystal Clock

Normally, a parallel resonant crystal will be connected between the pins XLI and XLO with the appropriate padding capacitors. Alternatively, it is possible to drive XLI directly by an external clock.

The clock frequency for the purpose of this specification will be known as XTAL frequency. The operational range for XTAL frequency is 1 - 12 MHz, though communicating ACS401s must be clocked at the same nominal frequency. The ACS401 has been designed to operate with a XTAL tolerance of 100 ppm giving a relative tolerance of 200 ppm between communicating modems.

The recommended frequency of 9.216 MHz, results in the standard range of synchronous communication frequencies tabulated in the section headed *Data Rate Selection*. Non-standard frequencies may be generated by using the appropriate value XTALor external clock.

Example: To generate a 38.4 kbps dual channel.

Select a 64 kbps dual channel using the data rate selection pins DR4/3/2/1 = 1/1/0/0, and use a XTAL frequency of:

XTAL = (38.4 / 64) * 9.216 MHz = 5.5296 MHz.

Other 'non-standard' transmission frequencies may be generated in the same way as long as the 1 - 12 MHz XTAL oscillator range is observed. A wider range of external clock frequencies may also be permissible - please check with Acapella.

Cint Capacitor - CNT

For a XTAL frequency range of 5 - 12 MHz the ACS401 requires a ceramic capacitor of value 22 nF - 33 nF +/- 20 % between pin CNT and GND. At frequencies lower than 5 MHz a capacitor of value 68 nF - 100 nF is recommended. It is essential that the CNT capacitor is placed very close to the ACS401.

DCDB

The Data Carrier Detect (DCDB) signal will go Low when the modems are locked and ready for data transmission. Prior to lock (DCDB = High), the data channels outputs RxD(1:4) are forced Low with the control lines XO(1:2) forced High.

Data Rate Selection

The following data rates apply to TxD1, TxD2, TxD3 and TxD4 and are based on the use of a 9.216 MHz XTALor clock.

'Standard' mode, DR4 = 1:

DR4	DR3	DR2	DR1	Data Rate	No. of Channels
1	0	0	0	128 kbps	Single
1	0	0	1	64 kbps	Single
1	0	1	0	32 kbps	Single
1	0	1	1	16 kbps	Single
1	1	0	0	64 kbps	Dual
1	1	0	1	32 kbps	Dual
1	1	1	0	32 kbps	Four
1	1	1	1	16 kbps	Four

'Double'mode, DR4 = 0:

DR4	DR3	DR2	DR1	Data Rate	No. of Channels
0	0	0	1	64 kbps	Single
0	0	1	0	32 kbps	Single
0	0	1	1	16 kbps	Single
0	1	0	1	32 kbps	Dual
0	0	0	0	16 kbps	Dual
0	1	1	1	16 kbps	Four

In 'standard' mode internal timing accommodates fiber length delays of up to 95 km, link budget permitting. In 'double'mode the internal timing accommodates fiber length delays of up to 190 km, link budget permitting. 'Double' mode essentially halves the frequency of the internal clock and therefore doubles the period of the internal machine cycle, this also has the effect of doubling the duration of LED/LASER transmit pulses, which in turn is likely to lead to improved link budgets, particularly where LEDs or LASERs of higher than recommended capacitance are employed.

Bandwidth * Channel Product

The ACS401 has a Bandwidth Channel Product (BCP) of 128 kHz in 'standard' mode and 64 kHz in 'double' mode using the recommended XTAL frequency of 9.216 MHz. The BCP is proportional to the XTAL frequency and is specified as:

BCP(kHz) = 128 * XTAL / (9.216 *10^6 * n)

XTAL = frequency of XTALoscillator. n = 1 for 'standard'mode; n = 2 for 'double' mode.

The given maximum bandwidth may be shared by up to 4 channels as shown in the following tables for both 'standard' and 'double' modes and a XTAL frequency of 9.216 MHz.

'Standard' mode - XTAL = 9.216 MHz

Bandwidth per channel	No of Channels	BCP
32 kHz	4	128 kHz
64 kHz	2	128 kHz
128 kHz	1	128 kHz
16 kHz	4	64 kHz
32 kHz	2	64 kHz
64 kHz	1	64 kHz
32 kHz	1	32 kHz
16 kHz	1	16 kHz

'Double' mode - XTAL= 9.216 MHz

Bandwidth per channel	No of Channels	BCP
16 kHz	4	64 kHz
32 kHz	2	64 kHz
64 kHz	1	64 kHz
16 kHz	2	32 kHz
32 kHz	1	32 kHz
16 kHz	1	16 kHz

Power consumption will be minimised by choosing the lowest BCP.

Control Signals

The control signal set XI(1:2) are oversampled at a rate of:

XTAL / 18,432 (Hz) in 'standard' mode

XTAL / 36,864 (Hz) in 'double' mode

The signals are filtered by a 4-bit filter ensuring that the data applied to these inputs is not easily corrupted. These signals may be used for control data regarded as critical. The sampling frequency and filtering dictates a minimum Low or High time for data applied to inputs XI(1:2) of:

> (18,432 * 4) / XTAL(s) in 'standard' mode

> (36,864 * 4) / XTAL (s) in 'double'mode

Therefore, with the recommended XTAL frequency of 9.216 MHz and 'standard' mode operation, the minimum High or Low time for data applied to XI(1:2) for successful propagation is 8 ms.

The logic status of XI(1:2) is propagated over the link and appears at the far-end at XO(1:2). When the devices are out of lock (DCDB = High), then XO1 = XO2 = High.

Transmission Clock TxCL

The ACS401 gives a choice between internally and externally generated transmission clocks. When the CKC pin is held Low, TxCL is configured as an output producing a clock at the frequency defined by DR(1:4). When the CKC pin is held High, TxCL is configured as an input, and will accept an externally produced transmission clock with a tolerance of up to 500 ppm with respect to the transmission rate determined by DR(1:4). Data is latched into the device on the rising edge of the TxCL clock independent of internal or external TxCL generation.

It is possible to propagate asynchronous data through the link. The TxCL clock will over-sample the data at the rate defined by DR(1-4). The choice of TxCLclock frequency dictates the sample rate of the asynchronous data appearing at the input TxD, and consequently the jitter on the output RxD at the far-end.

Example:

DR4/3/2/1	= 1000
CKC	= 0
Transmission data rate	= 128 kbps
TxD data rate	= 19.2 kbps

With this set-up the over-sample factor is 128 / 19.2 = 6.67, giving an effective jitter of ~15 %.

Receive Clock RxCL

In synchronous mode, data is valid on the rising edge of RxCL clock (see Figure 2. Timing diagrams). To ensure that the average receive frequency is the same as the transmitted frequency, RxCL is generated from a Digital Phase-Lock Loop (DPLL) system (except where master mode has been selected). The DPLLmakes periodic corrections to the output RxCL clock to compensate for differences in the XTAL frequencies. In the case of an externally supplied transmission clock TxCL, compensation is also made for differences in frequency between the supplied data clock and the selected clock rate defined by DR(1:4). The DPLL is adaptive and will minimise the frequency of correction and jitter, where the XTALfrequency and transmission clocks are tightly toleranced.

Diagnostic Modes

The ACS401 has eight diagnostic modes controlled by DM(1:3). These are shown in the following table.

Diagnostic Mode	Lock	DM3	DM2	DM1
Full-duplex	Drift	0	0	0
Full-duplex	Memory	0	0	1
Remote loopback	Active	0	1	0
Full-duplex	Random	0	1	1
Local loopback	Drift	1	0	0
Full-duplex slave	Active	1	0	1
Full-duplex master	Drift	1	1	0
Full-duplex	Active	1	1	1

Full-duplex

In the full-duplex configuration, the RxCL clock of both devices tracks the average frequency of the TxCL clock of the opposite end of the link. The receiving Digital Phase-Lock Loop (DPLL) system makes periodic adjustments to the RxCL clock to ensure that the average frequency is exactly the same as the far-end TxCL clock. In summary, each TxCL is an independent master clock and each RxCL a slave of the far-end TxCL clock.

Full-duplex slave

In slave mode the TxCL and the RxCL clock is derived from the TxCL clock of the far-end of the link, such that the average frequency is exactly the same. Clearly, it is essential that only one modem is configured in slave mode at a time. The CKC pin is overridden such that TxCL is always configured as an output. Since only one device in the modem pair may be configured in slave mode, the mode also selects active lock.

Full-duplex master

In master mode the RxCL clock is internally generated from the local TxCL clock. The local TxCLclock producing the RxCLclock may be internally or externally generated. Master mode is only valid if the far-end device is configured in slave mode or if the far-end TxCLclock is derived from the far-end RxCLclock. Only one modem in the communicating pair may be configured as a master.

Local Loopback

In local loopback mode, TxD data is looped back inside the near-end modem and is output at its own RxD output. The data is also sent to the far-end modem and synchronisation between the modems is maintained.

In local loopback mode data received from the far-end device is ignored, except to maintain lock. If concurrent requests occur for local and remote loopback, local loopback is selected.

The local loop diagnostic mode is used to test data flow up to, and back from, the local ACS401 and does not test the integrity of the link itself. Therefore, local loopback operates independently of synchronisation with a second modem (DCDB may be High or Low).

Remote Loopback

In remote loopback mode, the near-end modem sends a request to the far-end modem to loopback its received data, thus returning the data. The far-end modem also outputs the received data at its RxD. Both modems are exercised completely, as well as the LASERs/LEDs and the fiber optic link. The remote loopback test is normally used to check the integrity of the entire link from the near-end (initiating modem).

Whilst a device is responding to a request for remote loopback from the far-end, requests from the near-end to initiate remote loopbacks will be ignored.

Drift Lock

Communicating modems attain a stable state where the 'transmit' window of one modem coincides with the 'receive' window of the other, allowing for delay through the optical link. Adjustments to machine cycles are made automatically during operation, to compensate for differences in XTAL frequencies which would otherwise cause loss of synchronisation.

Drift lock synchronisation described above, depends on a difference in the XTALfrequencies at each end of the link, and the greater the difference the faster the locking. Therefore, if the difference between XTAL frequencies is very small (a few ppm), automatic locking may take tens of seconds or even minutes.

Drift lock will not operate if the two communicating devices are driven by a clock derived from a single source (i.e. tolerance of 0 ppm).

Active Lock

Active lock mode may be used to accelerate synchronisation of a pair of communicating modems. This mode synchronises the modems with less than 3.0 seconds delay, by adjusting the machine cycles of the modems. Active lock reduces the machine cycle of the device by 0.3 % ensuring rapid lock. After synchronisation the machine cycle reverts automatically to normal.

Note that only one device can be configured in active lock mode at any one time, and thus the DM(1:3) pins must not be permanently wired High on both devices in a production system. Active lock mode is usually invoked temporarily on power-up. This can be achieved on the ACS401 by connecting DM1, DM2 and DM3 together, and attaching that node to an RC arrangement with the capacitor to 5 V and the resistor to GND, to create a 5 V → 0 V ramp on power-up. The RC time constant should be > 5 seconds.

Active lock will succeed even when communicating devices are driven from clocks derived from a single source (i.e. 0 ppm).

Random Lock

This mode achieves moderate locking times (typically 4 seconds, worst case 12 seconds) with the advantage that the ACS401's are configured as peers. Communicating modems may be permanently configured in this mode (i.e. with hard-wired DM(1:3) pins).

Random lock operates even when communicating devices are driven from clocks derived from a single source. Random lock mode is compatible with drift lock and active lock.

Memory Lock

Following the assertion of a reset (PORB = 0) communicating devices will initiate an arbitration process where within 12 seconds the communicating modems will achieve synchronisation. One establishing itself as an active lock modem and the other establishing itself as a drift lock modem. On subsequent attempts to lock, typically where the fiber has been disconnected and a new fiber inserted, synchronisation will be achieved within 3 seconds. It is only necessary to apply PORB to one device in the communicating pair to initiate an arbitration process.

Since memory lock status (active or drift) uses on-chip storage, loss of power to the IC will require a new reset (PORB = 0). Furthermore, should there be a need to synchronise with a third modem, reset will again be required.

Mixing Lock modes

It is possible to mix all combinations of locking modes once the modems are locked, however, prior to synchronisation two modems configured in active lock will not operate. The effect of mixing locking modes on locking speed is tabulated below:

Device A	Device B	Locking Speed
Mode	Mode	
Drift	Drift	Drift
Drift	Active	Active
Drift	Random	Random
Drift	Memory	Random
Active	Active	Not allowed
Active	Random	Random
Active	Memory	Random
Random	Random	Random
Random	Memory	Random
Memory	Memory	Active*

* Memory lock has random lock speed for the first synchronisation

HBT Status pin ('Heartbeat' Indicator LED)

The ACS401 HBTpin affords a method of driving a display LED in a manner which is sympathetic to low power consumption. The HBT pin is pulsed to indicate 'locked'status (DCDB = 0) and 'out of lock' status (DCDB = 1). The frequency of pulses is 16 times greater for 'out of lock' than for 'lock'. The LED 'on' indicates power-up whilst the frequency of pulsing denotes locking status.

Since the display LED is on for at most 6.4 % of the total time, the HBT requires little power which may be further reduced by employing high efficiency LEDs. The formulas below presume 'standard' mode of operation; for 'double' mode the XTAL value should be divided by 2.

Powered-up, but not locked

Frequency (Hz): XTAL / 1.152 * 10^6
Duration (s): 73,728 / XTAL
On time (%): 6.4 % of time.
With 9.216 MHz XTAL and 'standard' mode
Frequency: 8 Hz (approx.)
Duration : 8 ms (approx.)

Powered-up and locked

Frequency (Hz): XTAL/ 18,432
Duration (s): 73,728 / XTAL
On time (%): 0.4 % of time.
With 9.216 MHz XTAL and 'standard' mode
Frequency: 0.5 Hz (approx.)
Duration : 8 ms (approx.)

The HBT pin is active High and can supply up to 16 mA at a voltage of > VDD - 0.5 Volts. The display LED should be placed between the HBTpin and GND with a series resistor. The resistor value is a function of the efficiency of the display LED, and the power budget.

Example: Calculating the HBT resistor value

LED on voltage: 2.0 V
VDD (ACS401): 5.0 V
Resistor voltage: 3.0 V
Current to LED: 2 mA (high efficiency LED)
Resistor value: 3 / 2 * 10-3 = 1500 Ω

Note: The LED referred to in this section is of the inexpensive display type and should not be confused with the LED that interfaces with the fiber optic cable itself.

ERC and ERL (Error Detector)

These signals can be used to give an indication of the quality of the optical link. Even when a DC signal is applied to the data, handshake and TxCL inputs, the ACS401 modem transmits approximately 40 kbps over the link in each direction. This control data is used to maintain the timing and the relative positioning of 'transmit'and 'receive' windows.

The transmit and control data is constantly monitored to make sure it is compatible with the 3B4B format. If a coding error is detected than ERL will go High and will remain High until reset. ERL may be reset by asserting PORB or by removing the fiber-optic cable from one side of the link thereby forcing the device temporarily out of lock.

ERC produces a pulse on detection of each coding error. These pulses may be accumulated by means of an external electronic counter.

Please note that ERL and ERC detect coding errors and not data errors, nevertheless because of the complexity of the coding rules on the ACS401 the absence of detected errors on these pins will give a good indication of a high quality link.

LASER/LED Considerations

Since LEDs or LASERs from different suppliers may emit different wavelengths, it is recommended that the LASERs/LEDs in a communicating pair of modems are obtained from the same supplier. Furthermore, the emission spectrum is a function of temperature, so a temperature difference between the ends of a link reduces the responsivity of the receiving LASER/LED, resulting in a reduction in the link budget. Information is given in the suppliers' data sheets. The following manufacturers have components that will be tested with the ACS401 and Acapella will be glad to assist with contact names and addresses on request:

LED Suppliers

ABB-Hafo	(e.g.1A-212ST, 1A-212SMA)
Acapella	(e.g.A-ST, A-SMA)
GCA	(e.g.1A-212-ST-05, 1A-212-SM-02)
Honeywell	(e.g.HFE4214-013, HFE4404-013)

Duplex Suppliers

GCA	90-0359
Siemens	SBM 51214X

Operating Wavelengths

The ACS401 can support any wavelength LED, ELED or LASER, from 660 nm through to 1500 nm.

Power Supply Decoupling

The ACS401 contains a highly sensitive amplifier, capable of responding to extremely low current levels. To exploit this sensitivity it is important to reduce external noise to a low level compared to the input signal from the LASER/LED. The modem should have an independent power trace to the point where power enters the board.

Figure 3. shows the recommended power supply decoupling. The LASER/LED should be sited very close to the PINN, LAN and LAP pins. A generous ground plane should be provided, especially around the sensitive PINN, LAN and LAP pins. The modem should be protected from EMI/RFI sources in the standard ways.

Link Budgets

The link budget is the difference between the power coupled to the fiber via the transmit LASER/LED and the power required to realise the minimum input amplifier current via the receive LASER/LED/PIN. The link budget is normally specified in dB or dBm, and represents the maximum attenuation allowed between communicating LASER/LEDs. The budget is utilised in terms of the cable length, cable connectors and splices. It usually includes an operating margin to allow for degradation in LASER/LED performance. The power coupled to the cable, is a function of the efficiency of the LASER/LED, the current applied to the LASER/LED and the type of the fiber optic cable employed.

The conversion current produced by the reverse biased LASER/LED or PIN is a function of the LASER/LED/PIN efficiency and the fiber type. The conversion efficiency is measured in terms of its ability to convert the available optical power to current, known as the responsivity, given in (A/W). Some examples of link budgets are given in the tables headed, Link Budget Examples.

Digital Mode

The ACS401 may be used as a controller and data buffer which allows the device to be used with an external amplifier for non-fiber applications. Check with Acapella for details.

Data delay and skew

The Full Duplex Delay (FDD) of TxD and control signals XI(1:2) when using the recommended XTAL frequency of 9.216 MHz ($FDD_{9.216MHz}$) are as follows:

TxD $FDD_{9.216MHz}$	=	4 ms ('standard'mode)
TxD $FDD_{9.216MHz}$	=	8 ms ('double' mode)
XI $FDD_{9.216MHz}$	=	10 ms ('standard'mode)
XI $FDD_{9.216MHz}$	=	20 ms ('double' mode)

For other XTAL frequencies, the delay is inversely proportional to the XTAL frequency using the above delays as the constant of proportionality.

$FDD_{XTAL} = (9.216 * 10^6 / XTAL) * FDD_{9.216MHz}$

The synchronous data skew between the main data channels RxD1, RxD2, RxD3 and RxD4 across the link is zero data-bits.

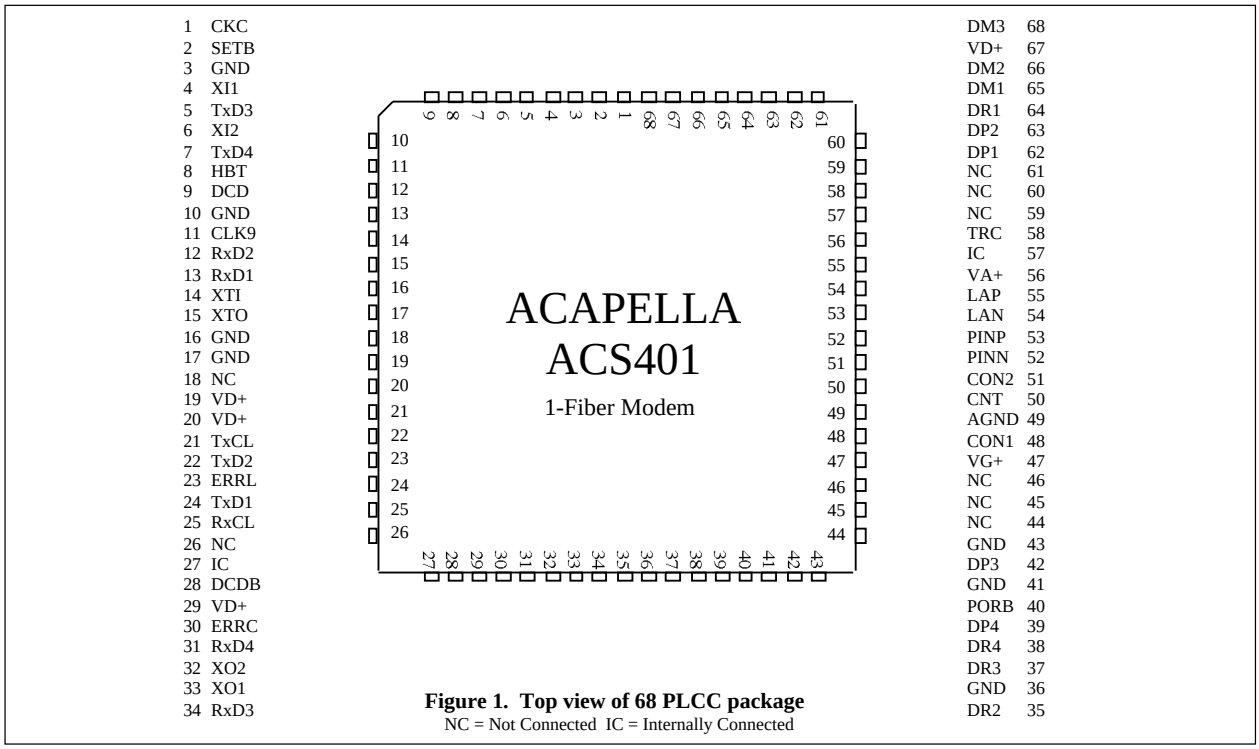
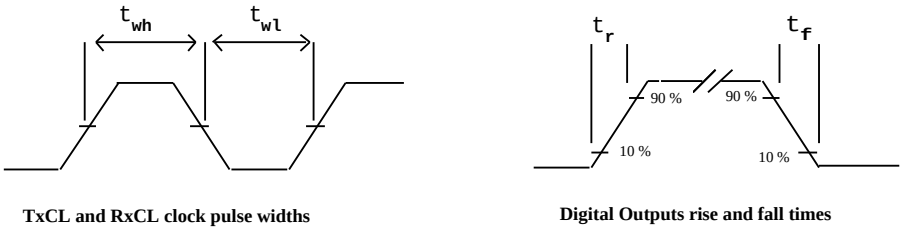


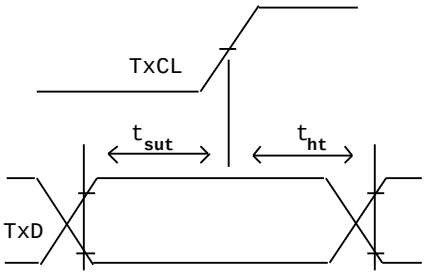
Figure 1. Top view of 68 PLCC package

NC = Not Connected IC = Internally Connected

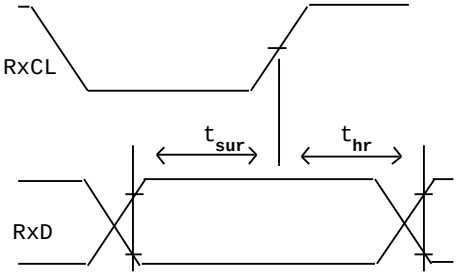


TxCL and RxCL clock pulse widths

Digital Outputs rise and fall times



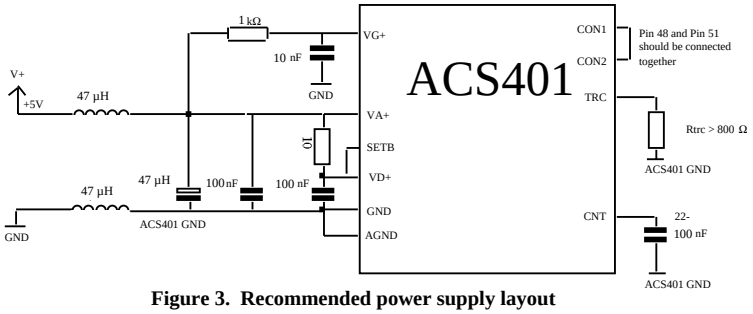
Transmit set-up and hold times



Receive set-up and hold times

Figure 2. Timing diagrams

VD+ pins 19, 20, 29 and 67.
GND pins 3, 10, 16, 17, 36, 41 and 43



All capacitors should be placed very close to the ACS401.

Figure 3. Recommended power supply layout

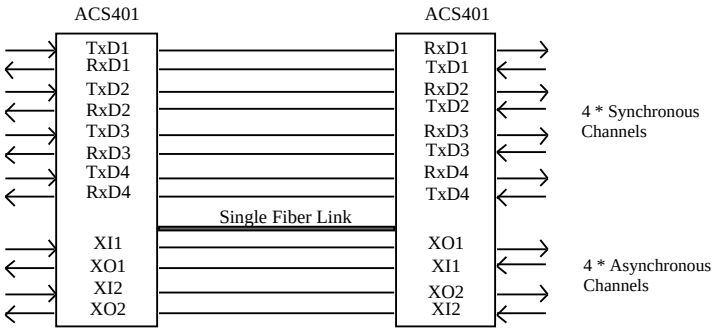


Figure 4. 6 Full-duplex channels over a single fiber

Single Fiber LED link

Link Budget Example (Rtrc set so LED launch current = 100 mApeak)

Fibertype	**Plastic**	**Glass**	**Glass**
Fibersize	**1000 micron**	**62.5 micron**	**50 micron**
Minimum transmit couple power to fiber (µW)	1000	100	50
Minimum LED responsivity (AW)	0.01	0.1	0.12
Minimum ACS401 sensitivity (nA)	500	500	500
Minimum input power to ACS401 amplifier (µW)	50	5	4.1
Link budget (dB)	13	13	11

Single Fiber Duplex LASER link

Link Budget Example (LASER launch power = 1 mW)

Fibertype	**Glass (single mode)**
Fibersize	**9 micron**
Minimum transmit couple power to fiber (µW)	1000
Minimum PIN responsivity (AW)	0.35
Minimum ACS401 sensitivity (nA)	500
Minimum input power to ACS401 amplifier (µW)	1.43
Link budget (dB) (single mode fiber attenuation = 0.3 dB km)	28.4

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Power supply VD+ and VA+ (VDD = VD+ or VA+)	VDD	-0.3	6.0	V
Input voltage (non-supply pins)	Vin	GND - 0.3	VDD + 0.3	V
Input current (except LAN,LAP,PINN,PINP,CNT)	Iin	-	10.0	mA
Input current (LAN, LAP,PINN,PINP,CNT)	Iin	-	1.0	mA
Storage temperature	Tstor	-50	160	˚C

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power supply (VA+ and DA+)	V+		5.0	5.25	V
Ambient temperature range	TA	-40	-	85	˚C

Static Digital Input Characteristics (for specified operating conditions)
Input pins: DR 1/2/3/4, DM 1/2/3, DP1/2/3/4 CKC, TXD1/2/3, PORB, TxCL(input)

Parameter	Symbol	Min	Typ	Max	Units
Vin High	Vih	2.0	-	-	V
Vin Low	Vil	-	-	0.8	V
Input currentIin	-	-	10	µA	

Static Digital Input Characteristics (for specified operating conditions)
Input pins: XI1, XI2, SETB.

Parameter	Symbol	Min	Typ	Max	Units
Vin High	Vih	2.0	-	-	V
Vin Low	Vil	-	-	0.8	V
Pull-up resistor	PU	50k	125k	340k	Ω
Input current (Note 1)	Iin	-	-	100	µA

Note 1: Input current is mainly attributed to pull-up resistor, so it applies when input is Low.The High input current is <10µA.

Static Digital Output Characteristics (for specified operating conditions)
Output pins: RxD1/2/3, XO1 XO2, DCDB, ERRL, ERRD, RxCL, CLK9, TxCL(output), HBT.

Parameter	Symbol	Min	Typ	Max	Units
Vout Low (Iin = 4mA) except HBT	Vol	0	-	0.5	V
Vout High (Iout = 4mA) except HBT	Voh	VDD-0.5	-	-	V
Vout Low (Iin - 16mA) HBT	Vol	0	-	0.5	V
Vout High (Iout = 16mA) HBT	Voh	VDD-0.5	-	-	V
Max load capcitance	CI	-	-	50	pF

Dynamic Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Crystal frequency (XT1, XTO)	XTAL	1.0	9.216	12	MHz
External clock (XTI) High or Low time	fclp	40	-	60	%
RxD and TxD data rate ‘standard’mode ‘double’mode	fclp	XTAL/576 XTAL/576	-	XTAL/72 XTAL/144	bps
RxCLand TxCLduty cycle (with TxCL= output)	twh twl	-	50	-	%
Frequency deviation at TxCLfrom selected value (with TxCL= input)	Fd	500	-	-	ppm
TxD to TxCLset-up time	tsut	300	-	-	ns
TxD to TxCLhold time	tht	25	-	-	ns
RxD to RxCLset-up time	tsur	-	0.5 * (1/RxCL)	-	ns
RxD to RxCLhold time	thr	-	0.5 * (1/RxCL)	-	ns
Digital output - fall time	tf	-	-	100	ns
Digital output - rise time	tr	-	-	100	ns
Power consumption with LASER/LED peak current = 50mA Single channel 64 kbps (Note 2)	Pc	-	35	-	mW

Note 2: Power consumption assumes CMOS loads. Check with Acapella for other bandwidth products.

Matching Characteristics (for specified operating conditions

Parameter	Symbol	Min	Typ	Max	Units
Crystal tolerance use parallel resonate crystal and recommended padding capacitors	Ct	-100	0	100	ppm
Minimum amplifier sensitivity		-	-	500	nA
Maximum amplifier input current	Imax	1	-	-	mA
Rtre placed between TRC and GND	Rtrc	0.8k	-	40k	Ω
Laser current (max limit) Rtrc=0.8 kOhm Rtrc=40 kOhms	Ilaser	75 1.8	100 2.5	125 3.2	mA
LED current Rtrc=0.8 kOhm Rtrc=40 kOhm	Iled	75 1.8	100 2.5	125 3.2	mA
Single-Fibermode Parameters					
LED capacitance with Vr=0 with Irec=500 nA with Irec=1000 nA	CI	- -	- -	50 100	pF
LED leakage current Vr=1.4	Lleak	-	-	500	nA
LED reverse bias	Vr	0.65	1.15	1.4	V
LASER PIN diode leakage current Vrp=4.0V	Pleak	-	-	100	nA
LASER PINdiode reverse bias	Vrp	-	-	4.0	V
Dual-Fibermode Parameters					
PIN capacitance with Vr=0	CI	-	-	20	pF
PINleakage current	Lleak	-	-	150	nA
PINreverse bias	Vr	0.95	1.15	1.4	V

Acapella Ltd.
Epsilon House
Chilworth Research Centre
Southampton SO16 7NP
England

UK Tel. 01703 769 008
UK Fax. 01703 768 612

Intn’l. Tel. +44 1703 769 008
Intn’l. Fax. +44 1703 768 612

Email: sales@acapella.co.uk
Web: www.acapella.co.uk

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