

Radiation Hardened Triple 3-Input NOR Gate

The Radiation Hardened ACS27MS is a Triple 3-Input NOR Gate. For each gate, a HIGH level on any input results in a LOW level on the Y output. A LOW level on all inputs results in a HIGH level on the Y output. All inputs are buffered and the outputs are designed for balanced propagation delay and transition times.

The ACS27MS is fabricated on a CMOS Silicon on Sapphire (SOS) process, which provides an immunity to Single Event Latch-up and the capability of highly reliable performance in any radiation environment. These devices offer significant power reduction and faster performance when compared to ALSTTL types.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the ACS27MS are contained in SMD 5962-98630. A “hot-link” is provided on our homepage for downloading.
www.intersil.com/spacedefense/spaceselect.asp

Features

- QML Qualified Per MIL-PRF-38535 Requirements
- 1.25 Micron Radiation Hardened SOS CMOS
- Radiation Environment
 - Latch-Up Free Under Any Conditions
 - Total Dose (Max.) 3×10^5 RAD(Si)
 - SEU Immunity $<1 \times 10^{-10}$ Errors/Bit/Day
 - SEU LET Threshold $>100\text{MeV}/(\text{mg}/\text{cm}^2)$
- Input Logic Levels. $V_{IL} = (0.3)(V_{CC}), V_{IH} = (0.7)(V_{CC})$
- Output Current $\pm 12\text{mA}$ (Min)
- Quiescent Supply Current $5.0\mu\text{A}$ (Max)
- Propagation Delay 17ns (Max)

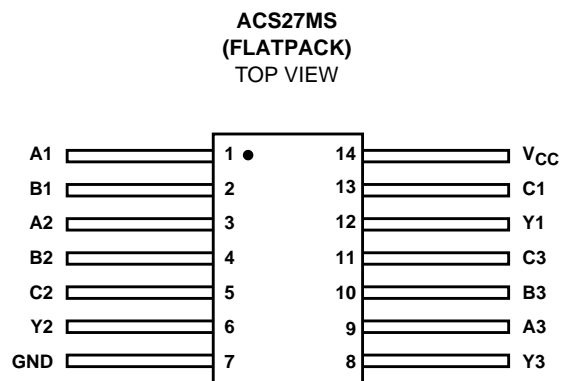
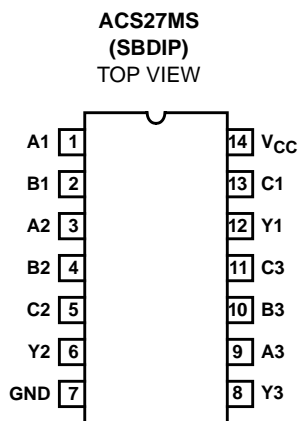
Applications

- High Speed Control Circuits
- Sensor Monitoring
- Low Power Designs

Ordering Information

ORDERING NUMBER	INTERNAL MARKETING NUMBER	TEMP. RANGE (°C)	PACKAGE	DESIGNATOR
5962F9863001VCC	ACS27DMSR-03	-55 to 125	14 Ld SBDIP	CDIP2-T14
ACS27D/SAMPLE-03	ACS27D/SAMPLE-03	25	14 Ld SBDIP	CDIP2-T14
5962F9863001VXC	ACS27KMSR-03	-55 to 125	14 Ld Flatpack	CDFP3-F14
ACS27K/SAMPLE-03	ACS27K/SAMPLE-03	25	14 Ld Flatpack	CDFP3-F14
5962F9863001V9A	ACS27HMSR-03	25	Die	NA

Pinouts



Die Characteristics

DIE DIMENSIONS:

Size: 2390µm x 2390µm (94 mils x 94 mils)
 Thickness: 525µm ±25µm (20.6 mils ±1 mil)
 Bond Pad: 110µm x 110µm (4.3 x 4.3 mils)

METALLIZATION: Al

Metal 1 Thickness: 0.7µm ±0.1µm
 Metal 2 Thickness: 1.0µm ±0.1µm

SUBSTRATE POTENTIAL

Unbiased Insulator

PASSIVATION:

Type: Phosphorous Silicon Glass (PSG)
 Thickness: 1.30µm ±0.15µm

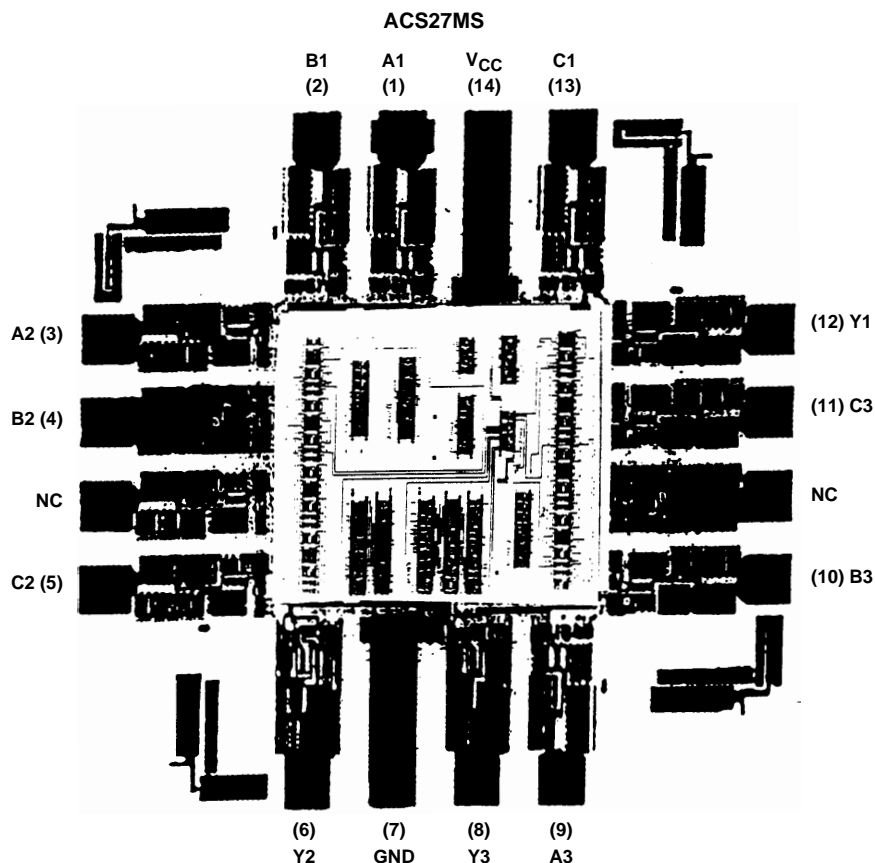
SPECIAL INSTRUCTIONS

Bond V_{CC} First

ADDITIONAL INFORMATION:

Worst Case Current Density: <2.0 x 10⁵ A/cm²
 Transistor Count: 97

Metallization Mask Layout



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