

# *ACS245MS*

# **Radiation Hardened Octal Non-Inverting Bidirectional Bus Transceiver**

January 1996

#### **Features**

- Devices QML Qualified in Accordance with MIL-PRF-38535
- Detailed Electrical and Screening Requirements are Contained in SMD# 5962-96707 and Intersil' QM Plan
- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose ......>300K RAD (Si)
- Single Event Upset (SEU) Immunity: <1 x 10<sup>-10</sup> Errors/Bit/Day
- SEU LET Threshold . . . . . . . . . . . >100 MEV-cm<sup>2</sup>/ma
- Dose Rate Survivability......>10<sup>12</sup> RAD (Si)/s, 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range . . . . . . . . . . -55°C to +125°C
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range ...... 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current  $\leq 1\mu A$  at VOL, VOH
- Fast Propagation Delay...... 15ns (Max), 10ns (Typ)

# Description

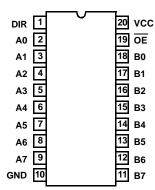
The Intersil ACS245MS is a Radiation Hardened octal non-inverting bidirectional bus transceiver intended for two-way asynchronous communication between data busses.

The ACS245MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened. high-speed, CMOS/SOS Logic Family.

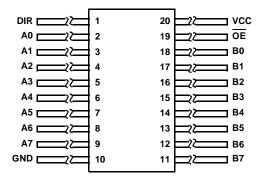
The ACS245MS is supplied in a 20 lead Ceramic Flatpack (K suffix) or a Dual-In-Line Ceramic Package (D suffix).

#### **Pinouts**

20 PIN CERAMIC DUAL-IN-LINE, MIL-STD-1835 DESIGNATOR CDIP2-T20. LEAD FINISH C TOP VIEW



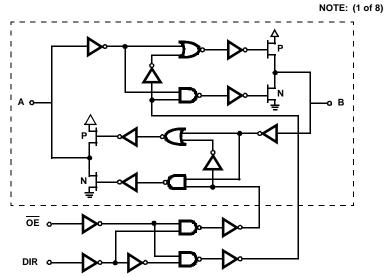
20 PIN CERAMIC FLATPACK, MIL-STD-1835 **DESIGNATOR CDFP4-F20, LEAD FINISH C TOP VIEW** 



# **Ordering Information**

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
5962F9670701VRC	-55°C to +125°C	MIL-PRF-38535 Class V	20 Lead SBDIP
5962F9670701VXC	-55°C to +125°C	MIL-PRF-38535 Class V	20 Lead Ceramic Flatpack
ACS245D/Sample	25°C	Sample	20 Lead SBDIP
ACS245K/Sample	25°C	Sample	20 Lead Ceramic Flatpack
ACS245HMSR	25°C	Die	Die

# **Functional Diagram**



#### **TRUTH TABLE**

INP		
ŌĒ	DIR	OPERATION
L	L	B Data to A Bus
L	Н	A Data to B Bus
Н	Х	Isolation

NOTE:

H = High Voltage Level, L = Low Voltage Level, X = Immaterial

All Intersil semiconductor products are manufactured, assembled and tested under ISO9000 quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site http://www.intersil.com

# ACS245MS

# Die Characteristics

#### **DIE DIMENSIONS:**

96 mils x 117 mils 2.44mm x 2.97mm

#### **METALLIZATION:**

Type: AISi

Metal 1 Thickness: 7.125kÅ ±1.125kÅ Metal 2 Thickness: 9kÅ ±1kÅ

## **GLASSIVATION:**

Type: SiO<sub>2</sub>

Thickness: 8kÅ ±1kÅ

# **WORST CASE CURRENT DENSITY:**

 $< 2.0 \times 10^5 \text{A/cm}^2$ 

#### **BOND PAD SIZE:**

 $110\mu m$  x  $110\mu m$  4.4 mils x 4.4 mils

# Metallization Mask Layout

## ACS245MS

