ACS112MS

Radiation Hardened Dual J-K Flip-Flop

January 1996

Features

- Devices QML Qualified in Accordance with MIL-PRF-38535
- Detailed Electrical and Screening Requirements are Contained in SMD# 5962-96704 and Intersil'sIntersil QM Plan
- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose . . . . . >300K RAD (Si)
- Single Event Upset (SEU) Immunity: <1 x 10^{-10} Errors/Bit/Day (Typ)
- SEU LET Threshold . . . . . >100 MEV-cm^2/mg
- Dose Rate Upset . . . . . >10^{11} RAD (Si)/s, 20ns Pulse
- Dose Rate Survivability . . . . . >10^{12} RAD (Si)/s, 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range . . . . . -55°C to +125°C
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range . . . . . 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current ≤ 1μA at VOL, VOH
- Fast Propagation Delay . . . . . 21ns (Max), 14ns (Typ)

Description

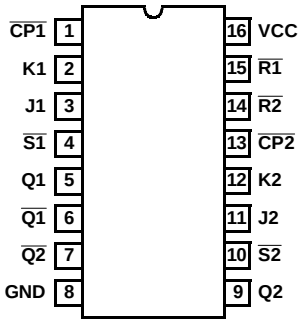
The Intersil ACS112MS is a Radiation Hardened Dual J-K Flip-Flop with Set and Reset. The output change states on the negative transition of the clock (CP1N or CP2N).

The ACS112MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of the radiation hardened, high-speed, CMOS/SOS Logic Family.

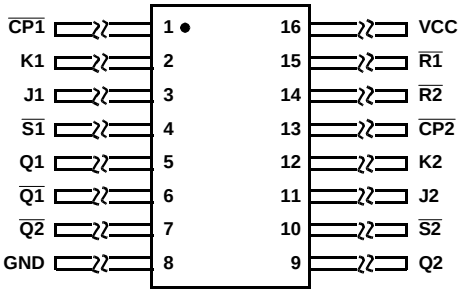
The ACS112MS is supplied in a 16 lead Ceramic Flatpack (K suffix) or a Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835, DESIGNATOR CDIP2-T16,
LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLATPACK
MIL-STD-1835, DESIGNATOR CDFP4-F16,
LEAD FINISH C
TOP VIEW



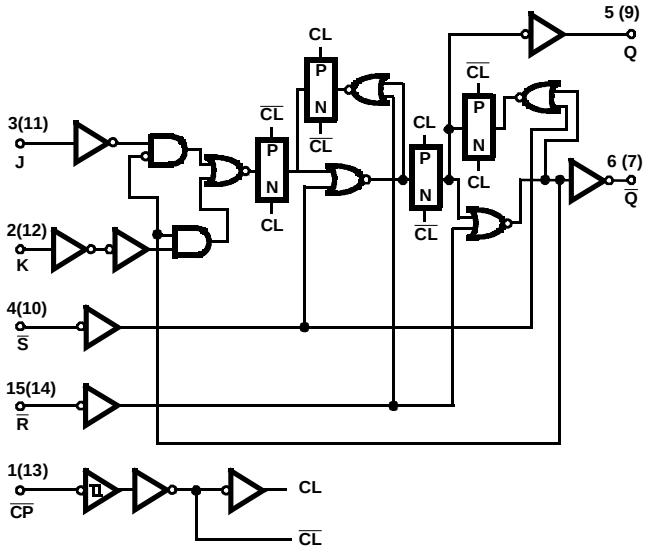
Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
5962F9670401VEC	-55°C to +125°C	MIL-PRF-38535 Class V	16 Lead SBDIP
5962F9670401VXC	-55°C to +125°C	MIL-PRF-38535 Class V	16 Lead Ceramic Flatpack
ACS112D/Sample	25°C	Sample	16 Lead SBDIP
ACS112K/Sample	25°C	Sample	16 Lead Ceramic Flatpack
ACS112HMSR	25°C	Die	Die

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 321-724-7143 | Intersil (and design) is a trademark of Intersil Americas Inc.

Spec Number **518816**
FN3571.1

Functional Diagram



TRUTH TABLE

INPUTS					OUTPUTS	
$\overline{S}$	$\overline{R}$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H (Note 2)	H (Note 2)
H	H	↓	L	L	No Change	
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	No Change	

NOTES:

1. H = High Steady State, L = Low Steady State, X = Immaterial, ↓ = High-to-Low Transition
2. Output States Unpredictable if $\overline{S}$ and $\overline{R}$ Go High Simultaneously after Both being Low at the Same Time

Die Characteristics

DIE DIMENSIONS:

88 mils x 88 mils
2.24mm x 2.24mm

METALLIZATION:

Type: AlSi
Metal 1 Thickness: 7.125kÅ ±1.125kÅ
Metal 2 Thickness: 9kÅ ±1kÅ

GLASSIVATION:

Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

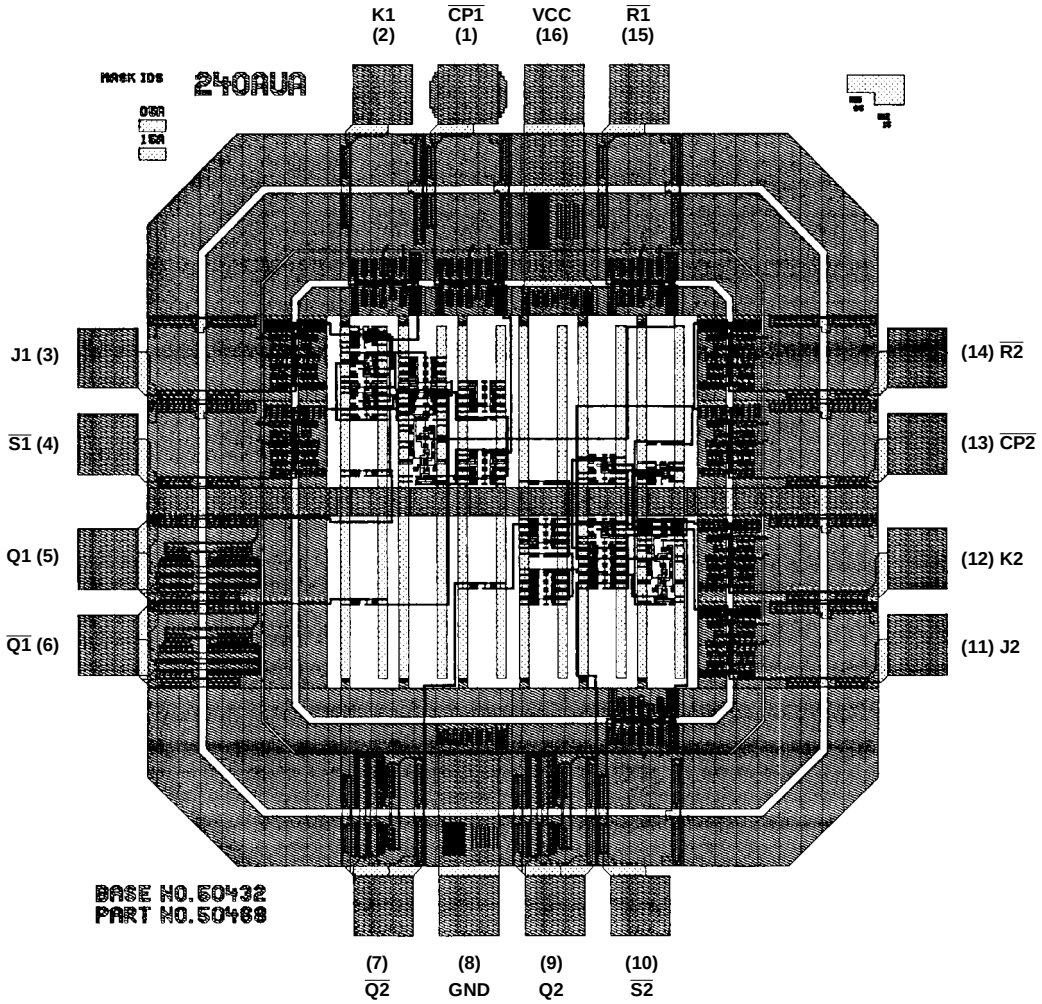
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:

110µm x 110µm
4.3 mils x 4.3 mils

Metallization Mask Layout

ACS112MS



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