![intersil logo]

Radiation Hardened Dual J-K Flip-Flop with Set and Reset

The Radiation Hardened ACS109MS is a Dual J-K Flip-Flop with Set and Reset. These Flip-Flops have independent J, $\overline{K}$, Set, Reset, and Clock inputs and Q and $\overline{Q}$ outputs. The outputs change state on the positive-going transition of the clock. Set and Reset are accomplished asynchronously by Low-level inputs. All inputs are buffered and the outputs are designed for balanced propagation delay and transition times.

The ACS109MS is fabricated on a CMOS Silicon on Sapphire (SOS) process, which provides an immunity to Single Event Latch-up and the capability of highly reliable performance in any radiation environment. These devices offer significant power reduction and faster performance when compared to ALSTTL types.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the ACS109MS are contained in SMD 5962-98632. A "hot-link" is provided on our homepage for downloading.
http://www.intersil.com/spacedefense/spaceselect.htm

Features

- QML Qualified Per MIL-PRF-38535 Requirements

- 1.25 Micron Radiation Hardened SOS CMOS

- Radiation Environment
  - Latch-Up Free Under Any Conditions
  - Total Dose (Max.) . . . . 3 x 10^5 RAD(Si)
  - SEU Immunity. . . . . <1 x 10^{-10} Errors/Bit/Day
  - SEU LET Threshold . . . . >100MeV/(mg/cm^2)

- Input Logic Levels. . . . V_{IL} = (0.3)(V_{CC}), V_{IH} = (0.7)(V_{CC})

- Output Current . . . . ±12mA (Min)

- Quiescent Supply Current . . . . 10μA (Max)

- Propagation Delay . . . . .25ns (Max)
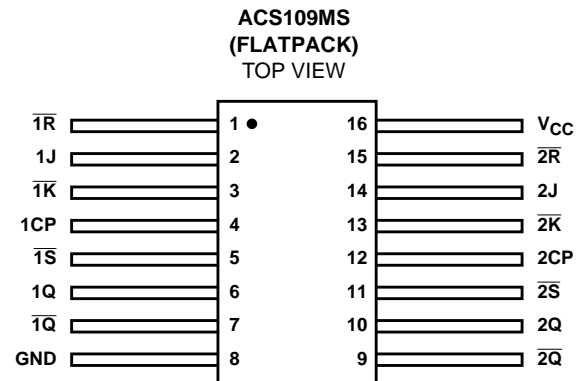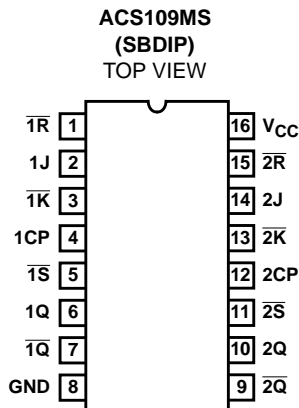
Applications

- High Speed Control Circuits

- Sensor Monitoring

- Low Power Designs

Ordering Information

ORDERING NUMBER	INTERNAL MARKETING NUMBER	TEMP. RANGE (°C)	PACKAGE	DESIGNATOR
5962F9863201VCC	ACS109DMSR-03	-55 to 125	16 Ld SBDIP	CDIP2-T16
ACS109D/SAMPLE-03	ACS109D/SAMPLE-03	25	16 Ld SBDIP	CDIP2-T16
5962F9863201VXC	ACS109KMSR-03	-55 to 125	16 Ld Flatpack	CDFP4-F16
ACS109K/SAMPLE-03	ACS109K/SAMPLE-03	25	16 Ld Flatpack	CDFP4-F16
5962F9863201V9A	ACS109HMSR-03	25	Die	NA

Pinouts

ACS109MS (SBDIP)
TOP VIEW

```
  1R  [1        16] VCC
  1J  [2        15] 2R
  1K  [3        14] 2J
 1CP  [4        13] 2K
  1S  [5        12] 2CP
  1Q  [6        11] 2S
  1Q  [7        10] 2Q
 GND  [8         9] 2Q
```

ACS109MS (FLATPACK)
TOP VIEW

```
  1R  ─ 1 ●      16 ─ VCC
  1J  ─ 2        15 ─ 2R
  1K  ─ 3        14 ─ 2J
 1CP  ─ 4        13 ─ 2K
  1S  ─ 5        12 ─ 2CP
  1Q  ─ 6        11 ─ 2S
  1Q  ─ 7        10 ─ 2Q
 GND  ─ 8         9 ─ 2Q
```

Die Characteristics

DIE DIMENSIONS:

Size: 2390µm x 2390µm (94 mils x 94 mils)
Thickness: 525µm ±25µm (20.6 mils ±1 mil)
Bond Pad: 110µm x 110µm (4.3 x 4.3 mils)

METALLIZATION: Al

Metal 1 Thickness: 0.7µm ±0.1µm
Metal 2 Thickness: 1.0µm ±0.1µm

SUBSTRATE POTENTIAL

Unbiased Insulator

PASSIVATION:

Type: Phosphorous Silicon Glass (PSG)
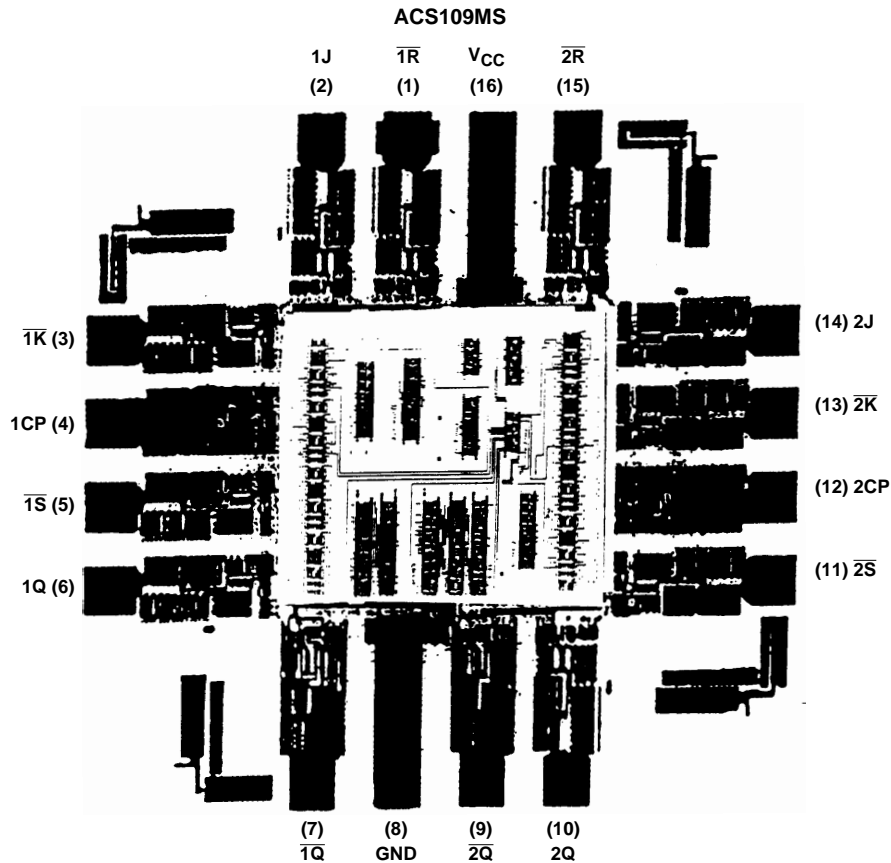Thickness: 1.30µm ±0.15µm

SPECIAL INSTRUCTIONS

Bond V_{CC} First

ADDITIONAL INFORMATION:

Worst Case Current Density: $<2.0 \times 10^5$ A/cm^2
Transistor Count: 236

Metallization Mask Layout

ACS109MS

1J (2) $\overline{1R}$ (1) V_{CC} (16) $\overline{2R}$ (15)

$\overline{1K}$ (3) (14) 2J

1CP (4) (13) $\overline{2K}$

$\overline{1S}$ (5) (12) 2CP

1Q (6) (11) $\overline{2S}$

(7) $\overline{1Q}$ (8) GND (9) $\overline{2Q}$ (10) 2Q

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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