Data Sheet | November 1998 | File Number 4542

## Radiation Hardened Hex Inverter with Open Drain Outputs

The Radiation Hardened ACS05MS is a Hex Inverter with open drain outputs. This device inverts a HIGH level on each input to a LOW level on the corresponding Y output. A LOW level on the input causes the corresponding Y output to enter a high impedance state, which can be pulled HIGH through a resistor to $V_{CC}$. All inputs are buffered and the outputs are designed for balanced propagation delay and transition times.

The ACS05MS is fabricated on a CMOS Silicon on Sapphire (SOS) process, which provides an immunity to Single Event Latch-up and the capability of highly reliable performance in any radiation environment. These devices offer significant power reduction and faster performance when compared to ALSTTL types.

**Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.**

**Detailed Electrical Specifications for the ACS05MS are contained in SMD 5962-98602. A "hot-link" is provided on our homepage with instructions for downloading. www.intersil.com/data/sm/index.asp**

## Features

- QML Qualified Per MIL-PRF-38535 Requirements
- 1.25 Micron Radiation Hardened SOS CMOS
- Radiation Environment
  - Latch-Up Free Under any Conditions
  - Total Dose . . . . . $3 \times 10^5$ RAD (Si)
  - SEU Immunity . . . . . $<1 \times 10^{-10}$ Errors/Bit/Day
  - SEU LET Threshold . . . . . >100MeV/(mg/cm$^2$)
- Input Logic Levels. . . . $V_{IL} = (0.3)(V_{CC})$, $V_{IH} = (0.7)(V_{CC})$
- Output Current . . . . . ±8mA (Min)
- Quiescent Supply Current . . . . . 100µA (Max)
- Propagation Delay . . . . . 20ns (Max)

## Applications

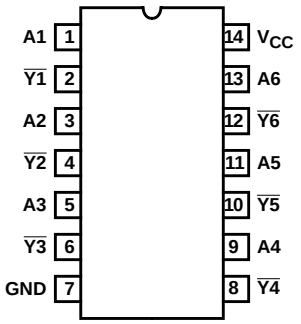
- High Speed Control Circuits
- Sensor Monitoring
- Low Power Designs

## Ordering Information

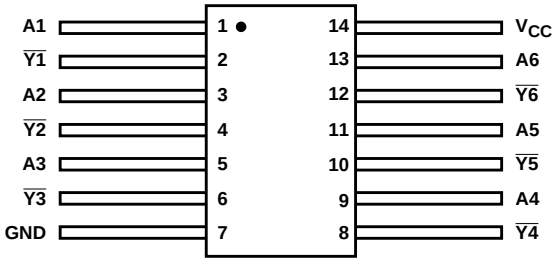
| ORDERING NUMBER | INTERNAL MKT. NUMBER | TEMP. RANGE ($^o$C) | PACKAGE | DESIGNATOR |
|---|---|---|---|---|
| 5962F9860201VCC | ACS05DMSR-03 | -55 to 125 | 14 Ld SBDIP | CDIP2-T14 |
| ACS05D/SAMPLE-03 | ACS05D/SAMPLE-03 | 25 | 14 Ld SBDIP | CDIP2-T14 |
| 5962F9860201VXC | ACS05KMSR-03 | -55 to 125 | 14 Ld Flatpack | CDFP4-F14 |
| ACS05K/SAMPLE-03 | ACS05K/SAMPLE-03 | 25 | 14 Ld Flatpack | CDFP4-F14 |
| 5962F9860201V9A | ACS05HMSR-03 | 25 | Die | N/A |

## Pinouts

**ACS05MS**
**(SBDIP)**
TOP VIEW




**ACS05MS**
**(FLATPACK)**
TOP VIEW



## Die Characteristics

**DIE DIMENSIONS:**

Size: 2390µm x 2390µm (94 mils x 94 mils)
Thickness: 525µm ±25µm (20.6 mils ±1 mil)
Bond Pad: 110µm x 110µm (4.3 x 4.3 mils)

**METALLIZATION:**

Metal 1 Thickness: 0.7µm ±0.1µm
Metal 2 Thickness: 1.0µm ±0.1µm

**SUBSTRATE POTENTIAL**

Unbiased Insulator

**PASSIVATION:**

Type: Phosphorous Silicon Glass (PSG)
Thickness: 1.30µm ±0.15µm

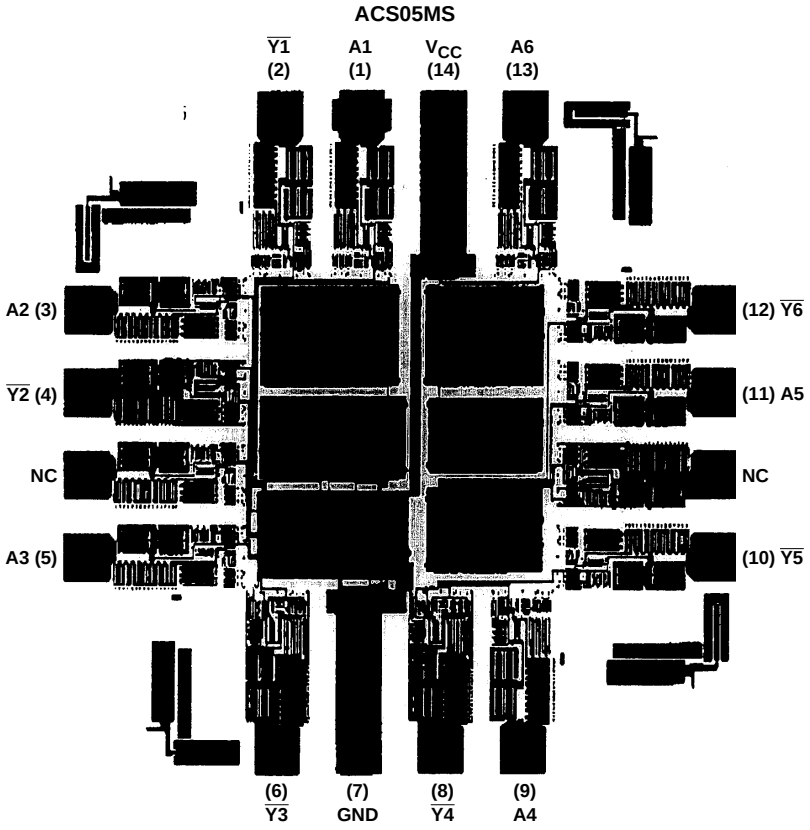
**SPECIAL INSTRUCTIONS:**

Bond $V_{CC}$ First

**ADDITIONAL INFORMATION:**

Worst Case Current Density: $<2.0 \times 10^5$ A/cm$^2$
Transistor Count: 46

## Metallization Mask Layout




All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.



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