

Radiation Hardened Hex Inverter

The Radiation Hardened ACS04MS is a Hex Inverter. This device simply inverts the level present on each input. All inputs are buffered and the outputs are designed for balanced propagation delay and transition times.

The ACS04MS is fabricated on a CMOS Silicon on Sapphire (SOS) process, which provides an immunity to Single Event Latch-up and the capability of highly reliable performance in any radiation environment. These devices offer significant power reduction and faster performance when compared to ALSTTL types.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the ACS04MS are contained in SMD 5962-98603. A "hot-link" is provided on our homepage with instructions for downloading. www.intersil.com/data/sm/index.asp

Features

- QML Qualified Per MIL-PRF-38535 Requirements
- 1.25 Micron Radiation Hardened SOS CMOS
- Radiation Environment
 - Latch-Up Free Under Any Conditions
 - Total Dose 3×10^5 RAD(Si)
 - SEU Immunity $<1 \times 10^{-10}$ Errors/Bit/Day
 - SEU LET Threshold $>100\text{MeV}/(\text{mg}/\text{cm}^2)$
- Input Logic Levels. . . . $V_{IL} = (0.3)(V_{CC})$, $V_{IH} = (0.7)(V_{CC})$
- Output Current $\pm 8\text{mA}$ (Min)
- Quiescent Supply Current $100\mu\text{A}$ (Max)
- Propagation Delay 15ns (Max)

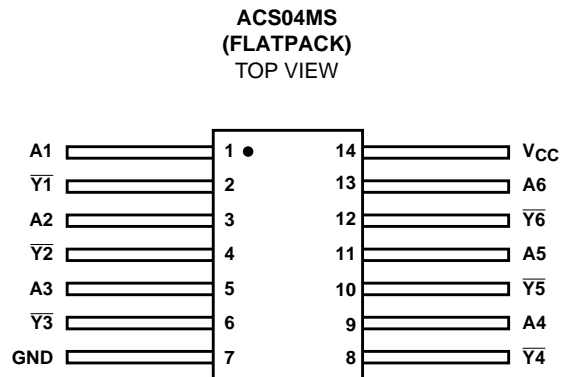
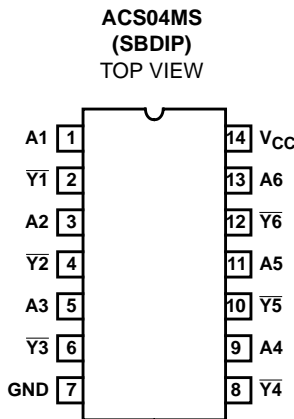
Applications

- High Speed Control Circuits
- Sensor Monitoring
- Low Power Designs

Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (°C)	PACKAGE	DESIGNATOR
5962F9860301VCC	ACS04DMSR-03	-55 to 125	14 Ld SBDIP	CDIP2-T14
ACS04D/SAMPLE-03	ACS04D/SAMPLE-03	25	14 Ld SBDIP	CDIP2-T14
5962F9860301VXC	ACS04KMSR-03	-55 to 125	14 Ld Flatpack	CDFP4-F14
ACS04K/SAMPLE-03	ACS04K/SAMPLE-03	25	14 Ld Flatpack	CDFP4-F14
5962F9860301V9A	ACS04HMSR-03	25	Die	N/A

Pinouts



Die Characteristics

DIE DIMENSIONS:

Size: 2390µm x 2390µm (94 mils x 94 mils)
 Thickness: 525µm ±25µm (20.6 mils ±1 mil)
 Bond Pad: 110µm x 110µm (4.3 x 4.3 mils)

METALLIZATION: Al

Metal 1 Thickness: 0.7µm ±0.1µm
 Metal 2 Thickness: 1.0µm ±0.1µm

SUBSTRATE POTENTIAL:

Unbiased Insulator

PASSIVATION:

Type: Phosphorous Silicon Glass (PSG)
 Thickness: 1.30µm ±0.15µm

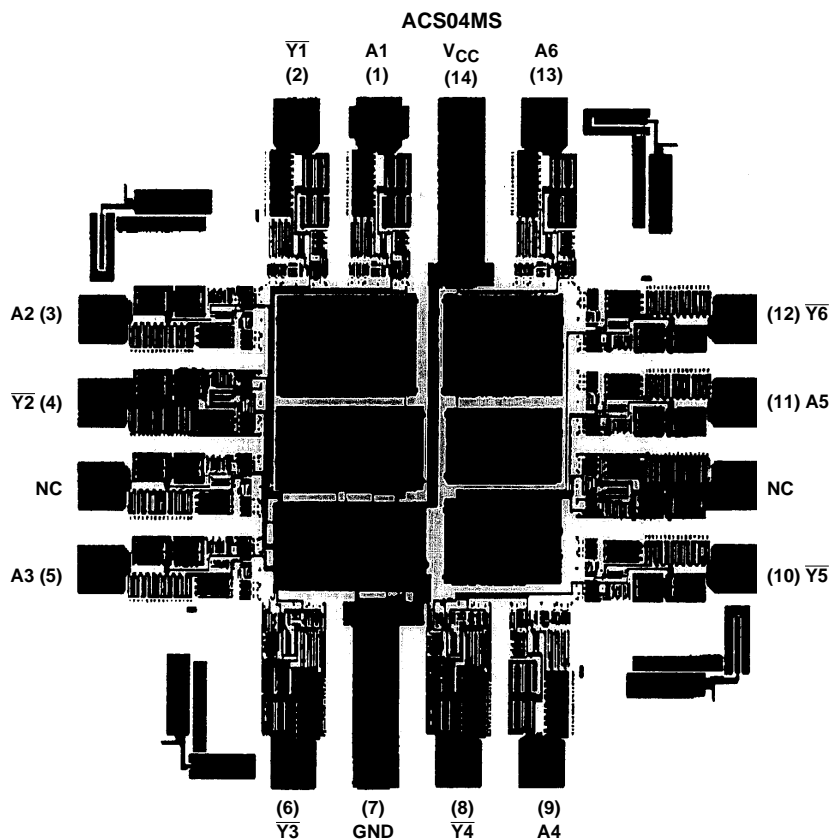
SPECIAL INSTRUCTIONS:

Bond V_{CC} First

ADDITIONAL INFORMATION:

Worst Case Current Density: <math><2.0 \times 10^5 \text{ A/cm}^2</math>
 Transistor Count: 82

Metallization Mask Layout



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Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
 P. O. Box 883, Mail Stop 53-204
 Melbourne, FL 32902
 TEL: (321) 724-7000
 FAX: (321) 724-7240

EUROPE

Intersil SA
 Mercure Center
 100, Rue de la Fusee
 1130 Brussels, Belgium
 TEL: (32) 2.724.2111
 FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
 7F-6, No. 101 Fu Hsing North Road
 Taipei, Taiwan
 Republic of China
 TEL: (886) 2 2716 9310
 FAX: (886) 2 2715 3029