



MICROCHIP

MCP3204/3208

2.7V 4-Channel/8-Channel 12-Bit A/D Converters with SPI® Serial Interface

FEATURES

- 12-bit resolution
- ± 1 LSB max DNL
- ± 1 LSB max INL (MCP3204/3208-B)
- ± 2 LSB max INL (MCP3204/3208-C)
- 4 (MCP3204) or 8 (MCP3208) input channels
- Analog inputs programmable as single-ended or pseudo differential pairs
- On-chip sample and hold
- SPI® serial interface (modes 0,0 and 1,1)
- Single supply operation: 2.7V - 5.5V
- 100ksps max. sampling rate at $V_{DD} = 5V$
- 50ksps max. sampling rate at $V_{DD} = 2.7V$
- Low power CMOS technology
 - 500 nA typical standby current, 2 μ A max.
 - 400 μ A max. active current at 5V
- Industrial temp range: -40°C to +85°C
- Available in PDIP, SOIC and TSSOP packages

APPLICATIONS

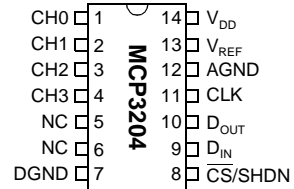
- Sensor Interface
- Process Control
- Data Acquisition
- Battery Operated Systems

DESCRIPTION

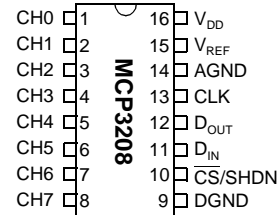
The Microchip Technology Inc. MCP3204/3208 devices are successive approximation 12-bit Analog-to-Digital (A/D) Converters with on-board sample and hold circuitry. The MCP3204 is programmable to provide two pseudo-differential input pairs or four single-ended inputs. The MCP3208 is programmable to provide four pseudo-differential input pairs or eight single-ended inputs. Differential Nonlinearity (DNL) is specified at ± 1 LSB, and Integral Nonlinearity (INL) is offered in ± 1 LSB (MCP3204/3208-B) and ± 2 LSB (MCP3204/3208-C) versions. Communication with the devices is done using a simple serial interface compatible with the SPI protocol. The devices are capable of conversion rates of up to 100ksps. The MCP3204/3208 devices operate over a broad voltage range (2.7V - 5.5V). Low current design permits operation with typical standby and active currents of only 500nA and 320 μ A, respectively. The MCP3204 is offered in 14-pin PDIP, 150mil SOIC and TSSOP packages, and the MCP3208 is offered in 16-pin PDIP and SOIC packages.

PACKAGE TYPES

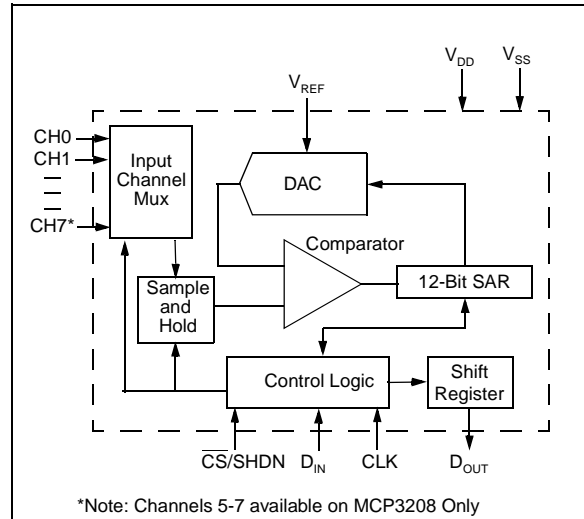
PDIP, SOIC, TSSOP



PDIP, SOIC



FUNCTIONAL BLOCK DIAGRAM



MCP3204/3208

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{DD} 7.0V
 All inputs and outputs w.r.t. V_{SS} -0.6V to V_{DD} +0.6V
 Storage temperature -65°C to +150°C
 Ambient temp. with power applied..... -65°C to +125°C
 Soldering temperature of leads (10 seconds) .. +300°C
 ESD protection on all pins > 4kV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

| NAME | FUNCTION |
|----------------------|----------------------------|
| V_{DD} | +2.7V to 5.5V Power Supply |
| DGND | Digital Ground |
| AGND | Analog Ground |
| CH0-CH7 | Analog Inputs |
| CLK | Serial Clock |
| D_{IN} | Serial Data In |
| D_{OUT} | Serial Data Out |
| $\overline{CS}/SHDN$ | Chip Select/Shutdown Input |
| V_{REF} | Reference Voltage Input |

ELECTRICAL CHARACTERISTICS

All parameters apply at $V_{DD} = 5V$, $V_{SS} = 0V$, $V_{REF} = 5V$, $T_{AMB} = -40^{\circ}C$ to $+85^{\circ}C$, $f_{SAMPLE} = 100ksps$ and $f_{CLK} = 20 * f_{SAMPLE}$, unless otherwise noted.

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|--------------|----------------|-----------------------|--------------------|--------------------|--|
| Conversion Rate | | | | | | |
| Conversion Time | t_{CONV} | | | 12 | clock cycles | |
| Analog Input Sample Time | t_{SAMPLE} | 1.5 | | | clock cycles | |
| Throughput Rate | f_{SAMPLE} | | | 100 50 | ksp/s ksp/s | $V_{DD} = V_{REF} = 5V$ $V_{DD} = V_{REF} = 2.7V$ |
| DC Accuracy | | | | | | |
| Resolution | | 12 | | | bits | |
| Integral Nonlinearity | INL | | ± 0.75 ± 1 | ± 1 ± 2 | LSB | MCP3204/3208-B MCP3204/3208-C |
| Differential Nonlinearity | DNL | | ± 0.5 | ± 1 | LSB | No missing codes over temperature |
| Offset Error | | | ± 1.25 | ± 3 | LSB | |
| Gain Error | | | ± 1.25 | ± 5 | LSB | |
| Dynamic Performance | | | | | | |
| Total Harmonic Distortion | | | -82 | | dB | $V_{IN} = 0.1V$ to $4.9V$ @ 1kHz |
| Signal to Noise and Distortion (SINAD) | | | 72 | | dB | $V_{IN} = 0.1V$ to $4.9V$ @ 1kHz |
| Spurious Free Dynamic Range | | | 86 | | dB | $V_{IN} = 0.1V$ to $4.9V$ @ 1kHz |
| Reference Input | | | | | | |
| Voltage Range | | 0.25 | | V_{DD} | V | Note 2 |
| Current Drain | | | 100 0.001 | 150 3 | μA μA | $\overline{CS} = V_{DD} = 5V$ |
| Analog Inputs | | | | | | |
| Input Voltage Range for CH0-CH7 in Single-Ended Mode | | V_{SS} | | V_{REF} | V | |
| Input Voltage Range for IN+ In pseudo-differential Mode | | IN- | | $V_{REF} + IN-$ | | |
| Input Voltage Range for IN- In pseudo-differential Mode | | $V_{SS} - 100$ | | $V_{SS} + 100$ | mV | |
| Leakage Current | | | 0.001 | ± 1 | μA | |

ELECTRICAL CHARACTERISTICS (CONTINUED)

| All parameters apply at $V_{DD} = 5V$, $V_{SS} = 0V$, $V_{REF} = 5V$, $T_{AMB} = -40^{\circ}C$ to $+85^{\circ}C$, $f_{SAMPLE} = 100ksps$ and $f_{CLK} = 20 * f_{SAMPLE}$, unless otherwise noted. | | | | | | |
|--|----------------------|-----------------|------------|--------------|------------|--|
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
| Analog Inputs (Continued) | | | | | | |
| Switch Resistance | | | 1K | | Ω | See Figure 4-1 |
| Sample Capacitor | | | 20 | | pF | See Figure 4-1 |
| Digital Input/Output | | | | | | |
| Data Coding Format | | Straight Binary | | | | |
| High Level Input Voltage | V_{IH} | $0.7 V_{DD}$ | | | V | |
| Low Level Input Voltage | V_{IL} | | | $0.3 V_{DD}$ | V | |
| High Level Output Voltage | V_{OH} | 4.1 | | | V | $I_{OH} = -1mA$, $V_{DD} = 4.5V$ |
| Low Level Output Voltage | V_{OL} | | | 0.4 | V | $I_{OL} = 1mA$, $V_{DD} = 4.5V$ |
| Input Leakage Current | I_{LI} | -10 | | 10 | μA | $V_{IN} = V_{SS}$ or V_{DD} |
| Output Leakage Current | I_{LO} | -10 | | 10 | μA | $V_{OUT} = V_{SS}$ or V_{DD} |
| Pin Capacitance (All Inputs/Outputs) | C_{IN} , C_{OUT} | | | 10 | pF | $V_{DD} = 5.0V$ (Note 1) $T_{AMB} = 25^{\circ}C$, $f = 1 MHz$ |
| Timing Parameters | | | | | | |
| Clock Frequency | f_{CLK} | | | 2.0 1.0 | MHz MHz | $V_{DD} = 5V$ (Note 3) $V_{DD} = 2.7V$ (Note 3) |
| Clock High Time | t_{HI} | 250 | | | ns | |
| Clock Low Time | t_{LO} | 250 | | | ns | |
| \overline{CS} Fall To First Rising CLK Edge | t_{SUCS} | 100 | | | ns | |
| Data Input Setup Time | t_{SU} | | | 50 | ns | |
| Data Input Hold Time | t_{HD} | | | 50 | ns | |
| CLK Fall To Output Data Valid | t_{DO} | | | 200 | ns | See Test Circuits, Figure 1-2 |
| CLK Fall To Output Enable | t_{EN} | | | 200 | ns | See Test Circuits, Figure 1-2 |
| \overline{CS} Rise To Output Disable | t_{DIS} | | | 100 | ns | See Test Circuits, Figure 1-2 |
| \overline{CS} Disable Time | t_{CSH} | 500 | | | ns | |
| D_{OUT} Rise Time | t_R | | | 100 | ns | See Test Circuits, Figure 1-2 (Note 1) |
| D_{OUT} Fall Time | t_F | | | 100 | ns | See Test Circuits, Figure 1-2 (Note 1) |
| Power Requirements | | | | | | |
| Operating Voltage | V_{DD} | 2.7 | | 5.5 | V | |
| Operating Current | I_{DD} | | 320 225 | 400 | μA | $V_{DD} = V_{REF} = 5V$, D_{OUT} unloaded $V_{DD} = V_{REF} = 2.7V$, D_{OUT} unloaded |
| Standby Current | I_{DDS} | | 0.5 | 2 | μA | $\overline{CS} = V_{DD} = 5.0V$ |

Note 1: This parameter is guaranteed by characterization and not 100% tested.

Note 2: See graphs that relate linearity performance to V_{REF} levels.

Note 3: Because the sample cap will eventually lose charge, effective clock rates below 10kHz can affect linearity performance, especially at elevated temperatures. See Section 6.2 for more information.

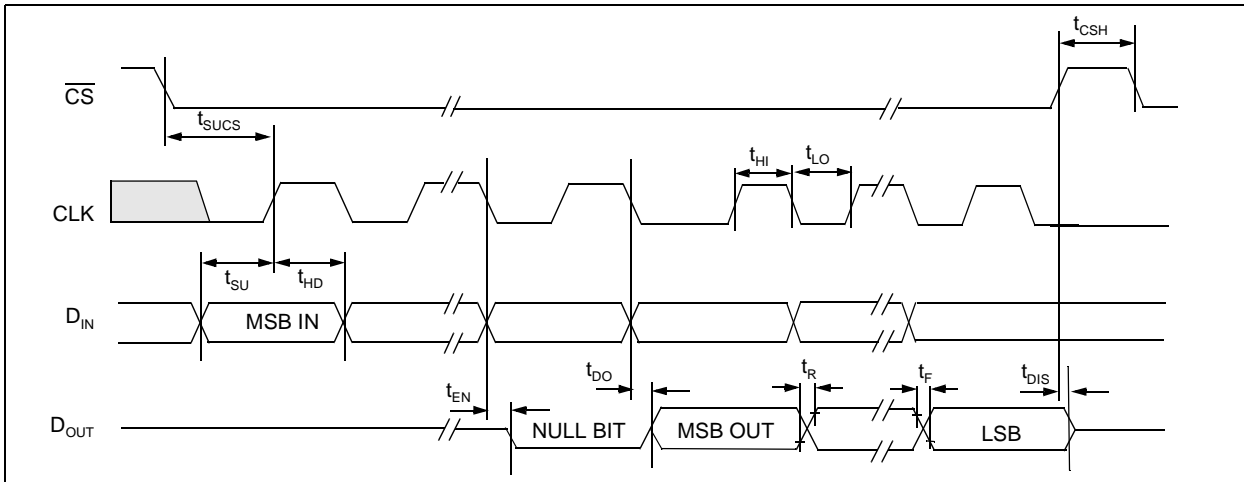


FIGURE 1-1: Serial Interface Timing.

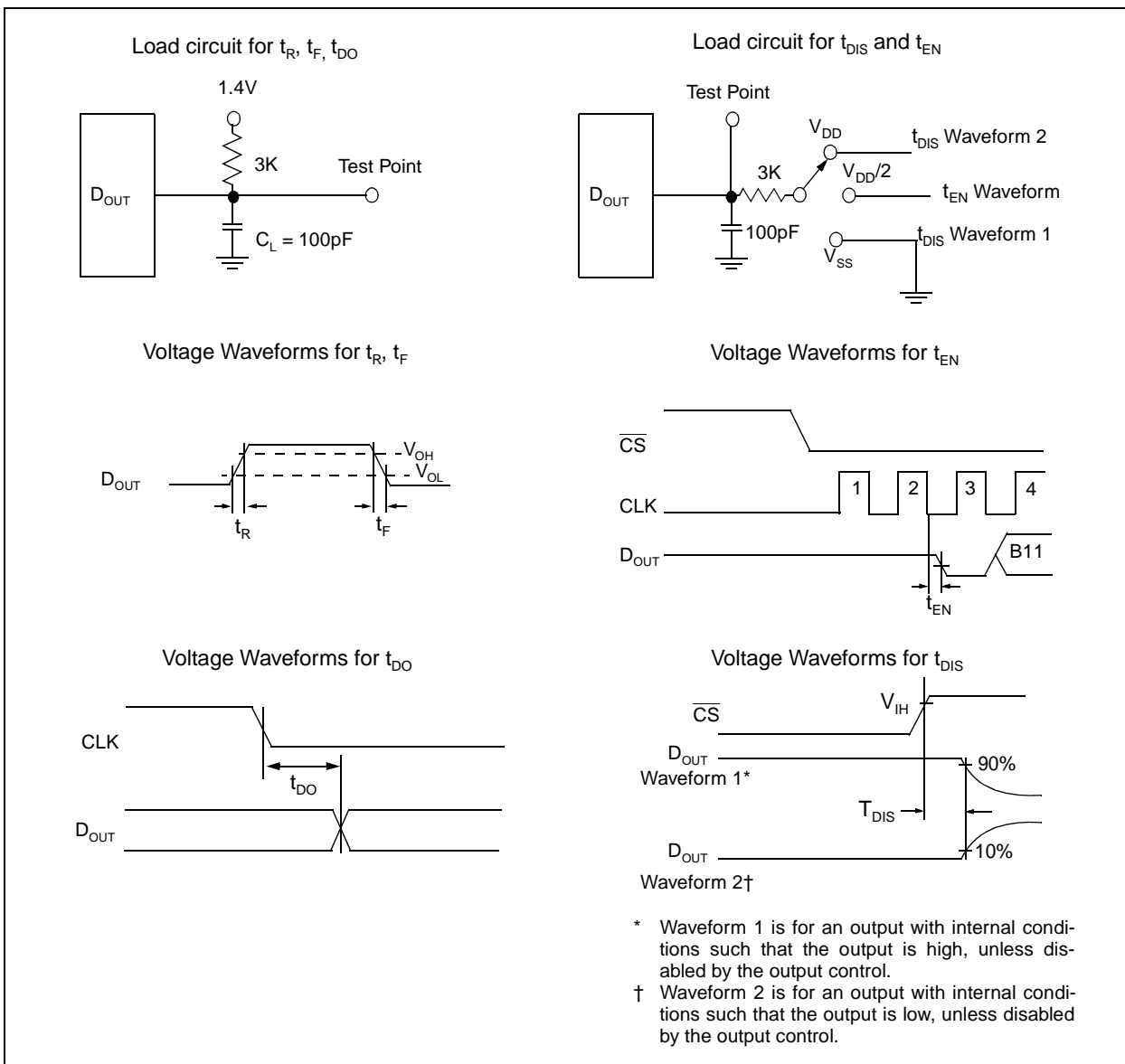


FIGURE 1-2: Test Circuits.

2.0 TYPICAL PERFORMANCE CHARACTERISTICS

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100\text{kpsps}$, $f_{CLK} = 20 * f_{SAMPLE}$, $T_A = 25^\circ\text{C}$

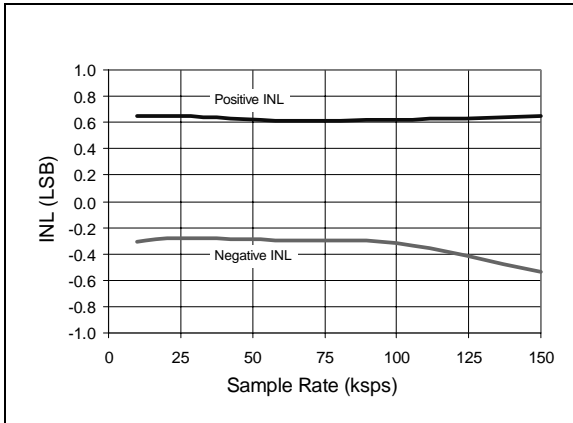


FIGURE 2-1: Integral Nonlinearity (INL) vs. Sample Rate.

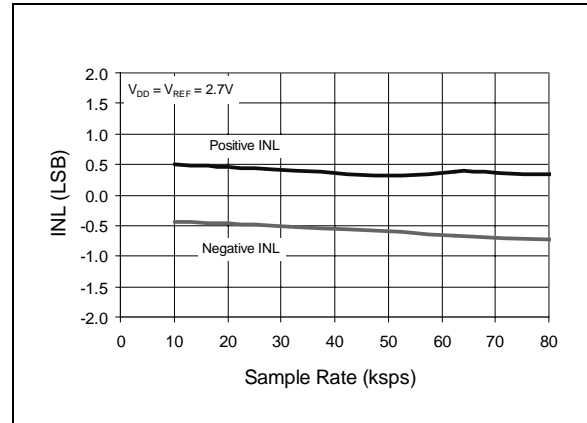


FIGURE 2-4: Integral Nonlinearity (INL) vs. Sample Rate ($V_{DD} = 2.7V$).

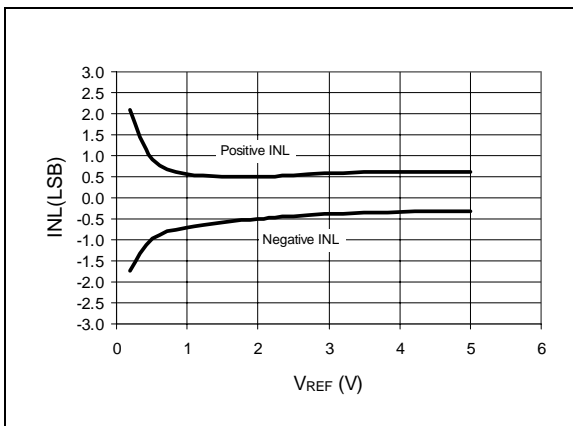


FIGURE 2-2: Integral Nonlinearity (INL) vs. V_{REF} .

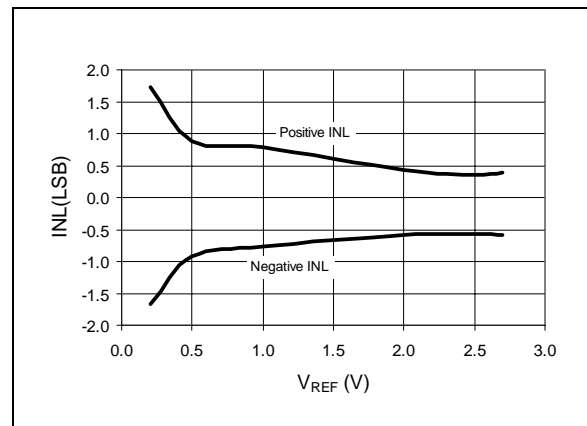


FIGURE 2-5: Integral Nonlinearity (INL) vs. V_{REF} ($V_{DD} = 2.7V$).

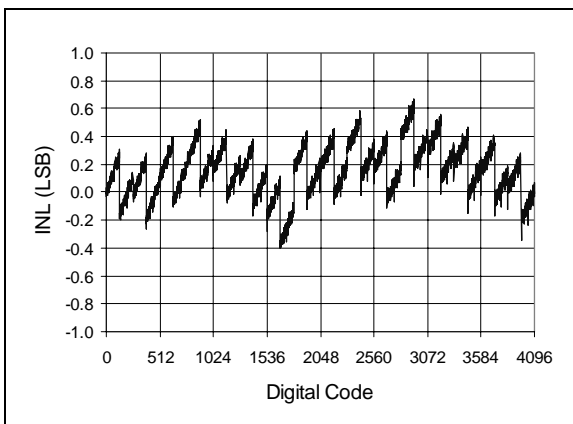


FIGURE 2-3: Integral Nonlinearity (INL) vs. Code (Representative Part).

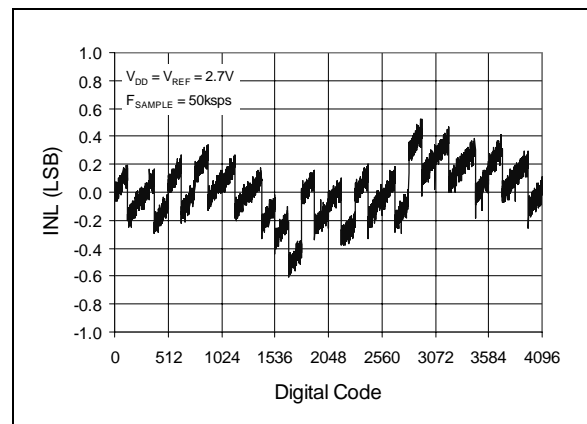


FIGURE 2-6: Integral Nonlinearity (INL) vs. Code (Representative Part, $V_{DD} = 2.7V$).

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Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100\text{kpsps}$, $f_{CLK} = 20 * f_{SAMPLE}$, $T_A = 25^\circ\text{C}$

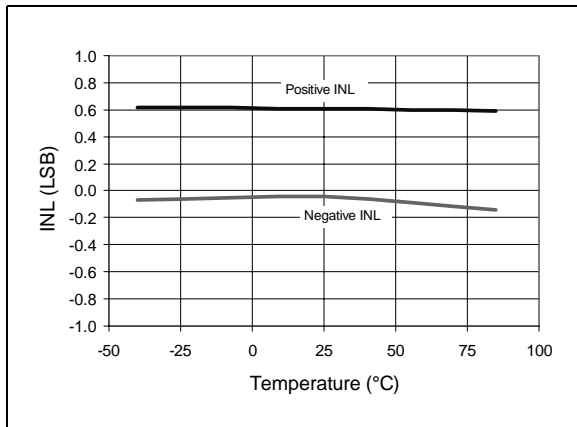


FIGURE 2-7: Integral Nonlinearity (INL) vs. Temperature.

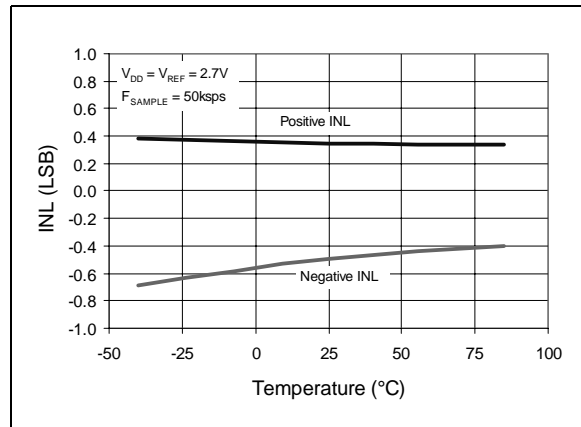


FIGURE 2-10: Integral Nonlinearity (INL) vs. Temperature ($V_{DD} = 2.7V$).

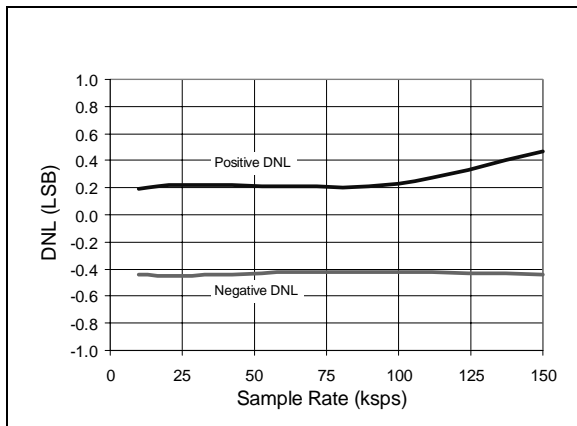


FIGURE 2-8: Differential Nonlinearity (DNL) vs. Sample Rate.

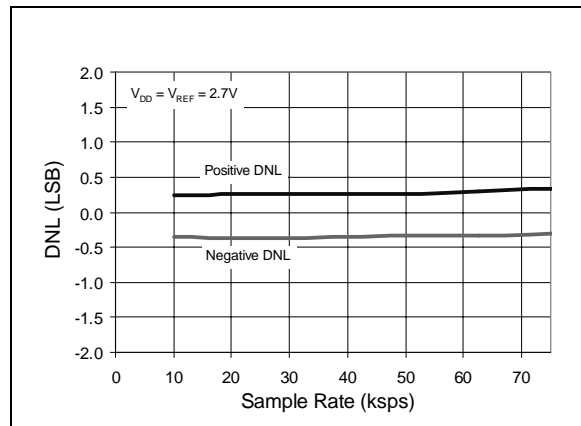


FIGURE 2-11: Differential Nonlinearity (DNL) vs. Sample Rate ($V_{DD} = 2.7V$).

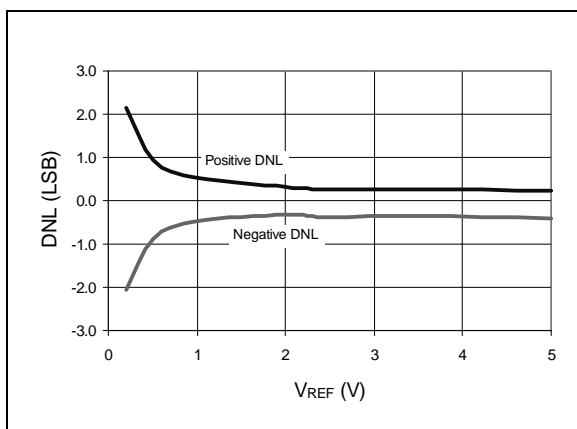


FIGURE 2-9: Differential Nonlinearity (DNL) vs. V_{REF} .

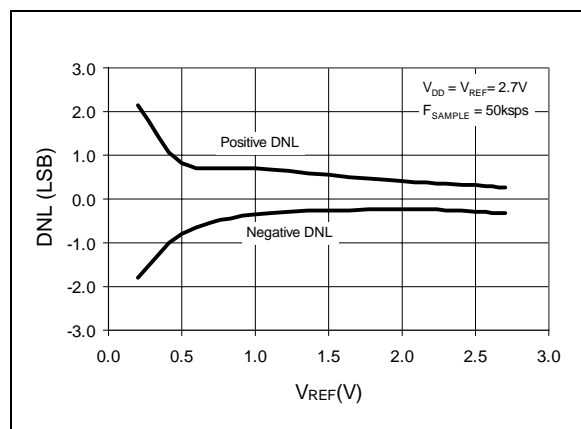


FIGURE 2-12: Differential Nonlinearity (DNL) vs. V_{REF} ($V_{DD} = 2.7V$).

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100kps$, $f_{CLK} = 20 * f_{SAMPLE}$, $T_A = 25^{\circ}C$

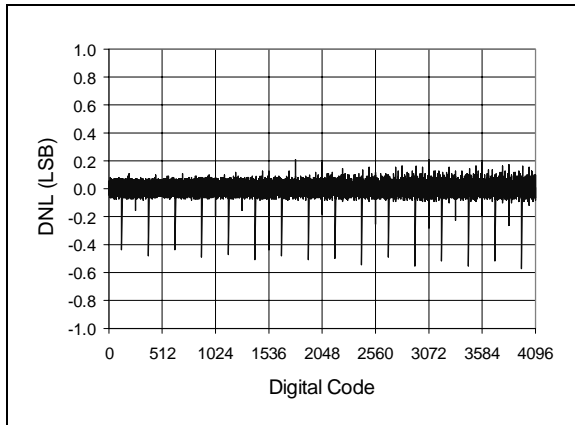


FIGURE 2-13: Differential Nonlinearity (DNL) vs. Code (Representative Part).

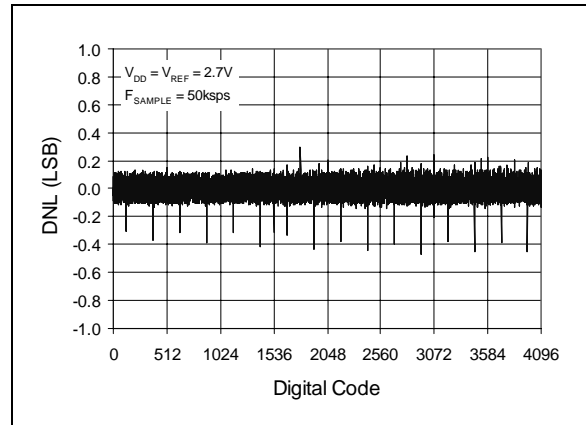


FIGURE 2-16: Differential Nonlinearity (DNL) vs. Code (Representative Part, $V_{DD} = 2.7V$).

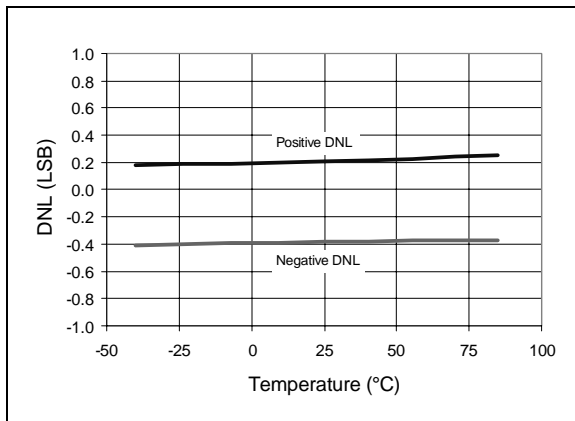


FIGURE 2-14: Differential Nonlinearity (DNL) vs. Temperature.

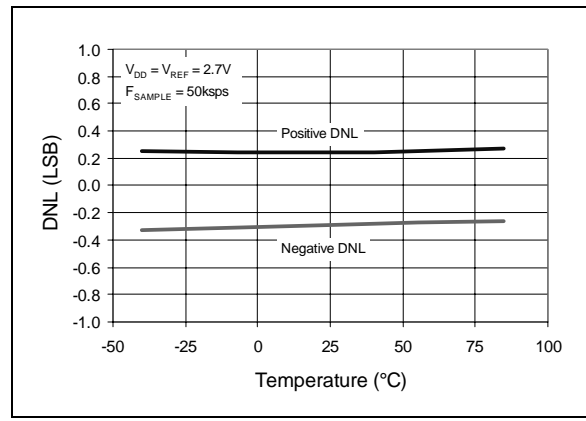


FIGURE 2-17: Differential Nonlinearity (DNL) vs. Temperature ($V_{DD} = 2.7V$).

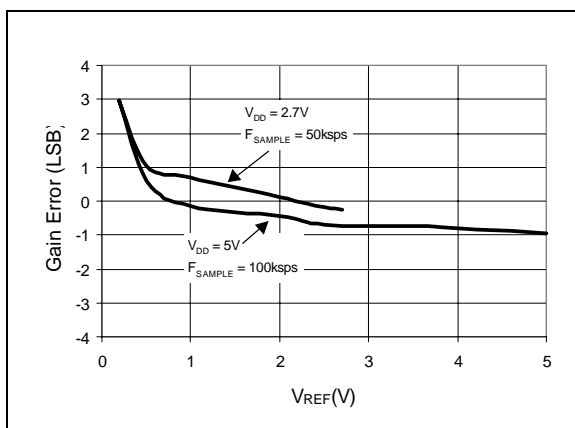


FIGURE 2-15: Gain Error vs. V_{REF} .

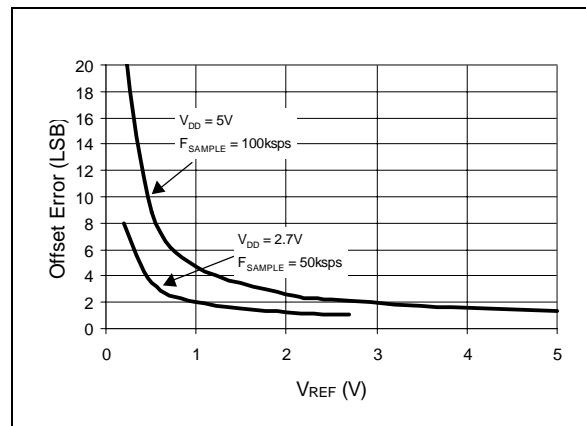


FIGURE 2-18: Offset Error vs. V_{REF} .

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Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100kps$, $f_{CLK} = 20 * f_{SAMPLE}$, $T_A = 25^{\circ}C$

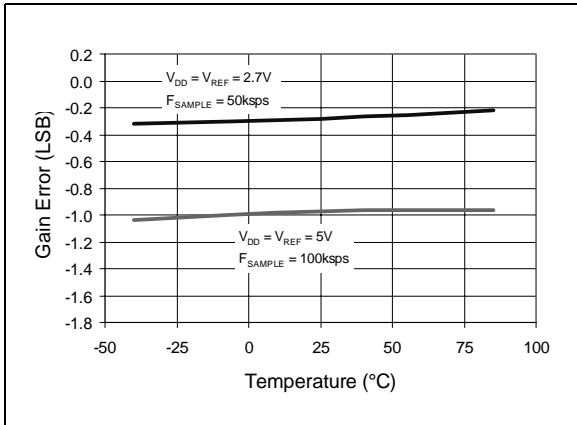


FIGURE 2-19: Gain Error vs. Temperature.

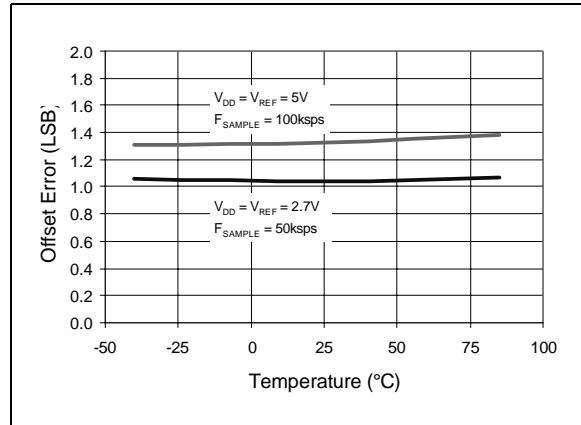


FIGURE 2-22: Offset Error vs. Temperature.

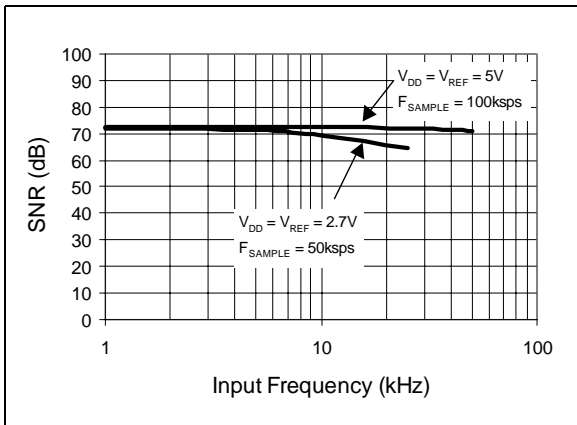


FIGURE 2-20: Signal to Noise (SNR) vs. Input Frequency.

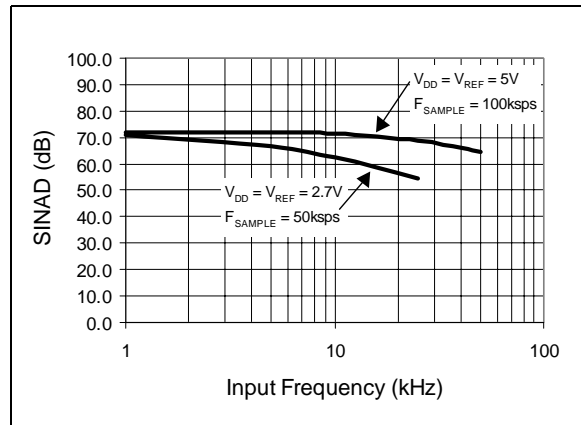


FIGURE 2-23: Signal to Noise and Distortion (SINAD) vs. Input Frequency.

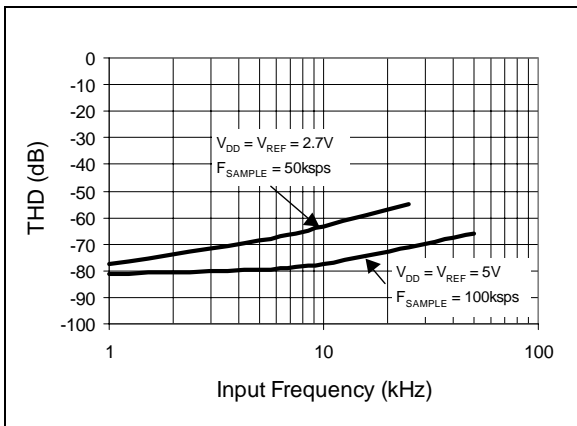


FIGURE 2-21: Total Harmonic Distortion (THD) vs. Input Frequency.

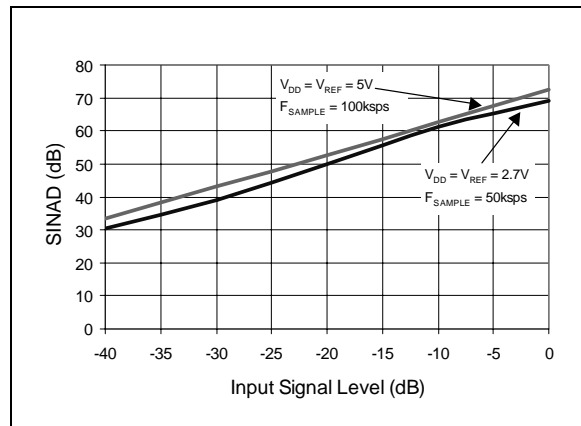


FIGURE 2-24: Signal to Noise and Distortion (SINAD) vs. Input Signal Level.

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100ksps$, $f_{CLK} = 20 * f_{SAMPLE}$, $T_A = 25^{\circ}C$

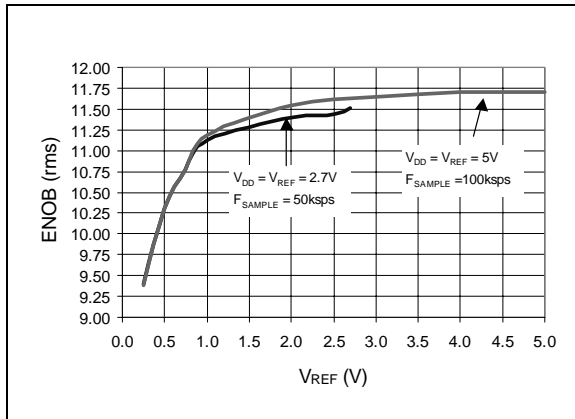


FIGURE 2-25: Effective Number of Bits (ENOB) vs. V_{REF} .

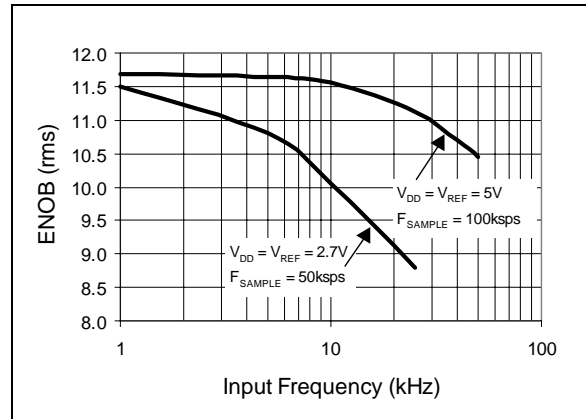


FIGURE 2-28: Effective Number of Bits (ENOB) vs. Input Frequency.

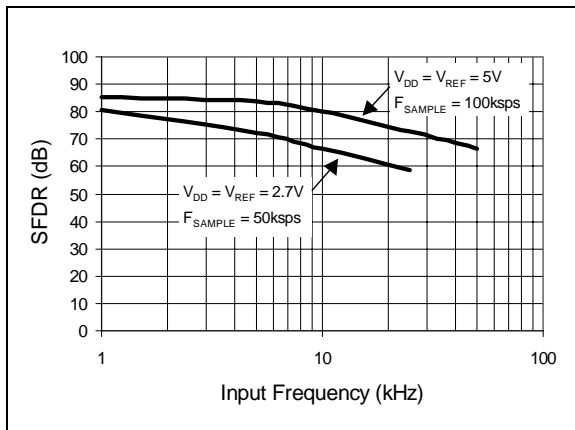


FIGURE 2-26: Spurious Free Dynamic Range (SFDR) vs. Input Frequency.

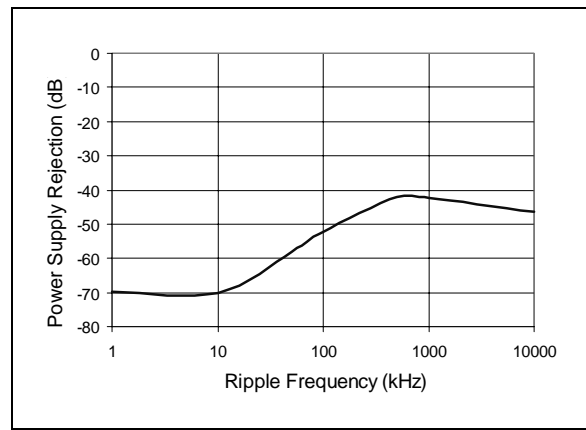


FIGURE 2-29: Power Supply Rejection (PSR) vs. Ripple Frequency.

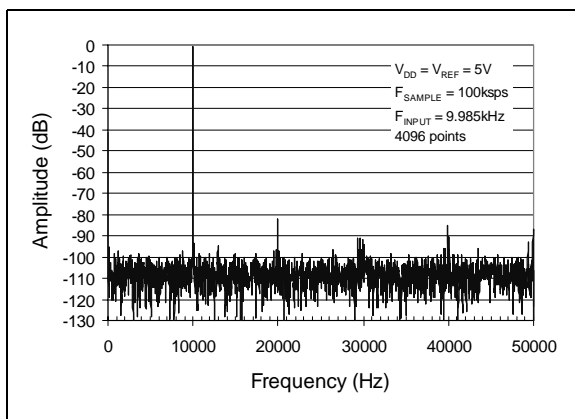


FIGURE 2-27: Frequency Spectrum of 10kHz input (Representative Part).

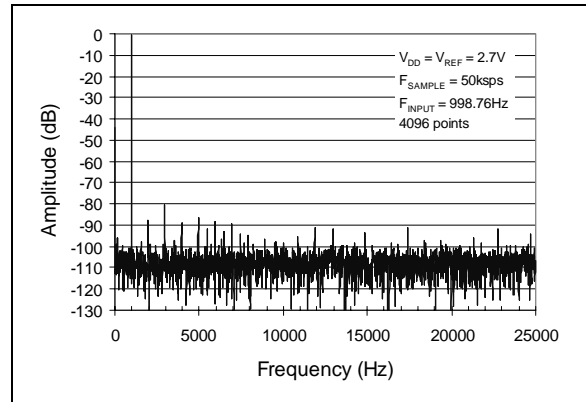


FIGURE 2-30: Frequency Spectrum of 1kHz input (Representative Part, $V_{DD} = 2.7V$).

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Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100kps$, $f_{CLK} = 20 * f_{SAMPLE}$, $T_A = 25^{\circ}C$

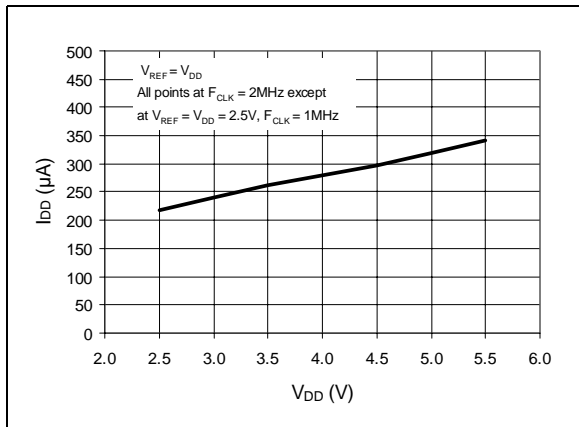


FIGURE 2-31: I_{DD} vs. V_{DD} .

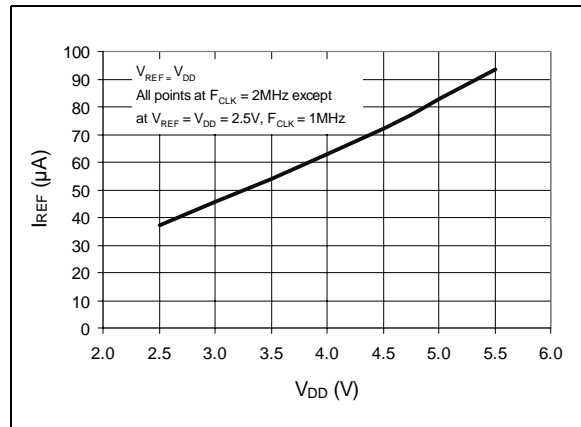


FIGURE 2-34: I_{REF} vs. V_{DD} .

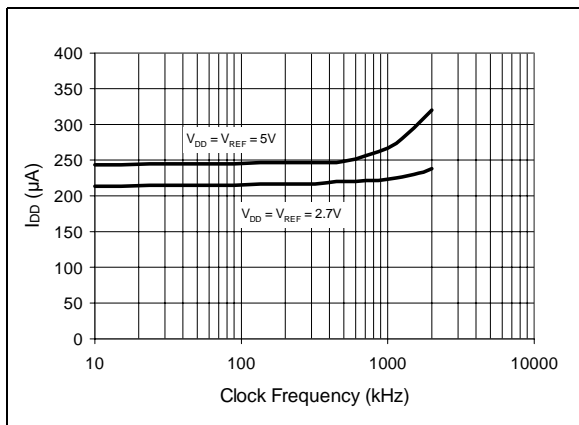


FIGURE 2-32: I_{DD} vs. Clock Frequency.

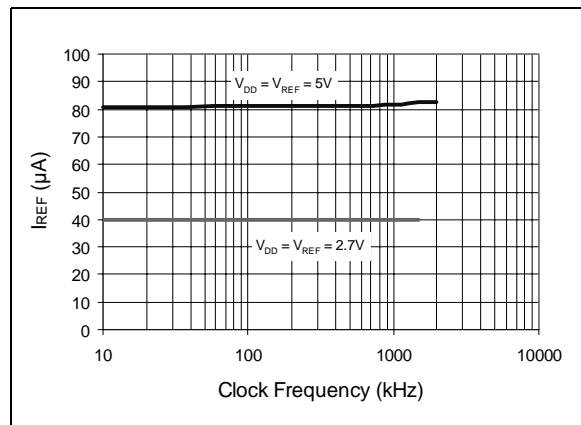


FIGURE 2-35: I_{REF} vs. Clock Frequency.

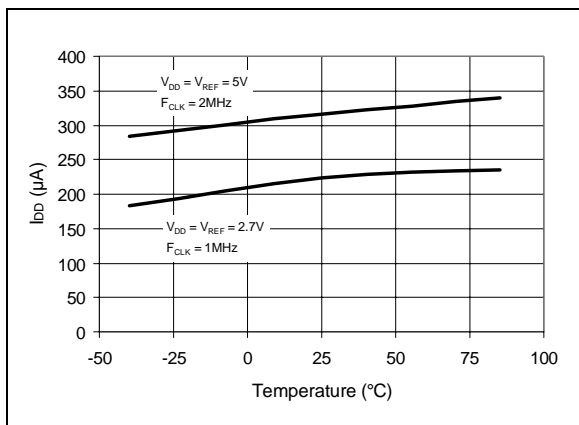


FIGURE 2-33: I_{DD} vs. Temperature.

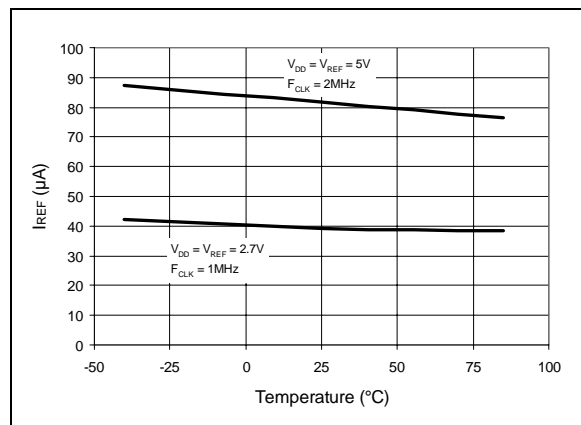


FIGURE 2-36: I_{REF} vs. Temperature.

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100ksp/s$, $f_{CLK} = 20 * f_{SAMPLE}$, $T_A = 25^\circ C$

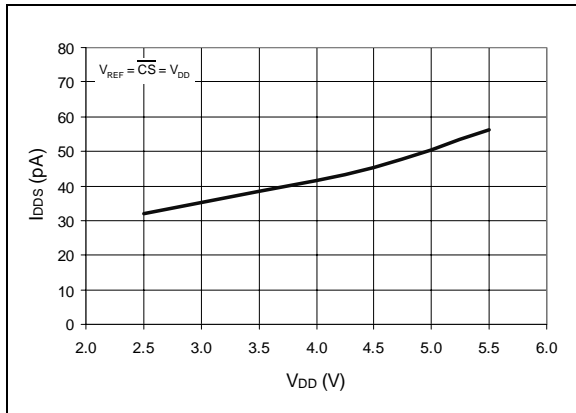


FIGURE 2-37: I_{DDS} vs. V_{DD} .

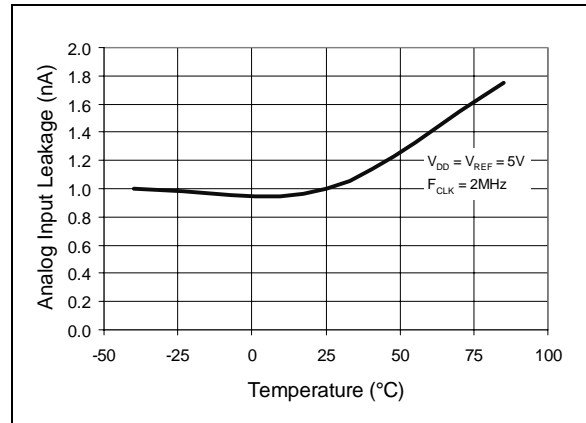


FIGURE 2-39: Analog Input Leakage Current vs. Temperature.

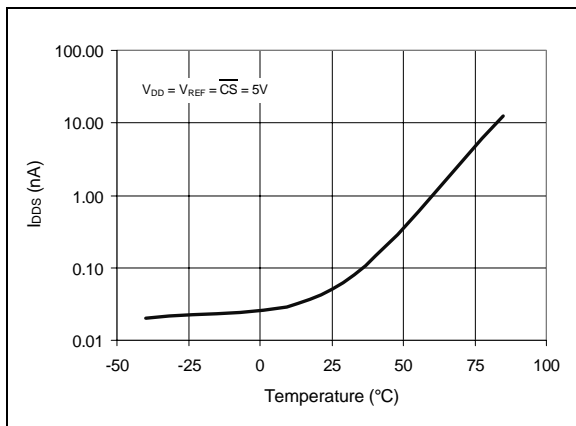


FIGURE 2-38: I_{DDS} vs. Temperature.

3.0 PIN DESCRIPTIONS

3.1 CH0 - CH7

Analog inputs for channels 0 - 7 respectively for the multiplexed inputs. Each pair of channels can be programmed to be used as two independent channels in single ended-mode or as a single pseudo-differential input where one channel is IN+ and one channel is IN-. See Section 4.1 and Section 5.0 for information on programming the channel configuration.

3.2 $\overline{\text{CS}}/\text{SHDN}$ (Chip Select/Shutdown)

The $\overline{\text{CS}}/\text{SHDN}$ pin is used to initiate communication with the device when pulled low and will end a conversion and put the device in low power standby when pulled high. The $\overline{\text{CS}}/\text{SHDN}$ pin must be pulled high between conversions.

3.3 CLK (Serial Clock)

The SPI clock pin is used to initiate a conversion and to clock out each bit of the conversion as it takes place. See Section 6.2 for constraints on clock speed.

3.4 DIN (Serial Data Input)

The SPI port serial data input pin is used to load channel configuration data into the device.

3.5 DOUT (Serial Data output)

The SPI serial data output pin is used to shift out the results of the A/D conversion. Data will always change on the falling edge of each clock as the conversion takes place.

3.6 AGND

Analog ground connection to internal analog circuitry.

3.7 DGND

Digital ground connection to internal digital circuitry.

4.0 DEVICE OPERATION

The MCP3204/3208 A/D Converters employ a conventional SAR architecture. With this architecture, a sample is acquired on an internal sample/hold capacitor for 1.5 clock cycles starting on the fourth rising edge of the serial clock after the start bit has been received. Following this sample time, the device uses the collected charge on the internal sample and hold capacitor to produce a serial 12-bit digital output code. Conversion rates of 100ksps are possible on the MCP3204/3208. See Section 6.2 for information on minimum clock rates. Communication with the device is done using a 4-wire SPI-compatible interface.

4.1 Analog Inputs

The MCP3204/3208 devices offer the choice of using the analog input channels configured as single-ended inputs or pseudo-differential pairs. The MCP3204 can be configured to provide two pseudo-differential input pairs or four single-ended inputs. The MCP3208 can be configured to provide four pseudo-differential input pairs or eight single-ended inputs. Configuration is done as part of the serial command before each conversion begins. When used in the pseudo-differential mode, each channel pair (i.e., CH0 and CH1, CH2 and CH3 etc.) are programmed as the IN+ and IN- inputs as part of the command string transmitted to the device. The IN+ input can range from IN- to ($V_{REF} + \text{IN-}$). The IN- input is limited to $\pm 100\text{mV}$ from the V_{SS} rail. The IN- input can be used to cancel small signal common-mode noise which is present on both the IN+ and IN- inputs.

When operating in the pseudo-differential mode, if the voltage level of IN+ is equal to or less than IN-, the resultant code will be 000h. If the voltage at IN+ is equal to or greater than $\{[V_{REF} + (\text{IN-})] - 1 \text{ LSB}\}$, then the output code will be FFFh. If the voltage level at IN- is more than 1 LSB below V_{SS} , then the voltage level at the IN+ input will have to go below V_{SS} to see the 000h output code. Conversely, if IN- is more than 1 LSB above V_{SS} , then the FFFh code will not be seen unless the IN+ input level goes above V_{REF} level.

For the A/D Converter to meet specification, the charge holding capacitor, (C_{SAMPLE}) must be given enough time to acquire a 12-bit accurate voltage level during the 1.5 clock cycle sampling period. The analog input model is shown in Figure 4-1.

In this diagram it is shown that the source impedance (R_S) adds to the internal sampling switch (R_{SS}) impedance, directly affecting the time that is required to charge the capacitor, C_{SAMPLE} . Consequently, larger source impedances increase the offset, gain, and integral linearity errors of the conversion. See Figure 4-2.

4.2 Reference Input

For each device in the family, the reference input (V_{REF}) determines the analog input voltage range. As the reference input is reduced, the LSB size is reduced accordingly. The theoretical digital output code produced by the A/D Converter is a function of the analog input signal and the reference input as shown below.

$$\text{Digital Output Code} = \frac{4096 * V_{IN}}{V_{REF}}$$

where:

V_{IN} = analog input voltage

V_{REF} = reference voltage

When using an external voltage reference device, the system designer should always refer to the manufacturer's recommendations for circuit layout. Any instability in the operation of the reference device will have a direct effect on the operation of the A/D Converter.

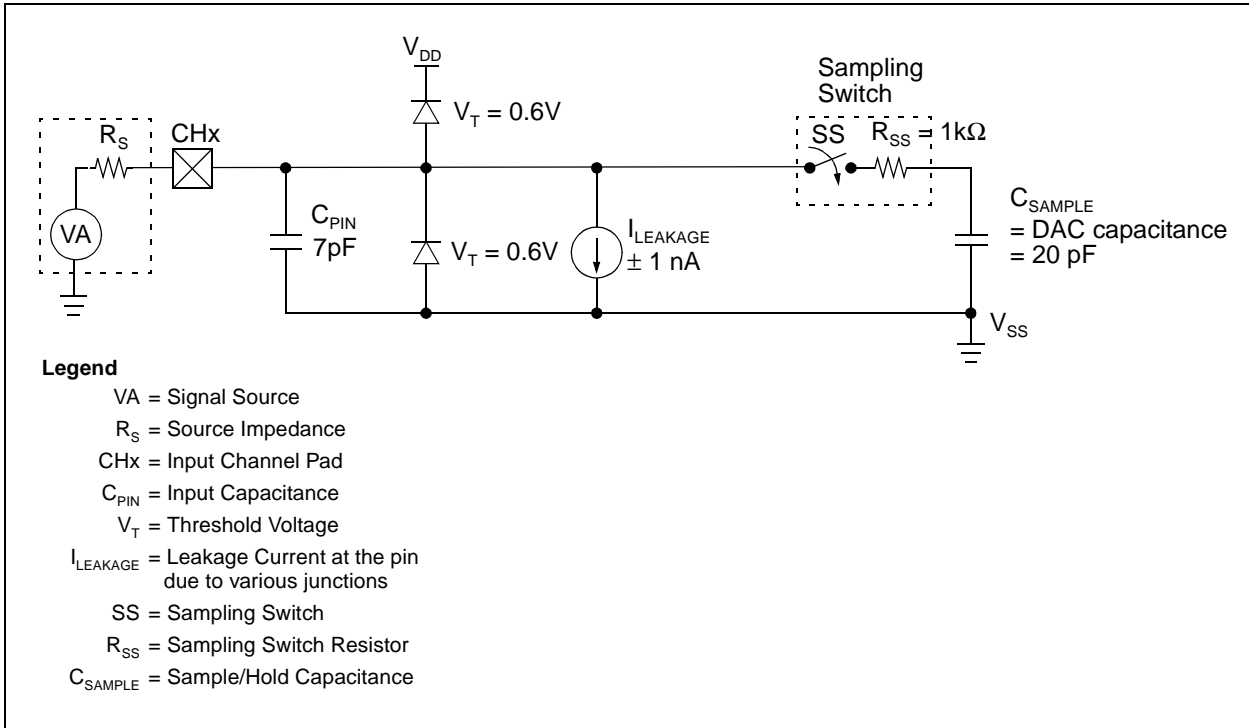


FIGURE 4-1: Analog Input Model

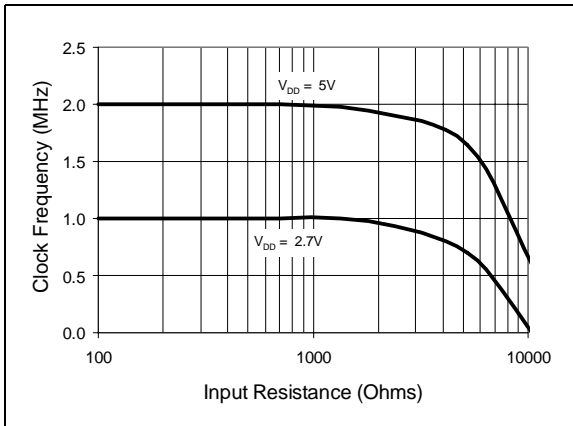


FIGURE 4-2: Maximum Clock Frequency vs. Input resistance (R_S) to maintain less than a 0.1LSB deviation in INL from nominal conditions.

5.0 SERIAL COMMUNICATIONS

Communication with the MCP3204/3208 devices is done using a standard SPI-compatible serial interface. Initiating communication with either device is done by bringing the \overline{CS} line low. See Figure 5-1. If the device was powered up with the \overline{CS} pin low, it must be brought high and back low to initiate communication. The first clock received with \overline{CS} low and D_{IN} high will constitute a start bit. The SGL/DIFF bit follows the start bit and will determine if the conversion will be done using single ended or differential input mode. The next three bits (D0, D1 and D2) are used to select the input channel configuration. Table 5-1 and Table 5-2 show the configuration bits for the MCP3204 and MCP3208, respectively. The device will begin to sample the analog input on the fourth rising edge of the clock after the start bit has been received. The sample period will end on the falling edge of the fifth clock following the start bit.

After the D0 bit is input, one more clock is required to complete the sample and hold period (D_{IN} is a don't care for this clock). On the falling edge of the next clock, the device will output a low null bit. The next 12 clocks will output the result of the conversion with MSB first as shown in Figure 5-1. Data is always output from the device on the falling edge of the clock. If all 12 data bits have been transmitted and the device continues to receive clocks while the \overline{CS} is held low, the device will output the conversion result LSB first as shown in Figure 5-2. If more clocks are provided to the device while \overline{CS} is still low (after the LSB first data has been transmitted), the device will clock out zeros indefinitely.

If necessary, it is possible to bring \overline{CS} low and clock in leading zeros on the D_{IN} line before the start bit. This is often done when dealing with microcontroller-based SPI ports that must send 8 bits at a time. Refer to Section 6.1 for more details on using the MCP3204/3208 devices with hardware SPI ports.

| CONTROL BIT SELECTIONS | | | | INPUT CONFIGURATION | CHANNEL SELECTION |
|------------------------|-----|----|----|---------------------|------------------------|
| SINGLE/DIFF | D2* | D1 | D0 | | |
| 1 | X | 0 | 0 | single ended | CH0 |
| 1 | X | 0 | 1 | single ended | CH1 |
| 1 | X | 1 | 0 | single ended | CH2 |
| 1 | X | 1 | 1 | single ended | CH3 |
| 0 | X | 0 | 0 | differential | CH0 = IN+ CH1 = IN- |
| 0 | X | 0 | 1 | differential | CH0 = IN- CH1 = IN+ |
| 0 | X | 1 | 0 | differential | CH2 = IN+ CH3 = IN- |
| 0 | X | 1 | 1 | differential | CH2 = IN- CH3 = IN+ |

*D2 is don't care for MCP3204

TABLE 5-1: Configuration Bits for the MCP3204.

| CONTROL BIT SELECTIONS | | | | INPUT CONFIGURATION | CHANNEL SELECTION |
|------------------------|----|----|----|---------------------|------------------------|
| SINGLE/DIFF | D2 | D1 | D0 | | |
| 1 | 0 | 0 | 0 | single ended | CH0 |
| 1 | 0 | 0 | 1 | single ended | CH1 |
| 1 | 0 | 1 | 0 | single ended | CH2 |
| 1 | 0 | 1 | 1 | single ended | CH3 |
| 1 | 1 | 0 | 0 | single ended | CH4 |
| 1 | 1 | 0 | 1 | single ended | CH5 |
| 1 | 1 | 1 | 0 | single ended | CH6 |
| 1 | 1 | 1 | 1 | single ended | CH7 |
| 0 | 0 | 0 | 0 | differential | CH0 = IN+ CH1 = IN- |
| 0 | 0 | 0 | 1 | differential | CH0 = IN- CH1 = IN+ |
| 0 | 0 | 1 | 0 | differential | CH2 = IN+ CH3 = IN- |
| 0 | 0 | 1 | 1 | differential | CH2 = IN- CH3 = IN+ |
| 0 | 1 | 0 | 0 | differential | CH4 = IN+ CH5 = IN- |
| 0 | 1 | 0 | 1 | differential | CH4 = IN- CH5 = IN+ |
| 0 | 1 | 1 | 0 | differential | CH6 = IN+ CH7 = IN- |
| 0 | 1 | 1 | 1 | differential | CH6 = IN- CH7 = IN+ |

TABLE 5-2: Configuration Bits for the MCP3208.

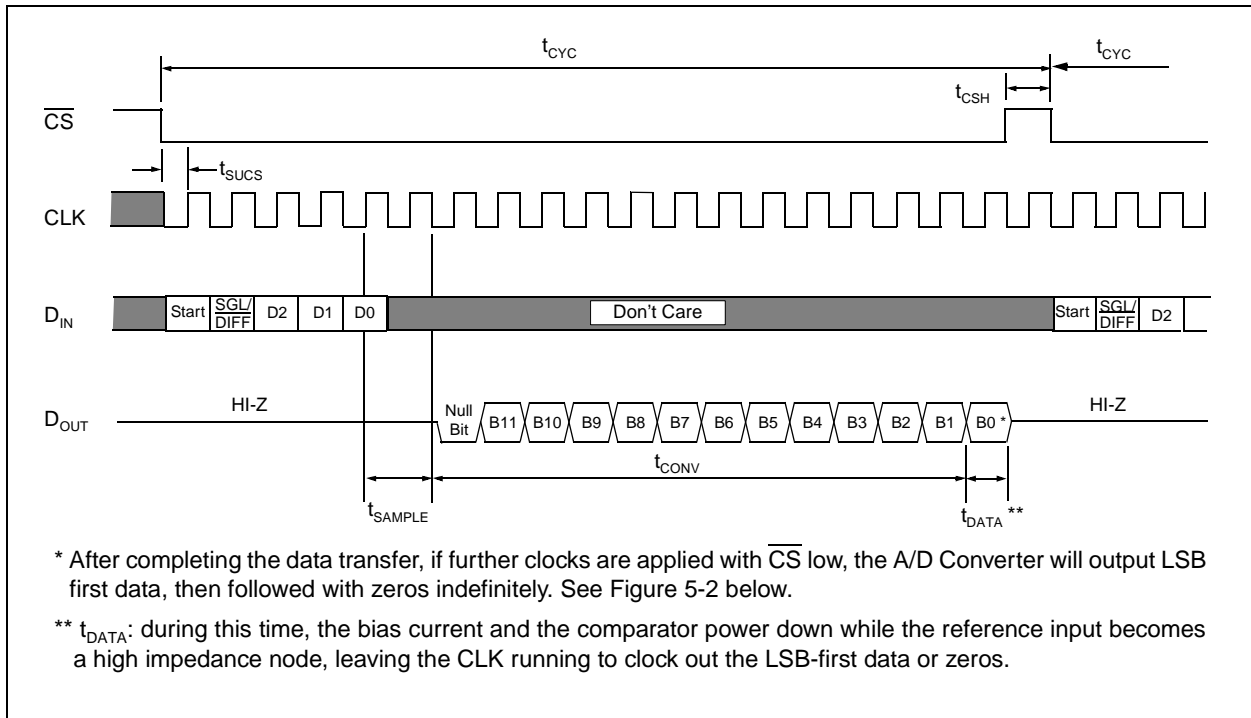


FIGURE 5-1: Communication with the MCP3204 or MCP3208.

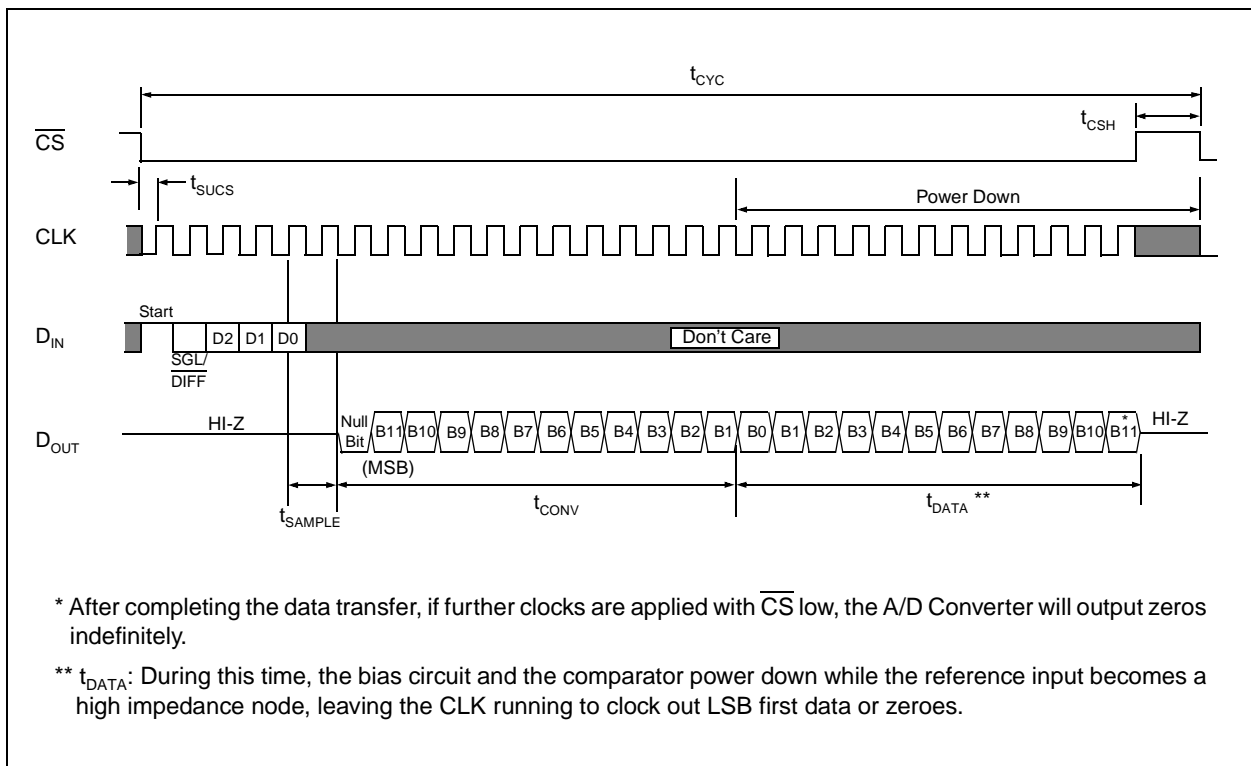


FIGURE 5-2: Communication with MCP3204 or MCP3208 in LSB First Format.

6.0 APPLICATIONS INFORMATION

6.1 Using the MCP3204/3208 with Microcontroller (MCU) SPI Ports

With most microcontroller SPI ports, it is required to send groups of eight bits. It is also required that the microcontroller SPI port be configured to clock out data on the falling edge of clock and latch data in on the rising edge. Because communication with the MCP3204/3208 devices may not need multiples of eight clocks, it will be necessary to provide more clocks than are required. This is usually done by sending 'leading zeros' before the start bit. As an example, Figure 6-1 and Figure 6-2 shows how the MCP3204/3208 can be interfaced to a MCU with a hardware SPI port. Figure 6-1 depicts the operation shown in SPI Mode 0,0 which requires that the SCLK from the MCU idles in the 'low' state, while Figure 6-2 shows the similar case of SPI Mode 1,1 where the clock idles in the 'high' state.

As shown in Figure 6-1, the first byte transmitted to the A/D Converter contains five leading zeros before the start bit. Arranging the leading zeros this way produces the output 12 bits to fall in positions easily manipulated by the MCU. The MSB is clocked out of the A/D Converter on the falling edge of clock number 12. After the second eight clocks have been sent to the device, the MCUs receive buffer will contain three unknown bits (the output is at high impedance for the first two clocks), the null bit and the highest order four bits of the conversion. After the third byte has been sent to the device, the receive register will contain the lowest order eight bits of the conversion results. Easier manipulation of the converted data can be obtained by using this method.

Figure 6-2 shows the same thing in SPI Mode 1,1 which requires that the clock idles in the high state. As with mode 0,0, the A/D Converter outputs data on the falling edge of the clock and the MCU latches data from the A/D Converter in on the rising edge of the clock.

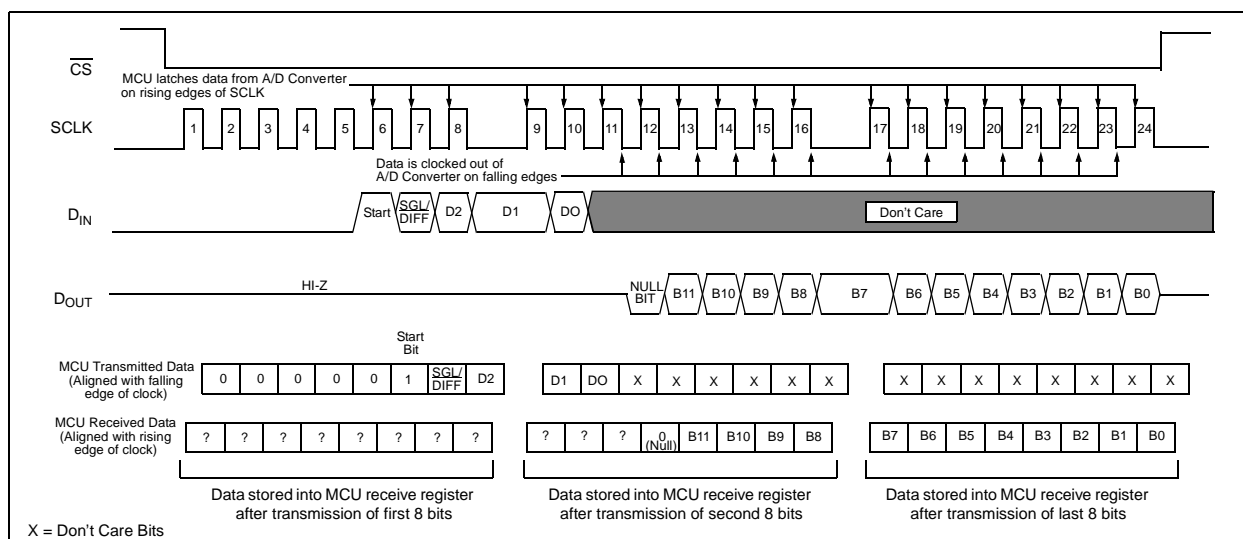


FIGURE 6-1: SPI Communication using 8-bit segments (Mode 0,0: SCLK idles low).

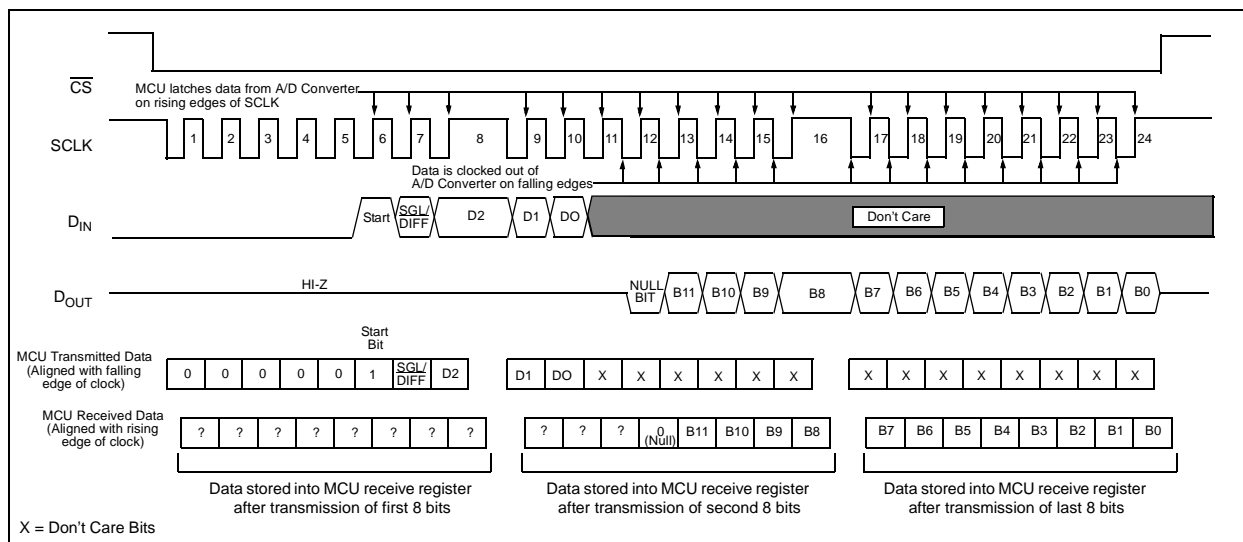


FIGURE 6-2: SPI Communication using 8-bit segments (Mode 1,1: SCLK idles high).

6.2 Maintaining Minimum Clock Speed

When the MCP3204/3208 initiates the sample period, charge is stored on the sample capacitor. When the sample period is complete, the device converts one bit for each clock that is received. It is important for the user to note that a slow clock rate will allow charge to bleed off the sample capacitor while the conversion is taking place. At 85°C (worst case condition), the part will maintain proper charge on the sample capacitor for at least 1.2ms after the sample period has ended. This means that the time between the end of the sample period and the time that all 12 data bits have been clocked out must not exceed 1.2ms (effective clock frequency of 10kHz). Failure to meet this criterion may induce linearity errors into the conversion outside the rated specifications. It should be noted that during the entire conversion cycle, the A/D Converter does not require a constant clock speed or duty cycle, as long as all timing specifications are met.

6.3 Buffering/Filtering the Analog Inputs

If the signal source for the A/D Converter is not a low impedance source, it will have to be buffered or inaccurate conversion results may occur. See Figure 4-2. It is also recommended that a filter be used to eliminate any signals that may be aliased back in to the conversion results. This is illustrated in Figure 6-3 where an op amp is used to drive the analog input of the MCP3204/3208. This amplifier provides a low impedance source for the converter input and a low pass filter, which eliminates unwanted high frequency noise.

Low pass (anti-aliasing) filters can be designed using Microchip's free interactive **FilterLab™** software. **FilterLab** will calculate capacitor and resistors values, as well as determine the number of poles that are required for the application. For more information on filtering signals, see the application note AN699 "Anti-Aliasing Analog Filters for Data Acquisition Systems."

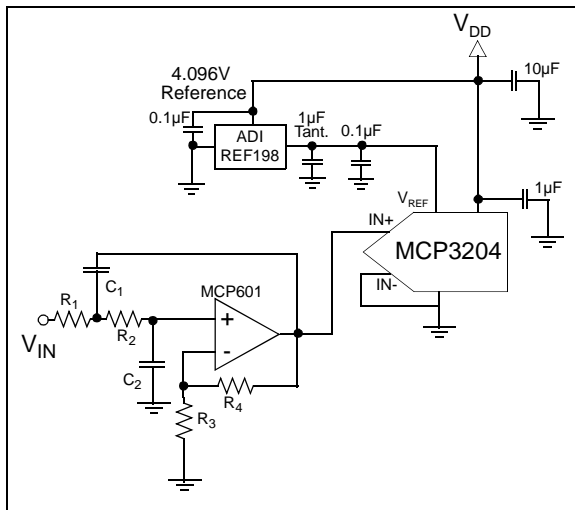


FIGURE 6-3: The MCP601 Operational Amplifier is used to implement a 2nd order anti-aliasing filter for the signal being converted by the MCP3204.

6.4 Layout Considerations

When laying out a printed circuit board for use with analog components, care should be taken to reduce noise wherever possible. A bypass capacitor should always be used with this device and should be placed as close as possible to the device pin. A bypass capacitor value of 1µF is recommended.

Digital and analog traces should be separated as much as possible on the board and no traces should run underneath the device or the bypass capacitor. Extra precautions should be taken to keep traces with high frequency signals (such as clock lines) as far as possible from analog traces.

Use of an analog ground plane is recommended in order to keep the ground potential the same for all devices on the board. Providing V_{DD} connections to devices in a "star" configuration can also reduce noise by eliminating return current paths and associated errors. See Figure 6-4. For more information on layout tips when using A/D Converters, refer to AN688 "Layout Tips for 12-Bit A/D Converter Applications".

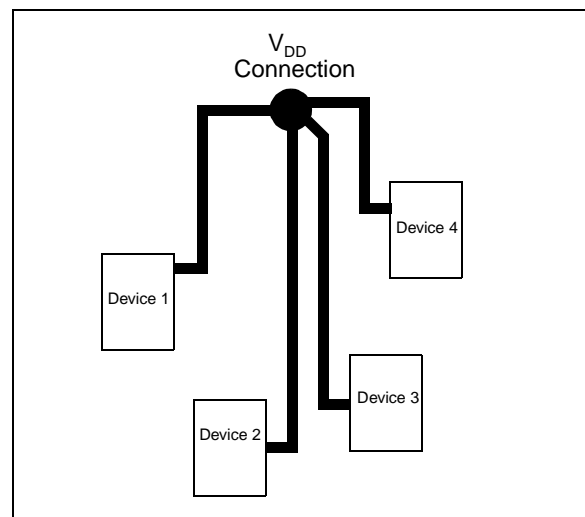


FIGURE 6-4: V_{DD} traces arranged in a 'Star' configuration in order to reduce errors caused by current return paths.

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MCP3204/3208

6.5 Utilizing the Digital and Analog Ground Pins

The MCP3204/3208 devices provide both digital and analog ground connections to provide another means of noise reduction. As shown in Figure 6-5, the analog and digital circuitry is separated internal to the device. This reduces noise from the digital portion of the device being coupled into the analog portion of the device. The two grounds are connected internally through the substrate which has a resistance of 5 -10 Ω .

If no ground plane is utilized, then both grounds must be connected to V_{SS} on the board. If a ground plane is available, both digital and analog ground pins should be connected to the analog ground plane. If both an analog and a digital ground plane are available, both the digital and the analog ground pins should be connected to the analog ground plane. Following these steps will reduce the amount of digital noise from the rest of the board being coupled into the A/D Converter.

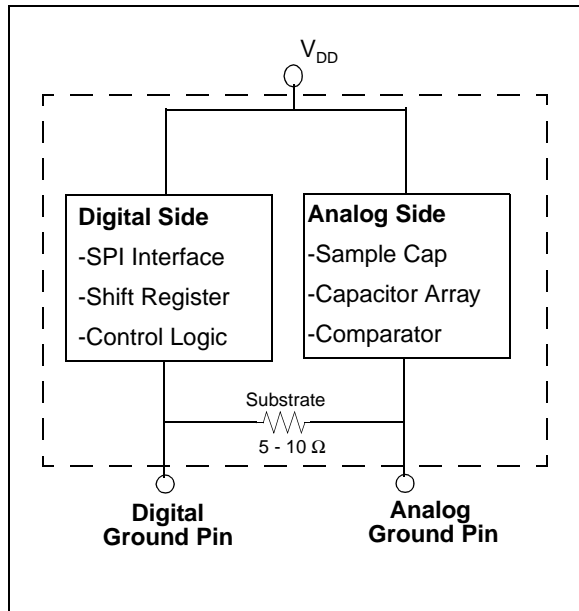
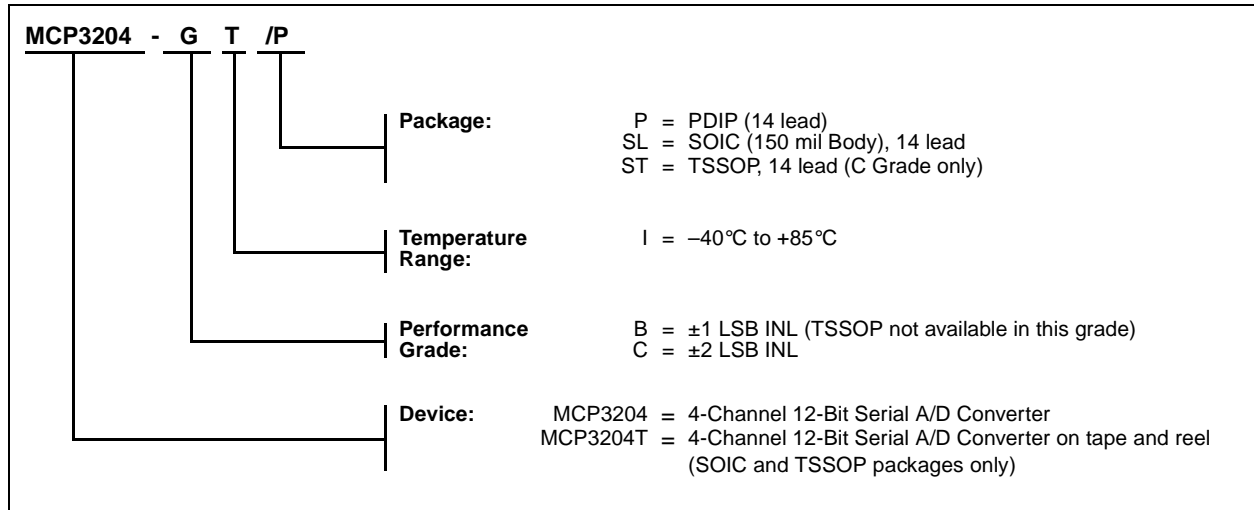


FIGURE 6-5: Separation of Analog and Digital Ground Pins.

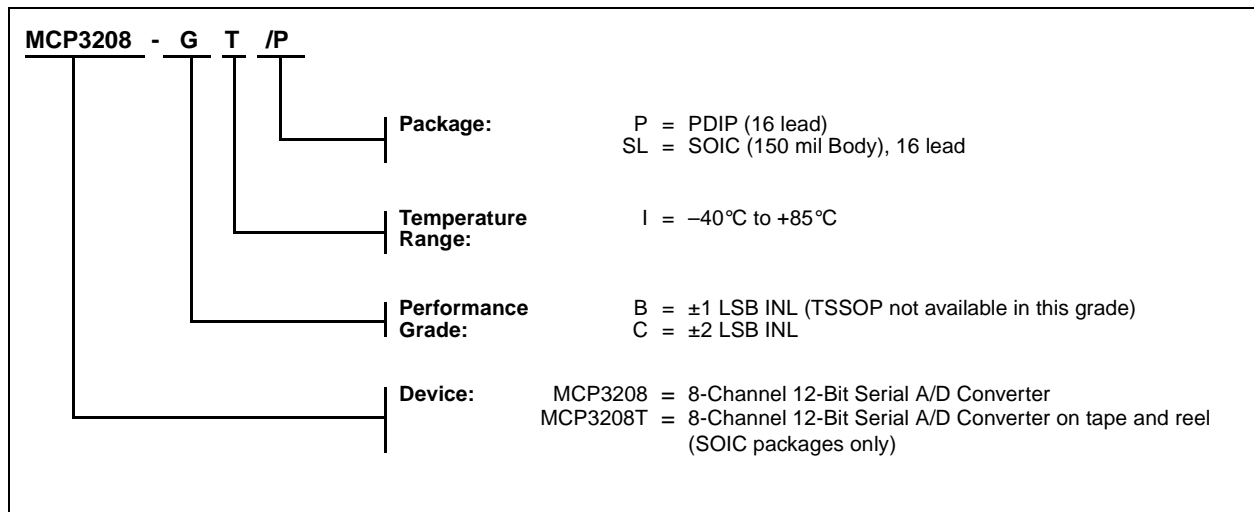
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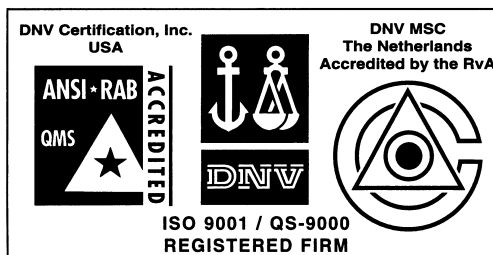
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