SERIAL BACKPLANE RETIMER DEVICE S2092

FEATURES

- On-chip high frequency PLL with internal loop filter for clock recovery
- Internal 100 Ω line-to-line termination on high speed differential input
- Supports data recovery from:
  2.488 to 2.67 Gbps (2.488 Gbps with FEC overhead data rate capability)
- Selectable reference frequencies
- Lock detect—monitors frequency of incoming data
- Low-jitter serial CML interface
- Single +3.3 V supply, 455 mW power dissipation (typ)
- Compact 7 mm x 7 mm 48 pin TQFP/TEP package

APPLICATIONS

- Dense Wavelength Division Multiplexing (DWDM) systems
- Serial Backplane interfaces
- 2.488 Gbps to 2.67 Gbps Short Haul Retiming
- Crosspoint interfaces

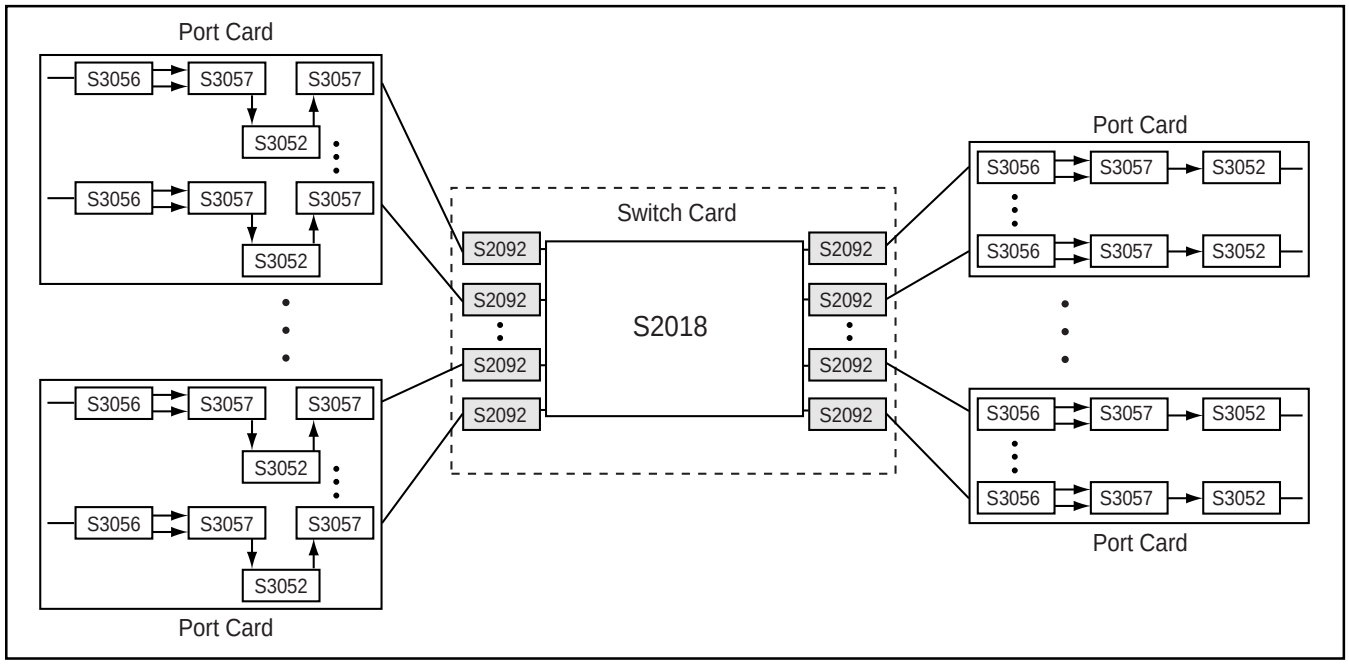
GENERAL DESCRIPTION

The function of the S2092 retimer device is to derive high speed timing signals for DWDM equipment. The S2092 is implemented using AMCC's proven Phase Lock Loop (PLL) technology. Figure 1 shows a typical network application.

The S2092 can receive a 2.488 Gbps to 2.67 Gbps scrambled NRZ signal. This range is dependent on the user's FEC needs and reference frequency selection. The S2092 recovers the clock from the data and outputs the retimed data.

The S2092 utilizes an on-chip PLL which consists of a phase detector, a loop filter, and a Voltage Controlled Oscillator (VCO). The phase detector compares the phase relationship between the VCO output and the serial data input. A loop filter converts the phase detector output into a smooth DC voltage, and the DC voltage is input to the VCO whose frequency is varied by this voltage. A block diagram is shown in Figure 2.

Figure 1. System Block Diagram



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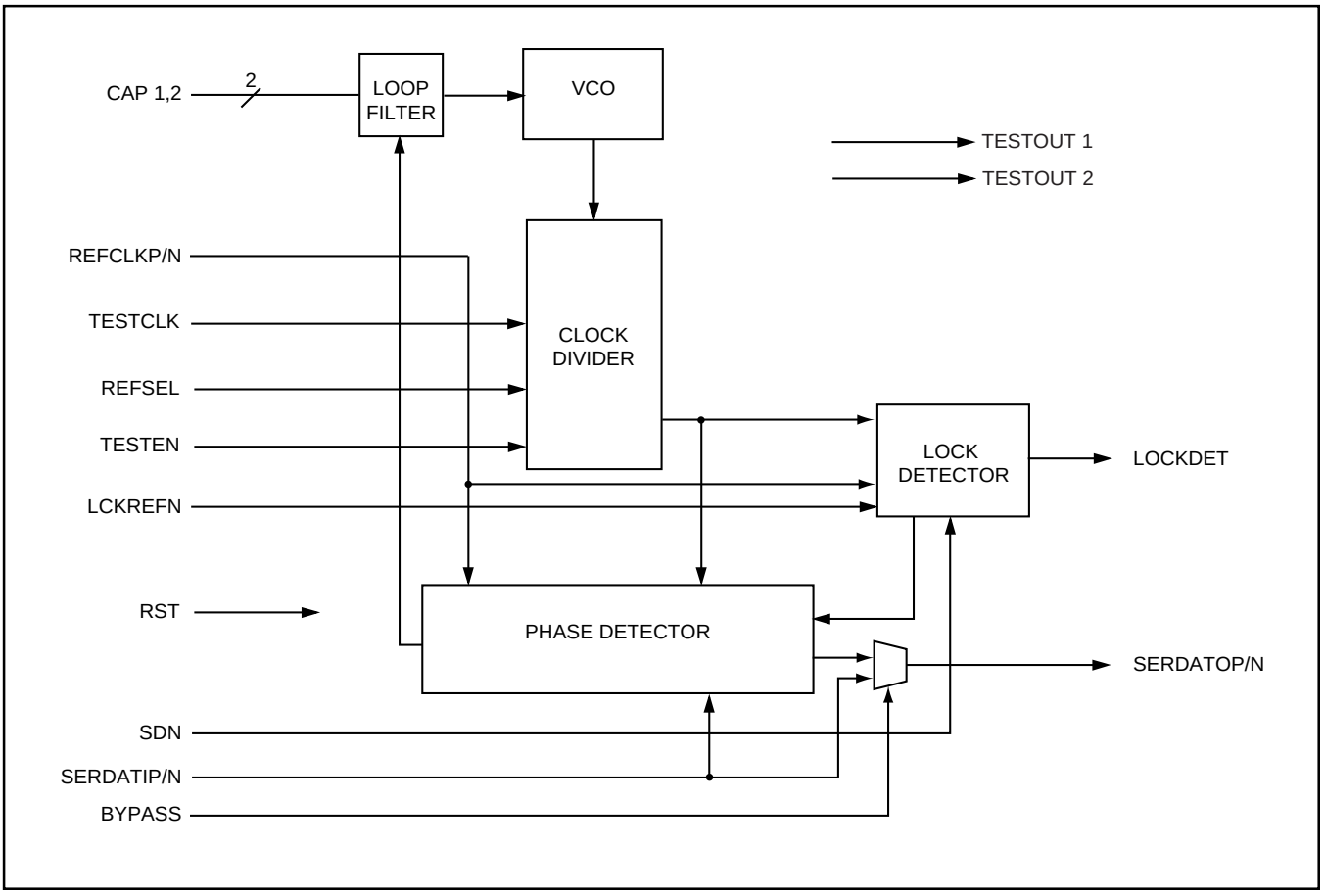
S2092 OVERVIEW

The S2092 supports clock recovery from 2.488 Gbps to 2.67 Gbps data rate. Differential serial data is input to the chip at the specified rate, and clock recovery is performed on the incoming data stream. An external oscillator is required to minimize the PLL lock time. Retimed data is output from the S2092.

Suggested Interface Devices

AMCC	S2018	17 x 17 3.2 Gbps Crosspoint Switch
AMCC	S3083	OC-48 16:1Transmitter
AMCC	S3063	OC-48 Differential 16:1 Transmitter
AMCC	S3044	OC-48 1:16 Receiver
AMCC	S3057	Multi-Rate SONET/SDH/ATM Transceiver
AMCC	S3067	Multi-Rate SONET/SDH/ATM Transceiver w/FEC
AMCC	S3056	Mulit-Rate Clock and Data Recovery Unit
AMCC	S3052	Mulit-Rate Performance Monitor

Figure 2. S2092 Functional Block Diagram



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S2092 FUNCTIONAL DESCRIPTION

The S2092 retimer device performs clock recovery function from 2.488 Gbps to 2.67 Gbps serial data links. The chip extracts the clock from the serial data inputs and provides retimed data outputs. A 155.52 to 166.63 or 19.44 to 20.83 MHz reference clock is required (REFCLK frequency is dependent on which FEC capability is required. See Table 2 for the number of bytes per 255 byte block to set the proper reference frequency.) for phase lock loop start up and proper operation under loss of signal conditions. An integral prescaler and phase lock loop circuit is used to multiply this reference to the nominal bit rate.

Data Retiming

Data retiming, as shown in the block diagram in Figure 2, generates a clock that is at the same frequency as the incoming data bit rate at the serial data input. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

Frequency stability without incoming data is guaranteed by an alternate reference input (REFCLK) that the PLL locks onto when data is lost. If the frequency of the incoming signal varies by a value greater than that stated in Table 7 with respect to REFCLKP/N, the PLL will be declared out of lock, and the PLL will lock to the reference clock. The assertion of SDN will also cause an out of lock condition.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density in a received data signal.

Lock Detect

The S2092 contains a lock detect circuit which monitors the integrity of the serial data inputs. If the received serial data fails the frequency test, the PLL will be forced to lock to the local reference clock. This will maintain the correct frequency of the recovered clock output under loss of signal or loss of lock conditions. If the recovered clock frequency deviates from the local reference clock frequency by more than that stated in Table 7, the PLL will be declared out of lock. The lock detect circuit will poll the input data stream in an attempt to reacquire lock to data. If the recovered clock frequency is determined to be within that range stated in Table 7, the PLL will be declared in lock and the lock detect output will go active. The assertion of SDN will also cause an out of lock condition.

Table 1. Reference Frequency Select

REFSEL	Reference Frequency
0	19.44 to 20.83 MHz
1	155.52 to 166.63 MHz

Table 2. FEC Modes

REFSEL	Reference Frequency for Data Rates with FEC Capability of X bytes per 255–Byte Block						
	X = 0	X = 3	X = 4	X = 5	X = 6	X = 7	X = 8
0	19.44 MHz	19.99 MHz	20.15 MHz	20.31 MHz	20.48 MHz	20.65 MHz	20.83 MHz
1	155.52 MHz	159.91MHz	161.21 MHz	162.53 MHz	163.87 MHz	165.26 MHz	166.63 MHz

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CHARACTERISTICS

Input Jitter Tolerance

Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1 dB optical/electrical power penalty. See Figure 3.

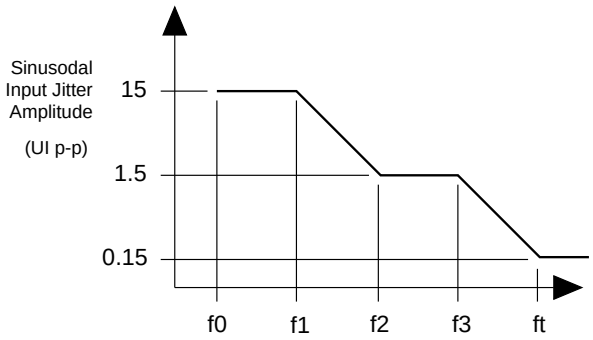
Jitter Transfer

The jitter transfer function is defined as the ratio of jitter on the output signal to the jitter applied on the input signal versus frequency. Jitter transfer requirements are shown in Figure 4. The measurement condition is that input sinusoidal jitter up to the mask level in Figure 4 be applied.

Jitter Generation

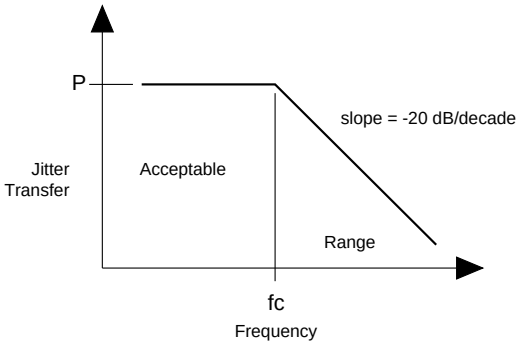
The jitter of the serial data outputs shall not exceed the value specified in Table 7. The conditions are stated with a serial data input with no jitter presented on SERDATIP/N. (See Table 7).

Figure 3. Input Jitter Tolerance Specification



Data Rate	f0 (Hz)	f1 (Hz)	f2 (Hz)	f3 (kHz)	ft (kHz)
2.488 Gbps	10	600	6000	100	1000

Figure 4. Jitter Transfer Specification



Data Rate	fc (kHz)	P (dB)
2.488 Gbps	2000	0.1

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Table 3. Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin#	Description
SERDATIP SERDATIN	Diff. CML	I	3 2	Serial Data In. Clock is recovered from the transitions on these inputs. Internally biased and terminated. (See Figure 8.)
BYPASS	LVTTL	I	46	Active High. Used to bypass the PLL. It allows transmission of the data input without clock recovery.
SDN	Single Ended LVPECL	I	45	Signal Detect. Active Low. A single-ended 10K PECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDN is inactive, the data on the Serial Data In (SERDATIP/N) pins will be internally forced to a constant zero and the PLL will be forced to lock to the REFCLK input. When SDN is active, data on the SERDATIP/N pins will be processed normally.
REFCLKP REFCLKN	Internally Biased Diff. LVPECL	I	6 7	Reference Clock. 155.52 to 166.63 or 19.44 to 20.83 MHz (see Tables 1 and 2 for additional reference clock frequencies) input used to establish the initial operating frequency of the clock recovery PLL and also used as a standby clock in the absence of data, during reset, or when SDN is inactive. Internally biased.
CAP1 CAP2		I	40 39	Loop Filter Capacitor. The external loop filter capacitor and resistors are connected to these pins. (See Figure 11.)
LCKREFN	LVTTL	I	17	Lock to Reference. Active Low. When active, the serial data output will be invalid.
TESTCLK	LVTTL	I	15	Test input signal used for production test. Leave open (no DC connection) for normal operation.
REFSEL	LVTTL	I	18	Selects the reference frequency (See Tables 1 and 2.)
RST	LVTTL	I	16	Active High. Resets lock detect circuit and VCO divide-by-N circuit for production test.
TESTEN	LVTTL	I	47	Test Enable. Active High. Bypasses the VCO for production test. Tie Low for normal operation.
SERDATOP SERDATON	Diff. CML	O	28 27	Serial Data Out. This signal is the delayed version of the incoming data stream (SERDATI).
LOCKDET	LVTTL	O	10	Lock Detect. Clock recovery indicator. Set High when the internal clock recovery has locked onto the incoming data stream. LOCKDET is an asynchronous output.
TESTOUT1		O	23	Test Output. Leave open (no DC connection) for normal operation.
TESTOUT2		O	33	Test Output. Leave open (no DC connection) for normal operation.
TESTMODE1	LVTTL	I	19	Test Mode Control. Keep High for normal operation.
TESTMODE2	LVTTL	I	20	Test Mode Control. Keep High for normal operation.

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Table 3. Pin Assignment and Descriptions (Continued)

Pin Name	Qty.	Pin#	Description
AVCC	2	37, 42	+3.3 V Analog power supply.
AGND	3	38, 41, 43	Analog GND connection.
VCC	8	1, 5, 9, 21, 24, 26, 29, 48	+3.3 V Power Supply.
GND	12	4, 8, 11, 12, 13, 14, 22, 25, 30, 31, 36, 44	Ground connection.
DNC	3	32, 34, 35	Do not connect. Used as test pins.

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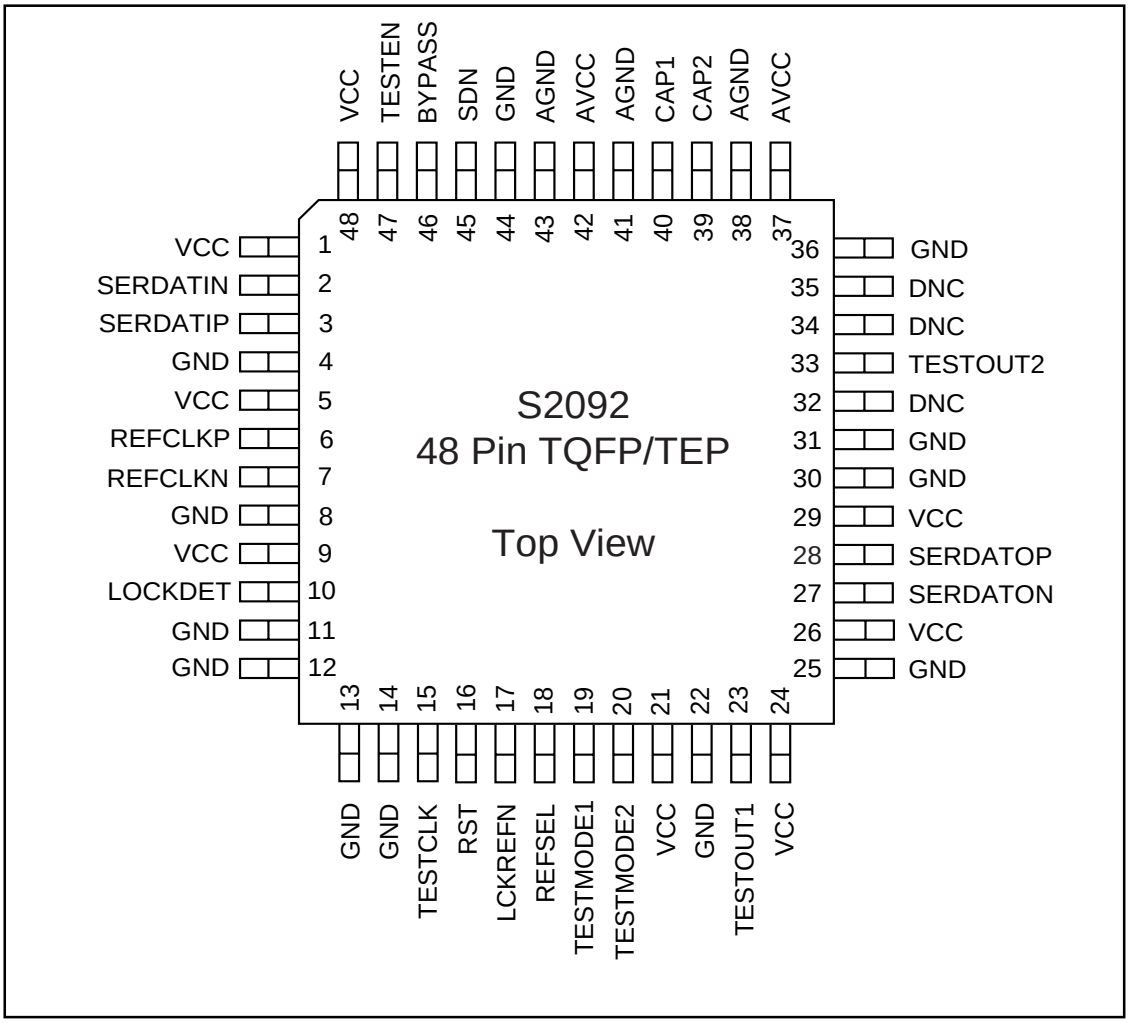
Figure 5. S2092 Pinout



Note: DNC used as test pins.

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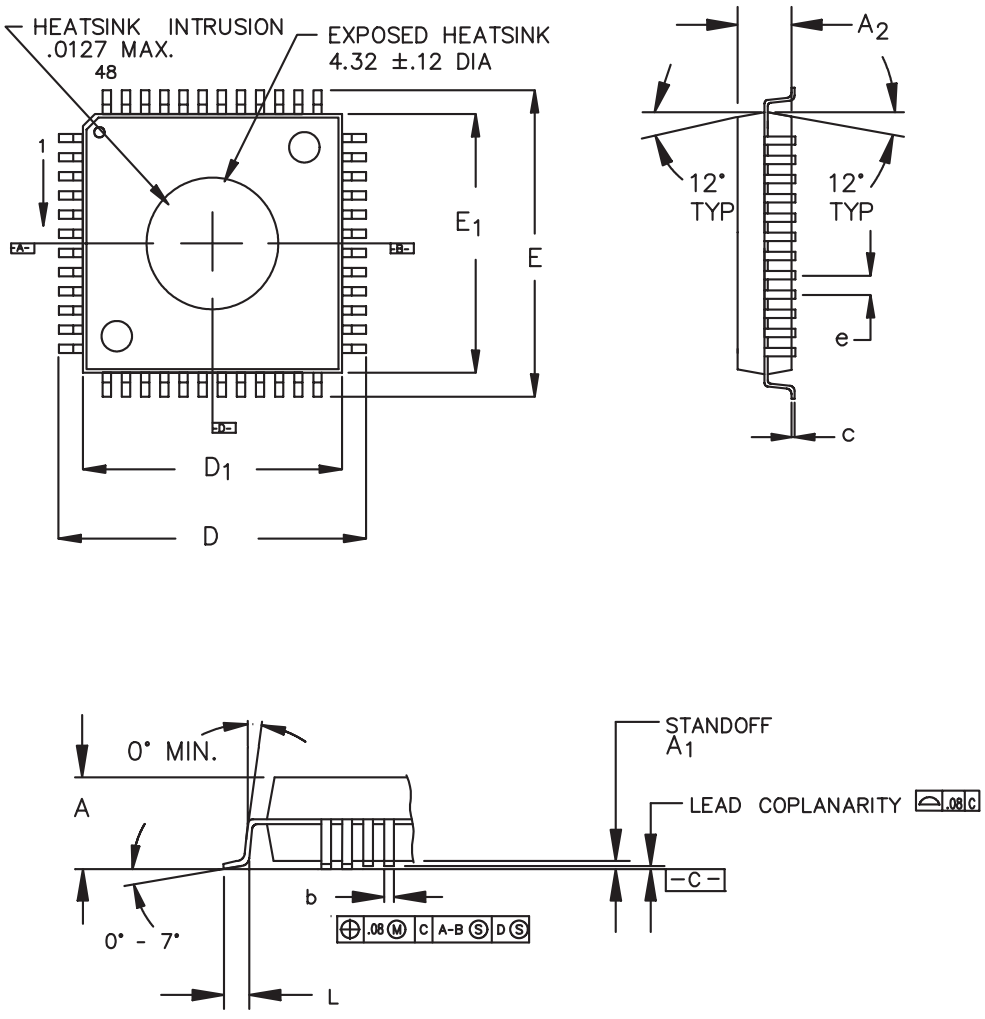
Figure 6. Compact 7 mm x 7 mm 48 Pin TQFP/TEP Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.05	1.35	8.80	6.90	8.80	6.90	0.75	0.50 BSC.	0.17	
NOM			1.40	9.00	7.00	9.00	7.00	0.60		0.22	1.27
MAX	1.60	0.15	1.45	9.20	7.10	9.20	7.10	0.50		0.27	

Thermal Management

Max Package Power	Θja
650 mW	50° C/W

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Table 4. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		+150	˚C
Voltage on V_{CC} with respect to GND	-0.5		3.47	V
Voltage on any LVTTL Input Pin	-0.5		V_{CC}	V
Voltage on any LVPECL Input Pin	0		V_{CC}	V
LVTTL Output Sink Current			1	mA
LVTTL Output Source Current			1	mA

Electrostatic Discharge (ESD) Ratings
The S2092 is rated to the following ESD voltages based on the human body model:
1. All pins are rated at 1500 V except pins 24, 37, 38, 41, 42, and 43.
2. Pins 24, 37, 38, 41, 42, and 43 are rated at 100 V.

Table 5. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias (Industrial)	-40		+85	˚C
Voltage on V_{CC} with respect to GND	3.13	3.3	3.47	V
Voltage on any LVTTL Input Pin	0		V_{CC}	V
Voltage on any LVPECL Input Pin	0		V_{CC}	V

Table 6. Reference Clock Requirements

Parameter	Description	Min	Typ	Max	Units	Conditions
FT	Frequency Tolerance	-100		+100	ppm	
TD_{1-2}	Symmetry	40		60	%	Duty cycle at 50% point
T_{RCR}, T_{RCF}	REFCLK Rise and Fall Time			1.5	ns	20% to 80%

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Table 7. Serial Data Timing, Input (SERDATIP/N), Output (SERDATOP/N)

Parameter	Description	Min	Typ	Max	Units	Conditions
VCO Operating Frequency		2.125	2.488	2.67	GHz	
T_{LOCK}	Data Acquisition Lock Time 19.44 to 20.83 MHz REFCLK			1800	µsec	Minimum transition density of 20%. Guaranteed but not tested. With device powered up and valid REFCLK.
	155.52 to 166.63 MHz REFCLK			250	µsec	
Input Jitter Tolerance	Serial Data Input Total Jitter Tolerance at 2.488 Gbps	0.4	0.5		UI	1 MHz < f < 5 MHz Data pattern = 2^7–1 PRBS
Data Output Jitter	VCO Locked to SERDATIP/N at 2.488 Gbps		0.0038	0.006	UI (rms)	1 MHz < f < 5 MHz Data pattern = 2^7–1 PRBS. With no jitter on serial data inputs.
R_{SR}, R_{SF}	Serial Data Output Rise and Fall Time		60	120	ps	20% to 80%, 50 Ω load, 1 pf cap.
PLL Specification	Frequency difference at which the receive PLL goes out of lock (REFCLK compared to the divided down VCO clock)	450	600	770	ppm	
PLL Specification	Frequency difference at which the receive PLL goes into lock (REFCLK compared to the divided down VCO clock)	220	300	390	ppm	

Table 8. CML Input DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
ΔV_{INDIFF}	Differential Input Voltage Swing	100		1900	mV	See Figure 7.
$\Delta V_{INSINGLE}$	Single-ended Input Voltage Swing	50		950	mV	See Figure 7.
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	

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Table 9. CML Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Condition
V_{OL}	CML Output Low Voltage	V_{CC} -1.0		V_{CC} -0.65	V	100 Ω line-to-line.
V_{OH}	CML Output High Voltage	V_{CC} -0.35		V_{CC} -0.2	V	100 Ω line-to-line.
$\Delta V_{OUTDIFF}$	CML Serial Output Differential Voltage Swing	800		1600	mV	100 Ω line-to-line. See Figure 7.
$\Delta V_{OUTSINGLE}$	CML Serial Output Single-ended Voltage Swing	400		800	mV	100 Ω line-to-line. See Figure 7.
R_O	Single Ended Output Resistance	40	50	60	Ω	

Table 10. LVTTL, LVPECL DC Characteristics

Parameter	Description	Min	Typ	Max	Unit	Conditions
V_{IH}	Input High Voltage (LVTLL)	2.0		3.47	V	TTL V_{CC} = Max
V_{IL}	Input Low Voltage (LVTTL)	0.0		0.8	V	TTL V_{CC} = Max
I_{IH}	Input High Current (LVTTL)			50	µA	V_{IN} = 2.4 V
I_{IL}	Input Low Current (LVTTL)	-500			µA	V_{IN} = 0.5 V
V_{OH}	Output High Voltage (LVTTL)	2.4			V	V_{IH} = Min. V_{IL} = Max. I_{OH} = -100 µA
V_{OL}	Output Low Voltage (LVTTL)			0.5	V	V_{IH} = Min. V_{IL} = Max. I_{OL} = 1 mA
V_{IL}	Input Low Voltage (LVPECL)	V_{CC} -2.0		V_{CC} -1.4	V	
V_{IH}	Input High Voltage (LVPECL)	V_{CC} -1.2		V_{CC} -0.5	V	
I_{IL}	Input Low Current (LVPECL)	-100		0	µA	
I_{IH}	Input High Current (LVPECL)	50		350	µA	
I_{CC}	Supply Current		138	187	mA	Outputs open.
P_D	Power Dissipation		455	650	mW	

Note: All parameters are specified with respect to the source termination and ground with V_{TTL} = Max. = 3.47 V.

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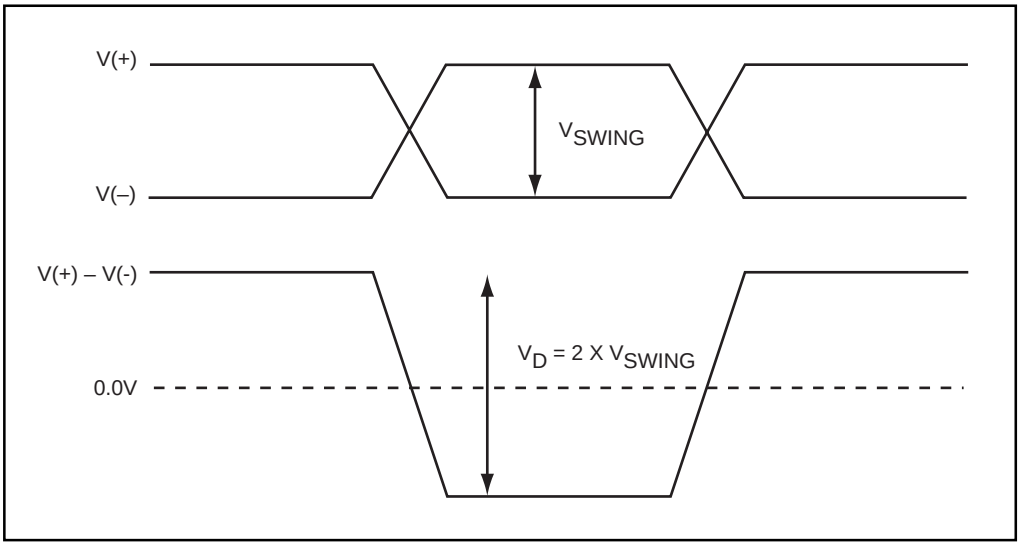
Table 11. Internally Biased Differential LVPECL Input Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IL}	Input Low Voltage	V_{CC} -2.0		V_{CC} -1.4	V	
V_{IH}	Input High Voltage	V_{CC} -1.2		V_{CC} -0.5	V	
I_{IL}	Input Low Current	-300		0	µA	$V_{IL} = V_{CC}$ -2
I_{IH}	Input High Current	-50		100	µA	$V_{IH} = V_{CC}$ -0.5
ΔV_{INDIFF}	Differential Input Voltage Swing	300		1200	mV	See Figure 7.
$\Delta V_{INSINGLE}$	Single-ended Input Voltage Swing	150		600	mV	See Figure 7.

Figure 7. Differential Voltage Measurement



Note: V(+) – V(-) is the algebraic difference of the input signals.

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Figure 8. +5 V Differential PECL Driver to S2092 Input AC Coupled Termination

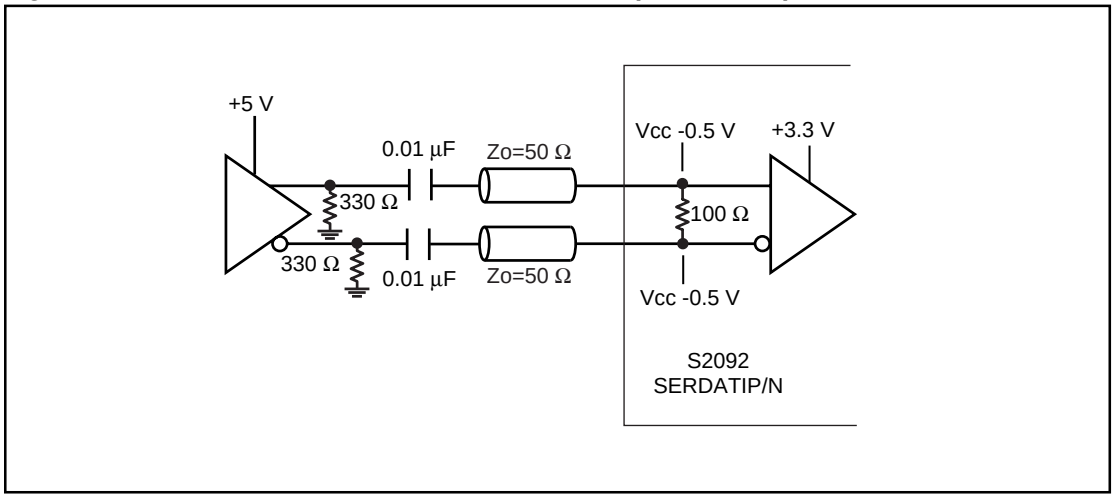

Figure 9. +5 V Differential PECL Driver to S2092 Reference Clock Input AC Coupled Termination

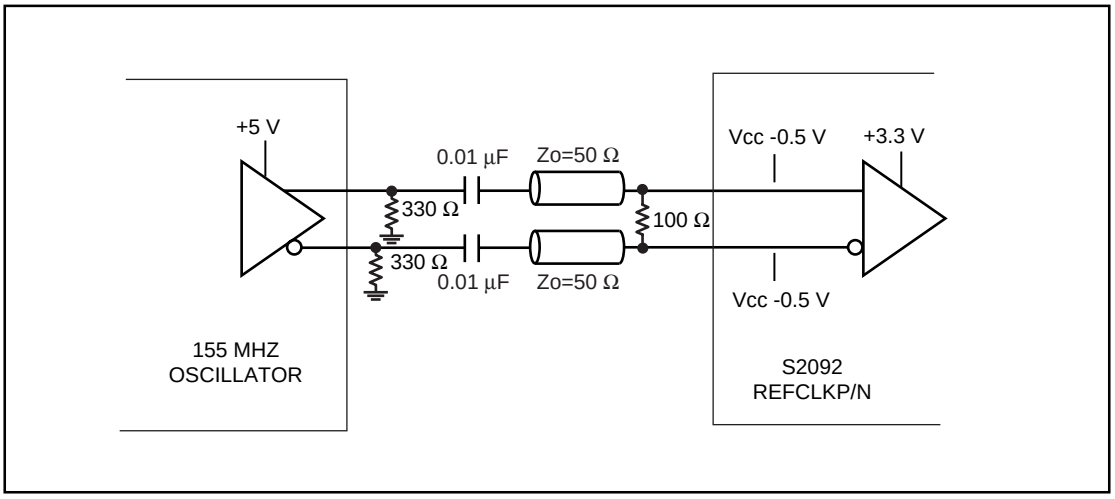

Figure 10. +3.3 V Differential LVPECL Driver to S2092 Reference Clock Input DC Coupled Termination

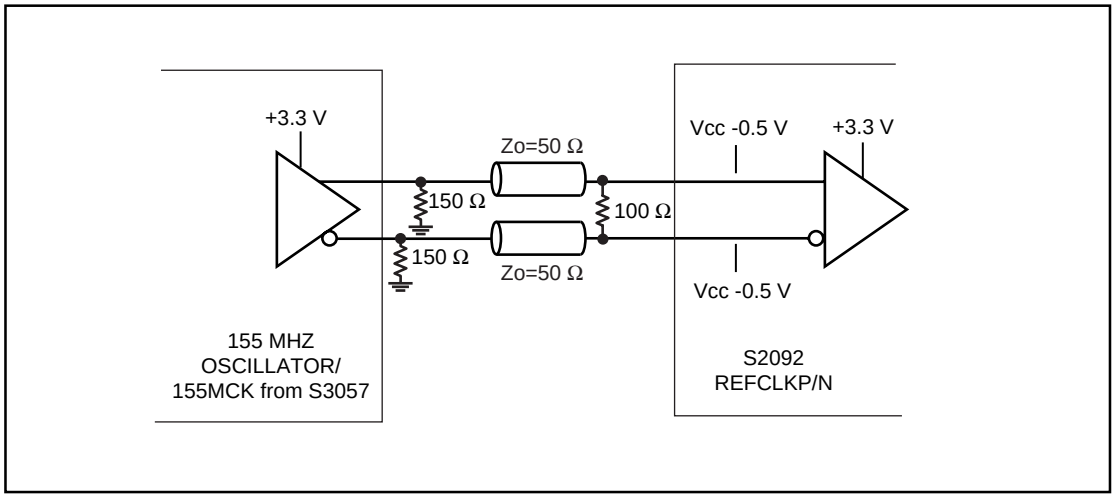

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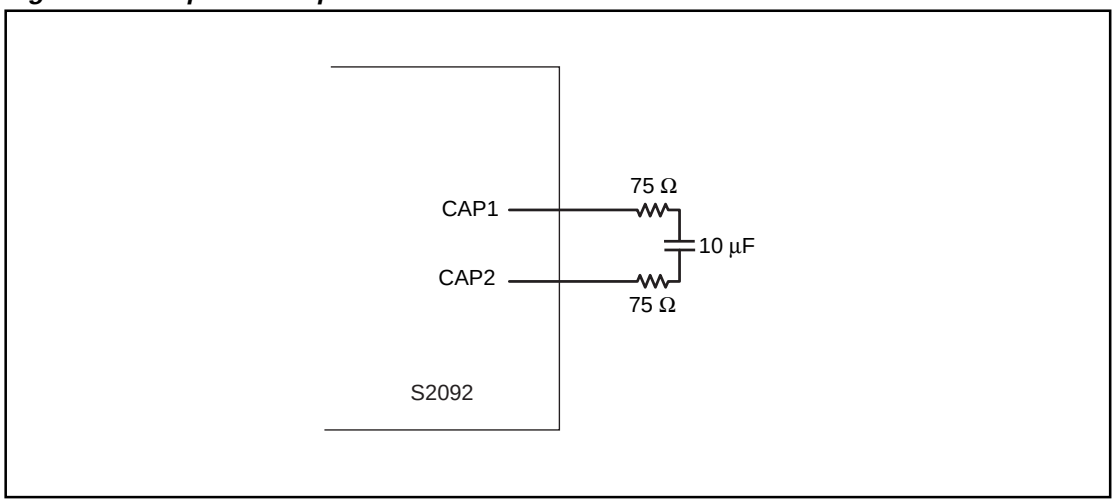
Figure 11. Loop Filter Capacitor Connections



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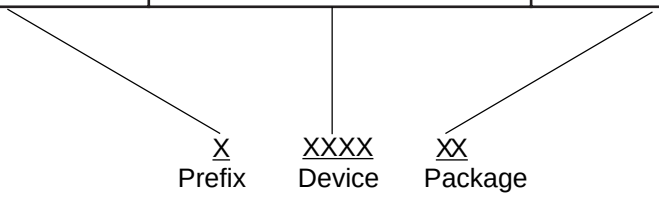
Ordering Information

PREFIX	DEVICE	PACKAGE
S – Integrated Circuit	2092	TT – 48 Pin TQFP/TEP



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