FIBRE CHANNEL/GIGABIT ETHERNET TRANSCEIVER S2070

FEATURES

- 1062 Mbps (Fibre Channel) line rates
- 1250 Mbps (Gigabit Ethernet) line rates
- Half and full VCO output rates
- Functionally compliant to IEEE 802.3z Gigabit Ethernet Specification and the ANSI X3T11 Fibre Channel Specification
- Transmitter incorporating phase-locked loop (PLL) clock synthesis from low speed reference
- Receiver PLL provides clock and data recovery
- 10-bit parallel TTL compatible interface
- Low-jitter serial LVPECL compatible interface
- Local loopback
- Single +3.3 V supply, 620 mW power dissipation
- 64 PQFP package
- Continuous downstream clocking from receiver
- Drives 30 m of Twinax cable directly

APPLICATIONS

- Workstation
- Frame buffer
- Switched networks
- Data broadcast environments
- Proprietary extended backplanes

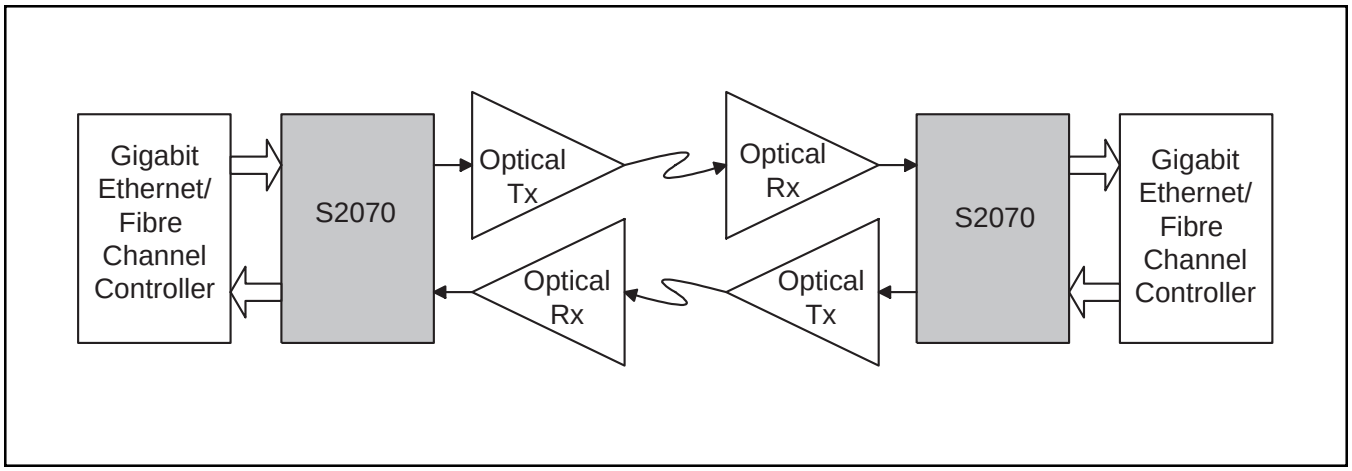
GENERAL DESCRIPTION

The S2070 transmitter and receiver chip facilitates high speed serial transmission of data over fiber optic, coax, or twinax interfaces. The device conforms to the requirements of the IEEE 802.3z Gigabit Ethernet Specification and the ANSI X3T11 Fibre Channel specification, and runs at 1062 Mbps or 1250 Mbps data rates with an associated 10-bit data word.

The chip provides parallel-to-serial and serial-to-parallel conversion, clock generation/recovery, and framing for block encoded data. The on-chip transmit PLL synthesizes the high-speed clock from a low-speed reference. The on-chip receive PLL performs clock recovery and data re-timing on the serial bit stream. The transmitter and receiver each support differential LVPECL compatible I/O for copper or fiber optic component interfaces with excellent signal integrity. Local loopback mode allows for system diagnostics. The chip requires a +3.3 V power supply and dissipates approximately 620 mW under typical conditions.

The S2070 can be used for a variety of applications including Fibre Channel, serial backplanes, and proprietary point-to-point links. Figure 1 shows a typical configuration incorporating the chip.

Figure 1. System Block Diagram



S2070 OVERVIEW

The S2070 transmitter and receiver provide serialization and deserialization functions for block encoded data to implement a Gigabit Ethernet or Fibre Channel interface. The S2070 functional block diagram is depicted in Figure 2. The sequence of operations is as follows:

Transmitter

1.10-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver

1. Clock and data recoverery from serial input
2. Serial-to-parallel conversion
3. Frame detection
4. 10-bit parallel output

The 10-bit parallel data input to the S2070 should be from a DC-balanced encoding scheme, such as the 8B/10B transmission code, in which information to be transmitted is encoded 8 bits at a time into 10-bit transmission characters[1]. For reference, Table 1 shows the mapping of the parallel data to the 8B/10B codes.

Loop Back

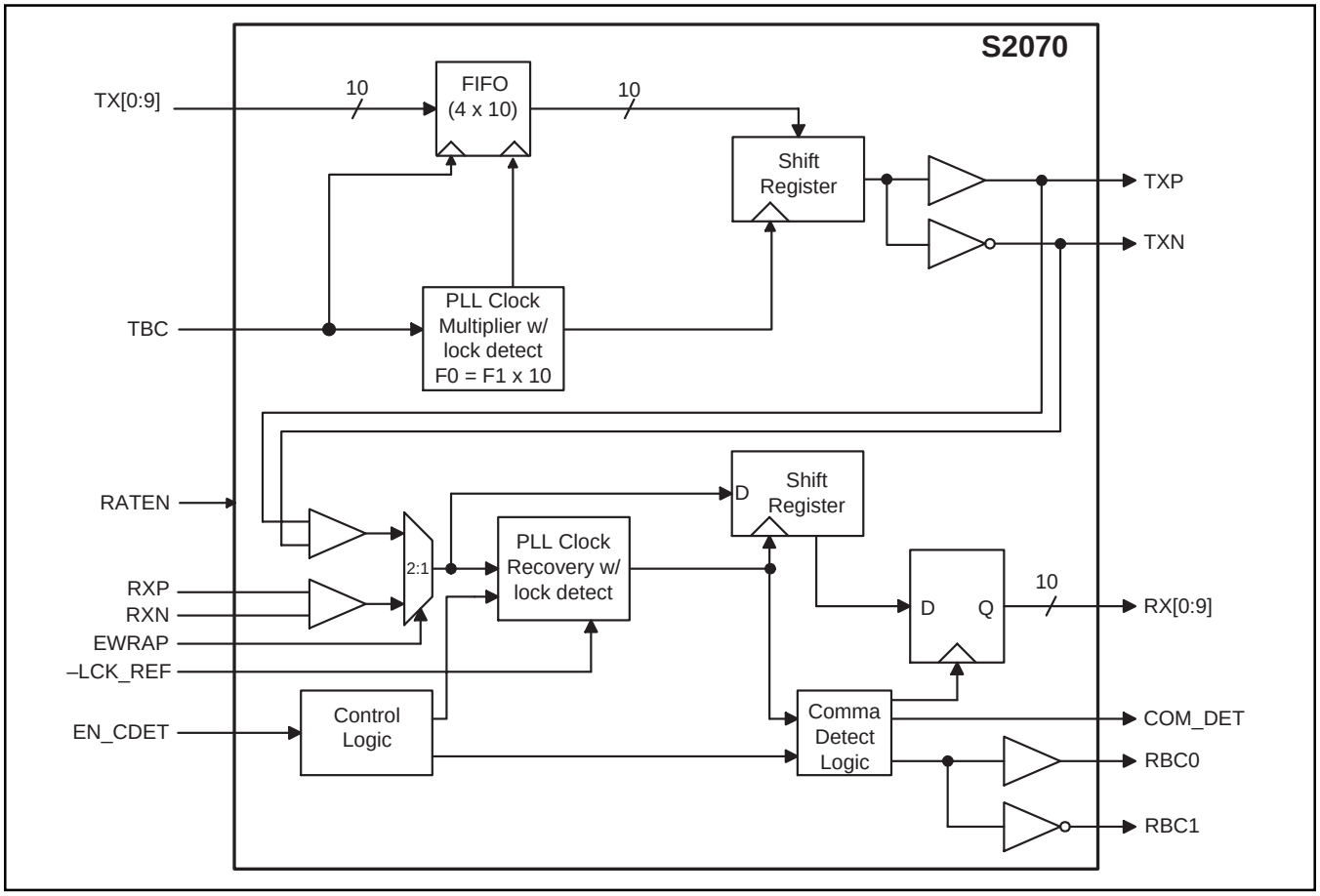
Local loopback provides a capability for performing off-line testing. This is useful for ensuring the integrity of the serial channel before enabling the transmission medium. It also allows for system diagnostics.

[1] A.X. Widmer and P.A. Franaszek, "A Byte Oriented DC Balanced (0,4) 8B/10B Transmission Code," IBM Research Report RC 9391, May 1982.

Table 1. Data Mapping to 8B/10B Alphabetic Representation

	Data Byte									
TX[0:9] or RX[0:9]	0	1	2	3	4	5	6	7	8	9
8B/10B Alphabetic Representation	a	b	c	d	e	i	f	g	h	j

Figure 2. Functional Block Diagram



TRANSMITTER DESCRIPTION

The S2070 transmitter accepts 10-bit parallel input data and serializes it for transmission over fiber optic or coaxial cable media. The chip is fully compatible with the IEEE 802.3z Gigabit Ethernet and ANSI X3T11 Fibre Channel standards. The S2070 uses a PLL to generate the serial rate transmit clock. The transmitter runs at 10 times the TBC input clock, and operates in either full rate or half rate mode.

Parallel-to-Serial Conversion

The parallel-to-serial converter takes in 10-bit wide data from the input latch and converts it to a serial data stream. Parallel data is latched into the transmitter on the positive going edge of TBC. The data is then clocked into the serial output shift register. The shift register is clocked by the internally generated bit clock which is 10x the TBC input frequency. TX[0] is transmitted first.

Transmit Byte Clock (TBC)

The Transmit Byte Clock (TBC) input must be supplied from a clock source with 100 ppm tolerance to assure that the transmitted data meets the Fibre Channel frequency limits. The internal serial clock is frequency locked to TBC.

TBC is input at full or half rate determined by the state of the RATEN input. Operating rates are shown in Table 2.

Transmit Latency

The average transmit latency is 4 parallel clocks.

Table 2. Operating Rates

RATEN	Parallel Input Rate (Mbps)	TBC Frequency (MHz)	Serial Output Rate (Gbps)
0	125	125	1.25
0	106.25	106.25	1.0625
1	62.5	62.5	0.625
1	53.125	53.125	0.53125

RECEIVER DESCRIPTION

Whenever a signal is present, the receiver attempts to recover the serial clock from the received data stream. The S2070 searches the serial bit stream for the occurrence of a positive polarity COMMA sync pattern (0011111xxx positive running disparity) to perform word synchronization. Once synchronization on both bit and word boundaries is achieved, the receiver provides the decoded data on its parallel outputs.

Clock Recovery Function

Clock recovery is performed on the input data stream. A simple state machine in the clock recovery macro decides whether to acquire lock from the serial data input or from the reference clock. The decision is based upon the frequency and run length of the input serial data.

The lock to reference frequency criteria ensure that the S2070 will respond to variations in the serial data input frequency (as compared to the reference frequency). The new lock state is dependent upon the current lock state, as shown in Table 3. The run-length criteria ensure that the S2070 will respond appropriately and quickly to a loss of signal. The run-length checker flags a condition of consecutive ones or zeros across 12 parallel words. Thus, 119 or less consecutive ones or zeros does not cause signal loss, 129 or more causes signal loss, and 120 – 128 may or may not, depending on how the data aligns across byte boundaries. If both the off-frequency detect test and the run-length test is satisfied, the CRU will attempt to lock to the incoming data.

Table 3. Lock to Reference Frequency Criteria

Current Lock State	PLL Frequency (vs. TBC)	New Lock State
Locked	< 488 ppm	Locked
	488 to 732 ppm	Undetermined
	> 732 ppm	Unlocked
Unlocked	< 244 ppm	Locked
	244 to 366 ppm	Undetermined
	> 366 ppm	Unlocked

In any transfer of PLL control between the serial data and the reference clock, the RBC0 and RBC1 remain phase continuous and glitch free, assuring the integrity of downstream clocking.

Reference Clock Input

The reference clock must be provided from a low jitter clock source. The frequency of the received data stream must be within 200 ppm of the reference clock to ensure reliable locking of the receiver PLL. A single reference clock is provided to both the transmit and receive PLLs.

Data Output

The S2070 provides either framed or unframed parallel output data, determined by the state of EN_CDET. With EN_CDET held ACTIVE, the S2070 will detect and align to the 8B/10B COMMA codeword anywhere in the data stream. When EN_CDET is INACTIVE, no attempt is made to synchronize on any particular incoming character. Upon change of state of the EN_CDET input, the COM_DET output response will be delayed by a maximum of 3 byte times.

The COM_DET output signal is ACTIVE whenever EN_CDET is active and the COMMA control character is present on the RX[0:9] parallel data outputs. The COM_DET output signal will be INACTIVE at all other times.

Parallel Output Clock Rate and Data Stretching

The S2070 supports both full rate and half rate outputs, selected via the RATEN input. Table 4 shows the operating rate scenarios. When RATEN is INACTIVE, a data clock is provided on RBC1 at the data rate. Data should be clocked on the rising edge of RBC1. When RATEN is ACTIVE the device is in full rate mode, and complementary TTL clocks are provided on the RBC0 and RBC1 outputs at 1/2 the data rate as required by the Fibre Channel standard. Data is clocked on the rising edges of both RBC0 and RBC1. See Figures 9 and 10.

Table 4. Operating Rates

RATEN	Serial Input Rate (Gbps)	RBC0 (MHz)	RCB1 (MHz)	Parallel Output Rate (Mbps)
0	1.25	62.5	62.5	125
0	1.0625	53.125	53.125	106.25
1	0.625	N/A	62.5	62.5
1	0.53125	N/A	53.125	53.125

Fibre Channel and Gigabit Ethernet standards require that the COMMA sync character appears on the rising edge of the RBC1 signal. In full rate mode the phase of the data is adjusted such that this requirement is met. No alignment is necessary when the S2070 is operating in half rate mode (RATEN INACTIVE) since the output clock frequency is equal to the parallel word rate.

In Fibre Channel and Gigabit Ethernet applications it is illegal for multiple consecutive COMMA characters to be generated. However, multiple consecutive COMMA characters can occur in serial backplane applications. The S2070 is able to operate properly when multiple consecutive COMMA characters are received: after the first COMMA is detected and aligned, the RBC0/RBC1 clock operates without glitches or loss of cycles. Additionally, COM_DET stays high while multiple COMMAs are being output.

Receive Latency

The average receive latency is 8 byte times.

OTHER OPERATING MODES

Loopback Mode

The S2070 supports internal loopback mode in which the serial data from the transmitter replaces external serial data. The loopback function is enabled when the loopback enable signal, EWRAP, is set ACTIVE.

The loopback mode provides the ability to perform system diagnostics and to perform off-line testing of the interface to guarantee the integrity of the serial channel before enabling the transmission medium. Figure 3 shows the basic loopback operation.

Figure 3. Loopback Operation

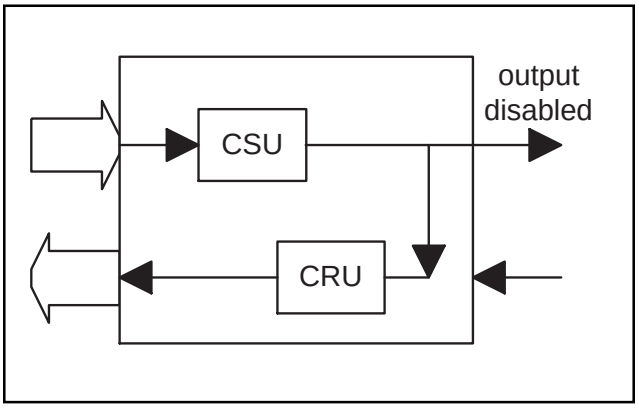


Table 5. Pin Description and Assignment

Pin Name	Level	I/O	Pin #	Description
TX[9] TX[8] TX[7] TX[6] TX[5] TX[4] TX[3] TX[2] TX[1] TX[0]	LVTTL	I	13 12 11 9 8 7 6 4 3 2	Transmit Data. Parallel data on this bus is clocked in on the rising edge of TBC. TX[0] is transmitted first.
TBC	LVTTL	I	22	Transmit Byte Clock. Reference clock input to the PLL clock multiplier. The frequency of TBC is the bit rate divided by 10. When TESTEN is active, TBC replaces the VCO clock to facilitate factory test. TBC should be supplied by a crystal controlled reference since jitter on this line directly translates to jitter on the output data.
RATEN	LVTTL	I	14	Rate Select. Active Low. This signal configures the PLL's for the appropriate TBC frequency. When inactive, the device operates in 1/2 rate mode. When active, the device operates in full rate mode. See Tables 2 and 4.
EN_CDET	LVTTL	I	24	Enable Comma Detect. Active High. When active, enables detection of the COMMA sync pattern to set the word frame boundary for the data to follow. When inactive, data is treated as unframed.
EWRAP	LVTTL	I	19	Enable Wrap. Active High. When active, the transmitter serial data outputs are internally routed to the receiver serial data inputs. TXP/N are static (logic 1) in this state. When inactive, the RXP/N serial inputs are selected (normal operation).
RXP RXN	Diff. LVPECL	I	54 52	(Externally capacitively coupled.) LVPECL Receive Serial Data Inputs. RXP is the positive differential input, RXN is negative. Internally biased to VCC -1.3 V.
–LCK_REF	LVTTL	I	27	Lock to Reference Input. Active Low. When inactive or open, the receive PLL will lock to the incoming data (normal operation). When active, the receive PLL is forced to lock to the TBC input.

Note: All TTL inputs have internal 15KΩ pull-up networks.

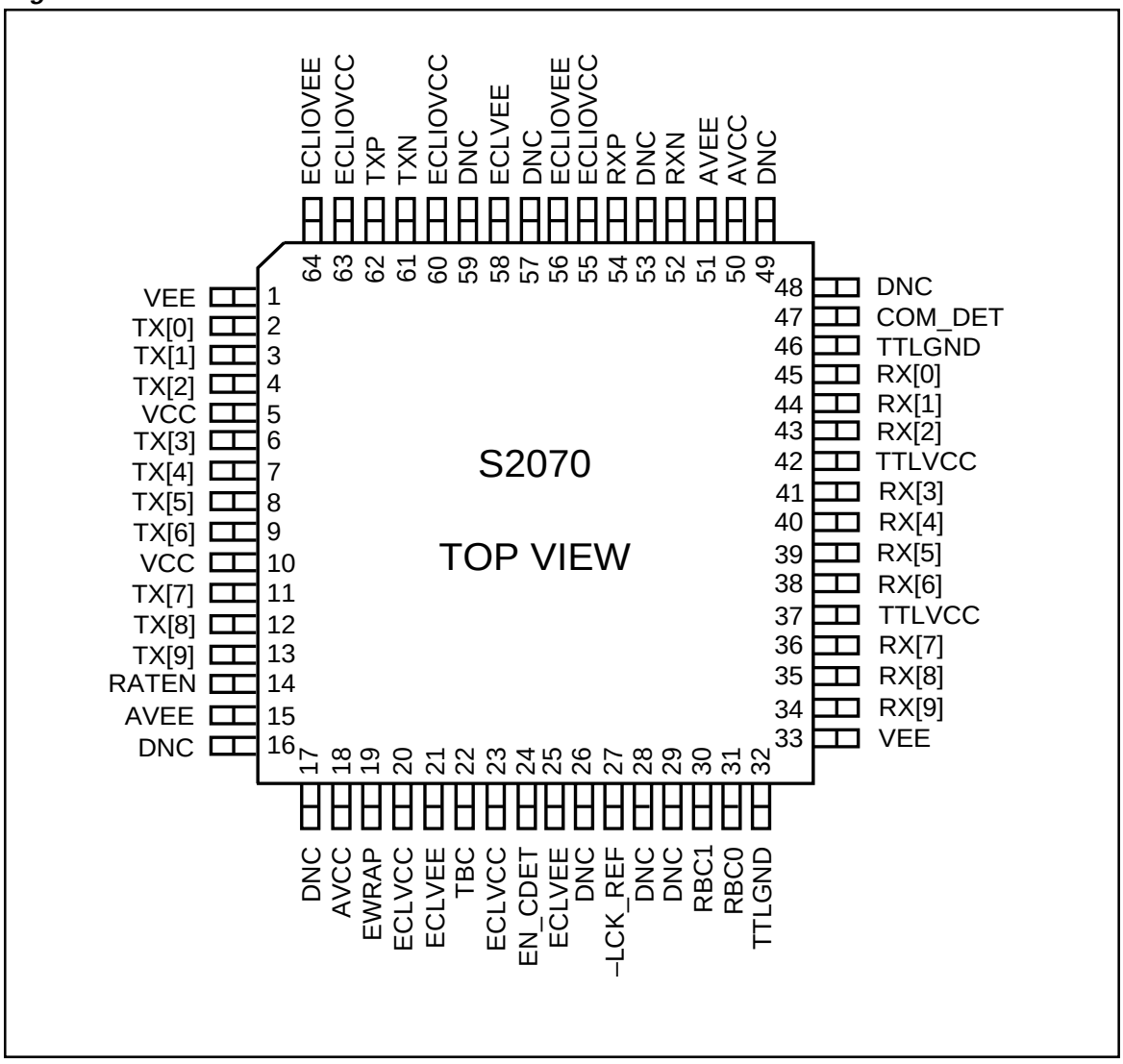
Table 5. Pin Description and Assignment (Continued)

Pin Name	Level	I/O	Pin #	Description
RX[9] RX[8] RX[7] RX[6] RX[5] RX[4] RX[3] RX[2] RX[1] RX[0]	LVTTL	O	34 35 36 38 39 40 41 43 44 45	Receive Data Outputs. For full rate output, parallel data on this bus is valid on the rising edges of RBC0 and RBC1. RX[0] is the first bit received.
RBC1 RBC0	LVTTL	O	30 31	Complementary Receive Byte Clocks. In full rate mode, parallel receive data is valid on the rising edges of RBC0 and RBC1 (see Figure 9, timing diagram). For half rate, output data is valid on the rising edge of RBC1. See Table 4.
COM_DET	LVTTL	O	47	Comma Detect. Active High. When EN_CDET is active, COM_DET indicates that the sync character is present on the parallel bus bits RX[0:9]. Upon detection of the COMMA sync character (0011111xxx positive polarity) this output data is valid on the rising edge of RBC1 and remains active for one RBC1 clock period. When EN_CDET is inactive, COM_DET is held Low (logic 0). Upon change of state of the EN_CDET input, the COM_DET output response will be delayed by a maximum of 3 byte times.
TXP TXN	Diff. LVPECL	O	62 61	Transmit Serial Data. These lines are static (TXN HIGH, TXP HIGH) when EWRAP is active. These lines are static (TXN HIGH, TXP LOW) when TXRST is active. Upon startup, these outputs are held static (TXN HIGH, TXP LOW) until the TXPLL has locked to the reference clock. Each output can drive 150 Ω to ground.

Table 6. Power and Ground Signals

Pin Name	Level	Pin #	Description
ECLVCC	+3.3 V	20, 23	Core Power Supply
ECLVEE	GND	21, 25, 58	Core Ground
ECLIOVCC	+3.3 V	55, 60, 63	LVPECL I/O Power Supply
ECLIOVEE	GND	56, 64	LVPECL I/O Ground
TTLVCC	+3.3 V	37, 42	LVTTL Power Supply
TTLGND	GND	32, 46	LVTTL Ground
AVCC	+3.3 V	18, 50	Analog Power Supply
AVEE	GND	15, 51	Analog Ground
VCC	+3.3 V	5, 10	Power
VEE	GND	1, 33	Ground
DNC	—	48	This pin cannot be tied Low. It should be floated, or tied High.
DNC	—	16, 17, 26, 28, 29, 49, 53, 57, 59	Not connected

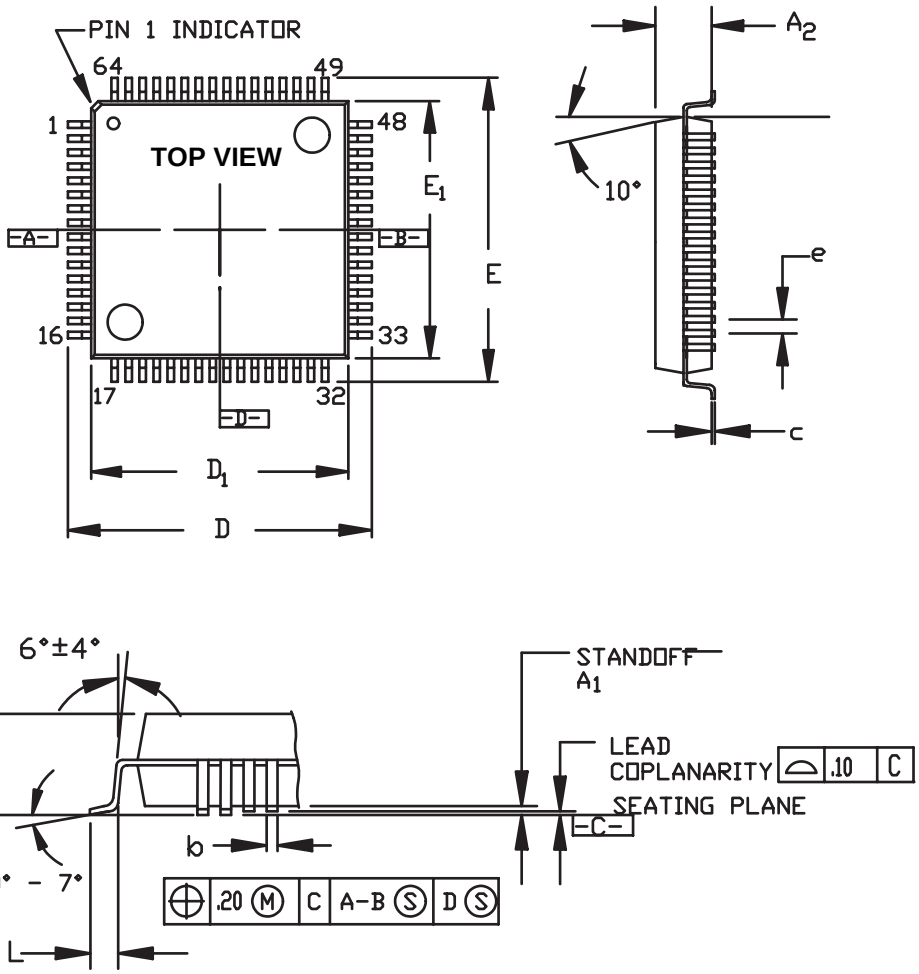
Figure 4. S2070 Pinout



Thermal Management

Device	Θja Still Air
S2070A (10mm package)	45 ˚ C/W
S2070B (14mm package)	45 ˚ C/W

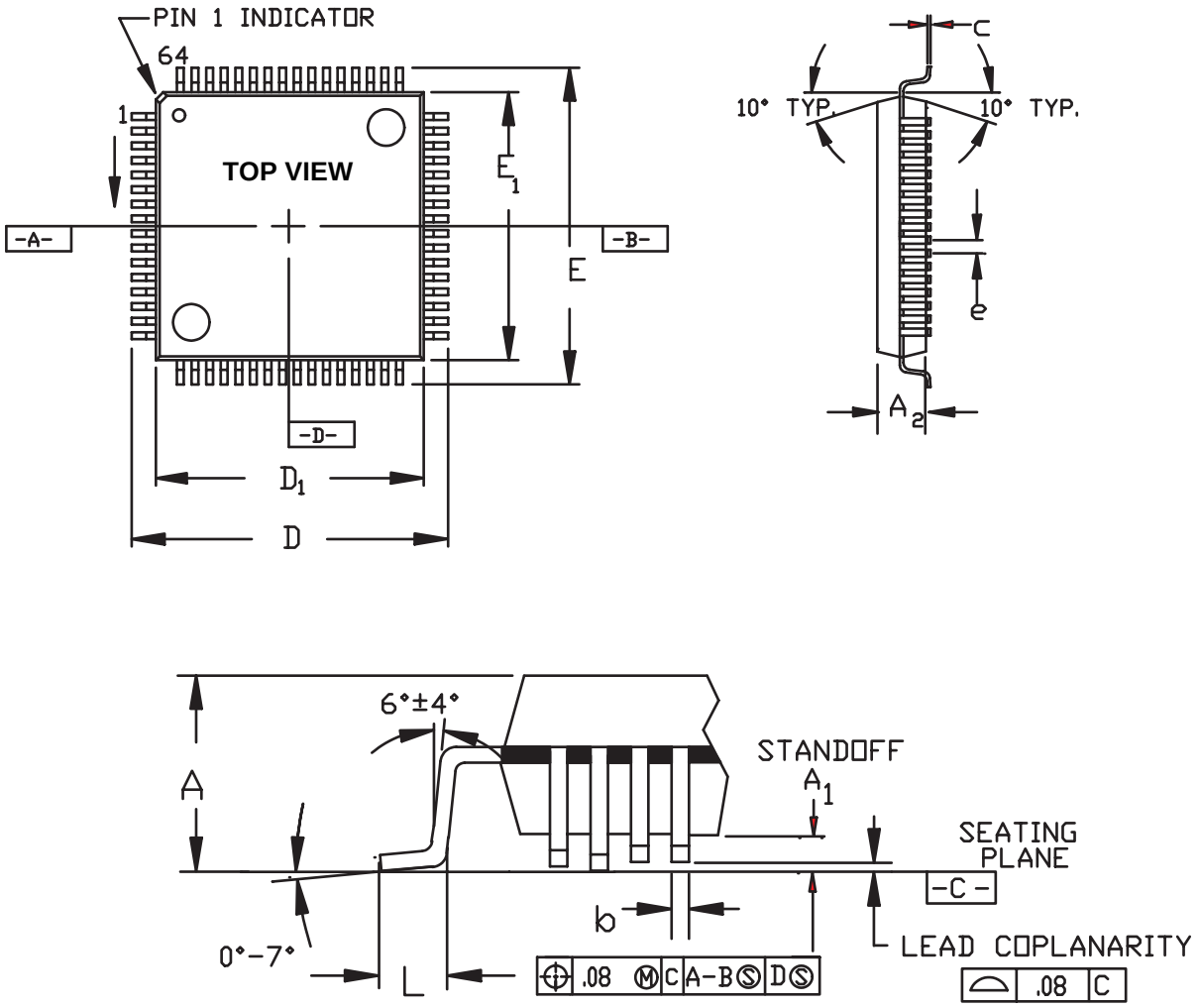
Figure 5. 14mm x 14mm 64 PQFP Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	b	e	c
MIN			1.90	16.95	13.90	16.95	13.90	0.78	0.30	0.80 BSC.	
NOM			2.00	17.20	14.00	17.20	14.00	0.88	0.35		
MAX	2.35	0.25	0.95	17.45	14.10	17.45	14.10	1.03	0.40		0.17

Figure 6. 10mm x 10mm 64 PQFP with Heat Spreader Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.25	1.95	13.00	9.90	13.00	9.90	0.78	0.50 BSC.	0.17	
NOM			2.00	13.20	10.00	13.20	10.00	0.88		0.22	
MAX	2.45	0.50	2.10	13.40	10.10	13.40	10.10	1.03		0.27	0.17

Table 7. Power and Ground Application Information

Function	Pin Names	Instructions
ANALOG	AVCC	Connect to low noise or filtered +3.3 V supply through a ferrite bead (600Ω at 100 MHz: Murrata BLM31B601S or equivalent). Provide dual local HF bypassing to AVEE (0.1 µf, 100 pf) for low inductance and resistance. A single low inductance 0.1 µf capacitor can be substituted for the pair (Vishay VJ0612 or equivalent, <0.5 nH max inductance).
	AVEE	Connect to ground plane.
LVPECL I/O	ECLIOVCC	Provide low impedance connection to +3.3 V. Provide dual local bypassing to GND plane (0.1 µf and 100 pf in parallel, or a single low inductance Vishay VJ0612 or equivalent 0.1 µf capacitor).
	ECLIOVEE	Connect to ground plane.
CORE	ECLVCC	Provide low impedance connection to +3.3 V. Provide dual local bypassing to GND plane (0.1 µf and 100 pf in parallel, or a single low inductance Vishay VJ0612 or equivalent 0.1 µf capacitor).
	ECLVEE	Connect to ground plane.
LVTTL I/O	LVTTLVCC	Provide low impedance connection to +3.3 V. Provide dual local bypassing to GND plane (0.1 µf and 100 pf in parallel, or a single low inductance Vishay VJ0612 or equivalent 0.1 µf capacitor).
	LVTTLVEE	Connect to ground plane.

Figure 7. Power and Ground Connection Diagram

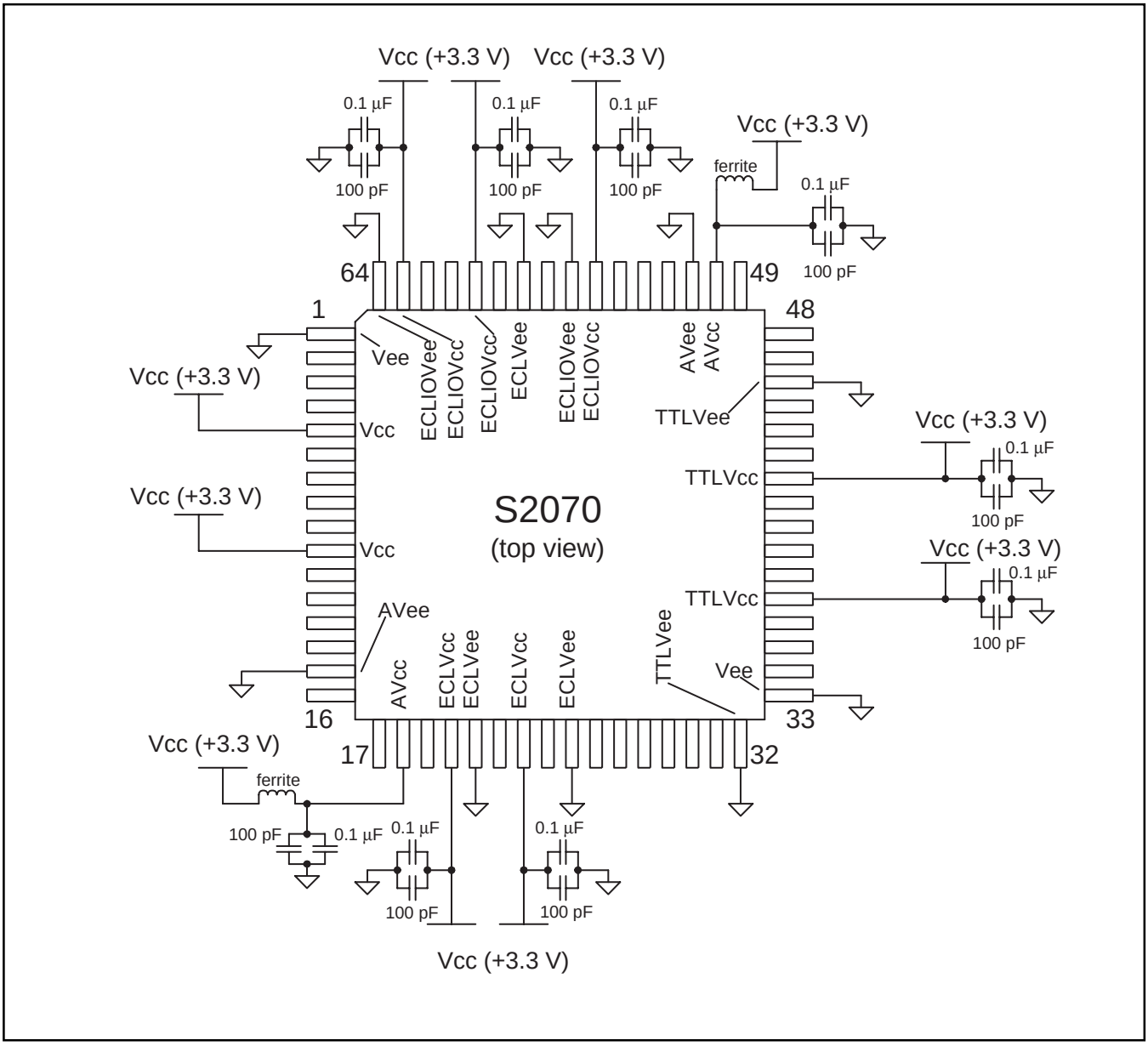


Figure 8. Transmitter Timing

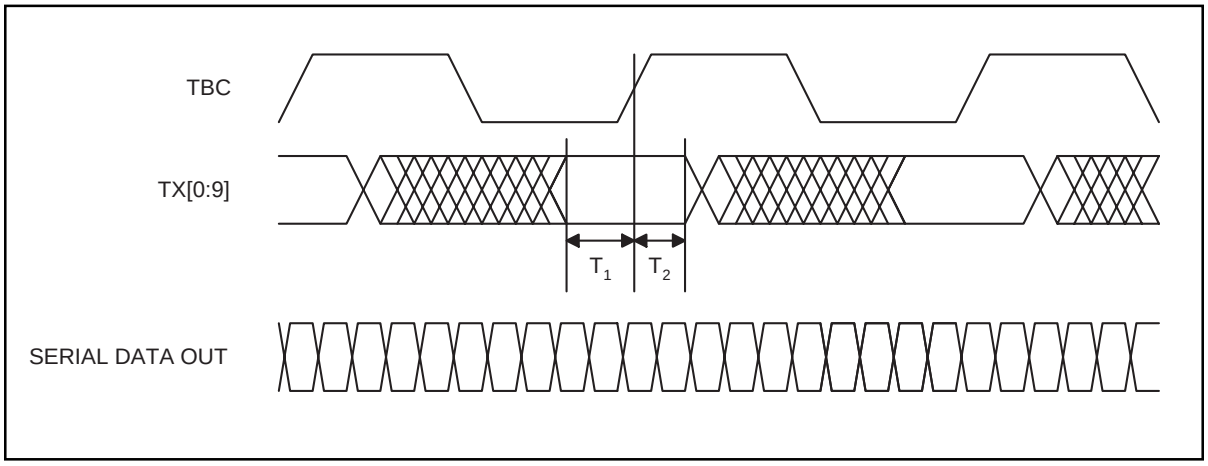


Table 8. S2070 Transmitter Timing

Parameters	Description	Min	Max	Units	Conditions
T_1	Data Setup w.r.t. ↑ TBC	1.2	-	ns	See Note 1.
T_2	Data Hold w.r.t. ↑ TBC	0.25	-	ns	
T_{SDR}, T_{SDF}	Serial Data Rise and Fall	-	270	ps	20% - 80%, tested on sample basis.
T_J	Serial Data Output total jitter (p-p)	-	0.23	UI	Peak-to-peak, measured on sample basis. Measured with ±K28.5 or 2^7-1 pattern at 1.062 GHz.
T_{DJ}	Serial Data Output deterministic jitter (p-p)	-	0.08	UI	Peak-to-peak, tested on a sample basis. Measured with ±K28.5 pattern at 1.062 GHz.
T_J	Serial Data Output total jitter (p-p)	-	192	ps	Peak-to-peak, measured on sample basis. Measured with ±K28.5 or 2^7-1 pattern at 1.25 GHz.
T_{DJ}	Serial Data Output deterministic jitter (p-p)	-	80	ps	Peak-to-peak, tested on a sample basis. Measured with ±K28.5 pattern at 1.25 GHz.

1. All AC measurements are made from the reference voltage level of the clock (+1.4 V) to the valid input or output data levels (+.8 V or +2.0 V).

Figure 9. Receiver Timing Full Rate Mode (RATEN Active)

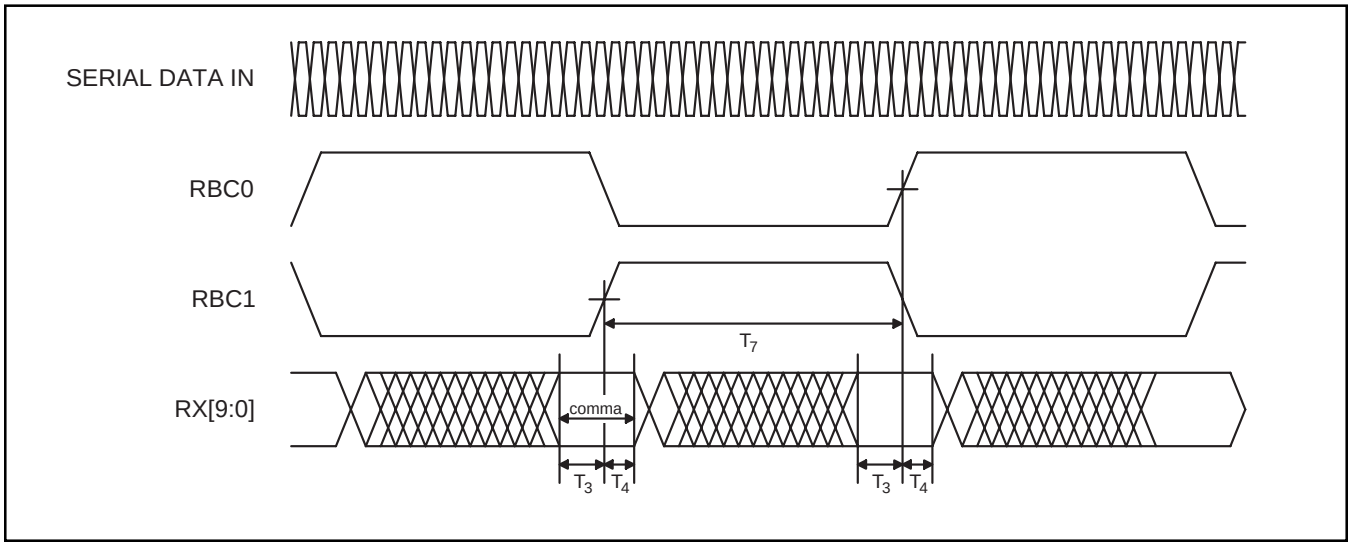


Figure 10. Receiver Timing Half Rate Mode (RATEN Inactive)

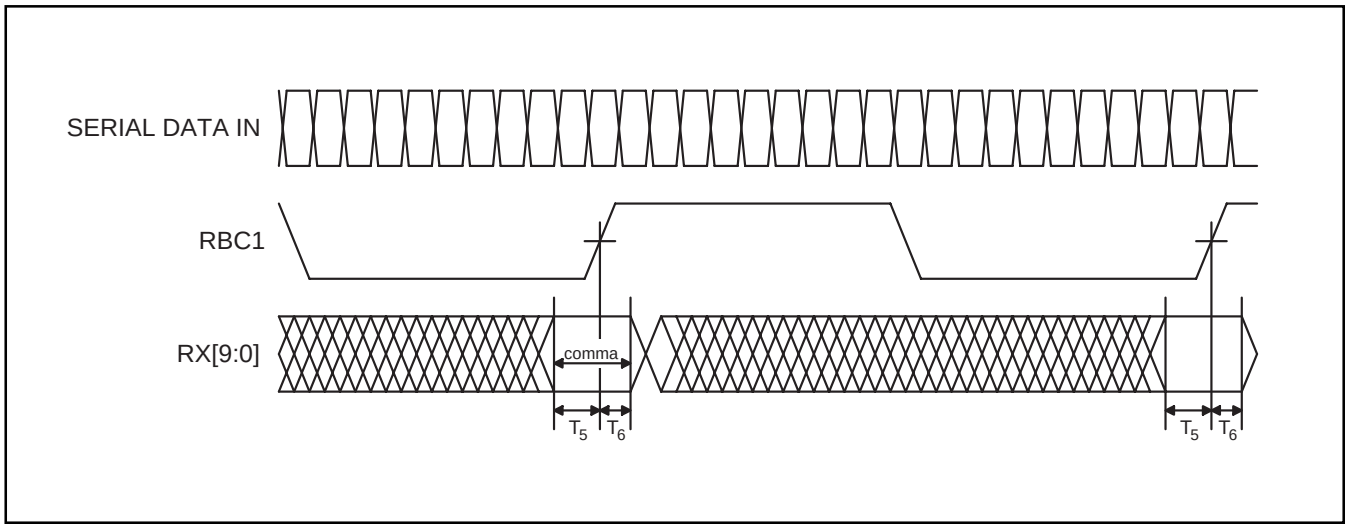


Table 9. S2070 Receiver Timing

Parameters	Description	Min	Max	Units	Conditions
T_3	Data valid before RBCI/O (full rate)	3.0	-	ns	
T_4	Data valid after RBCI/O (full rate)	2.0	-	ns	
T_5	Data Setup w.r.t. ↑ RBCI/O (half rate)	7.0	-	ns	
T_6	Data Hold w.r.t. ↑ RBCI/O (half rate)	6.0	-	ns	
T_7	RBC1 to RBC0 at 1.0625 Gbps at 1.25 Gbps	 9.2 7.5	 10 8.5	 ns ns	Skew.
T_{RCR}, T_{RCF}	RBC1, RBC0 Rise and Fall Time	-	2.4	ns	Measured +.8V to +2.0V.
T_{DR}, T_{DF}	Data Output Rise and Fall Time		2.4	ns	Measured +.8V to +2.0V.
T_{LOCK} (startup)	Startup acquision lock time (full rate data)	-	2.5	µs	
T_{LOCK} (reacquire)	Data Acquisition Lock Time following a phase shift (full rate data)	-	100	ns	90% input data eye; 10^{-9} BER (see Figure 16).
		-	250	ns	24% input data eye; 10^{-9} BER.
Duty Cycle	RBC1 (RBC0)	40	60	%	
T_J	Total Input Jitter Tolerance	0.7	-	UI	1.0625 Gbps data rate as specified in ANSI 3XT11 Fibre Channel.
T_{DJ}	Deterministic Input Jitter Tolerance	0.38	-	UI	1.0625 Gbps data rate as specified in ANSI 3XT11 Fibre Channel.
T_{RJ}	Random Input Jitter Tolerance	0.22	-	UI	1.0625 Gbps data rate as specified in ANSI 3XT11 Fibre Channel.
T_J	Total Input Jitter Tolerance	599	-	ps	1.25 Gbps data rate, as specified in IEEE 802.3z
T_{DJ}	Deterministic Input Jitter Tolerance	370	-	ps	1.25 Gbps data rate, as specified in IEEE 802.3z

All AC measurements are made from the reference voltage level of the clock (+1.4 V) to the valid input or output data levels (+.8 V or +2.0 V).

Table 10. Absolute Maximum Ratings

The following are the absolute maximum stress ratings for the S2070 device. Stresses beyond those listed may cause permanent damage to the devices. Absolute maximum ratings are stress ratings only and operation of the device at the maximums stated or any other conditions beyond those indicated in the Recommended Operating Conditions of the document are not inferred. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Min	Typ	Max	Units
Case Temperature Under Bias	-55		125	˚C
Junction Temperature Under Bias			150	˚C
Storage Temperature	-65		150	˚C
Voltage on VCC with Respect to GND	-0.5		+4.0	V
Voltage on any TTL Input Pin except TBC	-0.5		5.0	V
Voltage on TBC	0		VCC	V
Voltage on any LVPECL Input Pin	0		VCC	V
TTL Output Sink Current			8	mA
TTL Output Source Current			8	mA
Electrostatic Discharge (ESD) Rating	1000			V

[1] Human body model

Table 11. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	0		70	˚C
Junction Temperature Under Bias			130	˚C
Voltage on TTLVCC, ECLVCC, ECLIOVCC, and AVCC with respect to GND/VEE	3.135	3.3	3.465	V
Voltage on any TTL Input Pin except TBC	0	VCC	5.0	V
Voltage on any LVPECL Input Pin	VCC -2.0		VCC	V
Voltage on TBC	0		VCC	V

Table 12. Reference Clock Requirements

Parameters	Description	Min	Max	Units	Conditions
FT	Frequency Tolerance	-100	+100	ppm	
TD_{1-2}	Symmetry	40	60	%	Duty Cycle at 50% pt.
T_{RCR}, T_{RCF}	REFCLK Rise and Fall Time		2	ns	20% - 80%.
J_R	Random Jitter		100	ps	Peak-to-Peak.

Table 13. DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Comments
V_{OH}	Output High Voltage (TTL)	2.4	2.8	V_{CC}	V	V_{CC} = min, I_{OH} = 4 mA
V_{OL}	Output Low Voltage (TTL)	GND	0.1	0.4	V	V_{CC} = min, I_{OL} = 1 mA
V_{IH}	Input High Voltage (TTL)	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage (TTL)	GND		0.8	V	
I_{IH}	Input High Current (TTL)			40	µA	V_{IN} = 2.4 V, V_{CC} = Max
I_{IL}	Input High Current (TTL)			600	µA	V_{IN} = 0 V, V_{CC} = Max
I_{CC}	Supply Current		187	235	mA	Outputs open.
P_D	Power Dissipation		620	820	mW	Outputs open.
V_{DIFF}	Min. differential input voltage swing for differential LVPECL inputs	100		2200	mV	
ΔV_{OUT}	Serial Output Differential Voltage Swing	1600	2000	2200	mV	150 Ω to ground.
C_{IN}	Input Capacitance			3	pF	

OUTPUT LOAD

The S2070 serial outputs require a resistive load to set the output current. The recommended resistor value is 150 ohms to ground. This value can be varied to adjust drive current, signal voltage swing, and power usage on the board.

ACQUISITION TIME

With the input eye diagram shown in Figure 16, the S2070 will recover data with ≤ IE-9 BER within the time specified by T_{LOCK} in Table 9 after an instantaneous phase shift of the incoming data.

Figure 11. Serial Input Rise and Fall Time

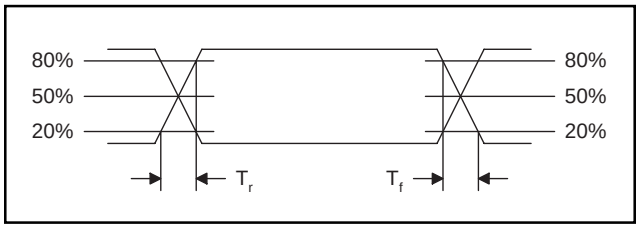


Figure 12. TTL Input/Output Rise and Fall Time

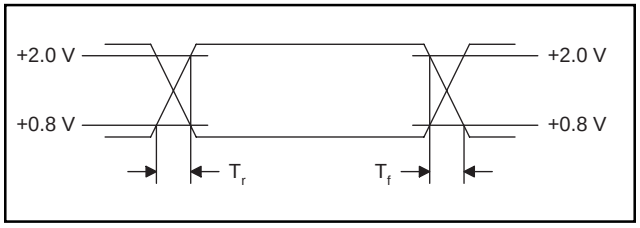


Figure 13. Serial Output Load

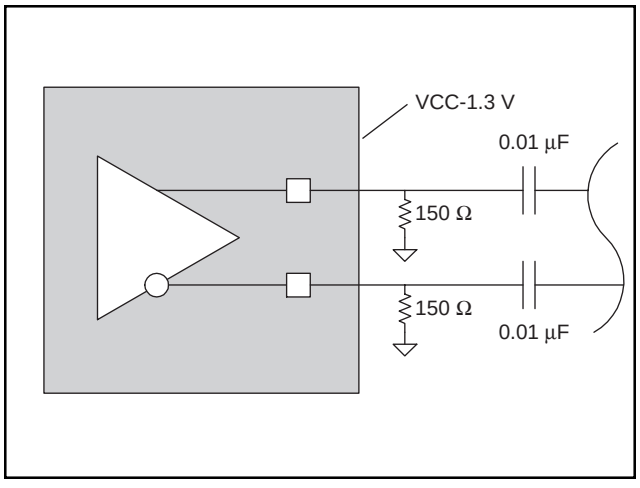


Figure 14. High Speed Differential Inputs

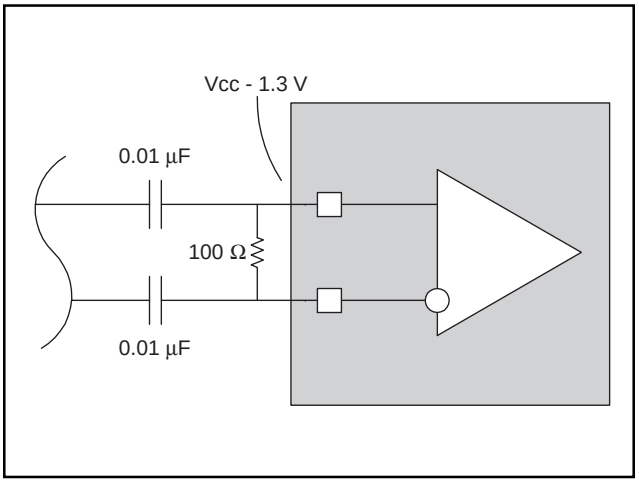


Figure 15. Receiver Input Eye Diagram Jitter Mask

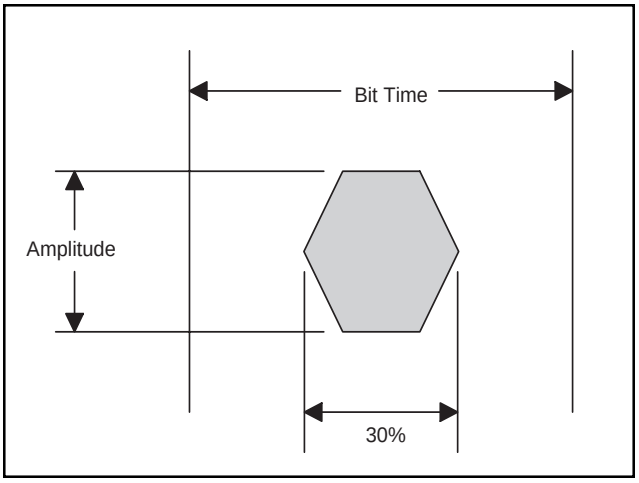
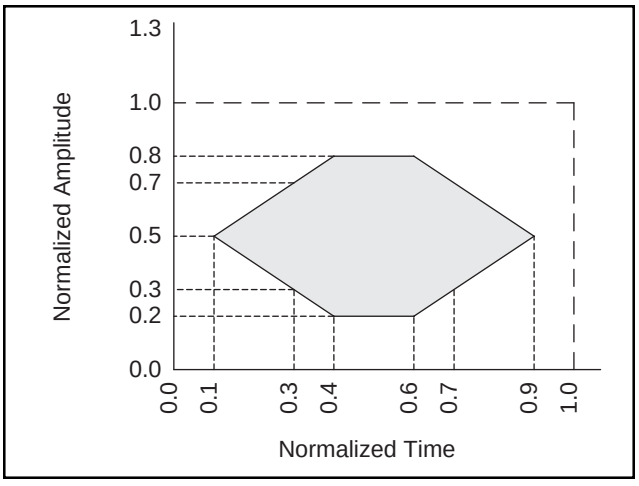
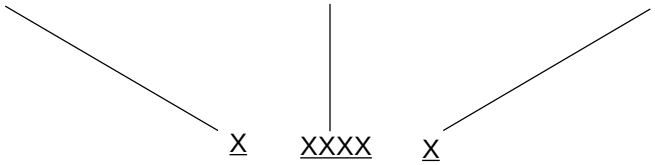


Figure 16. Acquisition Time Eye Diagram



Ordering Information

GRADE	PART NO.	PACKAGE
S- Commercial	2070	A–(64 PQFP w/Heat Spreader 10mm) B–(64 PQFP 14mm)



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