GIGABIT ETHERNET CHIPSET S2046/S2050

FEATURES

- Functionally compliant with the 802.3z specification
- S2046 transmitter incorporates phase-locked loop (PLL) providing clock synthesis from low-speed reference
- S2050 receiver PLL configured for clock and data recovery
- 1250 Mbps (Gigabit Ethernet) operation
- 10- or 20-bit parallel TTL compatible interface
- +3.3/+5V power supply
- Low-jitter serial PECL compatible interface
- Lock detect
- Local loopback
- Compact 52 PQFP package
- Gigabit Ethernet framing performed by receiver
- Continuous downstream clocking from receiver
- TTL compatible outputs possible with +5V I/O power supply

APPLICATIONS

High-speed data communications

- Ethernet backbone connections
- Mainframe
- Workstation
- Frame buffer
- Switched networks
- Data broadcast environments
- Proprietary extended backplanes

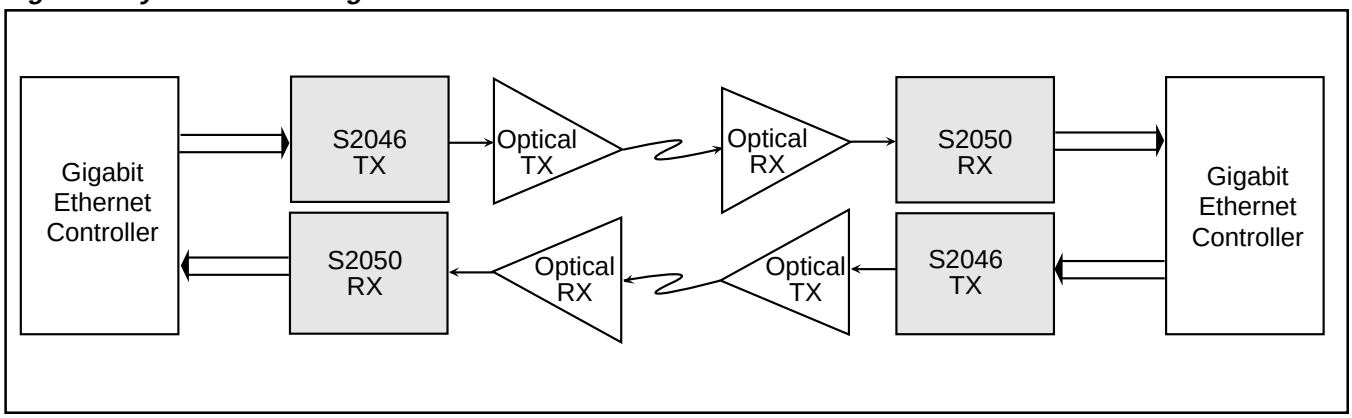
GENERAL DESCRIPTION

The S2046 and S2050 transmitter and receiver pair are designed to perform high-speed serial data transmission over fiber optic or coaxial cable interfaces conforming to the requirements of the proposed 802.3z specification. The chipset is Gigabit Ethernet compliant and supports 1250 Mbps with an associated 10 or 20-bit data word.

The chipset performs parallel-to-serial and serial-to-parallel conversion and framing for block-encoded data. The S2046 on-chip PLL synthesizes the high-speed clock from a low-speed reference. The S2050 on-chip PLL synchronizes directly to incoming digital signals, to receive the data stream. The transmitter and receiver each support differential PECL-compatible I/O for fiber optic component interfaces, to minimize crosstalk and maximize data integrity. Local loopback allows for system diagnostics. The I/O section can operate from either a +3.3V or a +5V power supply. (See *Ordering Information*.)

Figure 1 shows a typical network configuration incorporating the chipset.

Figure 1. System Block Diagram



S2046/S2050 OVERVIEW

The S2046 transmitter and S2050 receiver provide serialization and deserialization functions for block-encoded data to implement a Gigabit interface. Operation of the S2046/S2050 chips is straightforward, as depicted in Figure 2. The sequence of operations is as follows:

Transmitter
1. 10/20-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver
1. Clock and data recovery from serial input
2. Serial-to-parallel conversion
3. Frame detection
4. 10/20-bit parallel output

The 10/20-bit parallel data handled by the S2046 and S2050 devices should be from a DC-balanced encoding scheme, such as the 8B/10B transmission code, in which information to be transmitted is encoded 8 bits at a time into 10-bit transmission characters.

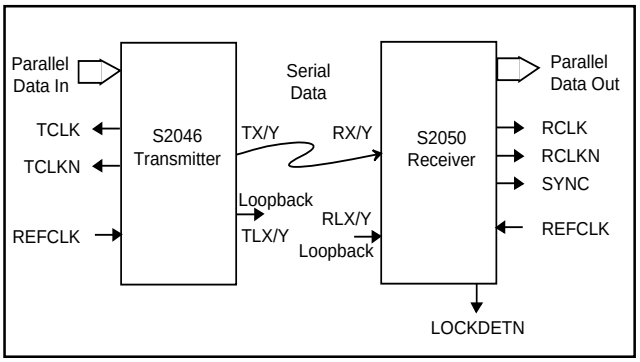
Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figure 5.

A lock detect feature is provided on the receiver, which indicates that the PLL is locked (synchronized) to the data stream.

Loopback

Local loopback is supported by the chipset, and provides a capability for performing offline testing of the interface to ensure the integrity of the serial channel before enabling the transmission medium. It also allows for system diagnostics.

Figure 2. Interface Diagram

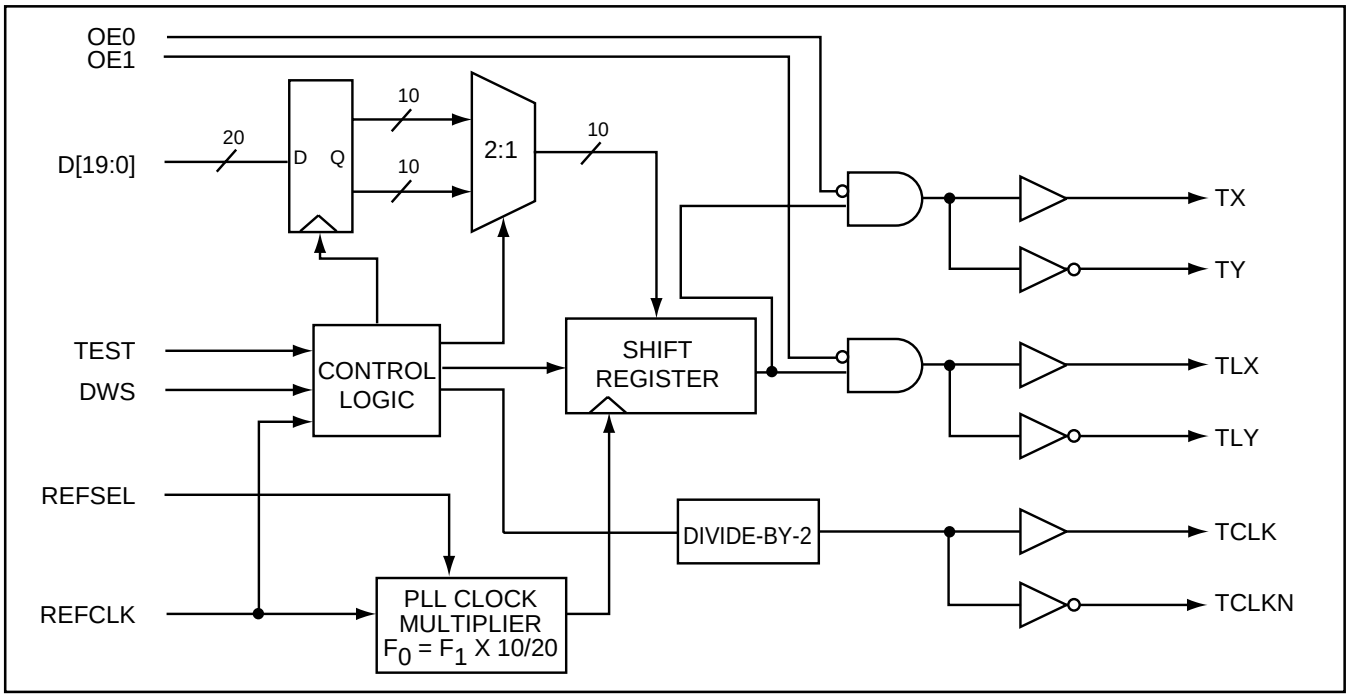


S2046 TRANSMITTER

Architecture/Functional Description

The S2046 transmitter accepts parallel input data and serializes it for transmission over fiber optic or coaxial cable media. The S2046 is fully compliant with the proposed 802.3z Specification, and supports the Gigabit Ethernet data rate of 1250 Mbps.

Figure 3. S2046 Functional Block Diagram



The parallel input data word can be either 10 bits or 20 bits wide, depending upon DWS pin selection. A block diagram showing the basic chip function is shown in Figure 3.

Parallel/Serial Conversion

The parallel-to-serial converter takes in 10-bit or 20-bit wide data from the input latch and converts it to a serial data stream. Parallel data is latched into the transmitter on the positive going edge of REFCLK. The data is then clocked synchronous to the clock synthesis unit serial clock into the serial output shift register. The shift register is clocked by the internally generated bit clock which is 10 or 20 times the REFCLK input frequency. The state of the serial outputs is controlled by the output enable pins, OE0 and OE1. D[10] is transmitted first in 10-bit mode. D[0] is transmitted first in 20-bit mode. Table 2 shows the mapping of the parallel data to the 8B/10B codes.

10-Bit/20-Bit Mode

The S2046 operates with either 10-bit or 20-bit parallel data inputs. Word width is selectable via the DWS pin. In 10-bit mode, D[10-19] are used and D[0-9] are ignored. See Table 2.

Reference Clock Input

The reference clock input (REFCLK) must be supplied with a PECL single-ended AC coupled crystal clock source with 100 PPM tolerance to assure that the transmitted data meets the proposed 802.3z Specification frequency limits. The internal serial clock is frequency locked to the reference clock. Refer to Table 1 for reference clock frequencies.

Table 1. Transmitter Operating Modes

DWS	REFSEL	Data Rate (Mbps/sec)	Word Width (Bits)	Reference Clock Frequency (MHz)	TCLK/TCLKN Frequency (MHz)
0	0	1250.0	20	62.5	62.5
1	1	1250.0	10	125.0	62.5

Table 2. Data Mapping to 8B/10B Alphabetic Representation

	First Data Byte										Second Data Byte									
TX[0:19] or RX[0:19]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
8B/10B alphabetic representation	a	b	c	d	e	f	g	h	i	j	a	b	c	d	e	f	g	h	i	j

↑ First bit transmitted in 20-bit mode ↑ First bit transmitted in 10-bit mode

Figure 4. S2050 Functional Block Diagram

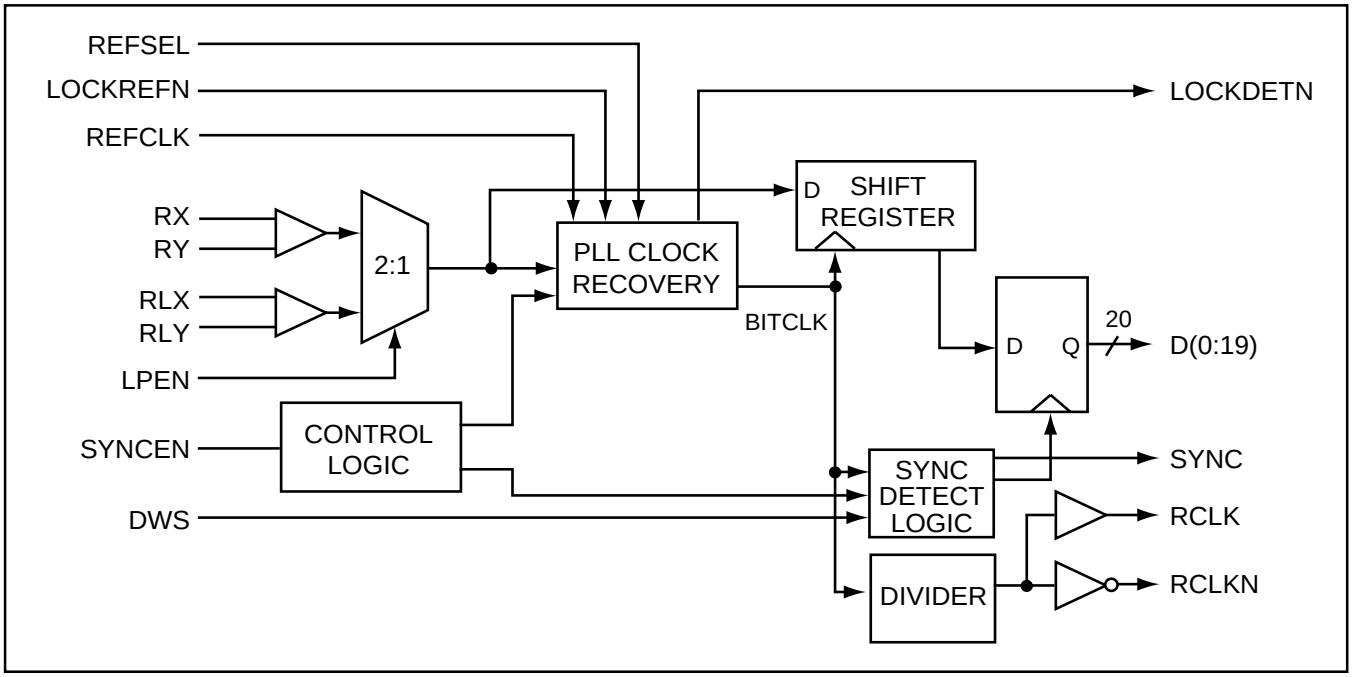
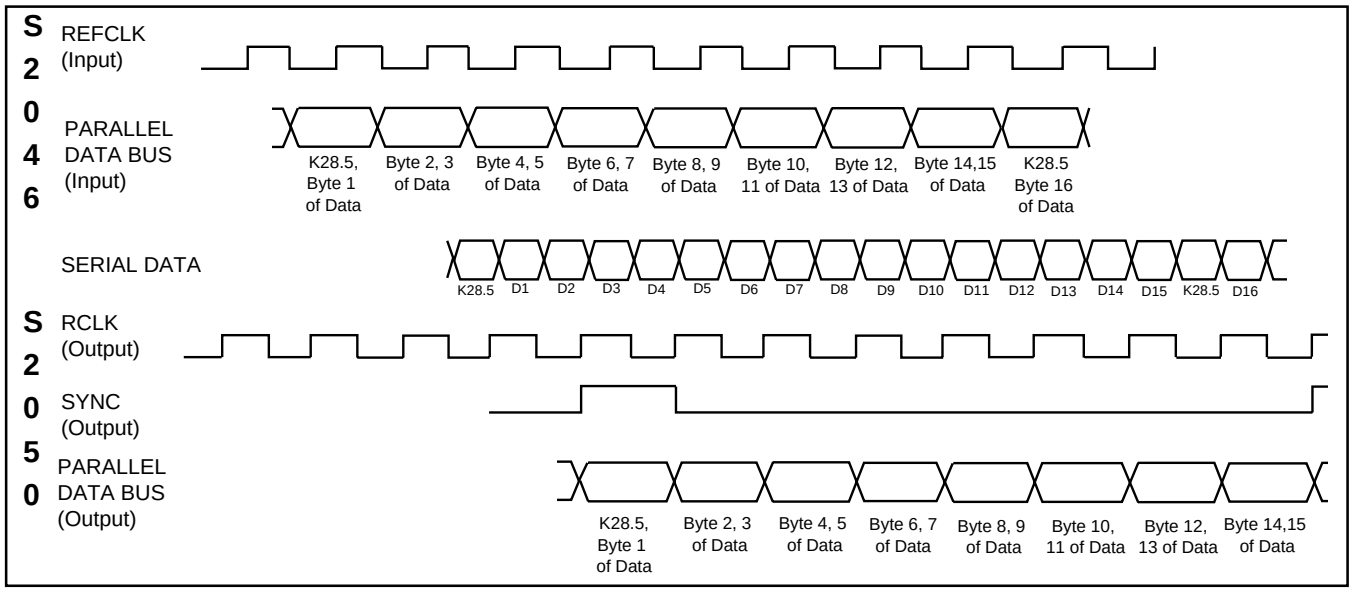


Figure 5. Functional Waveform



1. A.X. Widmer and P.A. Franaszek, “A Byte-Oriented DC Balanced (0,4) 8B/10B Transmission Code,” IBM Research Report RC 9391, May 1982.

S2050 RECEIVER

Architecture/Functional Description

The S2050 receiver is designed to implement the 802.3z specification receiver functions. A block diagram showing the basic chip function is provided in Figure 4.

Whenever a signal is present, the S2050 attempts to achieve synchronization on both bit and transmission-word boundaries of the received encoded bit stream. Received data from the incoming bit stream is provided on the device’s parallel data outputs.

The S2050 accepts serial encoded data from a fiber optic or coaxial cable interface. The serial input stream is the result of the serialization of 8B/10B encoded data by a compatible transmitter. Clock recovery is performed on-chip, with the output data presented to the transmission layer as 10- or 20-bit parallel data. The chip operates at the Gigabit Ethernet frequency of 1250 Mbps.

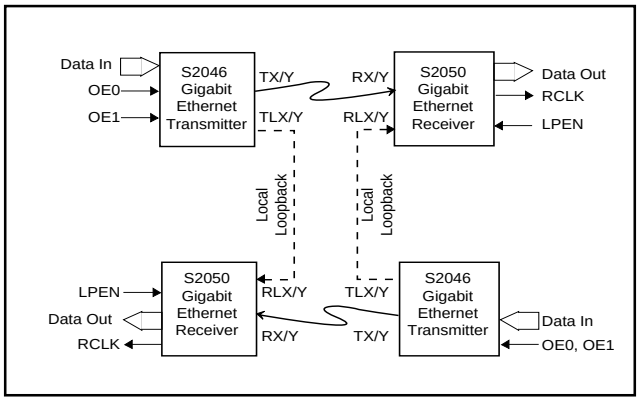
Serial/Parallel Conversion

Serial data is received on the RX, RY pins. The PLL clock recovery circuit will lock to the data stream if the clock to be recovered is within ±100 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The data is then clocked into the serial to parallel output registers. The parallel data out can be either 10 or 20 bits wide determined by the state of the DWS pin. The word clock (RCLKN) is synchronized to the incoming data stream word boundary by the detection of the COMMA synchronization pattern (0011111XXX, positive running disparity).

10-Bit/20-Bit Mode

The S2050 will operate with either 10-bit or 20-bit parallel data outputs. This option is selectable via the DWS pin. See Tables 2 and 3. In 10-bit mode, the 10:bit data word is output on D[10:19], and D[0:9] are driven to the logic high state.

Figure 6. Interface Diagram



Reference Clock Input

The reference clock input must be supplied with a PECL single-ended AC coupled crystal clock source at ±100 PPM tolerance. See Table 3 for reference clock frequencies.

Framing

The S2050 provides SYNC character recognition and data word alignment of the TTL level compatible output data bus. During the data realignment process, the RCLKN phase will be adjusted, and the byte previous to the comma character will be lost. No glitches will occur in the RCLKN signal due to the realignment. In systems where the SYNC detect function is undesired, a LOW on the SYNCEN input disables the SYNC function and the data will be “unframed”.

When framing is disabled by low SYNCEN, the S2050 simply achieves bit synchronization and begins to deliver parallel output data words whenever it has received full transmission words. No attempt is made to synchronize on any particular incoming character.

The SYNC output signal will go high whenever a COMMA character (0011111XXX, positive running disparity) is present on the parallel data outputs. The SYNC output signal will be low at all other times. This is true whether the S2050 is operating in 10-bit mode or in 20-bit mode.

Lock Detect

The S2050 lock detect function indicates the state of the phase-locked loop (PLL) clock recovery unit. The PLL will indicate lock within 2.5µs after the start of receiving serial data inputs. If the serial data inputs have an instantaneous phase jump (from a serial switch, for example) the PLL will not indicate an out-of-lock state, but will recover the correct phase alignment. If a run length of 80-160 bits is exceeded the loop will declare loss of lock. Input data rate variation (compared to REFCLK) can also cause loss of lock. Table 4 shows the response of the PLL loop circuit to input data rate variation. When lock is lost, the PLL will attempt to reacquire bit synchronization, and will shift from the serial input data to the reference clock so that the correct frequency downstream clocking will be maintained.

Table 3. Receiver Operating Modes

DWS	REFSEL	Data Rate (Mbits/sec)	Word Width (Bits)	Reference Clock Frequency (MHz)	RCLK/RCLKN Frequency (MHz)
0	0	1250.0	20	62.50	62.50
1	1	1250.0	10	125.0	62.5

Table 4. Response of PLL Loop Circuit to Input Data Rate Variation

PLL Present State	Input Data Rate Variation (compared to REFCLK)	LOCKDETN	PLL New State
Locked to REFCLK	0 - 244 ppm	H -->L	Locked to input data
	244 - 366 ppm	Indeterminate	Indeterminate
	>366 ppm	H	Locked to REF_CLK
Locked to Input Data	0 - 448 ppm	L	Locked to Input Data
	448 - 732 ppm	Indeterminate	Indeterminate
	>732 ppm	L -->H	Locked to REF_CLK

The LOCKDETN output will go to inactive when no data is present on the serial data inputs. When LOCKDETN is in the inactive state, it indicates that the PLL is locking to the local reference clock to maintain downstream clocking. When LOCKDETN is in the active state, it indicates that the PLL is attempting to lock to the incoming serial data. When serial data is restored, the LOCKDETN output will stay in the active state.

When lock is lost, the PLL will attempt to reacquire bit synchronization, and will shift from the serial input data to the reference clock so that the correct downstream clocking will be maintained. The PLL will continuously shift between the reference clock and the input data until input data has been restored. While the PLL is locked to the reference clock, LOCKDETN will remain active, with one exception: when all of the following conditions are met, the LOCKDETN output toggle between active and inactive, reflecting the internal PLL shift between reference clock and input data: (a) LOCKREFN is not active; (b) the signal (or noise) on the high-speed input is above the voltage input sensitivity threshold; (c) the signal (or noise) on the high-speed input varies from the reference clock by more than 244 ppm, and (d) the signal (or noise) on the high-speed input passes the run length criteria. When these conditions are met, LOCKDETN will toggle, and the RCLK/RCLKN outputs will also shift slightly in frequency.

In any transfer of PLL control from the serial data to the reference clock, the RCLK/RCLKN output remains phase continuous and glitch free, assuring the integrity of downstream clocking.

OTHER OPERATING MODES

Loopback

The S2046 and S2050 have secondary high-speed I/O to provide a local loopback path. The local loopback configuration is shown in Figure 6. When OE1 is active on the S2046, the high-speed data is passed out the TLX/Y output. Operation of the TLX/Y output is independent of the TX/Y output—data can be simultaneously output on both. With LPEN active on the S2050, data on the RLX/Y input is passed through to the parallel output. The local loopback path provides the capability to perform off-line testing and system diagnostics.

Operating Frequency Range

The S2046 and S2050 are optimized for operation at the Gigabit Ethernet rate of 1250.0 Mbit/s. REFCLK must be selected to be within 100 ppm of the desired byte or word clock rate.

Test Modes

The TEST pin on the S2046 and the SYNCEN pin on the S2050 provide a PLL bypass mode that can be used for operating the digital area of the chip. In this mode, clock signals are input through the reference clock pins. This can be used for testing the device during the manufacturing process or during an off-line self-test. Sync detection is always enabled in test mode.

The SYNCEN input on the S2050 must transition through mid-state in less than five REFCLK periods to insure that PLL bypass mode is not exerted. In order to guarantee that the S2050 enters PLL bypass mode, SYNCEN must be held in mid state for more than seven REFCLK cycles.

Table 5. S2046 Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	TTL	I	50 49 48 47 44 43 42 41 38 37 36 35 31 30 29 28 25 24 23 22	Parallel Input Data. Data is clocked in on the rising edge of REFCLK. In 20-bit mode, D[0] is transmitted first. In 10-bit mode, D[10:19] are used, D[0:9] are ignored, and D[10] is transmitted first.
GND	GND	—	20	This pin must be connected to ground.
DWS	Static TTL	I	19	Data Width Select. The level on this pin selects the parallel data bus width. When LOW, a 20-bit parallel bus width is selected, and D[0:19] are active. When HIGH, a 10-bit parallel data bus is selected, D[10:19] are active and D[0:9] are not used. (See Table 1).
OE1	Static TTL	I	1	Active LOW Output Enable control for TLX/TLY outputs. When inactive, TLX/TLY are disabled and remain in the logic low state.
OE0	Static TTL	I	2	Active LOW Output Enable control for TX/TY outputs. When inactive, TX/TY are disabled and remain in the logic low state.
REFCLK	PECL	I	16	Reference Clock. (Externally capacitively coupled.) A crystal-controlled reference clock for the PLL clock multiplier. The frequency of REFCLK is set by the REFSEL pin. (See Table 1.)
TCLK TCLKN	Diff. TTL	O	12 11	Transmit Clock. Differential TTL word rate clock true and complement. See Table 1 for frequency.
TLX TLY	Diff. PECL	O	5 4	Transmit Serial Loopback Output. Differential PECL outputs that are functionally equivalent to TX and TY. They are intended to be used for loopback testing. Enabled by OE1. TLX is the positive output, and TLY is the negative output.
TY TX	Diff. PECL	O	9 8	Transmit Serial Output. Differential PECL outputs that transmit the serial data and drive 150Ω to ground. Enabled by OE0. TX is the positive output, and TY is the negative output.

Table 5. S2046 Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
REFSEL	Static TTL	I	18	Reference Select. Selects the reference clock frequency. (See Table 1.)
ECLVCC	+3.3V	–	21, 39	Core +3.3V
TTLGND	GND	–	14, 15, 34	TTL Ground
TTLVCC	+5V/ 3.3V	–	17	TTL Power Supply
ECLIOVCC	+3.3V	–	3, 10	PECL I/O Power Supply
ECLIOVEE	GND	–	6, 7	PECL I/O GND
AVCC	+3.3V	–	27, 32	Analog Power Supply
AVEE	GND	–	26, 33	Analog Ground
ECLVEE	GND	–	13, 40, 51, 52	Core Ground
NC	–	–	45, 46	Not Connected

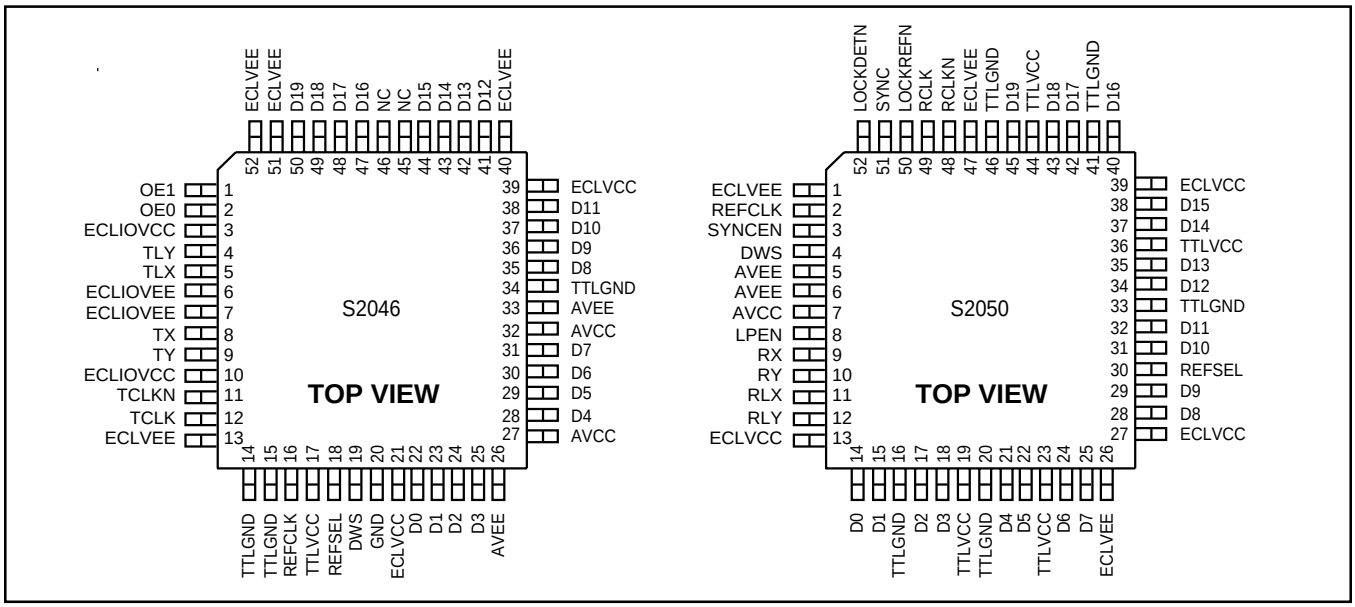
Table 6. S2050 Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	TTL	O	45 43 42 40 38 37 35 34 32 31 29 28 25 24 22 21 18 17 15 14	Parallel output data. The width of the parallel data bus is selected by the state of the DWS pin. Parallel data on this bus is clocked out on the falling edge of RCLK. In 20-bit mode, D[0] is the first bit received. In 10-bit mode, D[19:10] are used and D[9:0] are driven to the high state. In 10-bit mode, D[10] is the first bit received.
LOCKDETN	TTL	O	52	Lock Detect. Active Low. When active, LOCKDETN indicates that the PLL is locked to the incoming data stream. When inactive, it provides a system flag indicating that the PLL is locked to the local reference clock.
LPEN	TTL	I	8	Loop Enable. Active High. When active, LPEN selects the loopback differential serial input pins (RLX, RLY). When inactive, LPEN selects RX and RY (normal operation).
DWS	Static TTL	I	4	Data Width Select. The level on this pin selects the parallel data bus width. When LOW, a 20-bit parallel bus width is selected, and D[19:0] are active. When HIGH, a 10-bit parallel data bus is selected, D[19:10] are active and D[9:0] will go HIGH. (See Table 3.) A rising edge will reset the internal counters (used for test).
RCLK RCLKN	Diff. TTL	O	49 48	Receive Clock. Parallel data is clocked out on the falling edge of RCLK/RCLKN. After a sync word is detected, the period of the current RCLK and RCLKN is stretched to align with the word boundary. (See Table 3 for frequency.)
REFCLK	PECL	I	2	Reference Clock. (Externally capacitively coupled.) A free-running crystal-controlled reference clock for the PLL clock multiplier. The frequency of REFCLK is set by the REFSEL pin. (See Table 3.)
SYNC	TTL	O	51	Sync (Framing) Detected. Active High. Upon detection of a valid sync symbol (COMMA: 0011111XXX, positive running disparity), this output goes active for one RCLK period. When SYNC is active, the sync symbol is present on the parallel data bus bits D[9:0] in 20-bit mode or D[19:10] in 10-bit mode. SYNC is gated by SYNCEN.
RLX RLY	Diff. PECL	I	11 12	Receive Loopback Serial Inputs. (Externally capacitively coupled.) The serial loopback data inputs. RLX is the positive input, and RLY is the negative input.

Table 6. S2050 Pin Assignment and Descriptions (Continued)

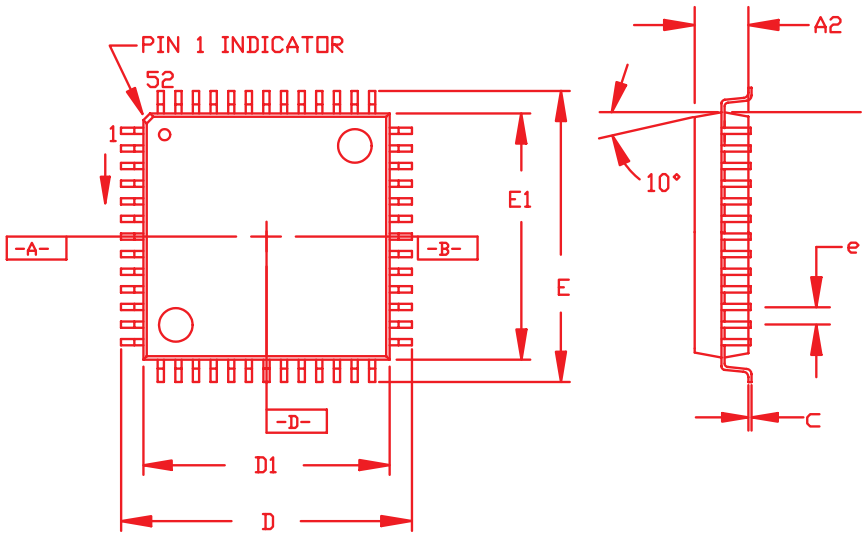
Pin Name	Level	I/O	Pin #	Description
RX RY	Diff. PECL	I	9 10	Receive Serial Input. (Externally capacitively coupled.) The received serial data inputs. RX is the positive input, and RY is the negative input.
SYNCEN	Static TTL	I	3	Enable Sync (Framing). Active High. (Multilevel.) When Active, enables SYNC output. When inactive data is treated as unframed data. Holding this input at mid-level for more than seven REFCLK cycles puts the device in PLL bypass (test) mode.
REFSEL	Static TTL	I	30	Reference Select. Input used to select the reference clock frequency. (See Table 3.)
LOCK_REFN	TTL	I	50	Lock to Reference. Active Low. When active, forces the PLL to lock to the REFCLK input and ignore the serial data inputs. When inactive, PLL locks to the serial data input (normal operation).
TTLVCC	+5V/ 3.3V	–	19, 23, 36, 44	TTL Power Supply
TTLGND	GND	–	16, 20, 33, 41, 46	TTL Ground
ECLVCC	+3.3V	–	13, 27, 39	Core Power Supply
ECLVEE	GND	–	1, 26, 47	Core Ground
AVCC	+3.3V	–	7	Analog Power Supply
AVEE	GND	–	5, 6	Analog Ground

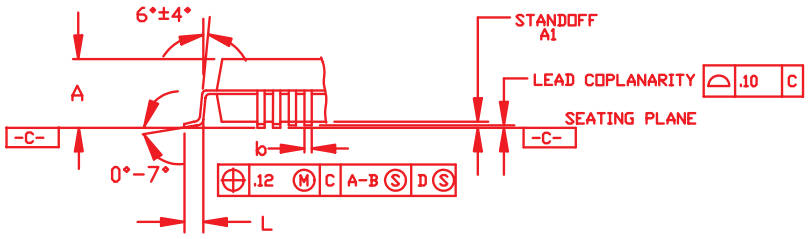
Figure 7. S2046 and S2050 52 PQFP Pinouts



TTLVCC = +5 V or +3.3 V for S2046 and S2050A; +3.3 V for S2050A-3
AVCC = +3.3 V
ECLVCC = +3.3 V
ECLIOVCC = +3.3 V
ECLIOVEE = 0V
TTLGND = 0V
ECLVEE = 0V
AVEE = 0V

Figure 8. 52 PQFP-HS — (10mm x 10mm) Plastic Quad Flat Pack





DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.25	1.95	12.95	9.90	12.95	9.90	0.73	0.65 BSC.	0.25	
NOM			2.00	13.20	10.00	13.20	10.00	0.88		0.30	
MAX	2.45	0.50	2.10	13.45	10.10	13.45	10.10	1.03		0.35	0.17

Table 7. Thermal Management

Device	Θja (Still Air)
S2046B	50 ˚ C/W
S2050A	50 ˚ C/W
S2050A-3	50 ˚ C/W

Table 8. Absolute Maximum Ratings

The following are the absolute maximum device stress ratings. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only. Operation of the device at these or any other conditions beyond those indicated in the electrical characteristics section of this document is not implied.

Parameter	Min	Typ	Max	Units
Case Temperature Under Bias	-55		125	˚C
Junction Temperature Under Bias	-55		150	˚C
Storage Temperature	-65		150	˚C
Voltage on VCC with Respect to Ground	-0.5		+7.0	V
Voltage on any TTL Input Pin	-0.7		VCC +.6V	V
Voltage on any PECL Input Pin	0		ECLVCC	V
TTL Output Sink Current			8	mA
TTL Output Source Current			8	mA
High Speed PECL Output Source Current			50	mA

Electrostatic Discharge (ESD) Ratings.
The S2046 and S2050 are rated to the following ESD voltages based on the human body model. All pins are rated above 500 V.

Table 9. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	0		70	˚C
Junction Temperature Under Bias			130	˚C
Voltage on TTLVCC with Respect to GND 5V Operation 3.3V Operation	 4.75 3.13	 5.0 3.3	 5.25 3.47	 V V
Voltage on any TTL Input Pin	0		5.25	V
Voltage on ECLVCC with Respect to GND	3.13	3.3	3.47	V
Voltage on any PECL Input Pin	ECLVCC -2.0		ECLVCC	V

Table 10. S2046 DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage (TTL) 3.3V Power Supply 3.3V Power Supply 5V Power Supply	 2.1 2.2 2.7			 V V V	 V_{CC} = min, I_{OH} = -2.4mA V_{CC} = min, I_{OH} = -.1mA V_{CC} = min, I_{OH} = -1mA
V_{OL}	Output LOW Voltage (TTL) 3.3V Power Supply 5V Power Supply			 .5 .5	 V V	 V_{CC} = min, I_{OL} = 2.4mA V_{CC} = min, I_{OL} = 4mA
V_{IH}	Input HIGH Voltage (TTL)	2.0	—		V	—
V_{IL}	Input LOW Voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH Current (TTL)	—	—	50	µA	V_{IN} = 2.4V
I_{IL}	Input LOW Current (TTL)	-500	—	-50	µA	V_{IN} = 0.5V
I_{CC}	Supply Current		123	160	mA	Outputs open, V_{CC} = V_{CC} max
P_D	Power Dissipation		.406	.554	W	Outputs open, V_{CC} = V_{CC} max
ΔV_{INCLK}	Single-ended REFCLK input swing	440	—	1300	mV	AC coupled
ΔV_{OUT}	Serial Output Voltage Swing	600	—	1300	mV	50Ω to V_{CC} -2.0V

Table 11. S2050 DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage (TTL) 3.3V Power Supply 3.3V Power Supply 5V Power Supply	 2.1 2.2 2.7			 V V V	 V_{CC} = min, I_{OH} = -2.4mA V_{CC} = min, I_{OH} = -.1mA V_{CC} = min, I_{OH} = -1mA
V_{OL}	Output LOW Voltage (TTL) 3.3V Power Supply 5V Power Supply			 .5 .5	 V V	 V_{CC} = min, I_{OL} = 2.4mA V_{CC} = min, I_{OL} = 4mA
V_{IH}	Input HIGH Voltage (TTL)	2.0	—	—	V	
V_{IL}	Input LOW Voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH Current (TTL)	—	—	50	µA	V_{IN} = 2.4V
I_{IL}	Input LOW Current (TTL)	-500	—	-50	µA	V_{IN} = 0.5V
I_{CC}	Supply Current		255	280	mA	Outputs open, V_{CC} = V_{CC} max
P_D	Power Dissipation 3.3V Supply 5V Supply		 0.91 1.1	 1.0 1.2	 W W	 Outputs open, V_{CC} = V_{CC} max Outputs open, V_{CC} = V_{CC} max
ΔV_{INCLK}	Single-ended REFCLK input swing	440	—	1300	mV	AC coupled
V_{DIFF}	Min. differential input voltage swing for differential PECL inputs	100		1300	mV	

Table 12. Reference Clock Requirements

Parameters	Description	Min	Max	Units	Conditions
FT	Frequency Tolerance S2046	-100	+100	ppm	–
FT	Frequency Tolerance S2050	-100	+100	ppm	–
TD_{1-2}	Symmetry	40	60	%	Duty Cycle at 50% pt.
T_{RCR}, T_{RCF}	REFCLK Rise and Fall Time	0.5	3.2	ns	20-80%
–	Random Jitter	-	100	ps	Peak-to-Peak

Table 13. Transmitter Timing

Parameters	Description	Min	Max	Units	Conditions
T_1	Data Setup w.r.t. ↑ REFCLK	2.0	-	ns	10 Bit.[1]
T_2	Data Hold w.r.t. ↑ REFCLK	1.0	-	ns	10 Bit.[1]
T_3	Data Setup w.r.t. ↑ REFCLK	2.0	-	ns	20 Bit.[1]
T_4	Data Hold w.r.t. ↑ REFCLK	2.0	-	ns	20 Bit.[1]
Total Jitter	Serial Data Output Total Jitter	-	192	ps	Peak-to-peak tested on a sample basis, 2^7–1 pattern.
T_{DJ}	Serial Data Output Determinsitic Jitter	-	80	ps	Peak-to-peak tested on a sample basis, IDLE pattern. Note: Random jitter is not measured, but can be calculated to be 112 ps p-p.
T_{SDR}, T_{SDF}	Serial Data Rise and Fall Time	-	300	ps	20% to 80% tested on a sample basis.
T_{SYNCEN}	SYNCEN Rise and Fall Time	-	20	ns	Rise, fall of SYNCEN input must not exceed this value.

1. All AC measurements are made from the reference voltage level of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Table 13. Receiver Timing

Parameters	Description	Min	Max	Units	Conditions
$T_{Lock\ Startup}$	Data Acquision Lock Time at Startup	-	2.5	µs	8B/10B IDLE pattern, sample basis.
$R_{SDR,}$ R_{SDF}	Serial Input Data Rise and Fall Time	-	300	ps	20% to 80% tested on a sample basis.
T_5	RCLKN to RCLK Skew	1.5	-	ns	
T_6	Data Setup w.r.t. ↑ RCLK/RCLKN	2.5	-	ns	10 Bit (see note).
T_7	Data Hold w.r.t. ↑ RCLK/RCLKN	1.5	-	ns	10 Bit (see note).
T_8	Data Setup w.r.t. ↓ RCLKN	2.1	-	ns	20 Bit (see note).
T_9	Data Hold w.r.t. ↓ RCLKN	6.3	-	ns	20 Bit (see note).
T_{DR}	Data Output Rise Time	-	2.4	ns	0.8 to 2.0V, 10 pF load.
T_{DF}	Data Output Fall Time	-	2.4	ns	0.8 to 2.0V, 10 pF load.
T_R	RCLK/RCLKN Rise Time	-	3.0	ns	
T_F	RCLK/RCLKN Fall Time	-	3.0	ns	
Duty Cycle	RCLK/RCLKN Duty Cycle	40	60	%	
T_J	Jitter Tolerance. Input data eye opening allocation at receiver for BER 1E-12.	599		ps	As specified in IEEE 802.3z (see Figure 19).
T_{DJ}	Determinstic Jitter Tolerance. Deterministic component of input jitter for jitter tolerance measurement	370		ps	As specified in IEEE 802.3z (see Figure 19).

Note: All AC measurements are made from the reference voltage level of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Figure 11. Transmitter Timing Diagram (10-bit Mode)

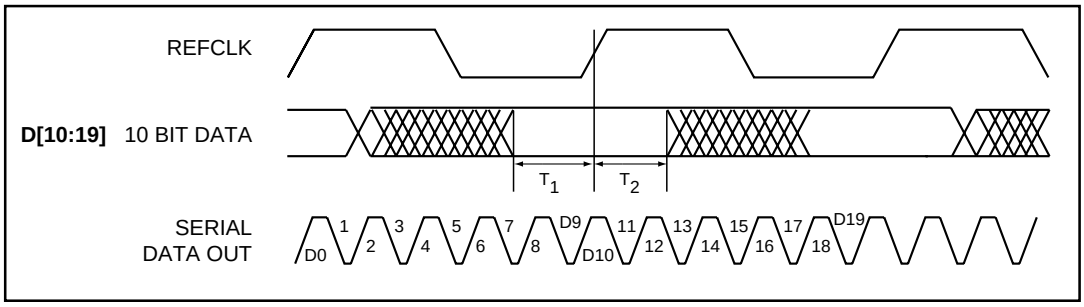


Figure 12. Receiver Timing Diagram (20-bit Mode)

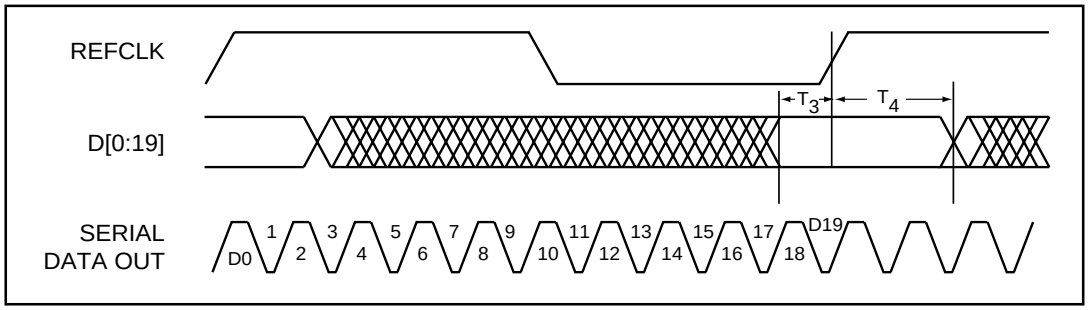


Figure 13. Receiver Timing Diagram (10-bit Mode)

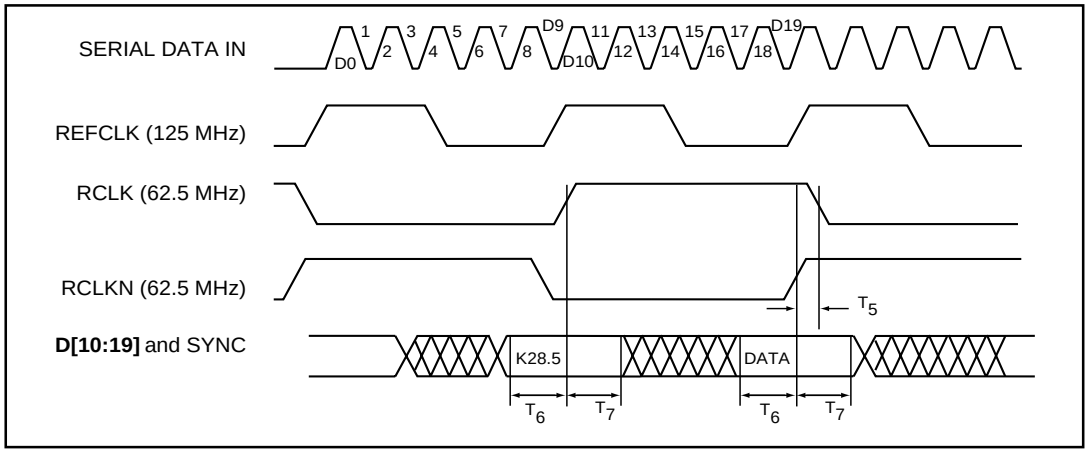


Figure 14. Receiver Timing Diagram (20-bit Mode)

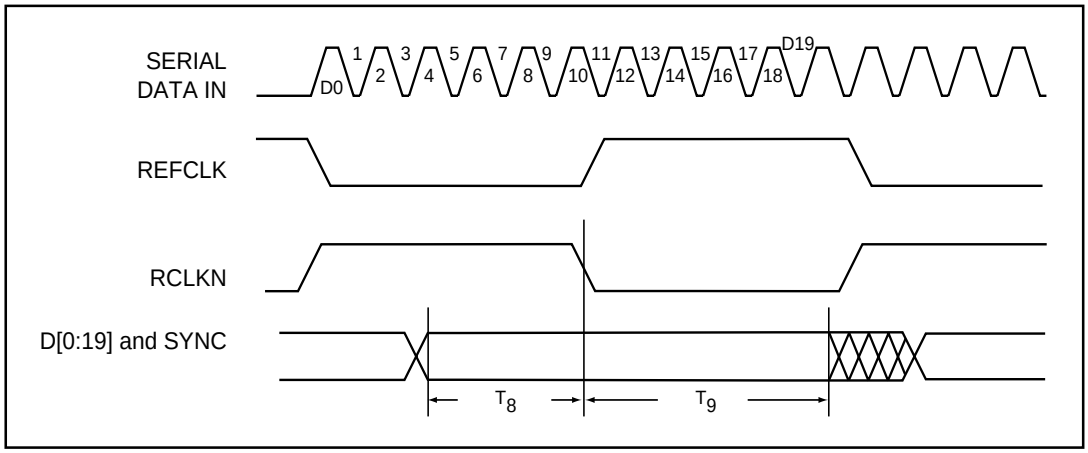


Figure 15. Serial Input Rise and Fall Time

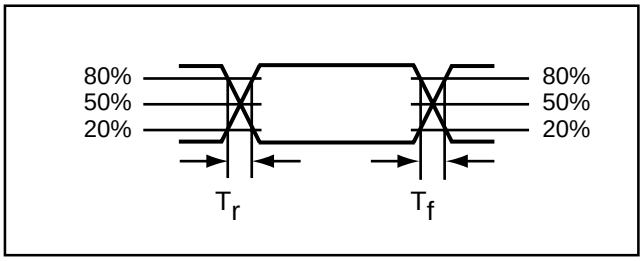


Figure 16. Serial Output Load

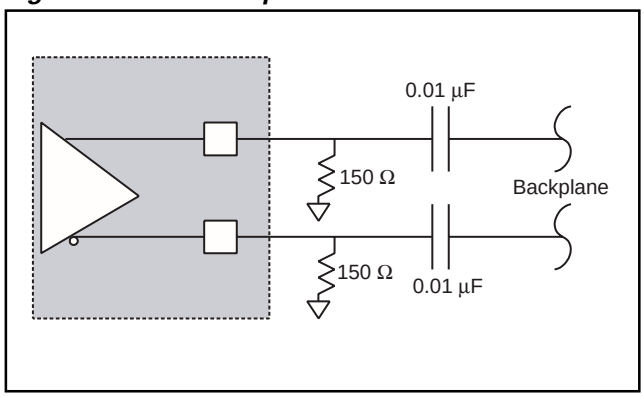


Figure 17. High Speed Differential Inputs

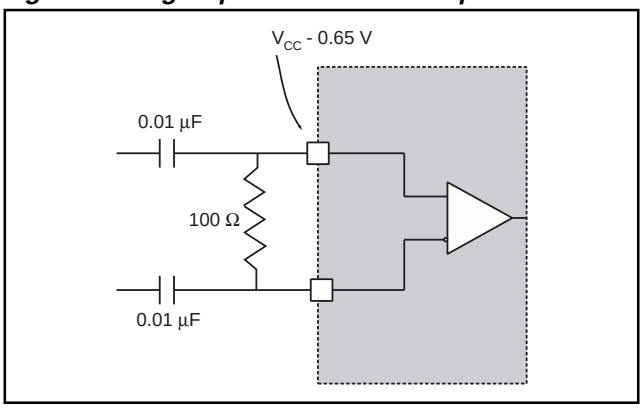


Figure 18. TTL Input Rise and Fall Time

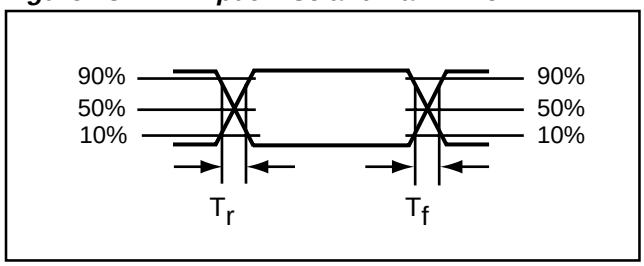


Figure 19. Receiver Input Eye Diagram Jitter Mask

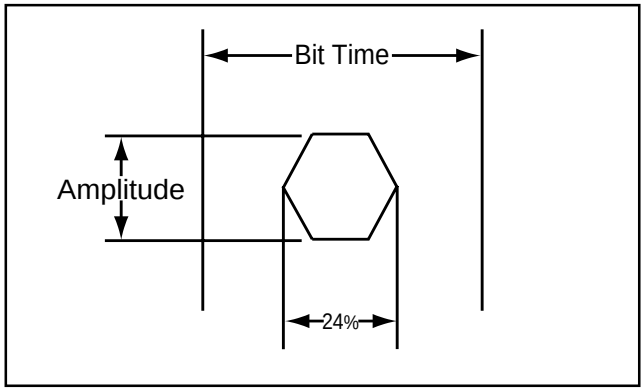
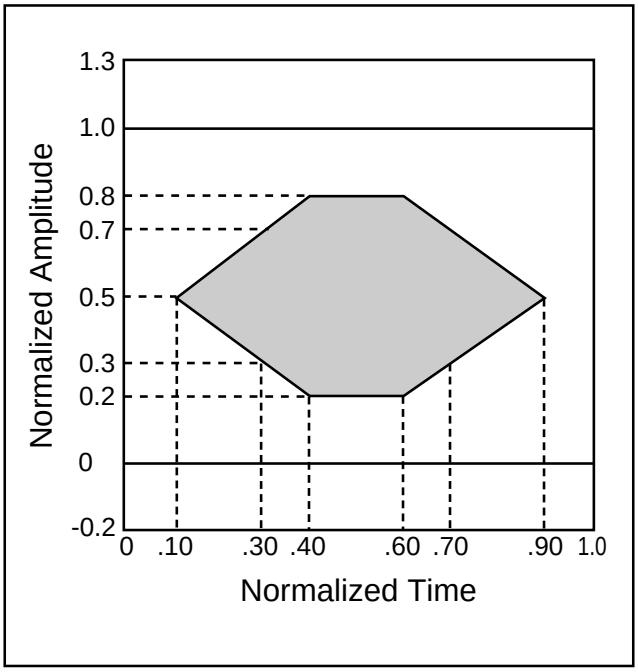
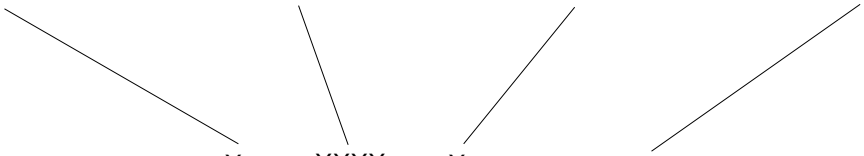


Figure 20. Acquisition Time Eye Diagram



Ordering Information

GRADE	TRANSMITTER	PACKAGE and VOLTAGE RATING	SHIPPING CONFIGURATION
S = Commercial	2046	B = 52 PQFP, +5 V OR +3.3 V I/O	Blank = trays /D = dry pack /TD = tape, reel, and dry pack
GRADE	**RECEIVER**	**PACKAGE**	**SHIPPING CONFIGURATION**
S = Commercial	2050	A = 52 PQFP, +5 V OR+3.3 V I/O A-3 = 52 PQFP, +3.3 V I/O only	Blank = trays /D = dry pack /TD = tape, reel, and dry pack



Example: S2046B-5—S2046 in a 52 PQFP package shipped in trays.

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