S3005/S3006 EVALUATION BOARD S6004

EVALUATION BOARD DESCRIPTION

The S6004 SONET Evaluation Board allows demonstration of AMCC's S3005 and S3006 SONET/SDH OC-3/12 transmitter/receiver chipset. This data sheet provides information on board contents and layout. It should be used in conjunction with the S3005/S3006 data sheets, which contain full technical details on chip operation.

Figure 1 depicts the layout of the evaluation board, showing the location of connectors and components. Power is supplied to the board from external supplies connected through the on-board banana jacks. Connectors allow easy access to all of the interface signals on the S3005/S3006 chips.

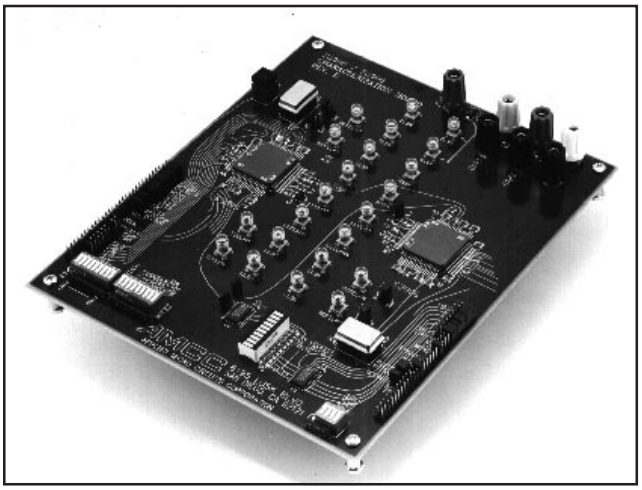
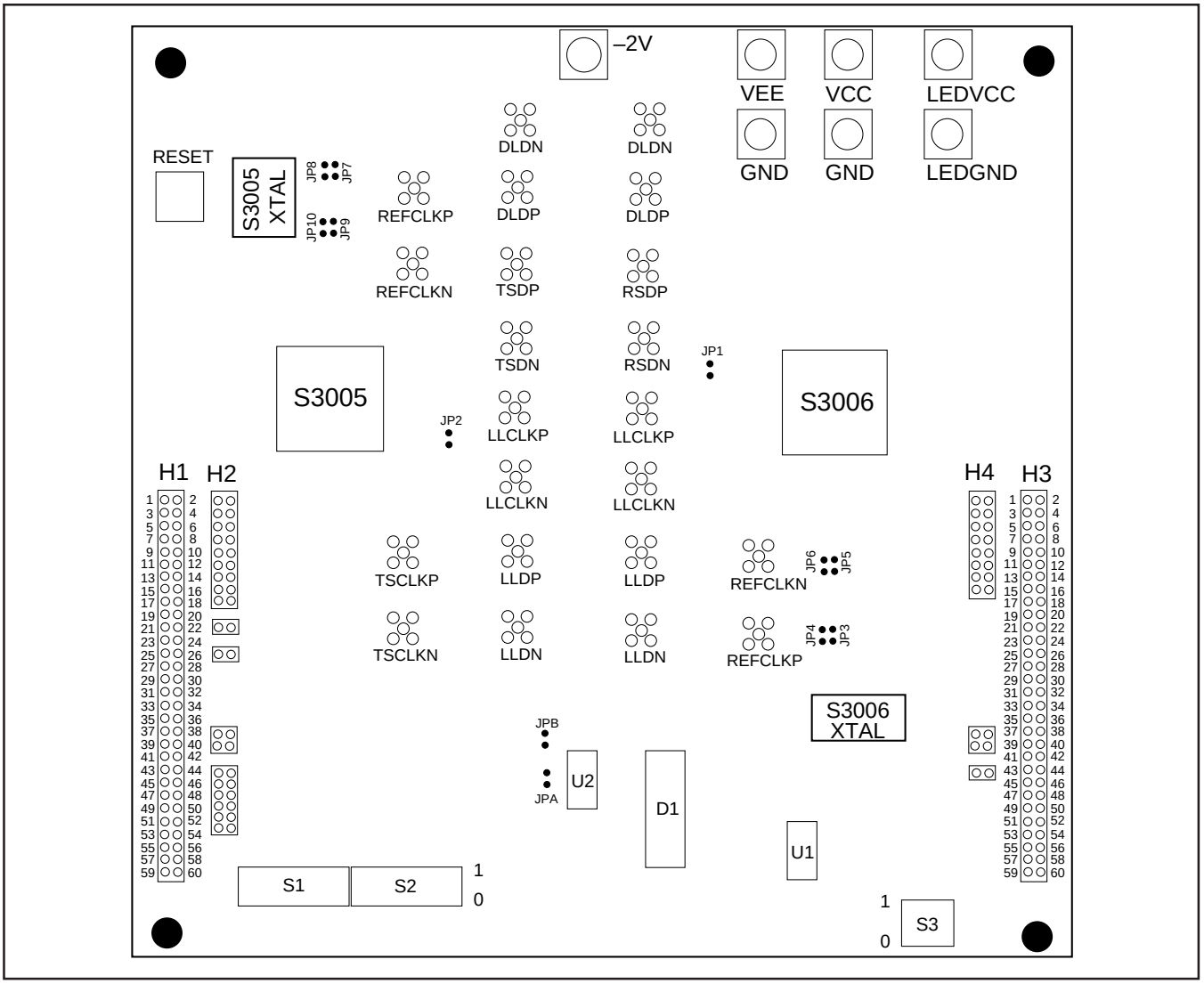


Figure 1. Board Layout



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ELECTRICAL CONNECTIONS

The 60-pin header strips H1 and H3 allow simple ribbon cable connections to and from a user-provided pattern generator. Parallel data can be input to the S3005 transmitter either through the connector pins, or by using DIP switch S1. The on-board LED bank provides checks on output signals. DIP switches S1, S2, and S3 allow access to the control signals of both the S3005 and S3006 chips.

Banana jacks are provided for the power connections. Coaxial SMA connectors are used for serial data link and external reference clock connections.

Refer to Figure 1 for locations of the connectors discussed in the following sections. All connectors, controls, and jumpers are labeled on the board.

Power Connections

Power connections are made through the on-board banana jacks (VCC, VEE, GND, LEDVCC, and LEDGND). Refer to Table 1 for recommended operating conditions. A –2V connection provides proper on-board termination for the DLDP/N outputs of the S3005 when connected to the DLDP/N inputs of the S3006.

Table 1. Power Connection Recommended Operating Conditions

Power Supply	Nominal Input Voltage
VCC	5 V
Ground	0 V
VEE	-4.5 or -5.2V
LEDVCC	5 V

Table 2. H1 Pin Descriptions

Pin Names	Pin No.	Level	I/O	Description	Pin Names	Pin No.	Level	I/O	Description
GND	1	-	-	Ground	GND	31	-	-	Ground
SYNC	2	TTL	I	Synchronization Enable	PCLK	32	TTL/CMOS	O	Parallel Clock
GND	3	-	-	Ground	GND	33	-	-	Ground
REFSEL1	4	TTL	I	Reference Select 1	GND	34	-	-	Ground
GND	5	-	-	Ground	GND	35	-	-	Ground
REFSEL0	6	TTL	I	Reference Select 0	LOCKDET	36	TTL	O	Lock Detect
GND	7	-	-	Ground	GND	37	-	-	Ground
MODE2	8	TTL	I	Mode Select 2	PIN0	38	TTL	I	Parallel data input
GND	9	-	-	Ground	GND	39	-	-	Ground
MODE1	10	TTL	I	Mode Select 1	PIN1	40	TTL	I	Parallel data input
GND	11	-	-	Ground	GND	41	-	-	Ground
MODE0	12	TTL	I	Mode Select 0	GND	42	-	-	Ground
GND	13	-	-	Ground	GND	43	-	-	Ground
DLCV	14	TTL	I	Diag. Line Code Violation	PIN2	44	TTL	I	Parallel data input
GND	15	-	-	Ground	GND	45	-	-	Ground
DLEB	16	TTL	I	Diag. Loopback Enable	PIN3	46	TTL	I	Parallel data input
GND	17	-	-	Ground	GND	47	-	-	Ground
LLEB	18	TTL	I	Line Loopback Enable	PIN4	48	TTL	I	Parallel data input
GND	19	-	-	Ground	GND	49	-	-	Ground
PAE	20	TTL/CMOS	O	Phase Alignment Event	PIN5	50	TTL	I	Parallel data input
GND	21	-	-	Ground	GND	51	-	-	Ground
RSTB	22	TTL	I	Master Reset	PIN6	52	TTL	I	Parallel data input
GND	23	-	-	Ground	GND	53	-	-	Ground
BYTCLKIP	24	TTL/CMOS	O	Reference Feedback Clock	PIN7	54	TTL	I	Parallel data input
GND	25	-	-	Ground	GND	55	-	-	Ground
TESTEN	26	TTL	I	Test Clock Enable	GND	56	-	-	Ground
GND	27	-	-	Ground	GND	57	-	-	Ground
PICLK	28	TTL	I	Parallel Input Clock	GND	58	-	-	Ground
GND	29	-	-	Ground	GND	59	-	-	Ground
GND	30	–	–	Ground	GND	60	-	-	Ground

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Transmitter Signals—Headers H1 and H2

Header H1 allows connection to a 60-pin ribbon cable or to single discrete cables. Controls for signals RSTB, DLEB, MODE0, and MODE1 are common to both transmitter and receiver and can be controlled via header H1. These signals can also be controlled by dipswitch S2 if H2 jumpers are installed.

Header H2 allows for DIP SWITCH control of signals SYNC, REFSEL [1:0], MODE [2:0], DLCV, DLEB, LLEB, TESTEN, and PIN[7:0]. Control of each signal will be transferred to the corresponding DIP switch SI or S2 when the corresponding jumpers are installed on H2. (See Table 3.)

Table 3. H2 Pin Descriptions

Pin Names	Pin No.	Level	I/O	Description
SYNC	1	TTL	Input	SYNC input (pin 58) of S3005
SYNC	2	TTL	Input	DIP Switch S2 position 9
REFSEL1	3	TTL	Input	REFSEL1 input (pin 28) of S3005
REFSEL1	4	TTL	Input	DIP Switch S2 position 8
REFSEL0	5	TTL	Input	REFSEL0 input (pin 27) of S3005
REFSEL0	6	TTL	Input	DIP Switch S2 position 7
MODE2	7	TTL	Input	MODE2 input (pin 66) of S3005
MODE2	8	TTL	Input	DIP Switch S2 position 6
MODE1	9	TTL	Input	MODE1 input (pin 63) of S3005 and (pin 28) of S3006
MODE1	10	TTL	Input	DIP Switch S2 position 5
MODE0	11	TTL	Input	MODE0 input (pin 65) of S3005 and (pin 29) of S3006
MODE0	12	TTL	Input	DIP Switch S2 position 4
DLCV	13	TTL	Input	DLCV input (pin 59) of S3005
DLCV	14	TTL	Input	DIP Switch S2 position 3
DLEB	15	TTL	Input	DLEB input (pin 26) of S3005 and (pin 57) of S3006
DLEB	16	TTL	Input	DIP Switch S2 position 2
LLEB	17	TTL	Input	LLEB input (pin 57) of S3005
LLEB	18	TTL	Input	DIP Switch S2 position 1
RSTB	19	TTL	Input	RSTB input (pin 29) of S3005 and (pin 21) of S3006
RSTB	20	TTL	Input	RESET switch
TESTEN	21	TTL	Input	TESTEN input (pin 31) of S3005
TESTEN	22	TTL	Input	DIP Switch S1 position 9
PIN0	23	TTL	Input	PIN0 input (pin 14) of S3005
PIN0	24	TTL	Input	DIP Switch S1 position 8
PIN1	25	TTL	Input	PIN1 input (pin 12) of S3005
PIN1	26	TTL	Input	DIP Switch S1 position 7
PIN2	27	TTL	Input	PIN2 input (pin 10) of S3005
PIN2	28	TTL	Input	DIP Switch S1 position 6
PIN3	29	TTL	Input	PIN3 input (pin 9) of S3005
PIN3	30	TTL	Input	DIP Switch S1 position 5
PIN4	31	TTL	Input	PIN4 input (pin 8) of S3005
PIN4	32	TTL	Input	DIP Switch S1 position 4
PIN5	33	TTL	Input	PIN5 input (pin 5) of S3005
PIN5	34	TTL	Input	DIP Switch S1 position 3
PIN6	35	TTL	Input	PIN6 input (pin 3) of S3005
PIN6	36	TTL	Input	DIP Switch S1 position 2
PIN7	37	TTL	Input	PIN7 input (pin 2) of S3005
PIN7	38	TTL	Input	DIP Switch S1 position 1

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Receiver Signals—Headers H3 and H4

Header H3 allows connection to a 60-pin ribbon cable or to single discrete cables. (Controls for signals RSTB, DLEB, MODE0, and MODE1 are common to both the transmitter and receiver and can be controlled via header H1. These signals can also be controlled by dipswitch S2 if H2 jumpers are installed. Mode2 is controlled via header H3. If the Mode2 jumper is installed, the Mode2 input will be low. If the Mode2 jumper is not installed, the Mode2 input will float to a high state.) When the associated pins on header H4 are jumpered, signals REFSEL [1:0] and TESTRST will be connected to DIP SWITCH S3. (See Table 3.) Without using any jumpers on these signal pins, they can be accessed directly by a 60-pin ribbon cable attached to header H3. Signal pins POUT [7:0] are always tied to LED bank D1, and can also be accessed by the same 60-pin ribbon cable by jumpering those outputs on header H4. Refer to Table 4 for pin descriptions of Header H3.

RESET

When the RSTB pins on Header H2 are shorted to each other, the push button switch on the top left of the board is connected to the S3005 and S3006 RSTB Master Reset inputs.

CRYSTAL REFERENCES AND CLOCK GENERATION

Two 19.44-MHz differential ECL crystal oscillators with 100-ppm stability are provided, one each for the transmitter and receiver. If a higher reference frequency is needed (38.88, 51.84, or 77.76 MHz), it can be selected by setting the two reference select input pins. The correct frequency is set with the REFSEL[1:0] inputs as shown in Table 6.

The output clock frequency can be 155.52 MHz (STS-3), 311.04 MHz (STS-3 CMI), or 622.08 MHz (STS-12). The output frequency is set with the MODE[2:0] inputs as shown in Table 7.

Table 4. H3 Pin Description

Pin Names	Pin No.	Level	I/O	Description	Pin Names	Pin No.	Level	I/O	Description
GND	1	-	-	Ground	GND	31	-	-	Ground
POUT0	2	TTL/CMOS	O	Parallel data output	POCLK	32	TTL/CMOS	O	Parallel Output Clock
GND	3	-	-	Ground	GND	33	-	-	Ground
POUT1	4	TTL/CMOS	O	Parallel data output	GND	34	-	-	Ground
GND	5	-	-	Ground	GND	35	-	-	Ground
POUT2	6	TTL/CMOS	O	Parallel data output	TESTEN	36	TTL	I	Test Clock Enable
GND	7	-	-	Ground	GND	37	-	-	Ground
POUT3	8	TTL/CMOS	O	Parallel data output	REFSEL1	38	TTL	I	Reference Select 1
GND	9	-	-	Ground	GND	39	-	-	Ground
POUT4	10	TTL/CMOS	O	Parallel data output	REFSEL0	40	TTL	I	Reference Select 0
GND	11	-	-	Ground	GND	41	-	-	Ground
POUT5	12	TTL/CMOS	O	Parallel data output	GND	42	-	-	Ground
GND	13	-	-	Ground	GND	43	-	-	Ground
POUT6	14	TTL/CMOS	O	Parallel data output	TESTRST	44	TTL	I	Test Reset
GND	15	-	-	Ground	GND	45	-	-	Ground
POUT7	16	TTL/CMOS	O	Parallel data output	LCV	46	TTL/CMOS	O	Line Code Violation
GND	17	-	-	Ground	GND	47	-	-	Ground
LOCKDET	18	TTL	O	Lock Detect	FP	48	TTL/CMOS	O	Frame Pulse
GND	19	-	-	Ground	GND	49	-	-	Ground
OOF	20	TTL	I	Out of Frame	-	50	-	-	-
GND	21	-	-	Ground	GND	51	-	-	Ground
LOS	22	ECL	I	Loss of Signal	-	52	-	-	-
GND	23	-	-	Ground	GND	53	-	-	Ground
MODE2	24	TTL	I	Operating Mode	-	54	-	-	-
GND	25	-	-	Ground	GND	55	-	-	Ground
-	26	-	-	-	GND	56	-	-	Ground
GND	27	-	-	Ground	GND	57	-	-	Ground
BYTCLKIP	28	TTL/CMOS	O	Ref. Feedback Clock	GND	58	-	-	Ground
GND	29	-	-	Ground	GND	59	-	-	Ground
GND	30	-	-	Ground	GND	60	-	-	Ground

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To use the S3005 crystal oscillator as its reference, install jumpers on JP8 and JP10. To use an external reference clock through the S3005 REFCLKP/N SMA connector, install jumpers on JP7 and JP9. To use the S3006 crystal oscillator as its reference, install jumpers on JP3 and JP5. To use an external reference clock through the S3006 REFCLKP/N SMA connector, install jumpers on JP4 and JP6. (See Table 9, Jumpers.)

LEDs

The bank of 10 LEDs (D1) display when the S3005/S3006 chips are locked, and also light when the appropriate POUT is in the high state. The function of each LED is shown in Table 8, and is also labeled on the board.

SMA Connectors

SMA connectors provide input/output capability for a number of signals, including serial data I/O and reference clocks. These connectors are labeled on the board and are also shown in Figure 1.

Jumpers

A number of jumpers allow the user to control various aspects of the characterization procedure. The function of each jumper is described in Table 9.

Table 6. REFSEL Settings

REFSEL1	REFSEL0	FREQUENCY
0	0	19.44 MHz
0	1	38.88 MHz
1	0	51.84 MHz
1	1	77.76 MHz

Table 7. Output Clock Frequency Settings

FREQ.	BYPASS MODE (TESTEN = 1)			NORMAL MODE (TESTEN = 0)		
	Mode2	Mode1	Mode0	Mode2	Mode1	Mode0
622.08 MHz	1	0	0	1	0	0
311.04 MHz	1	0	1	0	0	1
155.52 MHz	1	1	0	0	1	0

Table 5. H4 Pin Description

Pin Names	Pin No.	Level	I/O	Description
POUT0	1	TTL/CMOS	Output	POUT0 output (pin 14) of S3006
POUT0	2	TTL/CMOS	Output	Connected to H3 pin 2
POUT1	3	TTL/CMOS	Output	POUT1 output (pin 12) of S3006
POUT1	4	TTL/CMOS	Output	Connected to H3 pin 4
POUT2	5	TTL/CMOS	Output	POUT2 output (pin 10) of S3006
POUT2	6	TTL/CMOS	Output	Connected to H3 pin 6
POUT3	7	TTL/CMOS	Output	POUT3 output (pin 9) of S3006
POUT3	8	TTL/CMOS	Output	Connected to H3 pin 8
POUT4	9	TTL/CMOS	Output	POUT4 output (pin 8) of S3006
POUT4	10	TTL/CMOS	Output	Connected to H3 pin 10
POUT5	11	TTL/CMOS	Output	POUT5 output (pin 5) of S3006
POUT5	12	TTL/CMOS	Output	Connected to H3 pin 12
POUT6	13	TTL/CMOS	Output	POUT6 output (pin 3) of S3006
POUT6	14	TTL/CMOS	Output	Connected to H3 pin 14
POUT7	15	TTL/CMOS	Output	POUT7 output (pin 2) of S3006
POUT7	16	TTL/CMOS	Output	Connected to H3 pin 16
REFSEL1	17	TTL	Input	Dip Switch S3 position 1
REFSEL1	18	TTL	Input	Connected to H3 pin 38
REFSEL0	19	TTL	Input	Dip Switch S3 position 2
REFSEL0	20	TTL	Input	Connected to H3 pin 40
TESTRST	21	TTL	Input	Dip Switch S3 position 3
TESTRST	22	TTL	Input	Connected to H3 pin 44

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BIT ERROR RATE TEST PROCEDURE

The following method is commonly used to run a serial Bit Error Rate (BER) test on the S3006 device in STS-12 mode. This allows the use of a serial-out/serial-in bit error rate tester to verify the PLL frequency/phase lock capabilities and jitter tolerance testing.

1. Connect jumper wires between POUT[7:0] (H3 pins 2, 4, 6, 8, 10, 12, 14, 16) on the S3006 and PIN[7:0] (H1 pins 38, 40, 44, 46, 48, 50, 52, 54) on the S3005.

2. Connect a jumper wire between POCLK (H3 pin 32) on the S3006 and PICLK (H1 pin 28) on the S3005.

3. Connect the LLCLKP/N outputs of the S3006 to the REFCLKP/N inputs of the S3005 using SMA cables. (Be sure that jumpers JP7 and JP9 are connected and jumpers JP8 and JP10 are disconnected, as required when the S3005 REFCLKP/N SMA connectors are used for an external reference.)

4. Set TESTEN (H1 pin 26) on the S3005 High, to put the S3005 into bypass mode, which bypasses the PLL-generated clock source and enables the use of the REFCLKP/N as the bit rate clock input. (Note that in bypass mode, the frequency of the REFCLK must be appropriate for the desired data rate. Refer to the data sheet for more information.) Mode [2, 1, 0] should be 1, 0, 0 on both the S3005 and S3006.

At this point, serial data can be directed to the S3006, the parallel output data from the S3006 can be wrapped back to the parallel inputs of the S3005, and the serial outputs of the S3005 can be monitored.

Table 8. LEDs

LED	Function
D1-A	Tx LOCKDET
D1-B	Rx LOCKDET
D1-C	POUT0
D1-D	POUT1
D1-E	POUT2
D1-F	POUT3
D1-G	POUT4
D1-H	POUT5
D1-I	POUT6
D1-J	POUT7

Table 9. Jumpers

Jumper	Function
JP1	Connects S3006 op-amp power supply to enable S3006 PLL to function
JP2	Connects S3005 op-amp power supply to enable S3005 PLL to function
JP3, JP5	Connects on-board XTAL oscillator to S3006 REFCLK inputs
JP4, JP6	Connects REFCLKP/N SMA's to S3006 REFCLK inputs
JP7, JP9	Connects REFCLKP/N SMAs to S3005 REFCLK inputs
JP8, JP10	Connects on-board XTAL oscillator to S3005 REFCLK inputs
JPA, JPB	Connects S3005/S3006 LOCKDET outputs to LED

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