500-kHz Half-Bridge DC-DC Converter With Integrated Secondary Synchronous Rectification Drivers

FEATURES

- 12-V to 72-V Input Voltage Range
- Compatible with ETSI 300 132-2
- Integrated Half Bridge Primary Drivers (1-A Drive Capability)
- Secondary Synchronous Signals With Programmable Deadtime Delay
- Voltage Mode Control
- Voltage Feedforward Compensation
- High Voltage Pre-Regulator Operates During Start-Up
- Current Sensing On Low-Side Primary Device
- Frequency Foldback Eliminates Constant Current Tail
- Advanced Maximum Current Control During Start-Up and Shorted Load
- Low Input Voltage Detection
- Programmable Soft-Start Function
- Over Temperature Protection

APPLICATIONS

- Network Cards
- Power Supply Modules

DESCRIPTION

Si9122 is a dedicated half-bridge IC ideally suited to fixed telecom applications where efficiency is required at low output voltages (e.g. <3.3 V). Designed to operate within the fixed telecom voltage range of 33–72 V and withstand 100 V, 100 ms transients, the IC is capable of controlling and driving both the low and high-side switching devices of a half bridge circuit and also controlling the switching devices on the secondary side of the bridge. Due to the very low on-resistance of the secondary MOSFETs, a significant increase in the efficiency can be achieved as compared with conventional Schottky diodes. Control of the secondary devices is by means of a pulse transformer and a pair of inverters. Such a system has efficiencies well in excess of 90% even for low output voltages. On-chip control of the dead time delays between the primary and secondary synchronous signals keep efficiencies high and prevent accidental destruction of the power transformer. An external resistor sets the switching frequency from 200 kHz to 600 kHz.

Si9122 has advanced current monitoring and control circuitry which allow the user to set the maximum current in the primary circuit. Such a feature acts as protection against output shorting and also provides constant current into large capacitive loads during start-up or when paralleling power supplies. Current sensing is by means of a sense resistor on the low-side primary device.

FUNCTIONAL BLOCK DIAGRAM

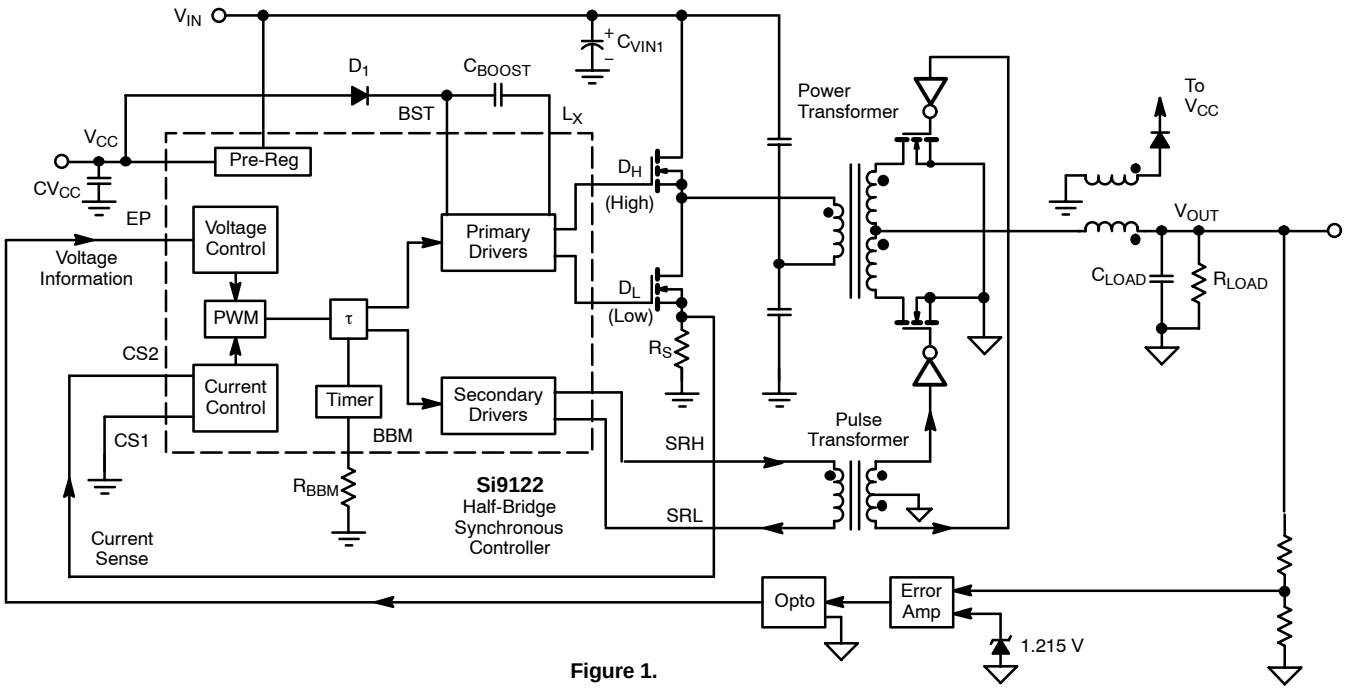


Figure 1.

TECHNICAL DESCRIPTION

Si9122 is a voltage mode controller for the half-bridge topology. With 100-V depletion mode MOSFET capability, the Si9122 is capable of powering directly from the high voltage bus to V_{CC} through an external PNP pass transistor, or may be powered through an external regulator directly through the V_{CC} pin. With PWM control, Si9122 provides peak efficiency throughout the entire line and load range. In order to simplify the traditional secondary synchronous rectification, Si9122 provides intelligent gate drive signals to control the secondary MOSFETs. With independent gate drive signals from the controller, transformer design is no longer limited by the gate to a source rating of the MOSFETs. Si9122 provides constant V_{GS} voltage, independent of line voltage to minimize the gate charge loss as well as conduction loss. A break-before-make function is included to prevent shoot through current or transformer shorting. Adjustable Break-Before-Make time is incorporated into the IC and is programmable by an external resistor value.

Si9122 is packaged in TSSOP-20 and MLP65-20 packages. In TSSOP-20 packaging, both standard and lead (Pb)-free options are available. The MLP65-20 package is lead (Pb)-free. In order to satisfy the stringent ambient temperature requirements, Si9122 is rated to handle the industrial temperature range of −40 to 85°C. When a situation arises which results in a rapid increase in primary (or secondary current) such as output shorted or start-up with a large output capacitor, control of the PWM generator is handed over to the the current loop. Monitoring of the load current is by means of a sense resistor on the primary low-side switch.

DETAILED BLOCK DIAGRAM

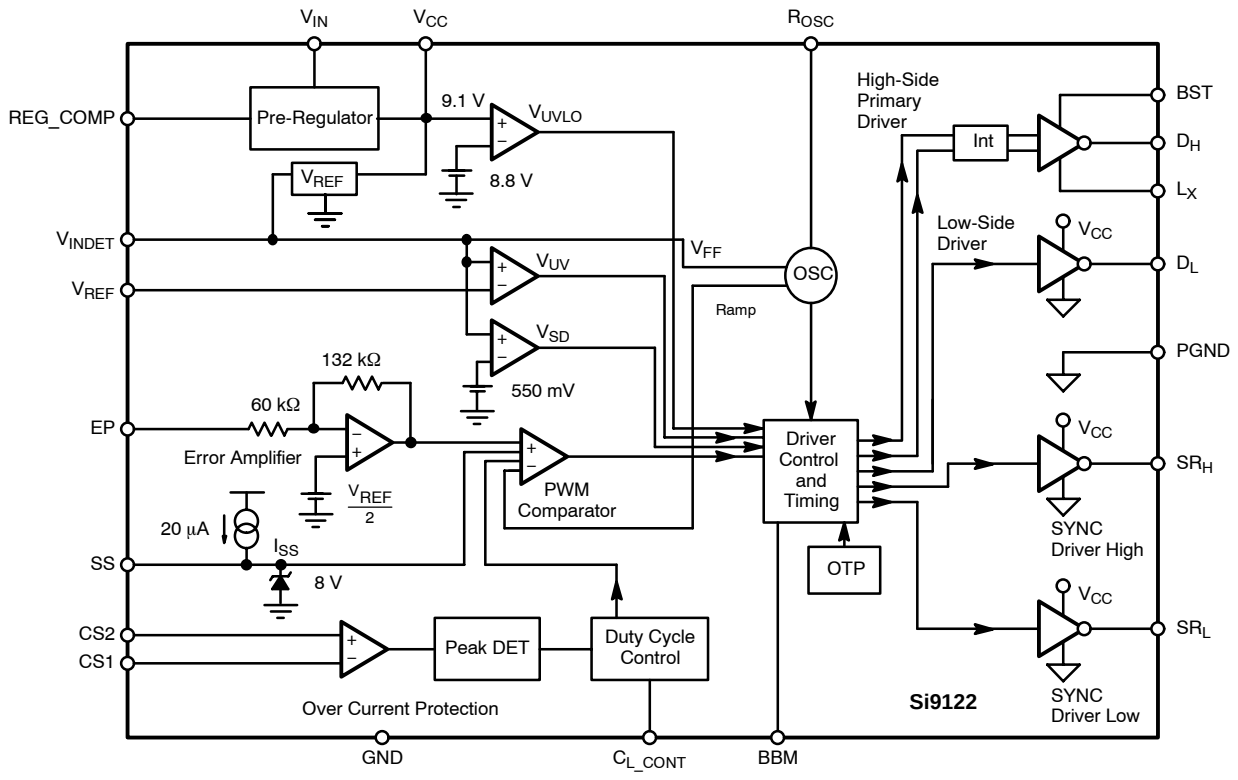


Figure 2.

ABSOLUTE MAXIMUM RATINGS (ALL VOLTAGES REFERENCED TO GND = 0 V)

V_{IN} (Continuous) . . . . . 75 V
V_{IN} (100 ms) . . . . . 100 V
V_{CC} . . . . . 14.5 V
V_{BST} (Continuous) . . . . . 90 V
(100 ms) . . . . . 115 V
V_{LX} . . . . . 75 V
$V_{BST} - V_{LX}$ . . . . . 15 V
V_{REF}, R_{OSC} . . . . . −0.3 V to V_{CC} + 0.3 V
Logic Inputs . . . . . −0.3 V to V_{CC} + 0.3 V
Analog Inputs . . . . . −0.3 V to V_{CC} + 0.3 V
HV Pre-Regulator Input Current (continuous) . . . . . 5 mA

Storage Temperature . . . . . −65 to 150°C
Operating Junction Temperature . . . . . 125°C
Power Dissipation[a]
TSSOP-20 . . . . . 850 mW
MLP65-20 . . . . . 2500 mW
Thermal Impedance (Θ_{JA})
TSSOP-20[b] . . . . . 75°C/W
MLP65-20[c] . . . . . 38°C/W

Notes
a. Device mounted on JEDEC compliant 1S2P test board..
b. Derate −14 mW/°C above 25°C.
c. Derate −26 mW/°C above 25°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE (ALL VOLTAGES REFERENCED TO GND = 0 V)

V_{IN} . . . . . 12 to 72 V
$C_{VIN1} \parallel C_{VIN2}$ . . . . . 100 µF/ESR ≤ 100 mΩ, 0.1 µF
V_{CC} Operating . . . . . 10 to 13.2 V
CV_{CC} . . . . . 4.7 µF
f_{OSC} . . . . . 200 to 600 kHz
R_{OSC} . . . . . 24 to 72 kΩ
R_{BBM} . . . . . 22 to 50 kΩ

C_{BBM}[h] . . . . . >680 pF
C_{SS} . . . . . 4.7 nF
C_{REF} . . . . . 0.1 µF
C_{BOOST} . . . . . 0.1 µF
C_{LOAD} . . . . . 150 µF
Analog Inputs . . . . . 0 to V_{CC} − 2 V
Digital Inputs . . . . . 0 to V_{CC}
Reference Voltage Output Current . . . . . 0 to 2.5 mA

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified f_{NOM} = 500 kHz, V_{IN} = 72 V V_{INDET} = 7.2 V; 10 V ≤ V_{CC} ≤ 13.2 V	Limits −40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Reference (3.3 V)						
Output Voltage	V_{REF}	V_{CC} = 12 V, 25°C Load = 0 mA	3.2	3.3	3.4	V
Short Circuit Current	I_{SREF}	V_{REF} = 0 V			−50	mA
Load Regulation	dVr/dIr	I_{REF} = 0 to −2.5 mA		−30	−75	mV
Power Supply Rejection	PSRR	@ 100Hz		60		dB
Oscillator						
Accuracy (1% R_{OSC})		R_{OSC} = 30 kΩ, f_{NOM} = 500 kHz	−20		20	%
Max Frequency	F_{MAX}	R_{OSC} = 24 kΩ		600		kHz
Foldback Frequency[d]	F_{FOBK}	f_{NOM} = 500 kHz, $V_{CS2} - V_{CS1}$ > 150 mV		100		
Error Amplifier						
Input Bias Current	I_{BIAS}	V_{EP} = 0 V	−40		−15	µA
Gain	A_V			−2.2		V/V
Bandwidth	BW			5		MHz
Power Supply Rejection	PSRR	@ 100Hz		60		dB
Slew Rate	SR			0.5		V/µs
Current Sense Amplifier						
Input Voltage CM Range	V_{CM}	V_{CS1} − GND, V_{CS2} − GND		±150		mV
Input Amplifier Gain	A_{VOL}			17.5		dB
Input Amplifier Bandwidth	BW			5		MHz

SPECIFICATIONS[a]

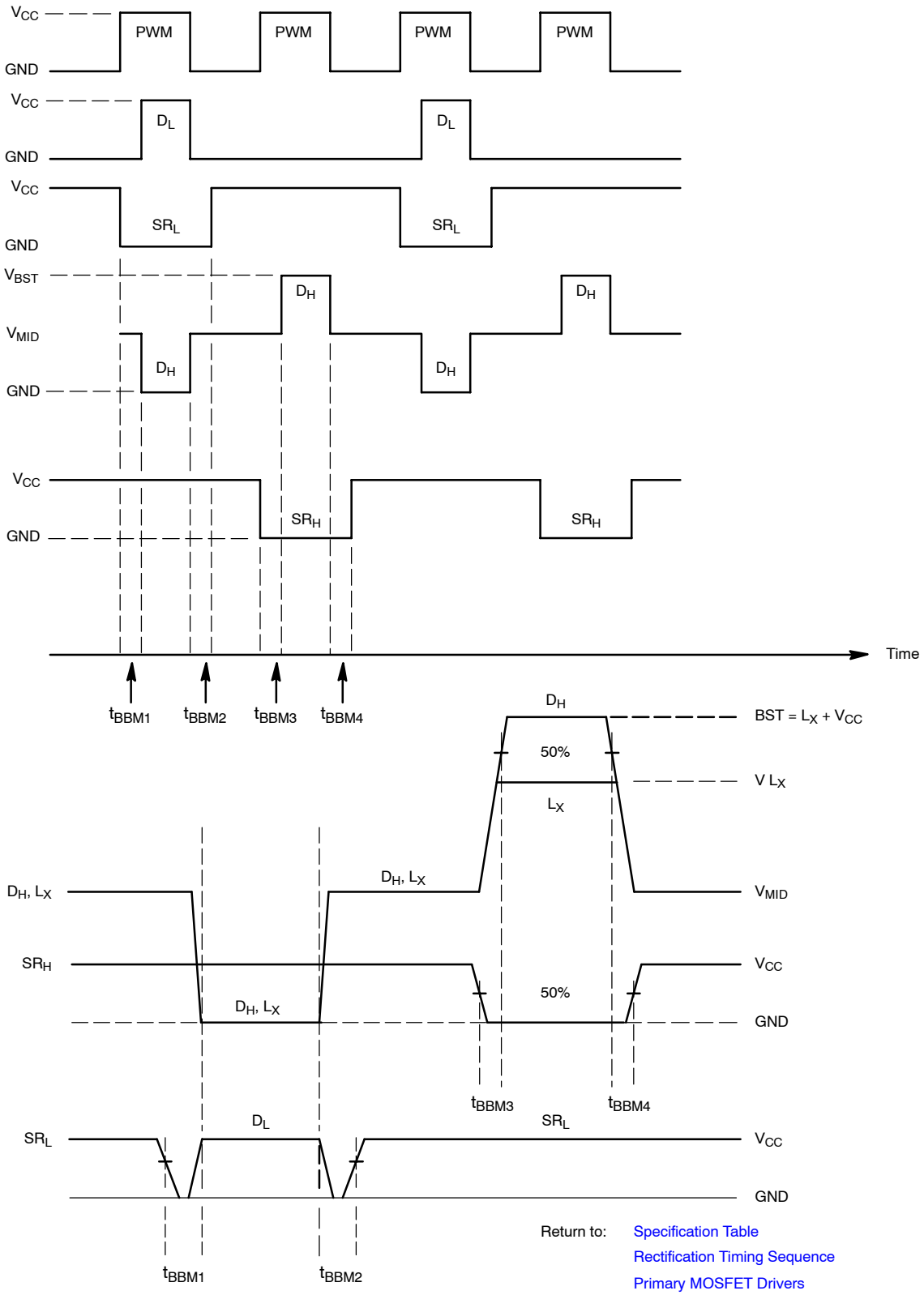
Parameter	Symbol	Test Conditions Unless Otherwise Specified f_{NOM} = 500 kHz, V_{IN} = 72 V V_{INDET} = 7.2 V; 10 V ≤ V_{CC} ≤ 13.2 V	Limits –40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Current Sense Amplifier						
Input amplifier Offset Voltage	V_{OS}			±5		mV
CL_CONT Current	I_{CL_CONT}	dV_{CS} = 0		120		µA
		dV_{CS} = 100 mV		0		
		dV_{CS} = 170 mV		>2		mA
Lower Current Limit Threshold	V_{TLCL}	$I_{PD} = I_{PU} - I_{CL\_CONT} = 0$ See Figure 6		100		mV
Upper Current Limit Threshold	V_{THCL}	I_{PD} > 2 mA		150		
Hysteresis		I_{PU} < 500 µA		–50		
CL_CONT Clamp Level	$C_{L\_CONT(min)}$	I_{PU} = 500 µA	0.6		1.5	V
PWM Operation						
Duty Cycle[e]	D_{MAX}	f_{OSC} = 500 kHz, V_{EP}= 0 V	90	92	95	%
	D_{MIN}	f_{OSC} = 500 kHz, V_{EP}= 1.75 V		<15		
		$V_{CS2} - V_{CS1}$ > 150 mV		3		
Pre-Regulator						
Input Voltage	$+V_{IN}$	I_{IN} = 10 µA			72	V
Input Leakage Current	I_{LKG}	V_{IN} = 72 V, V_{CC} > V_{REG}			10	µA
Regulator Bias Current	I_{REG1}	V_{IN} = 72 V, V_{INDET} < V_{SD}		86	200	
	I_{REG2}	V_{IN} = 72 V, V_{INDET} > V_{REF}		8	14	mA
Regulator_Comp	I_{SOURCE}	V_{CC} = 12 V	–29	–19	–9	µA
	I_{SINK}		50	82	110	
Pre-Regulator Drive Capacility	I_{START}	V_{CC} < V_{REG}	20			mA
V_{CC} Pre-Regulator Turn Off Threshold Voltage	V_{REG1}	V_{INDET} > V_{REF}	7.4	9.1	10.4	V
		V_{INDET} > V_{REF}, T_A = 25°C	8.5	9.1	9.7	
	V_{REG2}	V_{INDET} = 0 V		9.2		
Undervoltage Lockout	V_{UVLO}	V_{CC} Rising	7.15	8.8	9.8	
		V_{CC} Rising, T_A = 25°C	8.1	8.8	9.3	
V_{UVLO} Hysteresis[g]	$V_{UVLOHYS}$			0.5		
Soft-Start						
Soft-Start Current Output	I_{SS}	Start-Up Condition	12	20	28	µA
Soft-Start Completion Voltage	V_{SS_COMP}	Normal Operation	7.35	8.05	8.85	V
Shutdown						
V_{INDET} Shutdown FN	V_{SD}	V_{INDET} Rising	350	550	720	mV
V_{INDET} Hysteresis		V_{INDET}		200		
V_{INDET} Input Threshold Voltages						
$V_{INDET} - V_{IN}$ Under Voltage	V_{UV}	V_{INDET} Rising	3.13	3.3	3.46	V
V_{INDET} Hysteresis		V_{INDET}		0.3		
Over Temperature Protection						
Activating Temperature		T_J Increasing		160		°C
De-Activating Temperature		T_J Decreasing		130		
Converter Supply Current (V_{CC})						
Shutdown	I_{CC1}	Shutdown, V_{INDET} = 0 V	50		350	µA
Switching Disabled	I_{CC2}	V_{INDET} < V_{REF}	4	8	12	mA
Switching w/o Load	I_{CC3}	V_{INDET} > V_{REF}, f_{NOM} = 500 kHz	5	10	14	
Switching with C_{LOAD}	I_{CC4}	V_{CC} = 12 V, $C_{DH} = C_{DL}$ = 3 nF $C_{SRH} = C_{SRL}$ = 0.3 nF		21		

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified f_{NOM} = 500 kHz, V_{IN} = 72 V V_{INDET} = 7.2 V; 10 V ≤ V_{CC} ≤ 13.2 V	Limits −40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Output MOSFET DH Driver (High-Side)						
Output High Voltage	V_{OH}	Sourcing 10 mA	V_{BST} − 0.3			V
Output Low Voltage	V_{OL}	Sinking 10 mA			V_{LX} + 0.3	
Boost Current	I_{BST}	V_{LX} = 72 V, V_{BST} = V_{LX} + V_{CC}	1.3	1.9	2.7	mA
L_X Current	I_{LX}	V_{LX} = 72 V, V_{BST} = V_{LX} + V_{CC}	−1.1	−0.7	−0.4	
Peak Output Source	I_{SOURCE}	V_{CC} = 10 V		−1.0	−0.75	A
Peak Output Sink	I_{SINK}		0.75	1.0		
Rise Time	t_r	C_{DH} = 3 nF		35		ns
Fall Time	t_f			35		
Output MOSFET DLDriver (Low-Side)						
Output High Voltage	V_{OH}	Sourcing 10 mA	V_{CC} − 0.3			V
Output Low Voltage	V_{OL}	Sinking 10 mA			0.3	
Peak Output Source	I_{SOURCE}	V_{CC} = 10 V		−1.0	−0.75	A
Peak Output Sink	I_{SINK}		0.75	1.0		
Rise Time	t_r	C_{DL} = 3 nF		35		ns
Fall Time	t_f			35		
Synchronous Rectifier (SRH, SRL) Drivers						
Output High Voltage	V_{OH}	Sourcing 10 mA	V_{CC} − 0.4			V
Output Low Voltage	V_{OL}	Sinking 10 mA			0.4	
Break-Before-Make Time[f]	t_{BBM1}	T_A = 25°C, R_{BBM} = 33 kΩ, See Figure 3		55		ns
	t_{BBM2}			40		
	t_{BBM3}	T_A = 25°C,R_{BBM} = 33 kΩ, L_X = 72 V		35		
	t_{BBM4}			55		
Peak Output Source	I_{SOURCE}	V_{CC} = 10 V		−100		mA
Peak Output Sink	I_{SINK}			100		
Rise Time	t_r	C_{SRH} = C_{SRL} = 0.3 nF		35		ns
Fall Time	t_f			35		
Voltage Mode						
Error Amplifier	t_{d1DH} t_{d2DL}	Input to high-side switch off		< 200		ns
		Input to low-side switch off		< 200		
Current Mode						
Current Amplifier	t_{d3DH} t_{d4DL}	Input to high-side switch off		< 200		ns
		Input to low-side switch off		< 200		

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum (−40° to 85°C).
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. F_{MIN} when V_{CL_CONT} at clamp level. Typical foldback frequency change +20%, −30% over temperature.
e. Measured on SRL or SRH outputs.
f. See Figure 3 for Break-Before-Make time definition.
g. V_{UVLO} tracks V_{REG1} by a diode drop
h. C_{BBM} may be required to reduce noise into BBM pin for non-optimum layout.

TIMING DIAGRAM FOR MOS DRIVERS

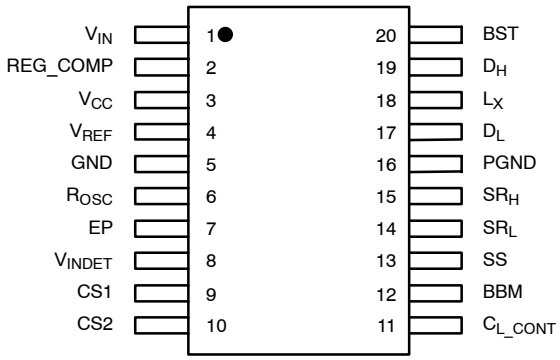


Return to: Specification Table
Rectification Timing Sequence
Primary MOSFET Drivers
Secondary MOSFET Drivers

Figure 3.

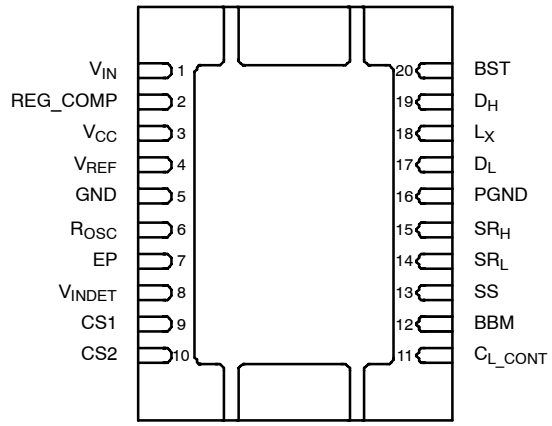
PIN CONFIGURATION

Si9122DQ (TSSOP-20)



Top View

Si9122DLP (MLP65-20)



Top View

ORDERING INFORMATION

Standard Part Number	Lead (P_b)-Free Part Number	Temperature Range	Package
Si9122DQ-T1	Si9122DQ-T1—E3	–40 to 85°C	TSSOP-20
	Si9122DLP-T1—E3		MLP65-20

Eval Kit	Temperature Range	Board Type
Si9122DB Issue 3	–10 to 70°C	Surface Mount and Thru-Hole

PIN DESCRIPTION

Pin Number	Name	Function
1	V_{IN}	Input supply voltage for the start-up circuit.
2	REG_COMP	Control signal for an external pass transistor.
3	V_{CC}	Supply voltage for internal circuitry
4	V_{REF}	3.3-V reference, decoupled with 1-µF capacitor
5	GND	Ground
6	R_{OSC}	External resistor connection to oscillator
7	EP	Voltage control input
8	V_{INDET}	V_{IN} under voltage detect and shutdown function input. Shuts down or disables switching when V_{INDET} falls below preset threshold voltages and provides the feed forward voltage.
9	CS1	Current limit amplifier negative input
10	CS2	Current limit amplifier positive input
11	C_{L_CONT}	Current limit compensation
12	BBM	Programmable Break-Before-Make time connection to an external resistor to set time delay
13	SS	Soft-Start control – external capacitor connection
14	SR_L	Signal transformer drive, sequenced with the primary side.
15	SR_H	Signal transformer drive, sequenced with the primary side.
16	PGND	Power ground.
17	D_L	Low-side gate drive signal – primary
18	L_X	High-side source and transformer connection node
19	D_H	High-side gate drive signal – primary
20	BST	Bootstrap voltage to drive the high-side n-channel MOSFET switch

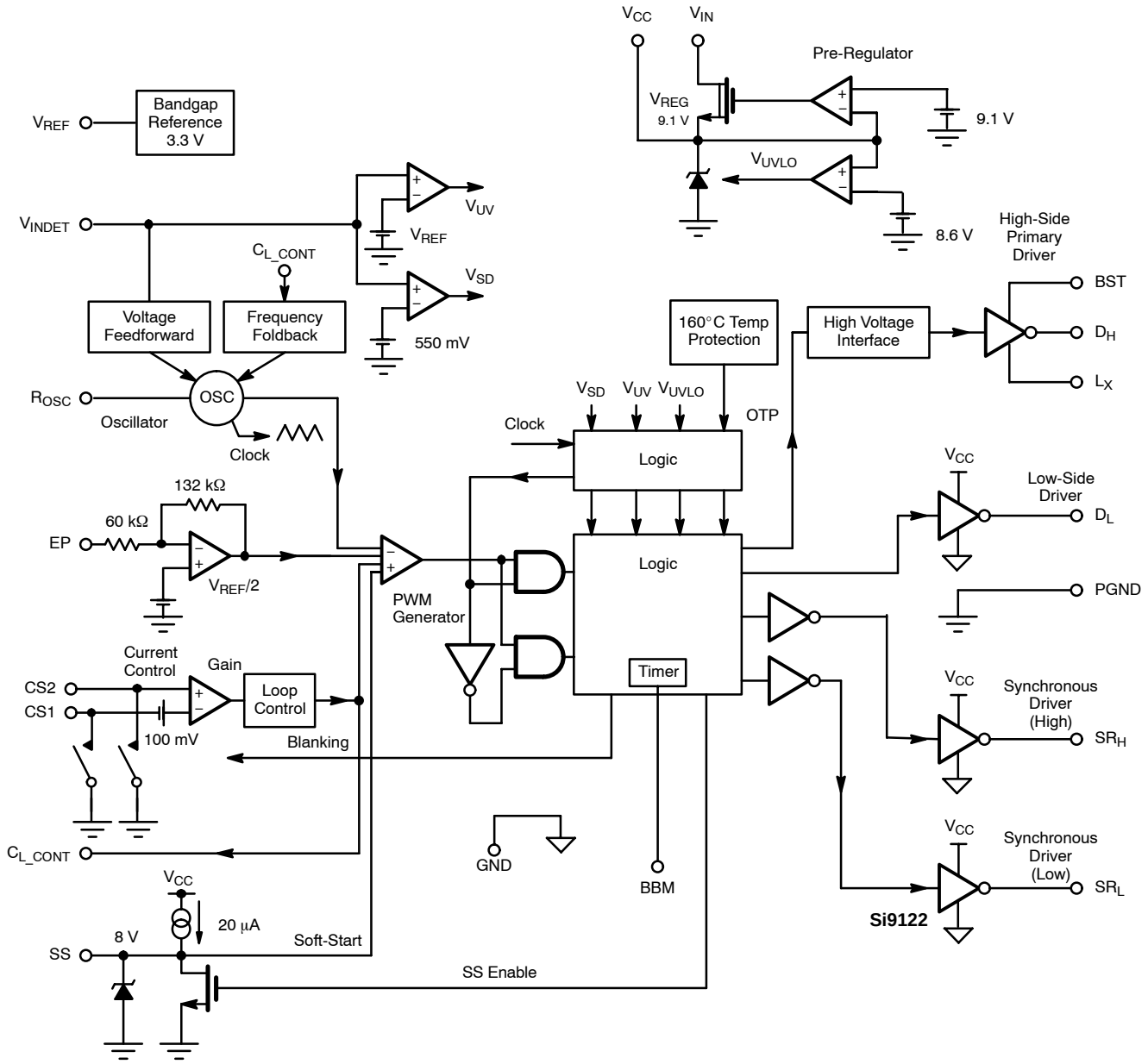


Figure 4. Detailed Functional Block

DETAILED OPERATION

Start-Up

When V_{INEXT} rises above 0 V, the internal pre-regulator begins to charge up the Vcc capacitor. Current into the external V_{CC} capacitor is limited to typically 40 mA by the internal DMOS device. When Vcc exceeds the UVLO voltage of 8.8 V a soft-start cycle of the switch mode supply is initiated. The V_{CC} supply continues to be charged by the pre-regulator until V_{CC} equals Vreg. During this period, between V_{UVLO} and V_{REG}, excessive load current will result in V_{CC} falling below V_{UVLO} and stopping switch mode operation. This situation is avoided by the hysteresis between V_{REG} and V_{UVLO} and correct sizing of the V_{CC} capacitor, bootstrap capacitor and the soft-start capacitor. The value of the V_{CC} capacitor should therefore be chosen to be capable of maintaining switch mode operation until the V_{CC} can be supplied from the external circuit (e.g via a power transformer winding and zener regulator). Feedback from the output of the switch mode supply charges V_{CC} above V_{REG} and fully disconnects the pre-regulator, isolating V_{CC} from V_{IN}. V_{CC} is then maintained above V_{REG} for the duration of switch mode operation. In the event of an over voltage condition on V_{CC}, an internal voltage clamp turns on at 14.5 V to shunt excessive current to GND.

Care needs to be taken if there is a delay prior to the external circuit feeding back to the V_{CC} supply. To prevent excessive power dissipation within the IC it is advisable to use an external PNP device. A pin has been incorporated on the IC, (REG_COMP) to provide compensation when employing the external device. In this case the V_{IN} pin is connected to the base of the PNP device and controls the current, while the REG_COMP pin determines the frequency compensation of the circuit. To understand the operation please refer to Figure 5.

The soft-start circuit is designed for the dc-dc converter to start-up in an orderly manner and reduce component stress on the IC. This feature is programmable by selecting an external C_{SS}. An internal 20-µA current source charges C_{SS} from 0 V to the final clamped voltage of 8 V. In the event of UVLO or shutdown, V_{SS} will be held low (<1 V) disabling driver switching. To prevent oscillations, a longer soft-start time may be needed for high capacitive loads and high peak output current applications.

Reference

The reference voltage of Si9122 is set at 3.3 V. The reference voltage is de-coupled externally with 0.1-µF capacitor. The V_{REF} voltage is 0 V in shutdown mode and has 50-mA source capability.

Voltage Mode PWM Operation

Under normal load conditions, the IC operates in voltage mode and generates a fixed frequency pulse width modulated signal to the drivers. Duty cycle is controlled over a wide range to maintain output voltage under line and load variation. Voltage feed forward is also included to take account of variations in supply voltage V_{IN}.

In the half-bridge topology requiring isolation between output and input, the reference voltage and error amplifier must be supplied externally, usually on the secondary side. The error information is thus passed to the power controller through an opto-coupling device. This information is inverted, hence 0 V represents the maximum duty cycle, whilst 2 V represents minimum duty cycle. The error information enters the IC via pin EP, and is passed to the PWM generator via an inverting amplifier. The relationship between Duty cycle and V_{EP} is shown in the Typical Characteristic Graph, Duty Cycle vs. V_{EP} 25°C, page 19. Voltage feedforward is implemented by taking the attenuated V_{IN} signal at V_{INDET} and directly modulating the duty cycle. The relationship between Duty cycle and V_{INDET} is shown in the the Typical Characteristic Graph, Duty Cycle vs. V_{INDET}, page 16.

At start-up, i.e., once V_{CC} is greater than V_{UVLO}, switching is initiated under soft-start control which increases primary switch on-times linearly from D_{MIN} to D_{MAX} over the soft-start period. Start-up from a V_{INDET} power down is also initiated under soft-start control.

Half-Bridge and Synchronous Rectification Timing Sequence

The PWM signal generated within the Si9122 controls the low and high-side bridge drivers on alternative cycles. A period of inactivity always results after initiation of the soft-start cycle until the soft-start voltage reaches approximately 1.2 V and PWM controlled switching begins. The first bridge driver to switch is always the low-side, D_L as this allows charging of the high-side boost capacitor.

The timing and coordination of the drives to the primary and secondary stages is very important and shown in Figure 3. It is essential to avoid the situation where both of the secondary MOSFETs are on when either the high or the low-side switch are active. In this situation the transformer would effectively be presented with a short across the output. To avoid this, a dedicated break-before-make circuit is included which will generate non overlapping waveforms for the primary and the secondary drive signals. This is achieved by a programmable timer which delays the switching on of the primary driver relative to the switching off of the related secondary and subsequently delays the switching on of the secondary relative to the switching off of the related primary.

Typical variation in the t_{BBM3} and t_{BBM4} delay with L_X voltage is shown in graphs t_{BBM3}, t_{BBM4} and for R_{BBM} = 33 kΩ. This is due to a reduction in propagation delay through the high-side driver path as the L_X voltage increases and must be considered in setting the delay for the system level design. Variation of BBM time with R_{BBM} is shown in graph t_{BBM1} to t_{BBM4} vs. R_{BBM}.

Primary High- and Low-Side MOSFET Drivers

The drive voltage for the low-side MOSFET switch is provided directly from V_{CC}. The high-side MOSFET however requires the gate voltage to be enhanced above V_{IN}. This is achieved by bootstraping the V_{CC} voltage onto the L_X voltage (the high-side MOSFET source). In order to provide the bootstrapping an external diode and capacitor are required as shown on the application schematic. The capacitor will charge up after the low-side driver has turned on. The switch gate drive signals D_H and D_L are shown in Figure 3.

Secondary MOSFET Drivers

The secondary side MOSFETs are driven from the Si9122 via a center tapped pulse transformer and inverter drivers. The waveforms from the IC SRH and SRL are shown in Figure 3. Of importance is the relative voltage between SRH and SRL, i.e. that which is presented across the primary of the pulse transformer. When both potentials of SRL and SRH are equal then by the action of the inverting driver both secondary MOSFETs are left on.

Oscillator

The oscillator is designed to operate at a nominal frequency of 500 kHz. The 500-kHz operating frequency allows the converter to minimize the inductor and capacitor size, improving the power density of the converter. The oscillator and therefore the switching frequency is programmable by attaching a resistor to the R_{OSC} pin. Under overload conditions the oscillator frequency is reduced by the current overload protection to enable a constant current to be maintained into a low impedance circuit.

Current Limit

Current mode control providing constant current operation is achieved by monitoring the differential voltage between the CS1and CS2 pins which are connected across a primary low-side sense resistor. Once this differential voltage exceeds the 100-mV trigger point, the voltage on the C_{L_CONT} pin is pulled lower at a rate proportional to the excess voltage and the value of the external capacitor connected between the C_{L_CONT} pin and ground. If the voltage between CS1 and CS2 exceeds 150 mV the C_{L_CONT} capacitor is discharged rapidly resulting in minimum duty cycle and frequency immediately.

Lowering the C_{L_CONT} voltage results in PWM control of the output drive being taken over by the current limit control loop. Current control works to initially reduce the switching duty cycle down to D_{MIN} (12.5%). Further reduction in the duty cycle is accompanied by a reduction in switching frequency at a rate proportional to the duty cycle. This prevents the on time of the primary drivers f_{nom} from reducing below 100 ns and avoiding a current tail. Frequency reduction occurs to a maximum of one fifth of the nominal frequency.

With constant current mode control of on time and with reduced operating frequency, protection of the MOSFET switches is increased during fault conditions. Minimum duty cycle and reduced frequency switching continues for the duration of the fault condition. The converter reverts to voltage mode operation immediately whenever the primary current fails to reach the limit level. C_{L_CONT} clamps to 6.5 V when not in current limit.

The soft-start function does not apply under current limit as this would constitute hiccup mode operation.

V_{IN} Voltage Monitor –V_{INDET}

The chip provides a means of sensing the voltage of V_{IN}, and withholding operation of the output drivers until a minimum voltage of V_{REF} (3.3 V, 300-mV hysteresis), is achieved. This is achieved by choosing an appropriate resistive tap between the ground and V_{IN}, and comparing this voltage with the reference voltage. When the applied voltage is greater than V_{REF}, the output drivers are activated as normal. V_{INDET} also provides the input to the voltage feed forward function.

However, if the divided voltage applied to the V_{INDET} pin is greater than V_{CC} –0.3 V, the high-side driver, D_H, will stop switching until the voltage drops below V_{CC} –0.3 V. Thus, the resistive tap on the V_{IN} divider must be set to accommodate the normal V_{CC} operating voltage to avoid this condition. Alternatively, a zener clamp diode from V_{INDET} to GND may also be used.

Shutdown Mode

If V_{INDET} is forced below the lower threshold, a minimum of 350 mV(V_{SD}), the device will enter SHUTDOWN mode. This powers down all unnecessary functions of the controller, ensures that the primary switches are off and results in a low level current demand from the V_{IN} or V_{CC} supplies.

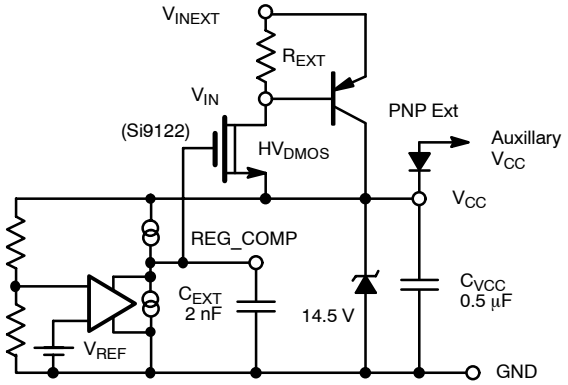


Figure 5. High-Voltage Pre-Regulator Circuit

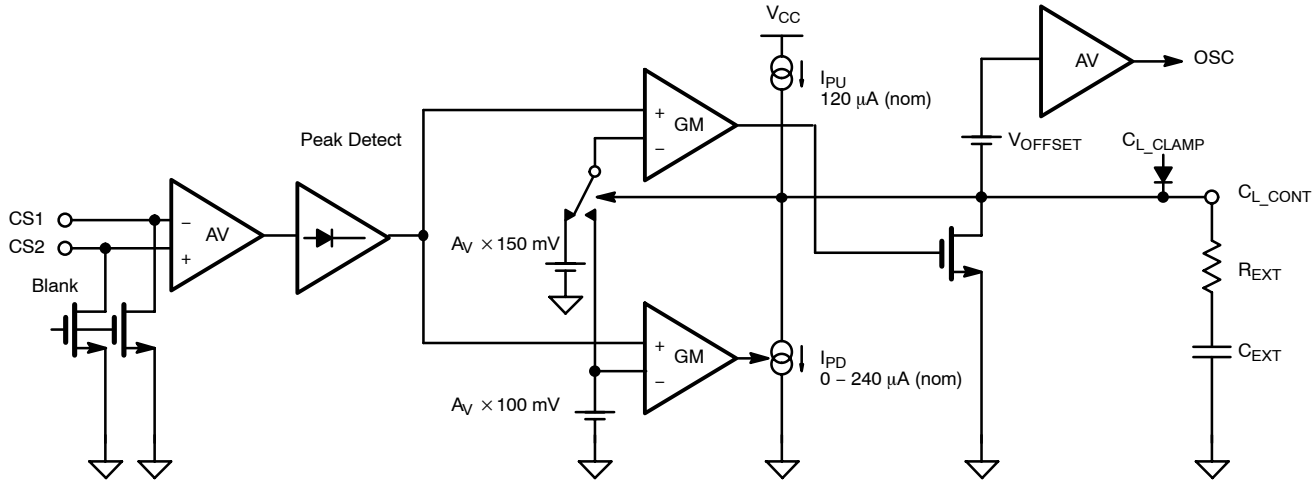
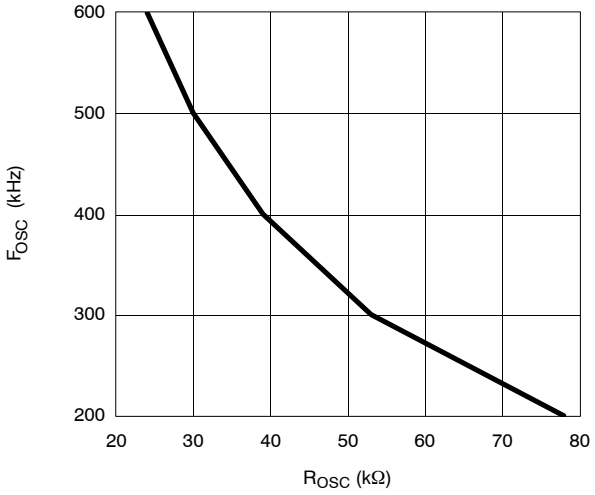


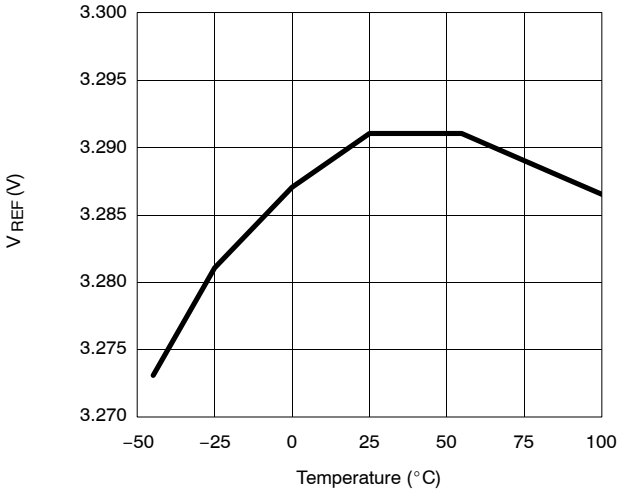
Figure 6 . Current Limit Circuit

TYPICAL CHARACTERISTICS

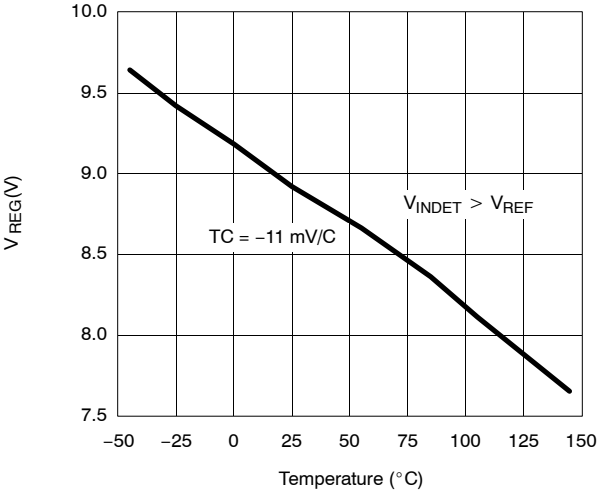
F_{OSC} vs. R_{OSC} @ V_{CC} = 12 V



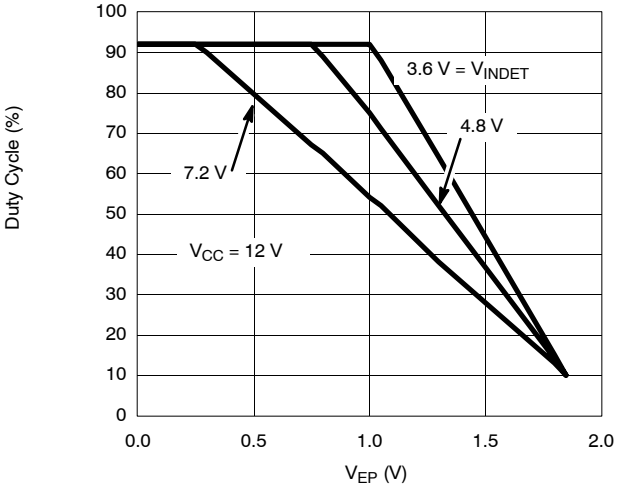
V_{REF} vs. Temperature, V_{CC} = 12 V



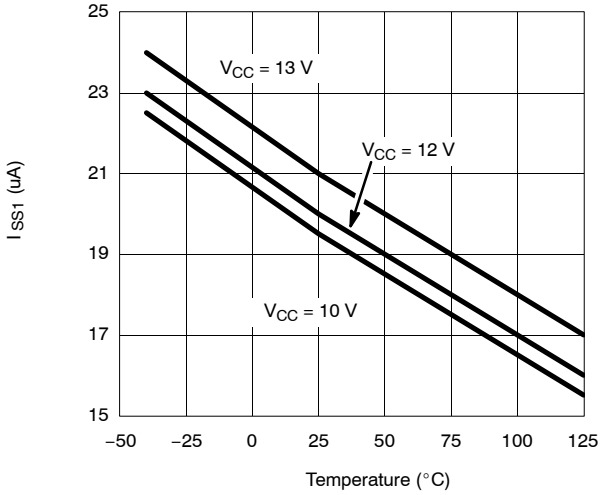
V_{REG} vs. Temperature, V_{IN} = 48 V



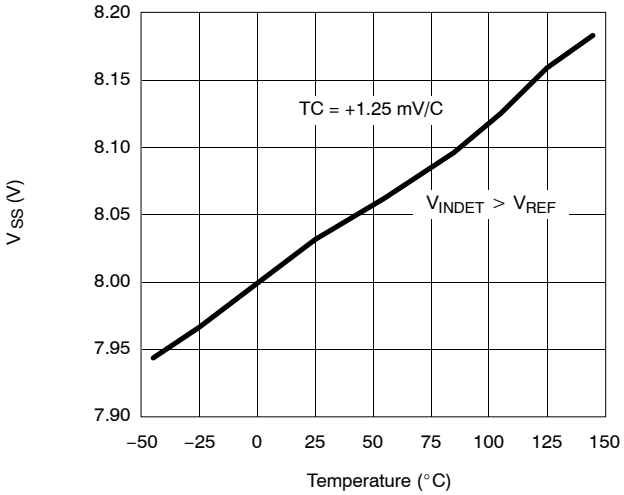
SRL, SRH Duty Cycle vs. V_{EP}



I_{SS} vs. Temperature

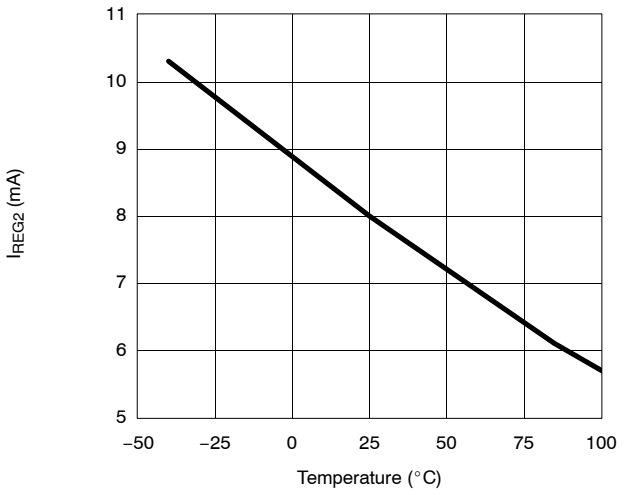


V_{SS} vs. Temperature, V_{CC} = 12 V

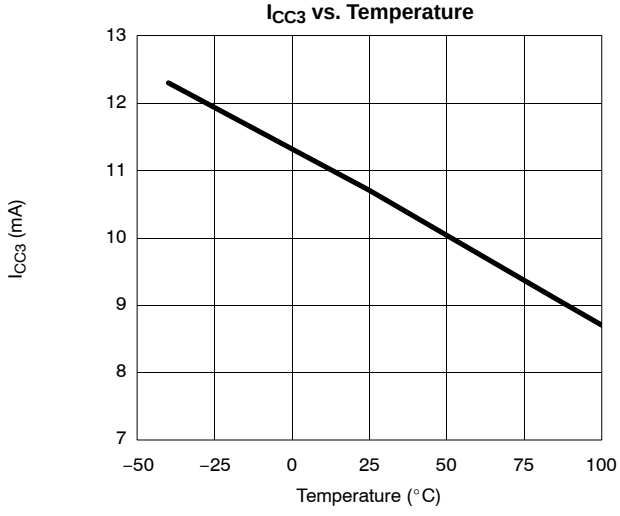


TYPICAL CHARACTERISTICS

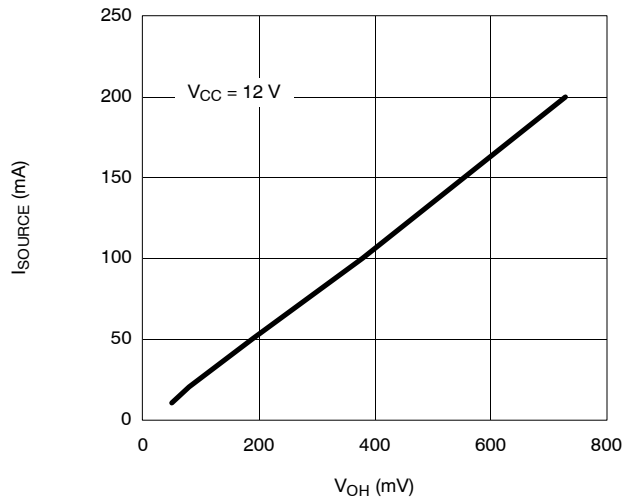
I_{REG2} vs. Temperature



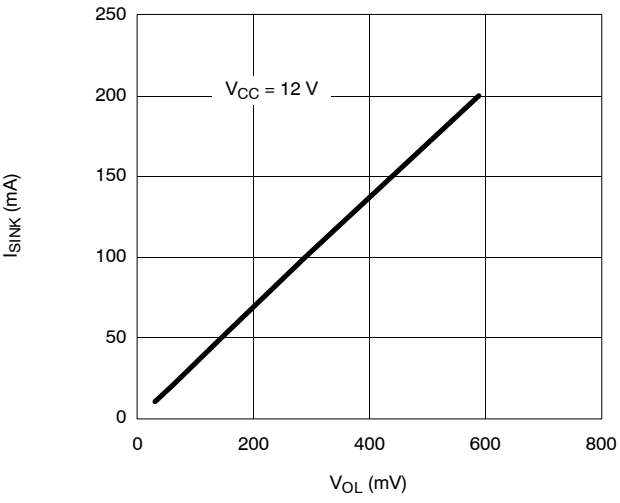
I_{CC3} vs. Temperature



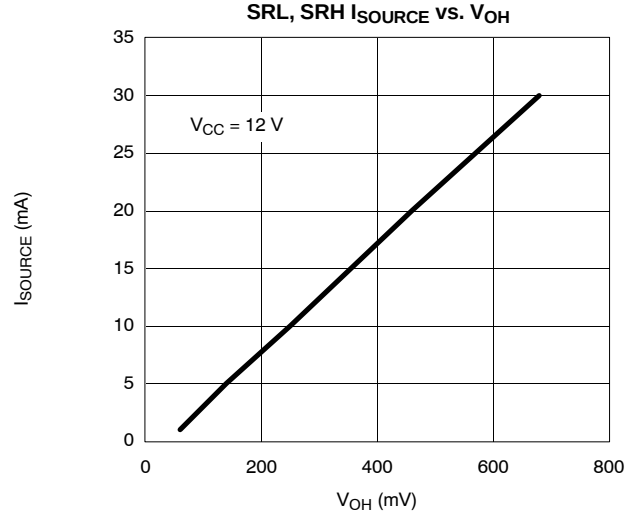
D_H, D_L I_{SOURCE} vs. V_{OH}



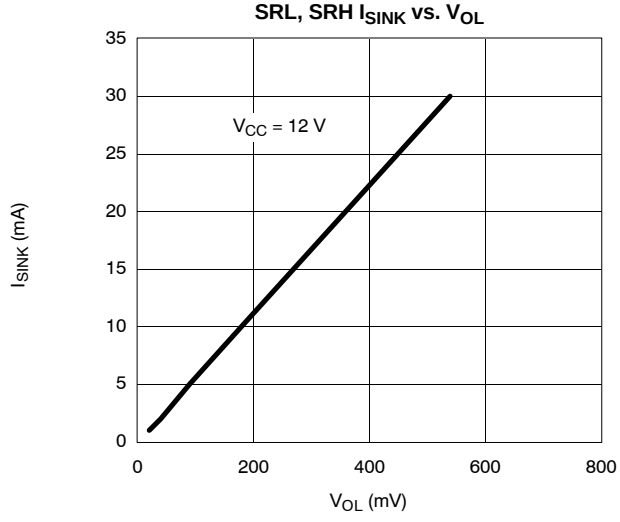
D_H, D_L I_{SINK} vs. V_{OL}



SRL, SRH I_{SOURCE} vs. V_{OH}



SRL, SRH I_{SINK} vs. V_{OL}



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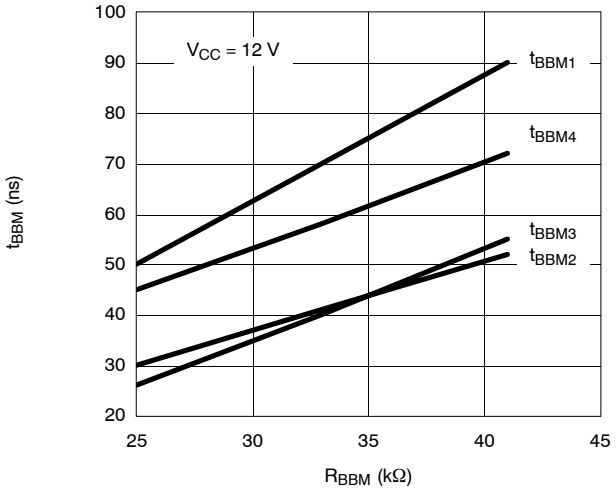
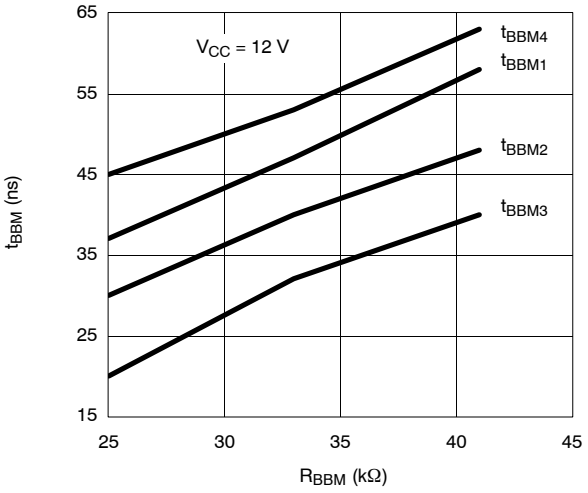
TYPICAL CHARACTERISTICS

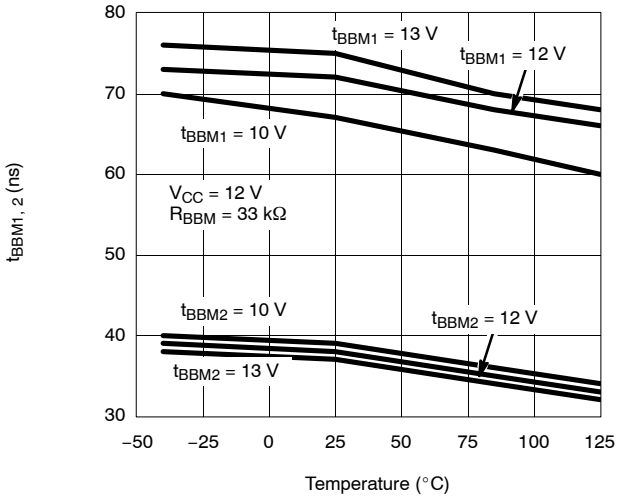
t_{BBM} vs. R_{BBM}, V_{EP} = 0 V



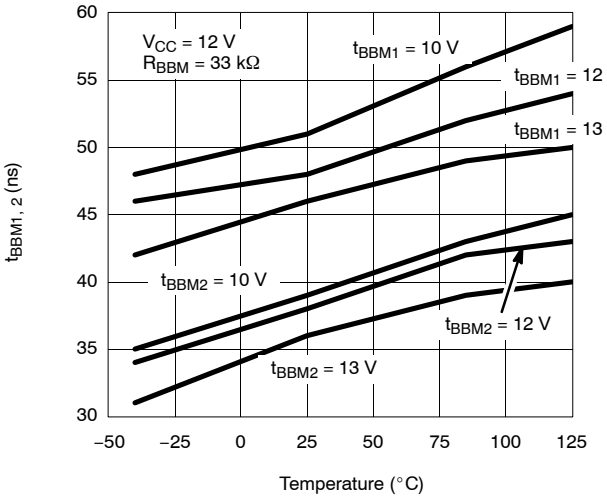
t_{BBM} vs. R_{BBM}, V_{EP} = 1.65 V



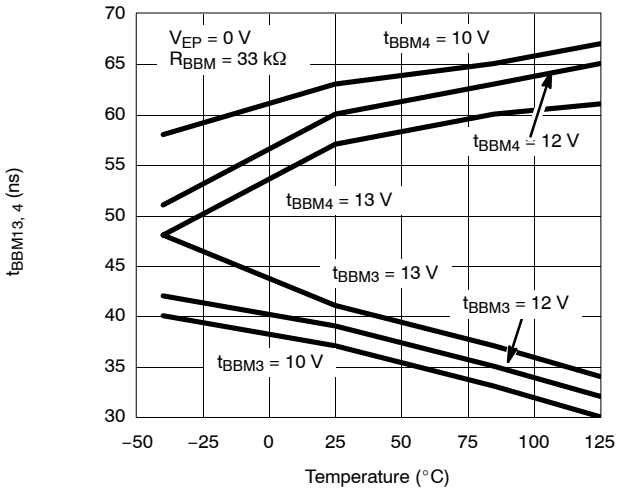
$t_{BBM1, 2}$ vs. Temperature, V_{EP} = 0 V



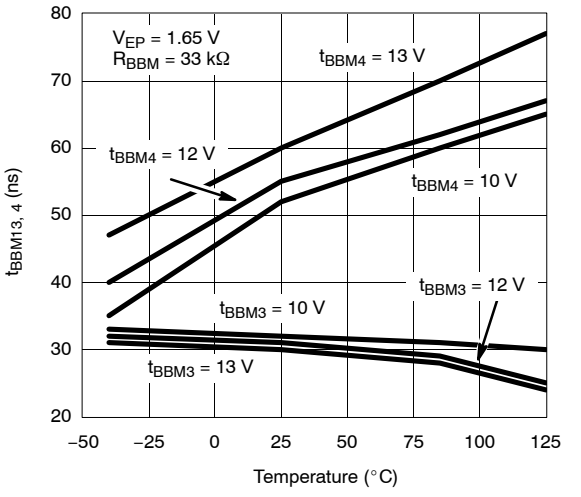
$t_{BBM1, 2}$ vs. Temperature, V_{EP} = 1.65 V



$t_{BBM3, 4}$ vs. Temperature, V_{EP} = 0 V

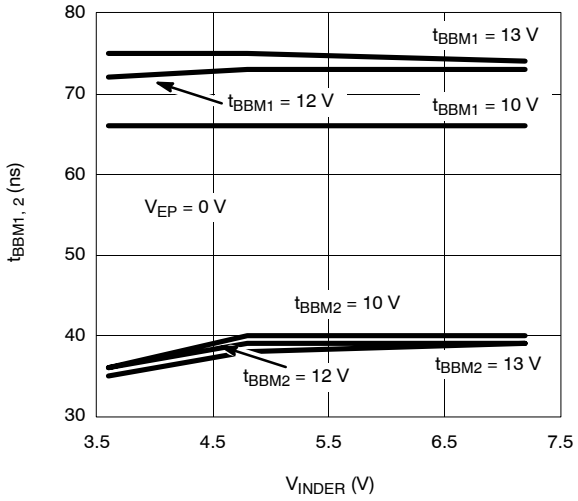


$t_{BBM3, 4}$ vs. Temperature, V_{EP} = 1.65 V

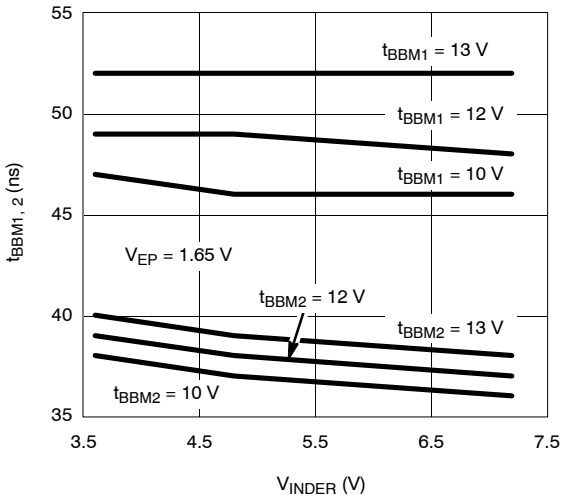


TYPICAL CHARACTERISTICS

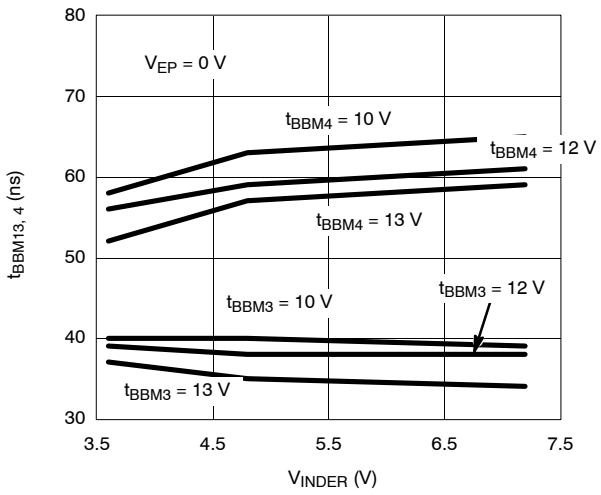
$t_{BBM1, 2}$ vs. V_{CC} vs. V_{INDET}



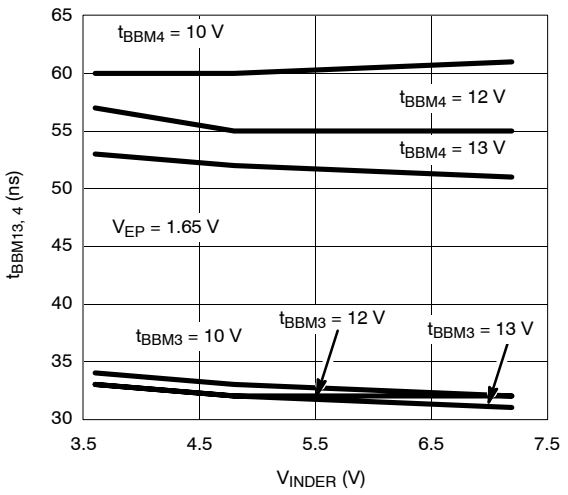
$t_{BBM1, 2}$ vs. V_{INDET} vs. V_{CC}



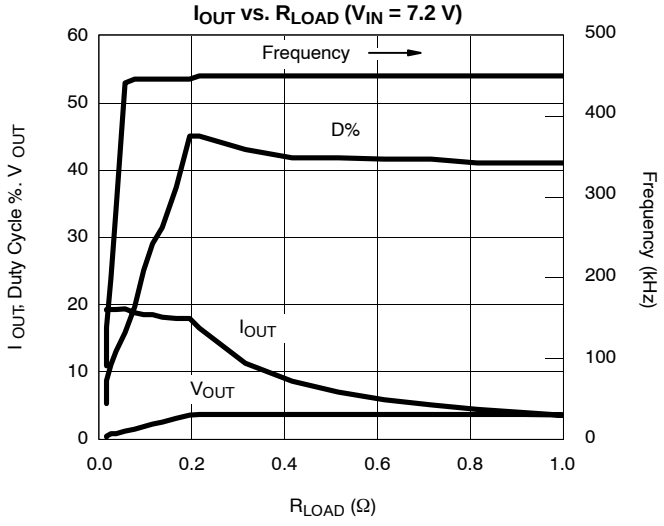
$t_{BBM3, 4}$ vs. V_{CC} vs. V_{INDET}



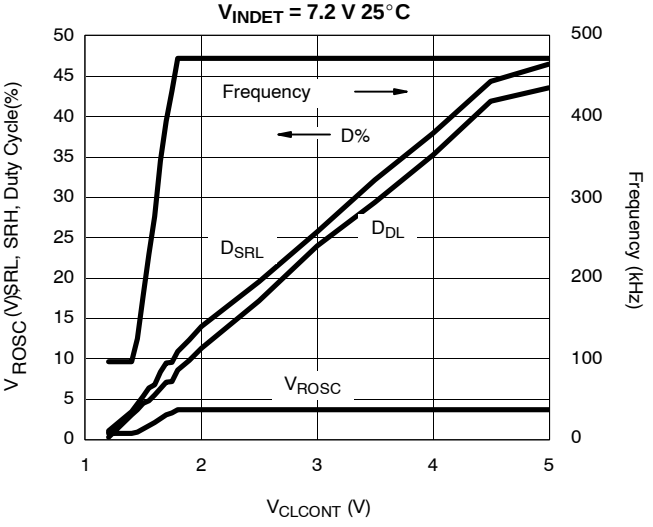
$t_{BBM3, 4}$ vs. V_{INDET} vs. V_{CC}



I_{OUT} vs. R_{LOAD} (V_{IN} = 7.2 V)



Current Sense Duty Cycle vs. V_{CLCONT}
V_{INDET} = 7.2 V 25°C



TYPICAL WAVEFORMS

Figure 7. Foldback Mode, R_L = 0.02 Ω

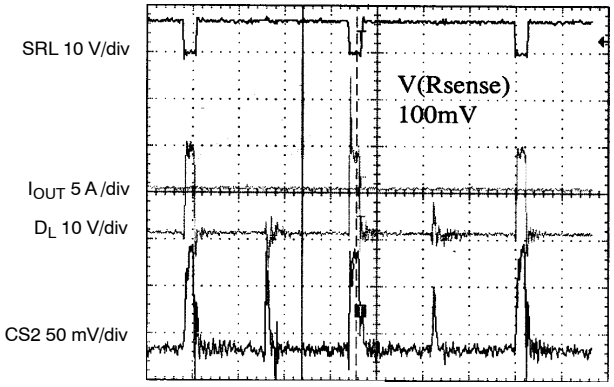


Figure 8. Normal Mode, R_L = 0.1 Ω

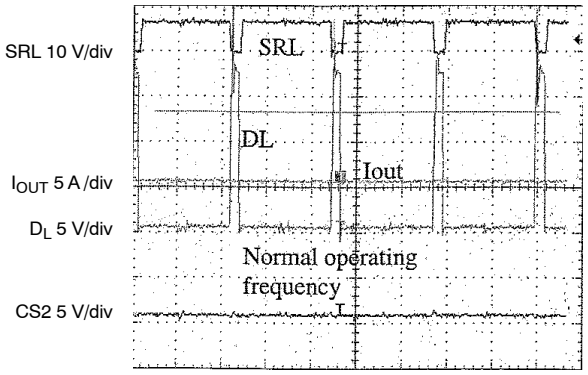


Figure 9. V_{CC} Ramp-Up

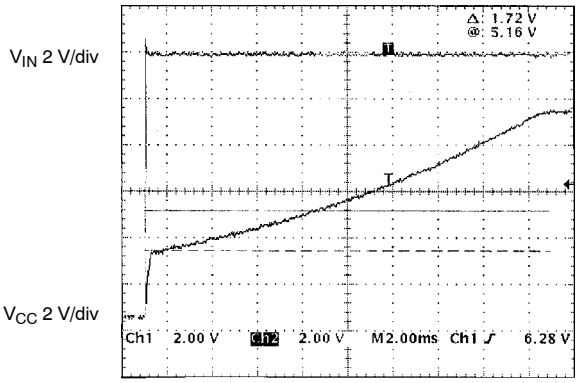


Figure 10. Over Load Recovery—Minimum Overshoot

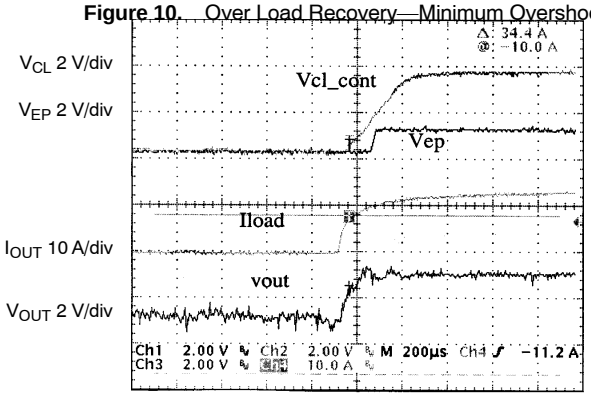


Figure 11. Effective BBM—Measured On Secondary

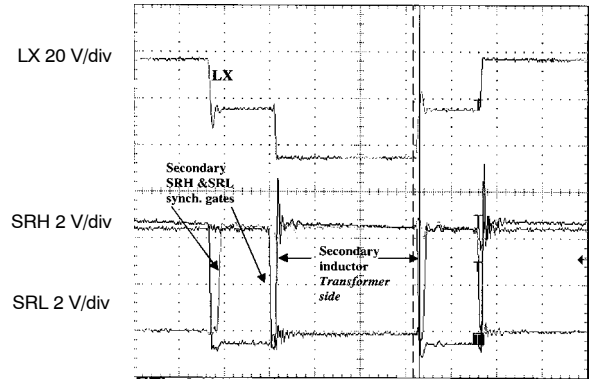
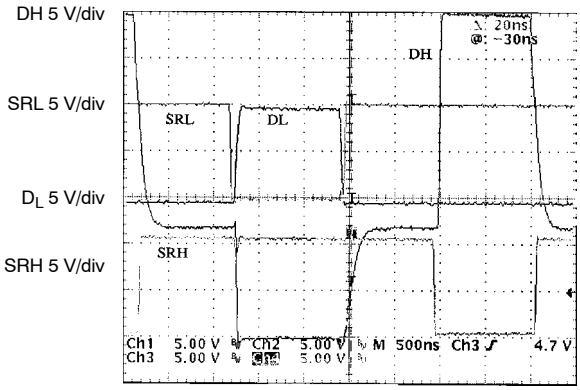


Figure 12. Drive Waveforms



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