

DATA SHEET

PEMD2; PIMD2; PUMD2
NPN/PNP resistor-equipped
transistors; R1 = 22 k Ω , R2 = 22 k Ω

Product specification
Supersedes data of 2002 Sep 05

2003 Jun 06

NPN/PNP resistor-equipped transistors; R1 = 22 k Ω , R2 = 22 k Ω

PEMD2; PIMD2; PUMD2

FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V _{CEO}	collector-emitter voltage	–	50	V
I _O	output current (DC)	–	100	mA
TR1	NPN (PIMD2: PNP)	–	–	–
TR2	PNP (PIMD2: NPN)	–	–	–
R1	bias resistor	22	–	k Ω
R2	bias resistor	22	–	k Ω

DESCRIPTION

NPN/PNP resistor-equipped transistors (see “Simplified outline, symbol and pinning” for package details).

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	PNP/PNP COMPLEMENT	NPN/PNP COMPLEMENT
	PHILIPS	EIAJ			
PEMD2	SOT666		D4	PEMB1	PEMH1
PIMD2	SOT457	SC-74	M5	–	–
PUMD2	SOT363	SC-88	D*2 ⁽¹⁾	PUMB1	PUMH1

Note

1. * = p: Made in Hong Kong.
* = t: Made in Malaysia.
* = W: Made in China.

NPN/PNP resistor-equipped transistors;
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SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PEMD2 PUMD2	<p>Top view</p> <p>MAM468</p>	1 2 3 4 5 6	emitter TR1 base TR1 collector TR2 emitter TR2 base TR2 collector TR1
PIMD2	<p>Top view</p> <p>MAM476</p>	1 2 3 4 5 6	emitter TR2 base TR2 collector TR1 emitter TR1 base TR1 collector TR2

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor; for the PNP transistor with negative polarity					
V _{CBO}	collector-base voltage	open emitter	–	50	V
V _{CEO}	collector-emitter voltage	open base	–	50	V
V _{EBO}	emitter-base voltage	open collector	–	10	V
V _I	input voltage TR1 positive negative		–	+40	V
			–	–10	V
V _I	input voltage TR2 positive negative		–	+10	V
			–	–40	V
I _O	output current (DC)		–	100	mA
I _{CM}	peak collector current		–	100	mA
P _{tot}	total power dissipation SOT363	T _{amb} ≤ 25 °C note 1	–	200	mW
	SOT457	note 1	–	300	mW
	SOT666	notes 1 and 2	–	200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C
Per device					
P _{tot}	total power dissipation SOT363	T _{amb} ≤ 25 °C note 1	–	300	mW
	SOT457	note 1	–	600	mW
	SOT666	notes 1 and 2	–	300	mW

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
Per transistor				
R _{th j-a}	thermal resistance from junction to ambient	T _{amb} ≤ 25 °C		
	SOT363	note 1	625	K/W
	SOT457	note 1	417	K/W
	SOT666	notes 1 and 2	625	K/W
Per device				
R _{th j-a}	thermal resistance from junction to ambient	T _{amb} ≤ 25 °C		
	SOT363	note 1	416	K/W
	SOT457	note 1	208	K/W
	SOT666	notes 1 and 2	416	K/W

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor; for the PNP transistor with negative polarity						
I _{CBO}	collector-base cut-off current	V _{CB} = 50 V; I _E = 0	–	–	100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = 30 V; I _B = 0	–	–	1	μA
		V _{CE} = 30 V; I _B = 0; T _j = 150 °C	–	–	50	μA
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0	–	–	180	mA
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 5 mA	60	–	–	
V _{CEsat}	collector-emitter saturation voltage	I _C = 0.5 mA; I _B = 10 mA	–	–	150	V
V _{i(off)}	input-off voltage	I _C = 100 μA; V _{CE} = 5 V	–	1.1	0.8	V
V _{i(on)}	input-on voltage	I _C = 5 mA; V _{CE} = 0.3 V	2.5	1.7	–	V
R1	input resistor		15.4	22	28.6	k Ω
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
C _c	collector capacitance	I _E = I _e = 0; V _{CB} = –10 V; f = 1 MHz				
	TR1 (NPN) TR2 (PNP)		– –	– –	2.5 3	pF pF

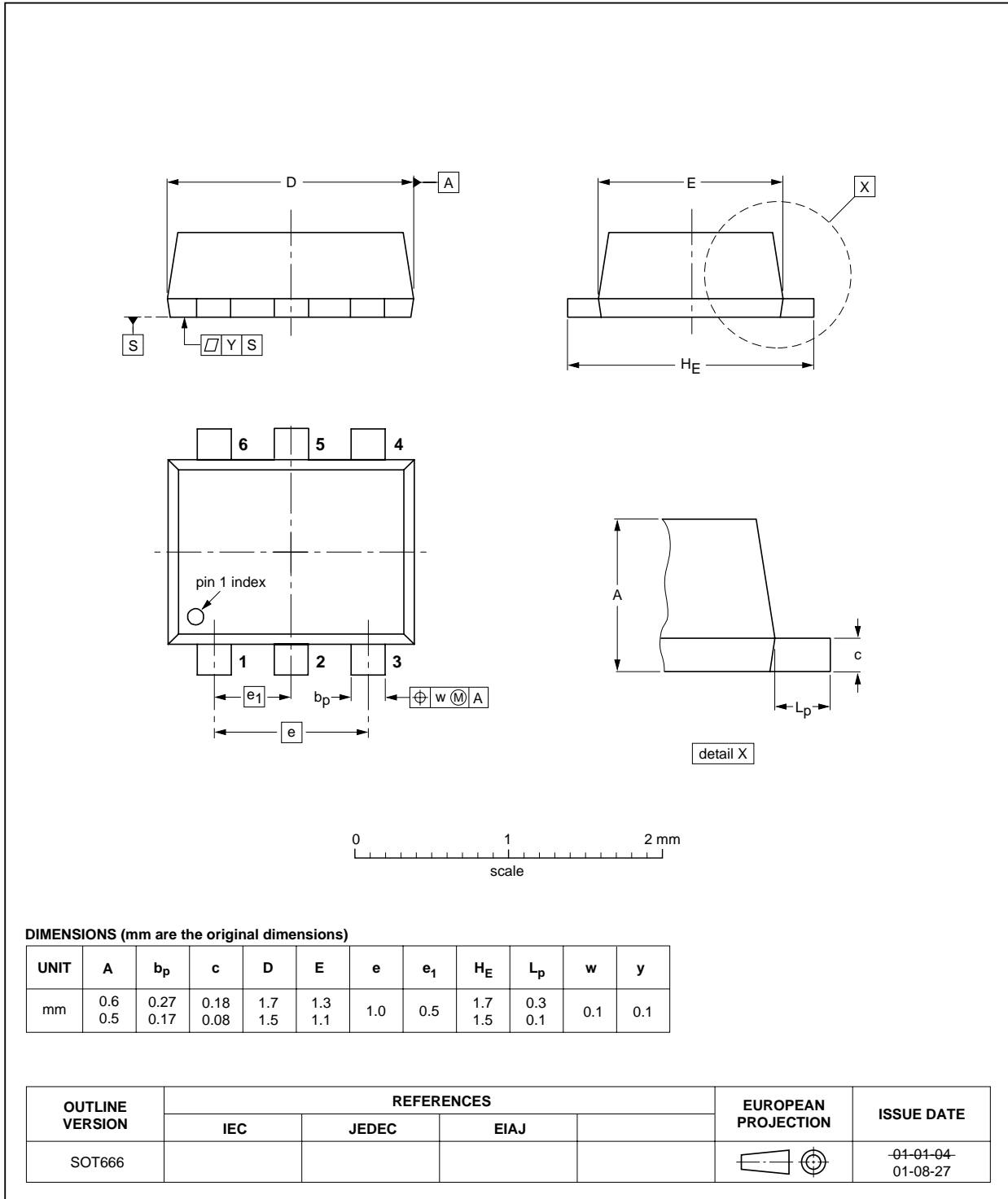
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PACKAGE OUTLINES

Plastic surface mounted package; 6 leads

SOT666



DIMENSIONS (mm are the original dimensions)

UNIT	A	b _p	c	D	E	e	e ₁	H _E	L _p	w	y
mm	0.6	0.27	0.18	1.7	1.3	1.0	0.5	1.7	0.3	0.1	0.1
	0.5	0.17	0.08	1.5	1.1			1.5	0.1		

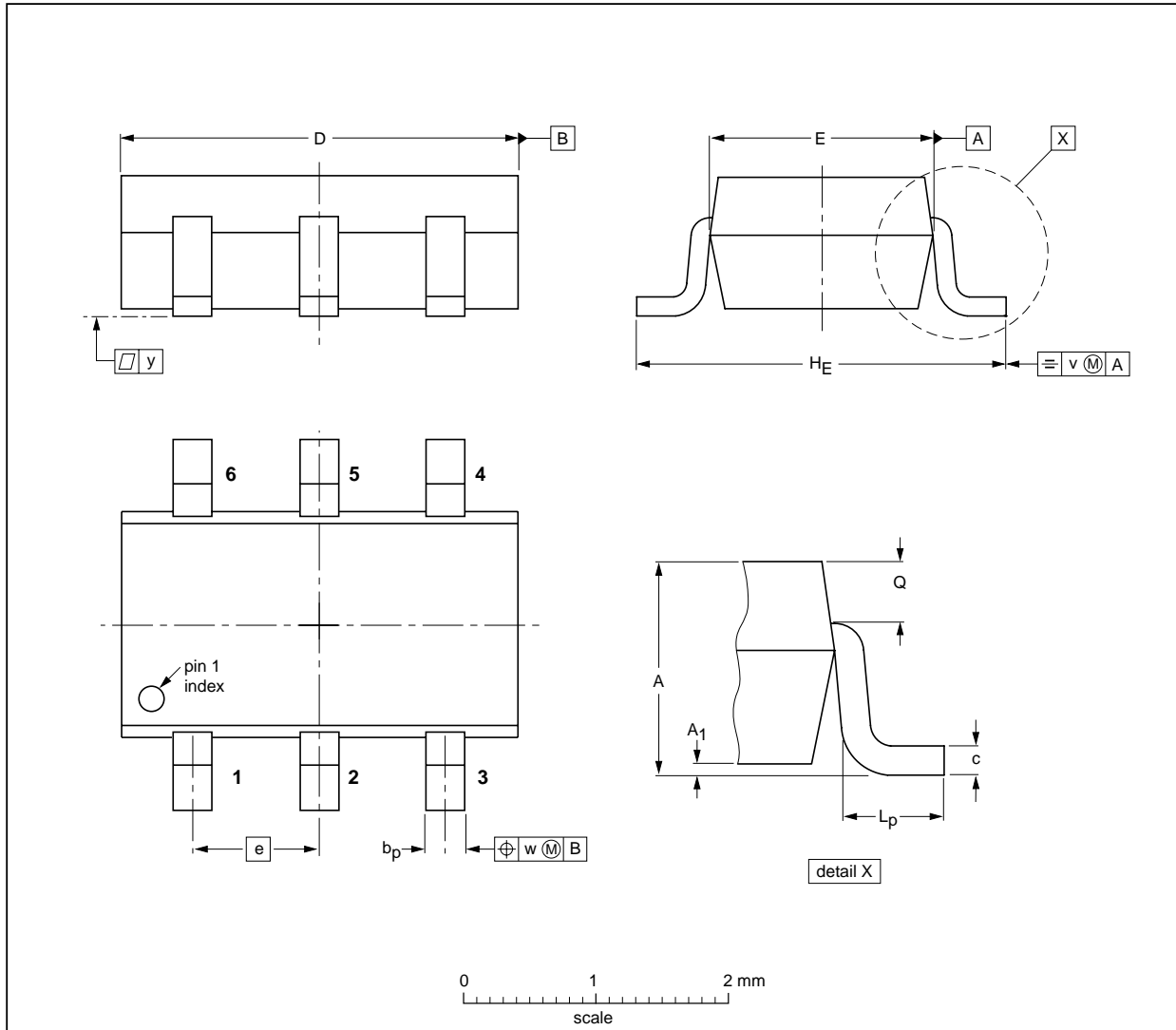
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT666						01-01-04 01-08-27

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SOT457



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b _p	c	D	E	e	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

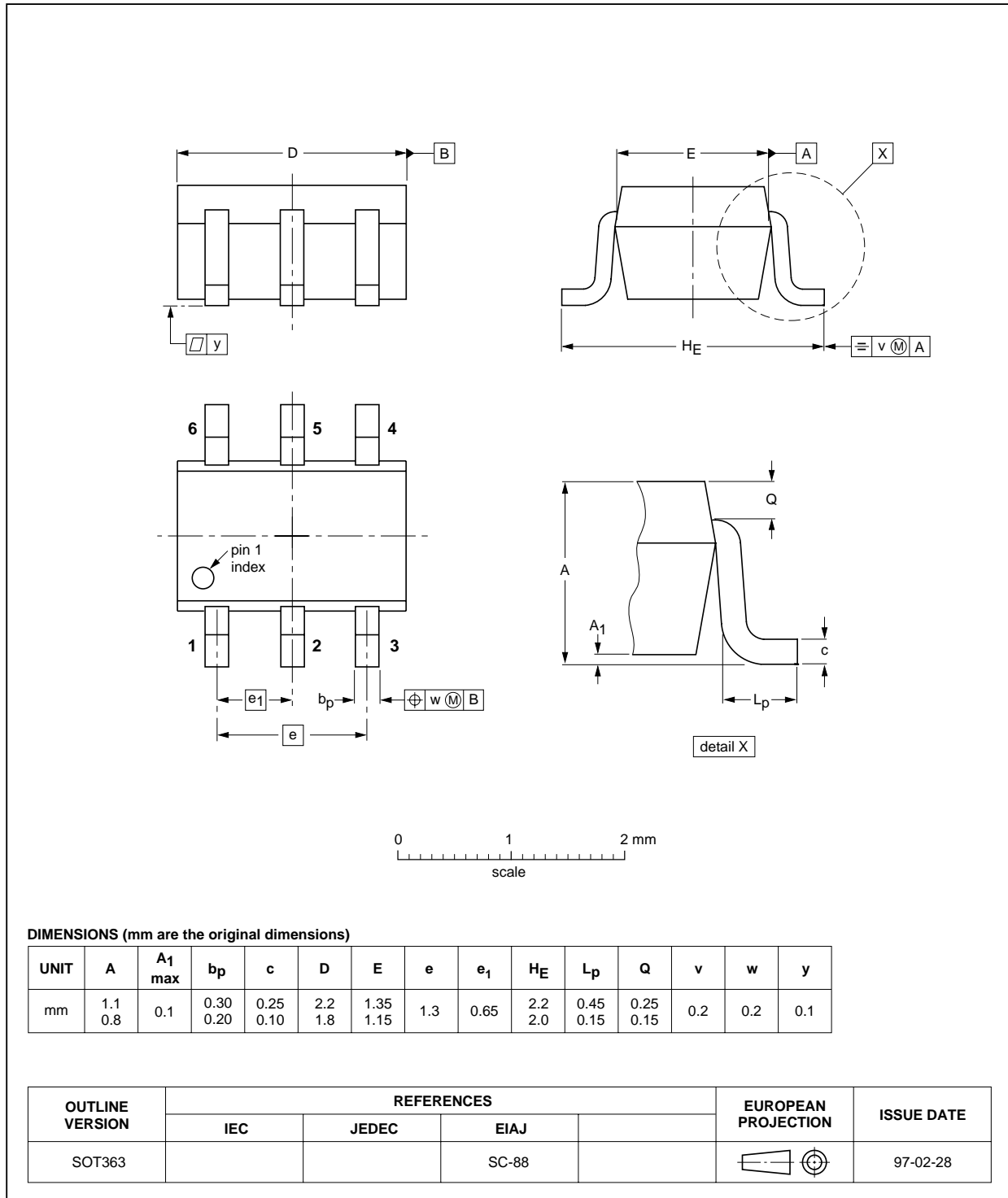
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT457			SC-74			97-02-28 01-05-04

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SOT363



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DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Notes

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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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NOTES

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