High Voltage Current Mode PWM Controller for ISDN Equipment

Ordering Information

$+V_{IN}$		Feedback Accuracy	Max Duty Cycle	Package Options		
Min	Max			14 Pin Plastic DIP	14 Pin Narrow Body SOIC	Die
15V	250V	< ± 1%	49%	HV9605P	HV9605NG	HV9605X

Features

- ☐ BiCMOS/DMOS technology
- ☐ Current mode control
- ☐ 49% duty cycle operation
- ☐ Programmable START/STOP capability
- ☐ 15V to 250V input range internal start-up regulator
- ☐ 6.0µA standby supply current for $+V_{IN}$ <20V
- ☐ 0.9mA operating supply current
- ☐ 5.0V V_{DD} supply operation
- ☐ 30KHz to 300KHz internal oscillator
- ☐ 15KHz to 150KHz converter output frequency
- ☐ 1.0MHz low offset error amplifier
- ☐ 1.20V 2% band gap reference
- ☐ Output driver optimized for under 10W applications
- ☐ Low driver output impedance with V_{DD} = 0V
- ☐ Fast (90nsec) over current shutdown
- ☐ All pins are ESD protected

General Description

The Supertex HV9605 is a BiCMOS/DMOS single-output, current mode, pulse width modulator IC designed to meet the requirements of ETR-060 for ISDN applications. In a 14 pin package, it provides all the necessary functions to implement a single-switch PWM with a minimum of external parts.

Utilizing Supertex's proprietary BiCMOS/DMOS technology, it requires less than one tenth of the operating power of conventional bipolar PWM ICs. Dynamic range for regulation is also increased to approximately 8 times that of similar bipolar parts. It operates directly from any DC input voltage between 15 and 250 VDC. The START and STOP input voltage thresholds can be programmed within the operating input voltage range by means of a resistor divider, provided $+V_{IN(START)} > +V_{IN(STOP)}$. The output stage is push-pull CMOS, eliminating the need for external clamping diodes. The clock frequency is set with a single external resistor.

Applications

- ☐ ISDN network terminations
- ☐ ISDN terminals
- ☐ ISDN terminal adapters
- ☐ Feature phones
- ☐ SLIC circuits
- ☐ PBX systems
- ☐ Modems
- ☐ Distributed power systems
- ☐ DC/DC converters

Absolute Maximum Ratings*

$+V_{IN}$, Input Voltage	-0.5V to +250V
Supply Voltage, V_{DD}	-0.5V to +10V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Power Dissipation @ 25°C, SOIC	750mW
Power Dissipation @ 25°C, Plastic DIP	1000mW

*All voltages referenced to GND

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Electrical Characteristics

Symbol	Parameters	Min	Typ	Max	Unit	Conditions
Pre-Regulator/Start-Up						
$+V_{IN}$	Regulator input voltage	15		250	V	
$+I_{IN}$	Input leakage current			6.0	µA	$+V_{IN}$=20V, Start=0V, Stop=0V
$+I_{IN}$	Input leakage current			50	µA	$+V_{IN}$ = 250V, V_{DD} = 4.7V
$+I_{START}$	Pre-regulator start-up current	5.0			mA	$+V_{IN}$ = 15V, Start & Stop 10MΩ to + V_{IN}
V_{DD}	Regulator output voltage	4.4	4.5	4.6	V	
UVLO	Under voltage lockout threshold	4.1	4.2	4.4	V	V_{DD} rising
HYST	Under voltage hysteresis	0.1	0.3	0.4	V	
Supply						
V_{DD}	Operating range	4.7		8.0	V	
I_{DD}	Supply current		0.9	1.3	mA	OUT open, f_{OUT} = 20KHz to 150KHz, V_{DD} = 5V
Start/Stop Control						
V_{START}	Start threshold	6.72	7.30	7.88	V	
I_{START}	Start input current			0.05	µA	$+V_{IN}$ = 18V
I_{STOP}	Stop input current			0.05	µA	$+V_{IN}$ = 18V
V_{CLAMP}	Zener clamp voltage on STOP Pin	20			V	
MOSFET Driver Output						
$V_{OUT(HIGH)}$	Output high voltage	4.85	4.90		V	I_{OUT} = 10mA, V_{DD} = 5.00V
$V_{OUT(LOW)}$	Output low voltage		0.05	0.15	V	I_{OUT} = -10mA
t_R	Rise time		30	50	nsec	C_L = 250pf
t_F	Fall time		20	50	nsec	C_L = 250pf
Oscillator						
f_{OUT}	Output converter frequency		150		KHz	R_T = 91KΩ
		45	50	55	KHz	R_T = 390KΩ
		31.5	35	38.5	KHz	R_T = 560KΩ
		18	20	22	KHz	R_T = 1.0MΩ
T_C	Temperature coefficient		100	300	PPM/°C	f_{OUT} = 50KHz
Δf/f	Voltage stability		1	3	%	f_{OUT} = 50KHz, 4.5V< V_{DD}<5.5V

Electrical Characteristics (continued)

Symbol	Parameters	Min	Typ	Max	Unit	Conditions
PWM						
D_{MAX}	Maximum duty cycle	49.0		49.9	%	f_{OUT} = 20KHz
D_{MIN}	Minimum duty cycle			0	%	
	Minimum pulse width before pulse drop out		80	125	nsec	
Reference						
V_{REF}	Reference output voltage	1.176	1.200	1.224	V	T_A = 25°C
V_{REF}	Load regulation		1.0	5.0	mV	0 < I_{REF} < 0.3mA
V_{REF}	Line regulation		2.0	5.0	mV	3.0V < V_{DD} < 5.5V
V_{REF}	Reference output voltage	1.159	1.200	1.241	V	-40°C < T_A < 85°C
	Long term stability		3.0		mV	T_A = 125°C, 1000hrs
$I_{REF(SHORT)}$	Short circuit current		0.5	1.0	mA	V_{REF} = SGND
Current Sensing						
V_{CS}	Usable control current sense range			V_{CS} (limit)	V	
$V_{CS\ (LIMIT)}$	Current limit threshold	0.6	0.7	0.8	V	
t_{DELAY}	Current limit delay to output		90	120	nsec	V_{CS} = 1.5V
Error Amplifier						
V_{FB}	Feedback voltage	1.188	1.200	1.212	V	REF shorted to NI, FB shorted to Comp, T_A = 25°C
I_{FB} or I_{NI}	Input bias current		25	200	nA	V_{FB} = 3.0V, V_{NI} = 2.5V
V_{OS}	Input offset voltage		5.0	25	mV	
V_{CM}	Common mode input range	0		V_{DD}-1	V	
A_{VOL}	Open loop voltage gain	65	90		dB	
BW	Unity gain bandwidth	1.0	1.5		MHz	
I_{SOURCE}	Output current sourcing		-2	-1	mA	V_{FB} < V_{NI}
I_{SINK}	Output current sinking	2	4		mA	V_{FB} > V_{NI}
PSRR	Power supply rejection	50	72		dB	4.5V < V_{DD} < 5.5V, f=1KHz
Status Output						
I_{SINK}	Output current sinking	5.0	10		mA	V_{STATUS} = 2.0V
I_{SOURCE}	Output current sourcing	5.0	10	15	µA	
$V_{STATUS(HIGH)}$	High output voltage	V_{DD}-0.2		V_{DD}	V	No load
$V_{STATUS(LOW)}$	Low output voltage		1.0	2.0	V	Sinking 5mA
			0.02	0.04	V	Sinking 100µA
t_R	Rise time	1.0	5.0		msec	4.7nF From Status to GND

Pin Description

SGND - Common connection for all low level signal and digital circuits. While SGND and PGND must be electrically connected together, having separate common pins enhances the ability of the designer to prevent coupling of noise into critical circuits.

PGND - This pin provides common return for the high transient current of the output driver circuits. While PGND and SGND must be electrically connected, having a separate connection prevents common noise created by the high transient currents of the output driver from being injected into critical circuits.

$+V_{IN}$ - This is the start-up linear pre-regulator input which can accept DC input voltages in the range of 15V to 250V. With START and STOP set to more than 20V, the leakage current on this pin is less than 6.0µA at $+V_{IN}$ = 20V.

START - The resistive divider from $+V_{IN}$ sets the start voltage.

STOP - The resistive divider from $+V_{IN}$ sets the stop voltage.

V_{DD} - This is the supply pin for the PWM circuits. When the input voltage to the $+V_{IN}$ pin exceeds the start voltage the input regulator seeks to regulate the voltage on the capacitor connected to this pin to a nominal 4.5V.

OUT - This high current push-pull CMOS output is intended to drive the gate of a power MOSFET. In order to protect the power MOSFET in high electrical noise environment, this output appears as low impedance to PGND when V_{DD} is at zero volts.

CS - This is the current sense input to the PWM comparators. Under normal operation the over current limit is triggered when the voltage on this pin is at 0.70V and the loop control operating peak current may be set to any level below this, typically in the range of 0.2 to 0.5V.

COMP - The low impedance output of the error amplifier.

FB - The high impedance inverting input of the error amplifier.

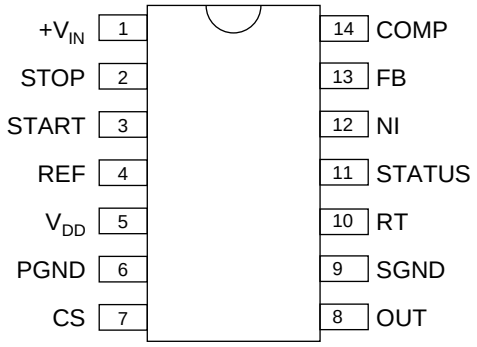
NI - The high impedance non-inverting input of the error amplifier.

REF - This pin provides a 2% accuracy 1.20V low output impedance buffered reference which is current limited to 0.5mAmps and should be bypassed, REF to SGND, with a 0.1µF ceramic capacitor.

RT - The resistor connected from this pin to SGND sets the frequency of the internal oscillator by setting the charging current for the internal timing capacitor. The oscillator frequency is twice the PWM output frequency.

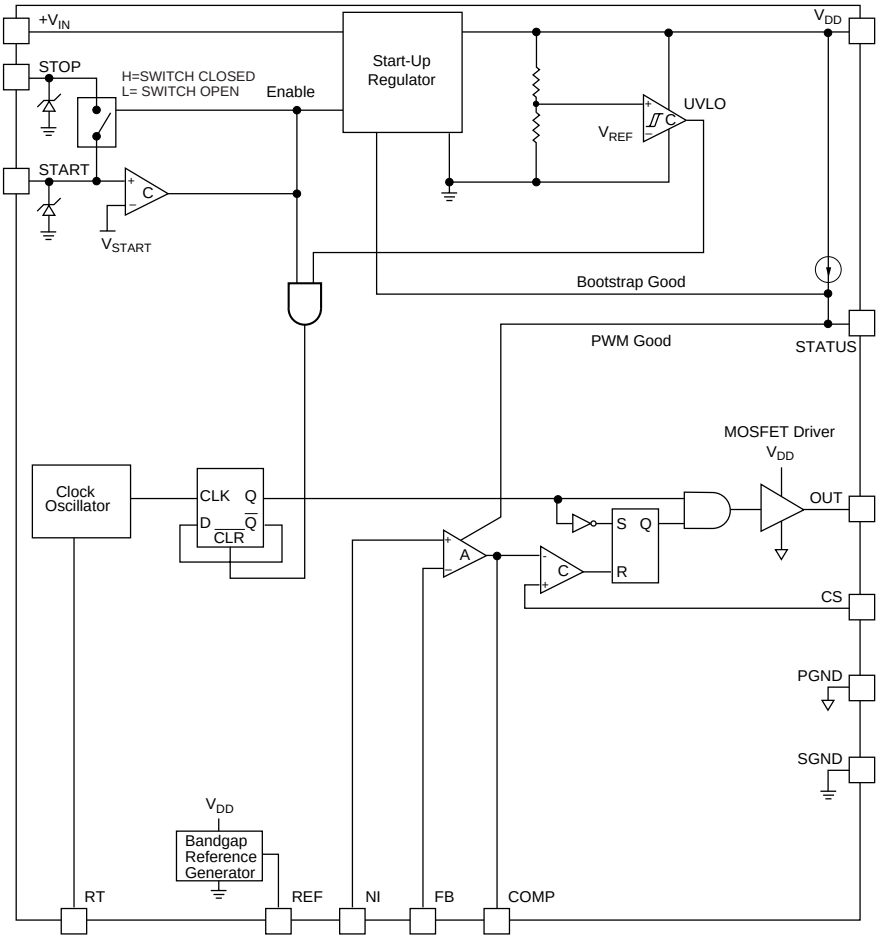
STATUS - This output is held low until the $+V_{IN}$ voltage reaches the programmed START voltage. It remains low until the bootstrap supply to V_{DD} forces the voltage above the internal regulator set point. It is further held low while the control amplifier output on the COMP pin is forced to its high limit by a low output from the converter. Once all these conditions are satisfied, this output will rise to V_{DD} with a time constant set by the external capacitor indicating that normal operation has been reached. This output may be used to control the reset of a microprocessor.

Pin Configuration

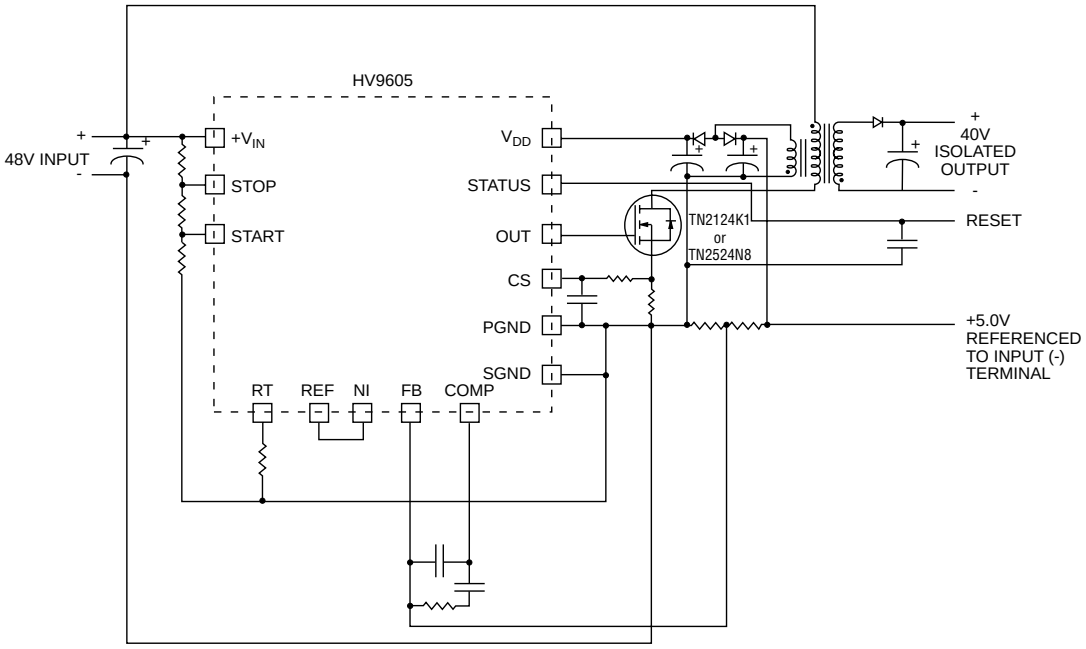


14 Pin SOIC/DIP Package

Functional Block Diagram



Typical Application Circuit



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