High-Voltage Switchmode Controllers with MOSFET

Ordering Information

MOSFET Switch		$+V_{IN}$		Feedback Voltage	Max Duty Cycle	Package Outlines	
BV_{DSS}	$R_{DS(ON)}$	Min	Max			14 Pin Plastic DIP	20 Pin Plastic PLCC
200V	5.0Ω	10V	120V	±1%	49%	HV9105P	HV9105PJ
200V	5.0Ω	10V	120V	±1%	99%	HV9108P	HV9108PJ

Standard temperature range for all parts is industrial (-40° to +85°C).

Features

- ❑ 10 to 120V input range
- ❑ 200V, 5Ω output MOSFET
- ❑ Current-Mode Control
- ❑ High Efficiency
- ❑ CCITT Compatible
- ❑ Internal Start-up Circuit

Applications

- ❑ DC/DC Converters
- ❑ Distributed Power Systems
- ❑ ISDN Equipment
- ❑ PBX Systems
- ❑ Modems

General Description

The Supertex HV9105 and HV9108 are high-efficiency high voltage SMPS ICs intended for use in power converters requiring extreme efficiency at output power levels of 5.0W or less. The low supply current (0.5mA max) allows them to be used to build supplies which meet CCITT I.430 performance recommendations (60% efficiency at .025W out).

The HV9105/08 provides all the functions necessary to build a single-switch current-mode converter of any common topology, with a minimum of external parts.

In addition to high efficiency, because it uses Supertex's proprietary high voltage BiCMOS/DMOS technology, the HV9105/08 offers numerous performance advantages when compared to conventional PWM ICs. Dynamic range is approximately 8 times wider than with bipolar ICs, both response speed and maximum clock rate are faster, and no external power resistors or zeners are necessary for high voltage starting.

Accessory circuits are included to provide either latching or nonlatching shutdown. When shut down, device dissipation is less than 4mW.

The HV9105/08 is intended for operation with input voltages from 10 to 120VDC.

Absolute Maximum Ratings

$+V_{IN}$, Input Voltage	120V
V_{DS}	200V
V_{DD}, Logic Voltage	15.0V
Control Inputs	-0.3V to V_{DD}+0.3V
I_D (Peak)	2.5A
Storage Temperature	-65°C to 150°C
Power Dissipation, Plastic DIP	750mW
Power Dissipation, PLCC	1400mW

For detailed circuit and application information, please refer to application notes AN-H13 and AN-H21 to AN-H24.

11/12/01

Electrical Characteristics

(V_{DD} = 10V, $+V_{IN}$ = 48V, Discharge = $-V_{IN}$ = 0V, R_{BIAS} = 820KΩ, R_{OSC} = 910KΩ, T_A = 25°C, unless otherwise specified)

Symbol	Parameters		Min	Typ	Max	Unit	Conditions
Reference							
V_{REF}	Output Voltage		3.92	4.00	4.08	V	R_L = 10MΩ
Z_{OUT}	Output Impedance[1]		15	30	45	KΩ	
I_{SHORT}	Short Circuit Current			100	130	µA	V_{REF} = $-V_{IN}$
ΔV_{REF}	Change in V_{REF} with Temperature			0.25		mV/°C	
Oscillator							
f_{MAX}	Maximum Oscillator Frequency		1.0	3.0		MHz	R_{OSC} = 0Ω
f_{OSC}	Initial Accuracy[2]		32	40	48	KHz	
	Voltage Stability[1]				15	%	9.5V < V_{DD} < 13.5V
	Temperature Coefficient[1]			170		ppm/°C	
PWM							
D_{MAX}	Maximum Duty Cycle[1]	HV9105	49.0	49.4	49.6	%	
		HV9108	99.0	99.4	99.6		
	Deadtime[1]	HV9108		100		nsec	
D_{MIN}	Minimum Duty Cycle				0	%	
	Minimum Pulse Width Before Pulse Drops Out[1]			110	175	nsec	
Error Amplifier							
V_{FB}	Feedback Voltage		3.96	4.00	4.04	V	V_{FB} Shorted to Comp
I_{IN}	Input Bias Current			25	500	nA	V_{FB} = 4.0V
V_{OS}	Input Offset Voltage			nulled at trim		mV	
A_{VOL}	Open Loop Voltage Gain[1]		60	80		dB	
gbw	Unity Gain Bandwidth[1]		0.5	0.8		MHz	
Z_{OUT}	Output Impedance[1]			See Fig. 2		Ω	
I_{SOURCE}	Output Source Current			-1.3	-1.0	mA	V_{FB} = 3.4V
I_{SINK}	Output Sink Current		50	80		µA	V_{FB} = 4.5V
PSRR	Power Supply Rejection[1]			See Fig. 1			
Current Limit							
V_{SOURCE}	Threshold Voltage		1.0	1.2	1.4	V	V_{FB} = 0V, R_L = 100Ω
t_d	Delay to Output[1]			150	200	ns	V_{SOURCE} = 1.5V, R_L = 100Ω
Pre-Regulator/Startup							
$+V_{IN}$	Allowable Input Voltage				120	V	I_{IN} = 10µA
	Input Leakage Current				10	µA	V_{DD} > 9.4V
V_{TH}	V_{DD} Pre-regulator Turn-off Threshold Voltage		7.8	8.6	9.4	V	I_{PREREG} = 10µA
V_{LOCK}	Undervoltage Lockout		7.0	8.1	8.9	V	R_L = 100Ω from Drain to V_{DD}

Notes:

1. Guaranteed by design. Not subject to production test.
2. Stray capacitance on OSC IN pin ≤5pF.

Electrical Characteristics (Continued)

(V_{DD} = 10V, $+V_{IN}$ = 48V, Discharge = $-V_{IN}$ = 0V, R_{BIAS} = 820KΩ, R_{OSC} = 910KΩ,T_A = 25°C, unless otherwise specified)

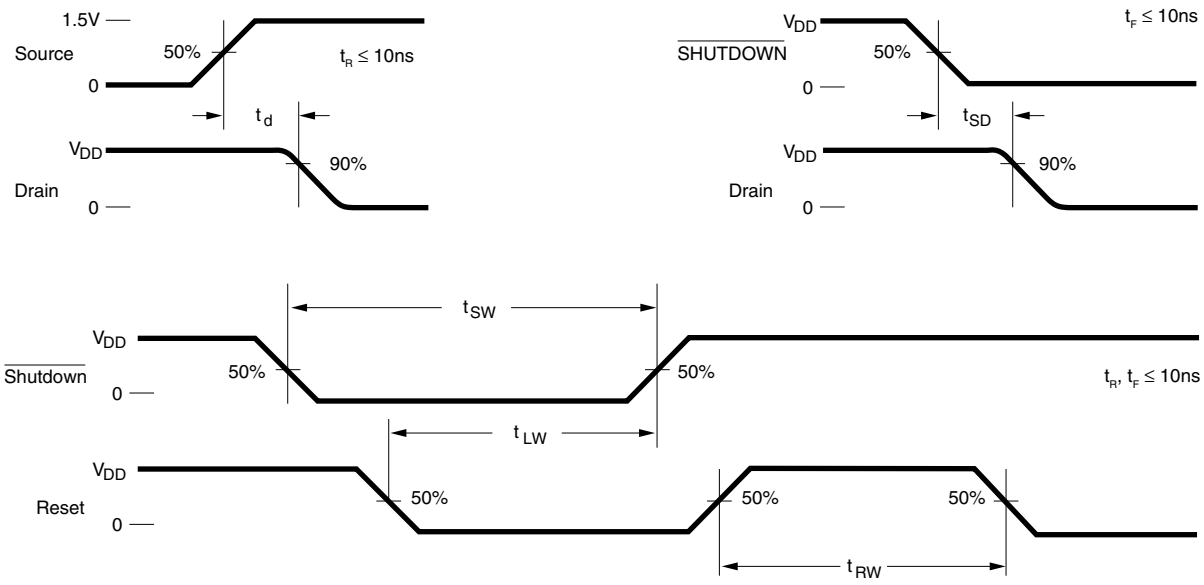
Symbol	Parameters	Min	Typ	Max	Unit	Conditions
Supply						
I_{DD}	Supply Current			0.6	mA	
			0.35		mA	$\overline{\text{Shutdown}}$ = $-V_{IN}$
I_{BIAS}	Bias Current		7.5		µA	
V_{DD}	Operating Range	9.0		13.5	V	
Logic						
t_{SD}	$\overline{\text{Shutdown}}$ Delay Time[1]		50	100	ns	V_{SOURCE} = $-V_{IN}$
t_{SW}	$\overline{\text{Shutdown}}$ Pulse Width[1]	50			ns	
t_{RW}	RESET Pulse Width[1]	50			ns	
t_{LW}	Latching Pulse Width[1]	25			ns	
V_{IL}	Input Low Voltage			2.0	V	
V_{IH}	Input High Voltage	7.0			V	
I_{IH}	Input High Current		1.0	5.0	µA	V_{IN} = 10V
I_{IL}	Input Low Current		-25	-35	µA	V_{IN} = 0V
MOSFET Switch						
BV_{DSS}	Breakdown Voltage	200	240		V	V_{SOURCE} = $\overline{\text{Shutdown}}$ = 0V, I_D = 100µA
$R_{DS(ON)}$	Drain-to-Source On-resistance		3.5	5.0	Ω	V_{SOURCE} = 0V, I_D = 100mA
I_{DSS}	OFF State Drain Leakage Current			10	µA	V_{SOURCE} = $\overline{\text{Shutdown}}$ = 0V, V_{DRAIN} = 100V
C_{DS}	Drain Capacitance		35		pF	V_{DS} = 25V, $\overline{\text{Shutdown}}$ = 0V

Note:
1. Guaranteed by design. Not subject to production test.

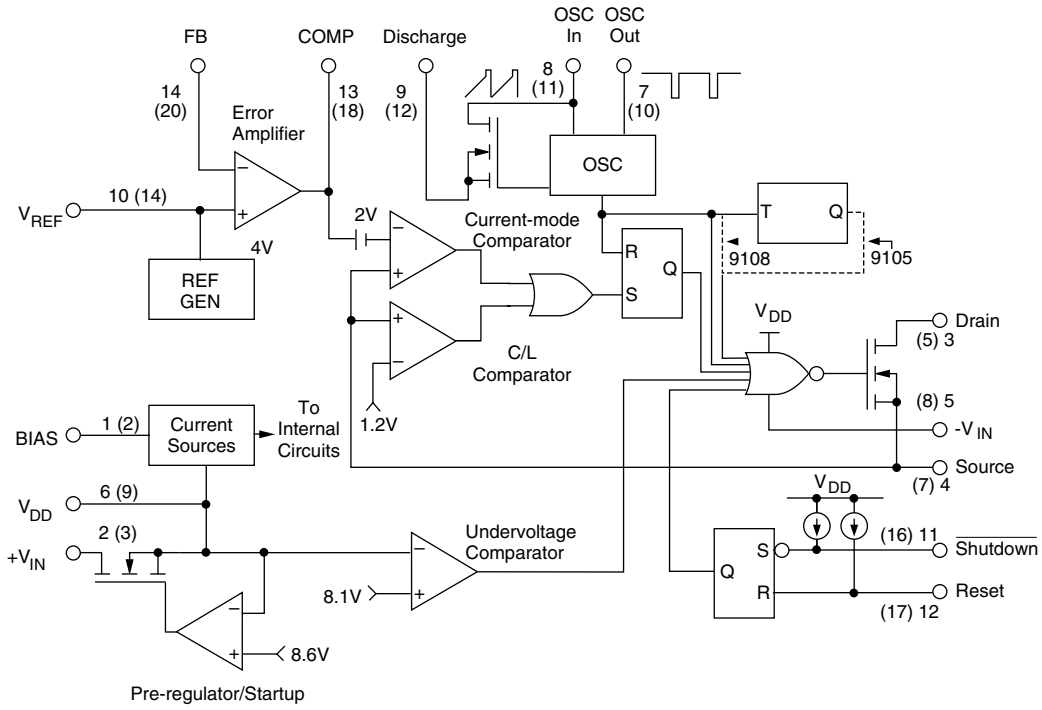
Truth Table

$\overline{\text{Shutdown}}$	Reset	Output
H	H	Normal Operation
H	H → L	Normal Operation, No Change
L	H	Off, Not Latched
L	L	Off, Latched
L → H	L	Off, Latched, No Change

Switching Waveforms



Functional Block Diagram



Pin numbers in parentheses are for PLCC package.

Typical Performance Curves

Fig. 1 PSRR – Error Amplifier and Reference

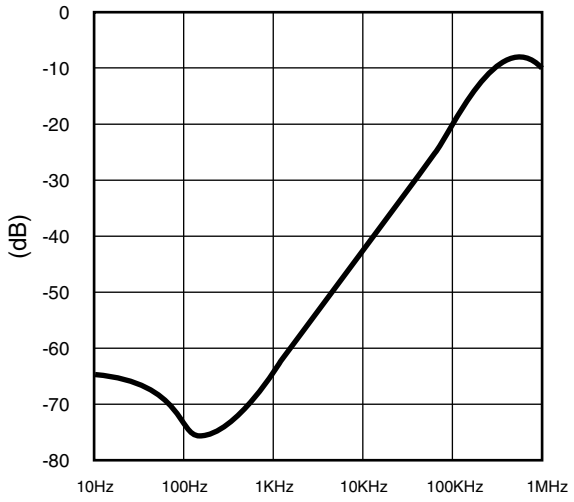


Fig. 2 Error Amplifier Output Impedance (Z_0)

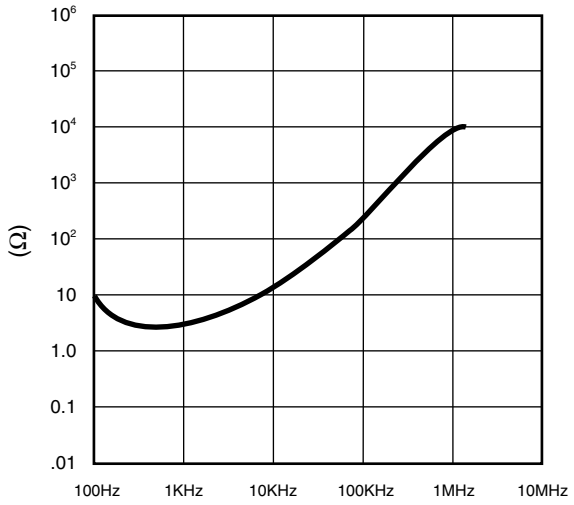


Fig. 3 Error Amplifier Open Loop Gain/Phase

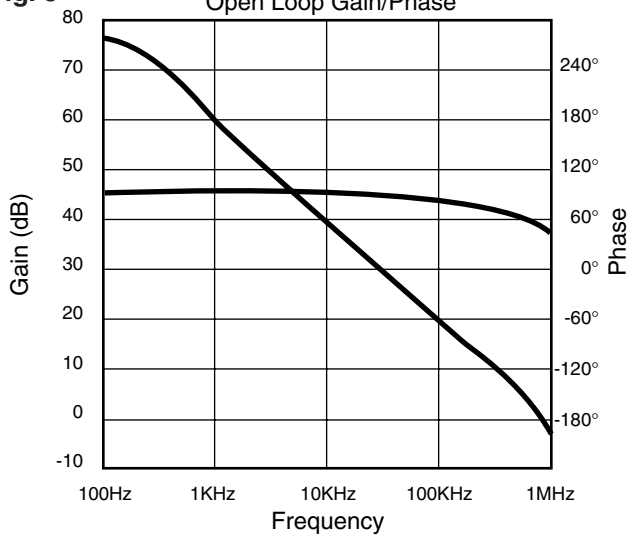
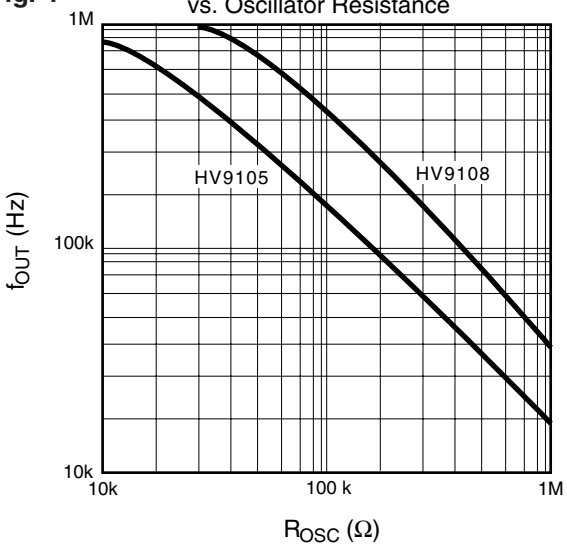
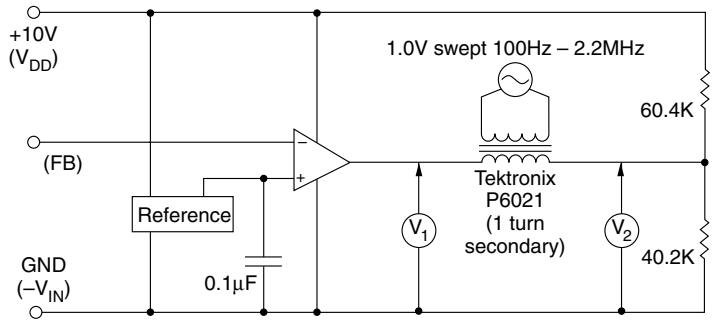


Fig. 4 Output Switching Frequency vs. Oscillator Resistance

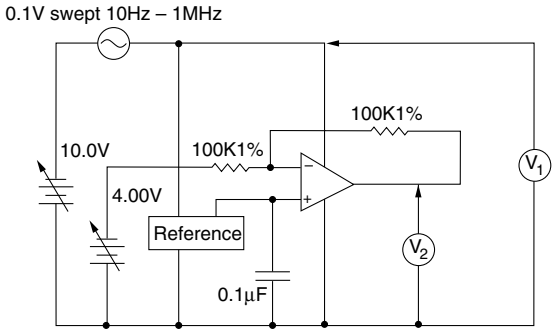


Test Circuits

Error Amp Z_{OUT}



PSRR



NOTE: Set Feedback Voltage so that
$V_{COMP} = V_{DIVIDE} \pm 1mV$ before connecting transformer

Technical Description

Preregulator

The preregulator/startup circuit for the HV9105/08 consists of a high-voltage N-channel depletion-mode DMOS transistor driven by an error amplifier to form a controlled current path between the V_{IN} terminal and the V_{DD} terminal of the HV9105/08. Maximum current (about 20 mA) occurs when $V_{DD} = 0$, with current reducing as V_{DD} rises. This path shuts off altogether when V_{DD} rises to somewhere between 7.8 and 9.4V, so that if V_{DD} is held at 10 or 12V by an external source (generally the supply the chip is controlling) no current other than leakage is drawn through the high voltage transistor. This minimizes dissipation.

An external capacitor between V_{DD} and V_{SS} is generally required to store energy used by the chip during the time between shutoff of the high voltage path and the V_{DD} supply's output rising enough to take over the powering of the chip. This capacitor generally also serves as the output filter capacitor for that output from the supply. 1.0μF is generally sufficient to assure against double-starting. Capacitors as small as 0.1μF can work when faster response from the V_{DD} line is required. The chosen capacitor should have very good high frequency characteristics and be mounted so that the sum of the lead length between capacitor and IC for both leads is less than 2.5 cm. Stacked polyester or ceramic capacitors work well. Electrolytic capacitors are generally not suitable.

A common resistor divider string is used to monitor V_{DD} for both the undervoltage lockout circuit and the shutoff circuit of the high voltage FET. Setting the undervoltage sense point about 0.6V lower on the string than the FET shutoff point guarantees that the undervoltage lockout always releases before the FET shuts off.

Bias Circuit

An external bias resistor, connected between the bias pin and V_{SS} is required by the HV9105/08 to set currents in a series of current mirrors used by the analog sections of the chip. Nominal external bias current requirement is 7.5μA, which can be set by a 820KΩ to 1.3MΩ resistor if a 10V V_{DD} is used, or a 1.2MΩ to 2.0MΩ resistor if a 12V V_{DD} is used. A precision resistor is NOT required; ± 5% is fine.

For extremely low power operation, the value of bias current can be reduced to as low as 4.0μA by further increases in the value of the bias resistor.

Clock Oscillator

The clock oscillator of the HV9105/08 consists of a ring of CMOS inverters, timing capacitors, a capacitor discharge FET, and, in the 50% maximum duty cycle version, a frequency dividing flip-flop. A single external resistor between the OSC In and OSC Out pins is required to set oscillator frequency (see Fig. 4). For the 50% maximum duty cycle versions the 'Discharge' pin is internally connected to GND. For the 99% duty cycle version, 'Discharge' can either be connected to V_{SS} directly or connected to V_{SS} through a resistor used to set a deadtime.

One difference exists between the Supertex HV9105/08 and competitive 9105 parts. The oscillator of the Supertex HV9105/08 is shut off when a shutoff command is received. This saves about 100μA of quiescent current, which aids in the construction of power supplies to meet CCITT specification I.430, and in other situations where an absolute minimum of quiescent power dissipation is required.

Reference

The reference section of the HV9105/08 consists of a stable bandgap reference followed by a buffer amplifier which scales the voltage up to approximately 4.0V. The scaling resistors of the reference buffer amplifier are trimmed during manufacture so that the output of the error amplifier when connected in a gain of -1 configuration is as close to 4.000V as possible. This nulls out any input offset of the error amplifier. As a consequence, even though the observed reference voltage of a specific part may not be exactly 4.0V, the feedback voltage required for proper regulation will be 4.0V.

A resistor of approximately 50KΩ is placed internally between the output of the reference buffer amplifier and the circuitry it feeds (reference output pin and non-inverting input to the error amplifier). This allows overriding the internal reference with a low-impedance voltage source ≤6.0V. In general, because the reference voltage of the Supertex HV9105/08 is not noisy, as some previous devices have been, overriding the reference should seldom be necessary.

Because the reference is a high impedance node, and usually there will be significant electrical noise near it, a bypass capacitor between the reference pin and V_{SS} is strongly recommended. The reference buffer amplifier is intentionally compensated to be stable with a capacitive load of 0.01 to 0.1μF.

Error Amplifier

The error amplifier is a true low-power differential input operational amplifier intended for around-the-amplifier compensation. It is of mixed CMOS-bipolar construction: a PMOS input stage is used so the common-mode range includes ground and the input impedance is very high. This is followed by bipolar gain stages which provide high gain without the electrical noise of all-MOS amplifiers. The amplifier is unity-gain stable.

Current Sense Comparators

The HV9105/08 uses a true dual comparator system with independent comparators for modulation and current limiting. This allows the designer greater latitude in compensation design, as there are no clamps (except ESD protection) on the compensation pin. Like the error amplifier, the comparators are of low-noise BiCMOS construction.

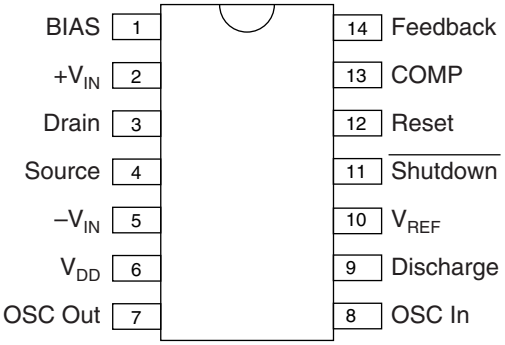
Remote Shutdown

The shutdown and reset pins can be used to perform either latching or non-latching shutdown of a converter as required. These pins have internal current source pull-ups so they can be driven from open-drain logic. When not used, they should be left open, or connected to V_{DD}.

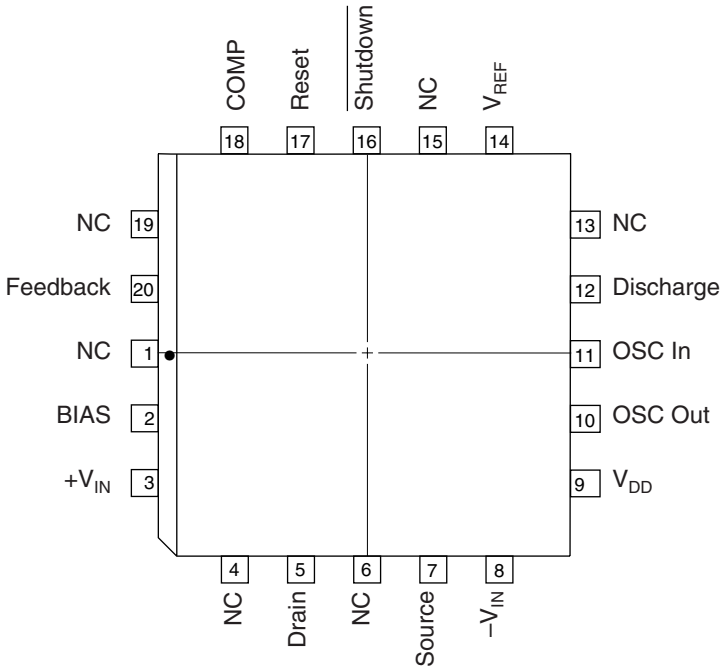
Main Switch

The main switch is a normal N-channel power MOSFET. Unlike the situation with competitive devices, the body diode can be used if desired without destroying the chip.

Pinout



14 Pin DIP Package



20-pin PJ Package
top view

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