Features

- JEDEC Standard 168-pin SDRAM DIMM
- PC-100 Spec Compliant – Lowest Latency
- Single 3.3V ± 0.3V Power Supply
- Unbuffered
- Fully Synchronous Operation
- Sustained Random Burst Reads (Same Bank Access)
  - 1-1-1-1 at 66MHz (CL=1)
  - 2-1-1-1 at 133MHz (CL=2)
- Programmable Burst Lengths: 1, 2, 4, 8, or Full page
- Early Auto-Precharge and Auto-Refresh Modes
- 64ms, 2048 Cycle Refresh
- LVTTL Compatible Inputs and I/Os
- On-Board Serial Presence Detect (SPD) EEPROM with Write Protect Input

Description

The Enhanced SDRAM (ESDRAM) DIMMs are low latency, high performance memory modules of 8, 16, and 32 MByte capacities, and are organized x64 bits wide. The DIMMs are 100% pin, function, and timing compatible with JEDEC standard 168-pin SDRAM DIMMs. The 8MB and 16MB DIMMs employ a single physical bank of memory while the 32MB DIMMs are built as two physical banks. Within each physical bank of memory are two logical banks, which are accessed through the use of BA0 (pin 122). All control, access, and data input signals are registered into each of the ESDRAM components through use of an external clock, CK0-CK3. The rising edge of the clock is used as the timing reference for all inputs and outputs.

ESDRAM DIMMs provide pipelined burst SRAM performance up to 66MHz and nearly the same at bus speeds up to 133MHz. The speed grade of each DIMM is specified to real system operation. No de-rating is necessary. For example, the 10ns DIMM operates at 100MHz in CL=2 mode, and the 7.5ns DIMM operates at 66MHz in CL=1 mode and up to 133MHZ in CL=2 mode.

All ESDRAM DIMMs operate from a 3.3V power supply, and all inputs and outputs are LVTTL compatible. See the ESDRAM component data sheet for a more detailed discussion of ESDRAM specifications and functional operation.

Pin Assignments

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	S3#
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	Vdd	48	DU	90	Vdd	132	RFU
7	DQ4	49	Vdd	91	DQ36	133	Vdd
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vdd	101	DQ45	143	Vdd
18	Vdd	60	DQ20	102	Vdd	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	NC	63	CKE1	105	NC	147	NC
22	NC	64	Vss	106	NC	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vdd	68	Vss	110	Vdd	152	Vss
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	S1#	156	DQ59
31	DU	73	Vdd	115	RAS#	157	Vdd
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	CK3
38	A10/AP	80	NC	122	BA0	164	NC
39	RFU	81	WP	123	RFU	165	SA0
40	Vdd	82	SDA	124	Vdd	166	SA1
41	Vdd	83	SCL	125	CK1	167	SA2
42	CK0	84	Vdd	126	RFU	168	Vdd

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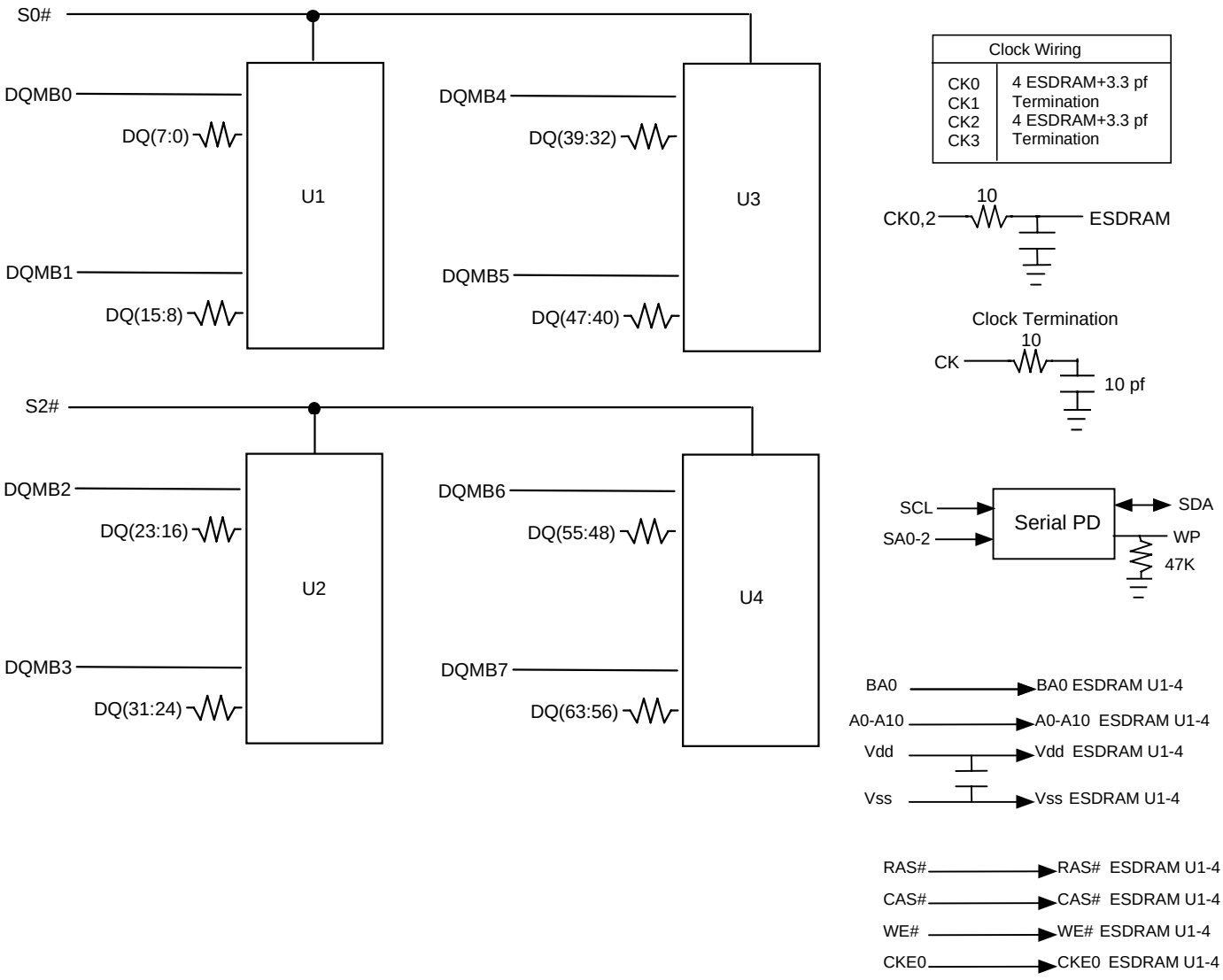
Pin Descriptions

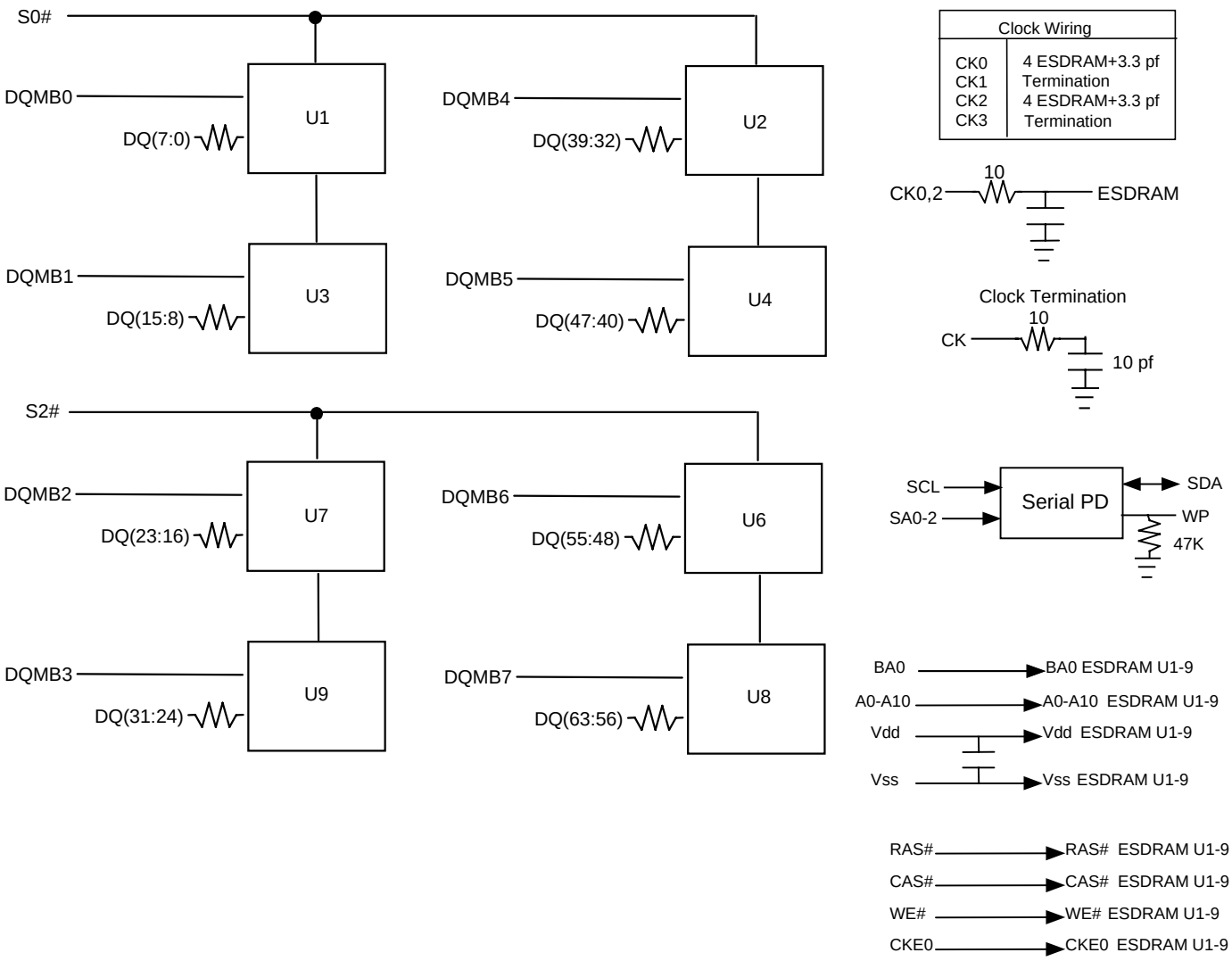
Symbol	Type	Function
CK0,1,2,3	Input	Clocks: All ESDRAM input signals are sampled on the positive edge of CK.
CKE0,1	Input	Clock Enables: CKE activates (high) or deactivates (low) the CK signals. Deactivating the clock initiates the Power-Down and Self-Refresh operations (all banks idle), or Clock Suspend operation. CKE is synchronous until the device enters Power-Down and Self-Refresh modes where it is asynchronous until the mode is exited.
S0,1,2,3#	Input	Chip Select: S# enables (low) or disables (high) the command decoder. When the command decoder is disabled, new commands are ignored but previous operations continue.
RAS#, CAS#, WE#	Input	Command Inputs: Sampled on the rising edge of CK, these inputs define the command to execute.
BA0	Input	Bank Address: This input defines to which bank a command is applied.
A0-A10	Input	Address Inputs: A0-A10 define the row address during the Bank Activate command. A0-A8 define the column address during Read and Write commands. A10/AP invokes the Auto-Precharge operation. During manual Precharge commands, A10/AP low specifies a single bank precharge while A10/AP high precharges all banks. The address inputs are also used to program the Mode Register.
DQ0-DQ63	Input/ Output	Data I/O: Data bus inputs and outputs. For Write cycles, input data is applied to these pins and must be set-up and held relative to the rising edge of clock. For Read cycles, the device drives output data on these pins after the CAS latency is satisfied.
DQMB0-7	Input	Data I/O Mask Inputs: DQMB0-7 inputs mask write data (zero latency) and acts as a synchronous output enable (2-cycle latency) for read data.
V_{DD}	Supply	Power Supply: +3.3 V
V_{SS}	Supply	Ground
SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bi-directional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence detect data transfer to and from the module
SA0-2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence detect device.
WP	Input	Serial Presence Detect Write Protect: Active high inhibits writes to the SPD EEPROM. WP must be driven low for normal read/write operations.
RFU	-	Reserved for Future Use: These pins should be left unconnected.
DU	-	Do not use.
NC	-	No connect - open pin.

1Mx64 (8MB) DIMM Functional Block Diagram – SM1M64DT



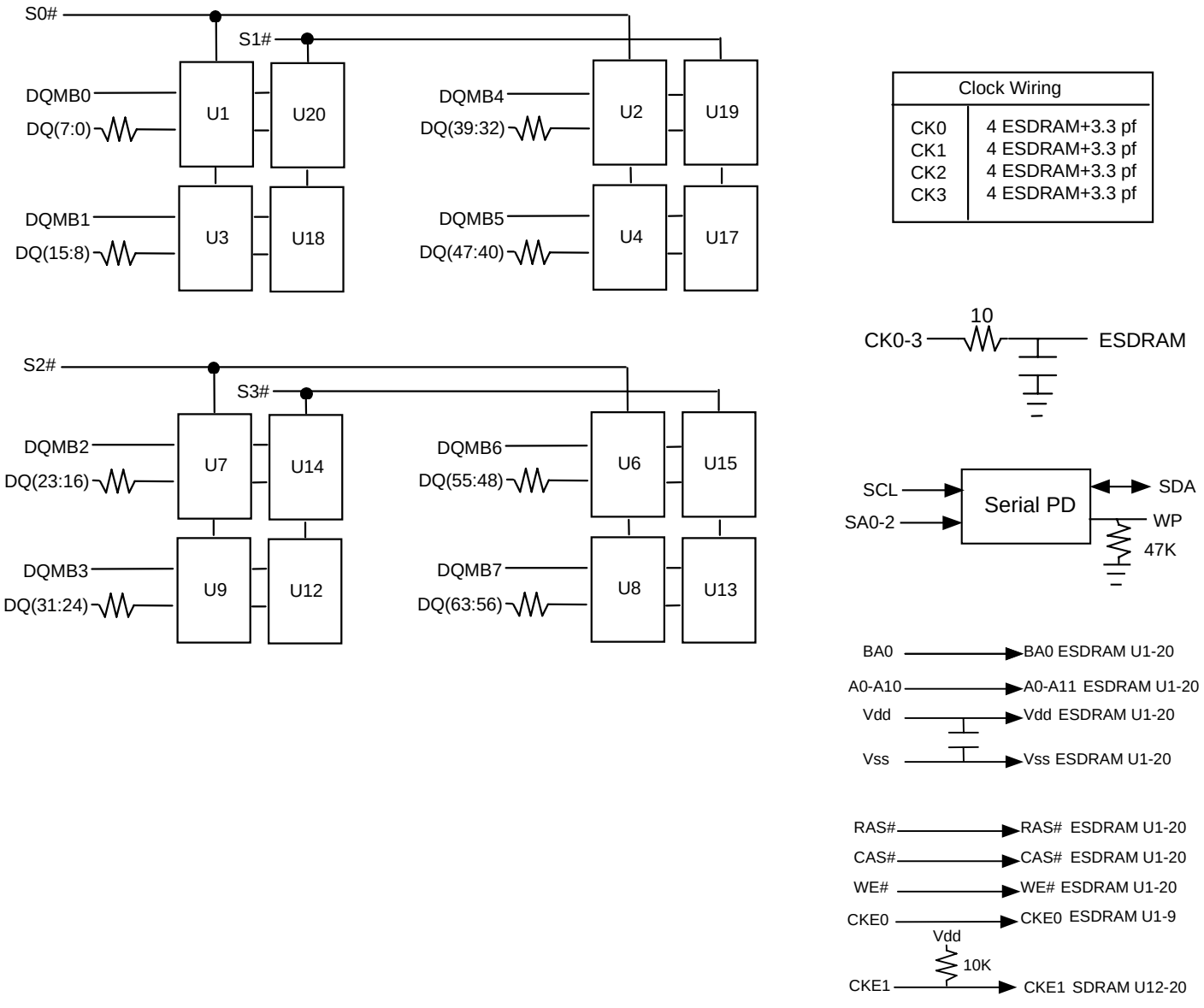
Note: All DQ resistor values are 10 ohms
All CK resistor values are 10 ohms
U1-U4 are SM2404T ESDRAM

2Mx64 (16MB) DIMM Functional Block Diagram – SM2M64DT



Note: All DQ resistor values are 10 ohms
All CK resistor values are 10 ohms
U1-U9 are SM2403T ESDRAM

4Mx64 (32MB) DIMM Functional Block Diagram – SM4M64DT



Note: All DQ resistor values are 10 ohms
All CK resistor values are 10 ohms
U1-U20 are SM2403T ESDRAM

Electrical Characteristics

Absolute Maximum Ratings

Description	Symbol	Value
Power Supply Voltage	V_{DD}	-1V to +4.6V
Voltage on any Pin with Respect to Ground	V_{IN}, V_{OUT}	-0.5V to +4.6V
Operating Temperature (ambient)	T_A	0°C to +70°C
Storage Temperature	T_{stg}	-55°C to +125°C
Power Dissipation	P_D	TBD
DC Output Current (I/O pins)	I_{OUT}	50mA

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these, or any other conditions above those listed in the operational section of the specification, is not implied. Exposure to conditions at absolute maximum ratings for extended periods may affect device reliability.

DC Operating Conditions (T_A = 0°C to 70°C)

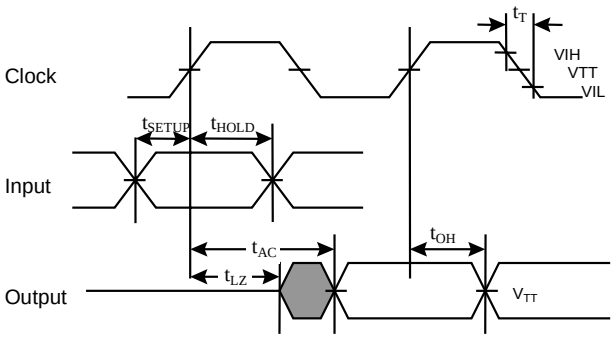
Symbol	Parameter		Min	Max	Units	Notes
V_{DD}	Supply Voltage		3.0	3.6	V	
V_{IH}	Input High Voltage		2.0	V_{DD} + 0.3	V	
V_{IL}	Input Low Voltage		-0.3	0.8	V	
I_{in1}	Input Leakage Current	CK0-CK3, S0-S3, DQMB0-DQMB7	-	±10	µA	
I_{in2}		CKE0-1	-	±15	µA	
I_{in3}		RAS, CAS, A0-A10, BA0, WE	-	±20	µA	
I_O	Output Leakage Current	DQ0-DQ63, SCL, SA0-SA2, SDA		±5	µA	
V_{OH}	Output High Voltage (I_{OUT} = -4mA)		2.4	V_{DD}	V	
V_{OL}	Output Low Voltage (I_{OUT} = +4mA)		0.0	0.4	V	

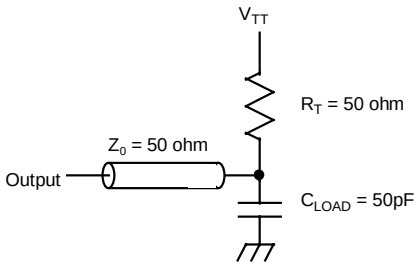
Capacitance (T_A = 25°C, f = 1MHz, VDD = 3.3V ±0.3V, not 100% tested)

Symbol	Parameter	8MB	16MB	32MB	Units
C_{In1}	Input Capacitance (BA0, A0-10, RAS, CAS, WE)	24	35	55	pF
C_{In2}	Input Capacitance (S0 - S3)	13	18	18	pF
C_{In3}	Input Capacitance (CK0 - CK3)	21	21	21	pF
C_{In4}	Input Capacitance (CKE0, CKE1)	24	35	35	pF
C_{In5}	Input Capacitance (DQMB0-DQMB7)	10	10	13	pF
C_{In6}	Input Capacitance (SCL, SA0-2)	10	10	10	pF
$C_{I/O1}$	I/O Capacitance (SDA)	13	13	13	pF
$C_{I/O2}$	I/O Capacitance (DQ0-63)	10	10	15	pF

AC Characteristics (T_A = 0°C to 70°C)

1. An initial pause of 200µs is required after power-up, then a Precharge All Banks command must be given followed by a minimum of eight Auto (CBR) Refresh cycles before the Mode Register Set operation can begin.
2. AC timing tests have V_{IL} = 0.8V and V_{IH} = 2.0V with the timing referenced to the V_{TT} = 1.4V crossover point.





AC Output Load Circuit

3. The transition time is measured between V_{IH} and V_{IL} (or between V_{IH} and V_{IL}).
4. AC measurements assume t_T = 1ns.
5. In addition to meeting the transition rate specification, the clock and CKE must transition V_{IH} and V_{IL} (or between V_{IH} and V_{IL}) in a monotonic manner.

Clock and Clock Enable Parameters

Symbol	Parameter	7.5		10		Units	Notes
		Min	Max	Min	Max		
t_{CK2}	Clock Cycle Time, CL = 2, 3	7.5	-	10	-	ns	
t_{CK1}	Clock Cycle Time, CL = 1	15	-	20	-	ns	
t_{AC2}	Clock Access Time, CL = 2, 3	-	4.5	-	5	ns	1, 2
t_{AC1}	Clock Access Time, CL = 1	-	12	-	15	ns	1, 2
t_{CKH2}	Clock High Pulse Width, CL = 2, 3	2.8	-	3.5	-	ns	3
t_{CKH1}	Clock High Pulse Width, CL = 1	5	-	6	-	ns	3
t_{CKL2}	Clock Low Pulse Width, CL = 2, 3	2.8	-	3.5	-	ns	3
t_{CKL1}	Clock Low Pulse Width, CL = 1	5	-	6	-	ns	3
t_{CKES}	Clock Enable Setup Time	2	-	2.5	-	ns	
t_{CKEH}	Clock Enable Hold Time	1	-	1	-	ns	
t_{CKESP}	CKE Setup Time (Power Down Mode)	2	-	2.5	-	ns	
t_T	Transition Time (Rise and Fall)	-	4	-	4	ns	

Notes:
1. Access time is measured at 1.4V (LVTTL). See AC Test Load.
2. Access time is based on a clock rise time of 1ns. If clock rise time is longer than 1ns, then (t_{rise}/2-0.5) ns must be added to the access time.
3. Assumes clock rise and fall times are equal to 1ns. If rise or fall time exceeds 1ns, other AC timing parameters must be compensated by an additional [(t_{rise}+t_{fall})/2-1] ns.

Common Parameters

Symbol	Parameter	7.5		10		Units	Notes
		Min	Max	Min	Max		
t_{CS}	Command Setup Time	2	-	2.5	-	ns	
t_{CH}	Command Hold Time	1	-	1	-	ns	
t_{AS}	Address and Bank Select Setup Time	2	-	2.5	-	ns	
t_{AH}	Address and Bank Select Hold Time	1	-	1	-	ns	
t_{RCD}	RAS to CAS Delay	15	-	20	-	ns	
t_{RC}	Bank Cycle Time	37.5	120,000	50	120,000	ns	
t_{RAS}	Active Command Period	22.5	120,000	30	120,000	ns	
t_{RP}	Precharge Time	15	-	20	-	ns	
t_{RRD}	Bank to Bank Delay Time	15	-	20	-	ns	
t_{CCD}	CAS to CAS Delay Time (Same Bank)	7.5	-	10	-	ns	

Refresh Cycle

Symbol	Parameter	7.5		10		Units	Notes
		Min	Max	Min	Max		
t_{REF}	Refresh Period	-	64	-	64	ms	1, 2
t_{SREX}	Self Refresh Exit Time	2CLK+t_{RC}	-	2CLK+t_{RC}	-	ns	3

Notes:
1. 4096 cycles.
2. Any time that the refresh period has been exceeded, a minimum of two Auto-Refresh (CBR) commands must be given to "wake up" the device.
3. Self-Refresh exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self-Refresh Exit is not completed until t_{RC} is satisfied once the Self-Refresh Exit command is registered.

Read Cycle

Symbol	Parameter	7.5		10		Units	Notes
		Min	Max	Min	Max		
t_{OH2}	Data Out Hold Time CL = 2,3	3	-	3	-	ns	
t_{OH1}	Data Out Hold Time CL = 1	2	-	2	-	ns	
t_{LZ}	Data Out to Low Impedance	0	-	0	-	ns	
t_{HZ2}	Data Out to High Impedance CL = 2, 3	-	7.5	-	8	ns	1
t_{HZ1}	Data Out to High Impedance CL = 1	-	4.5	-	5	ns	1
t_{DQZ}	DQM Data Out Disable Latency	2	-	2	-	CLK	

Notes:
1. Referenced to the time at which the output achieves an open circuit condition, not to output voltage levels.

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Write Cycle

Symbol	Parameter	7.5		10		Units	Notes
		Min	Max	Min	Max		
t_{OS}	Data In Setup Time	2	-	2.5	-	ns	
t_{OH}	Data In Hold Time	1	-	1	-	ns	
t_{DPL}	Data Input to Precharge	7.5	-	10	-	ns	
t_{DAL}	Data In to Active/Refresh	24	-	30	-	ns	1
t_{DQW}	DQM Write Mask Latency	0	-	0	-	CLK	

Notes:
1. t_{DAL} must satisfy $t_{DPL} + t_{RP}$.

Clock Frequency and Latency

Symbol	Parameter	Speed Sort				Units	Notes
		7.5		10			
f_{CK}	**Clock Frequency**	**133**	**66**	**100**	**50**	**MHz**	
t_{CK}	Clock Cycle Time	7.5	15	10	20	ns	
t_{AA}	CAS Latency	2	1	2	1	t_{CK}	
t_{RCD}	RAS to CAS Delay	2	1	2	1	t_{CK}	
t_{RL}	RAS Latency	4	2	4	2	t_{CK}	
t_{RC}	Bank Cycle Time	5	3	5	3	t_{CK}	
t_{RAS}	Minimum Bank Active Time	3	2	3	2	t_{CK}	
t_{RP}	Precharge Time	2	1	2	1	t_{CK}	
t_{DPL}	Data In to Precharge	1	1	1	1	t_{CK}	
t_{DAL}	Data In to Active/Refresh	3	2	3	2	t_{CK}	
t_{RRD}	Bank to Bank Delay Time	2	1	2	1	t_{CK}	
t_{CCD}	CAS to CAS Delay Time	1	1	1	1	t_{CK}	
t_{WL}	Write Latency	0	0	0	0	t_{CK}	
t_{DQW}	DQM Write Mask Latency	0	0	0	0	t_{CK}	
t_{DQZ}	DQM Data Disable Latency	2	2	2	2	t_{CK}	
t_{CSL}	Clock Suspend Latency	1	1	1	1	t_{CK}	

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Serial Presence Detect (SPD) for PC-133 DIMMs

Byte	Description		8MB	16MB	32MB	8MB	16MB	32MB
			SPD Entry			** Hex Code **		
0	Number of bytes written into EEPROM		128	128	128	80	80	80
1	Total number of SPD bytes		256	256	256	08	08	08
2	Memory Type		SDRAM	SDRAM	SDRAM	04	04	04
3	Number of Row Addresses		11	11	11	0B	0B	0B
4	Number of Column Addresses		8	9	9	08	09	09
5	Number of Module Banks		1	1	2	01	01	02
6	Module Data Width		x64	x64	x64	40	40	40
7	Module Data Width (cont'd)		0	0	0	00	00	00
8	Voltage Interface Levels		LVTTL	LVTTL	LVTTL	01	01	01
9	Cycle Time at max CAS Latency	-7.5 -10	7.5 ns 10.0 ns	7.5 ns 10.0 ns	7.5 ns 10.0 ns	75 A0	75 A0	75 A0
10	ESDRAM Clock Access Time	-7.5 -10	4.5 ns 5.0 ns	4.5 ns 5.0 ns	4.5 ns 5.0 ns	45 50	45 50	45 50
11	DIMM config (non-parity, parity, ECC)		--- Non-parity ---			00	00	00
12	Refresh Rate and Type		--- 31.25us / Self ---			83	83	83
13	Primary ESDRAM Width		x16	x8	x8	10	08	08
14	Error Checking Data Width		N/A	N/A	N/A	00	00	00
15	Min. CAS-to-CAS Delay (tCCD)		1 clk	1 clk	1 clk	01	01	01
16	Burst Lengths Supported		--- 1,2,4,8,Full Pg ---			8F	8F	8F
17	Number of Banks on ESDRAM Device		2	2	2	02	02	02
18	CAS Latencies Supported		1,2,3	1,2,3	1,2,3	07	07	07
19	CS Latency		0	0	0	01	01	01
20	Write Latency		0	0	0	01	01	01
21	ESDRAM Module Attributes		--- Unbuffered ---			00	00	00
22	ESDRAM Device Attributes		Early RAS Precharge, +/-10% Vdd, Precharge All			07	07	07
23	Min. Clock Cycle Time at CL=2	-7.5 -10	7.5 ns 10.0 ns	7.5 ns 10.0 ns	7.5 ns 10.0 ns	75 A0	75 A0	75 A0
24	Clock Access Time at CL=2 (tAC2)	-7.5 -10	4.5 ns 5.0 ns	4.5 ns 5.0 ns	4.5 ns 5.0 ns	45 50	45 50	45 50
25	Min. Clock Cycle Time at CL=1	-7.5 -10	15.0 ns 20.0 ns	15.0 ns 20.0 ns	15.0 ns 20.0 ns	3C 50	3C 50	3C 50
26	Clock Access Time at CL=1 (tAC1)	-7.5 -10	12.0 ns 15.0 ns	12.0 ns 15.0 ns	12.0 ns 15.0 ns	30 3C	30 3C	30 3C

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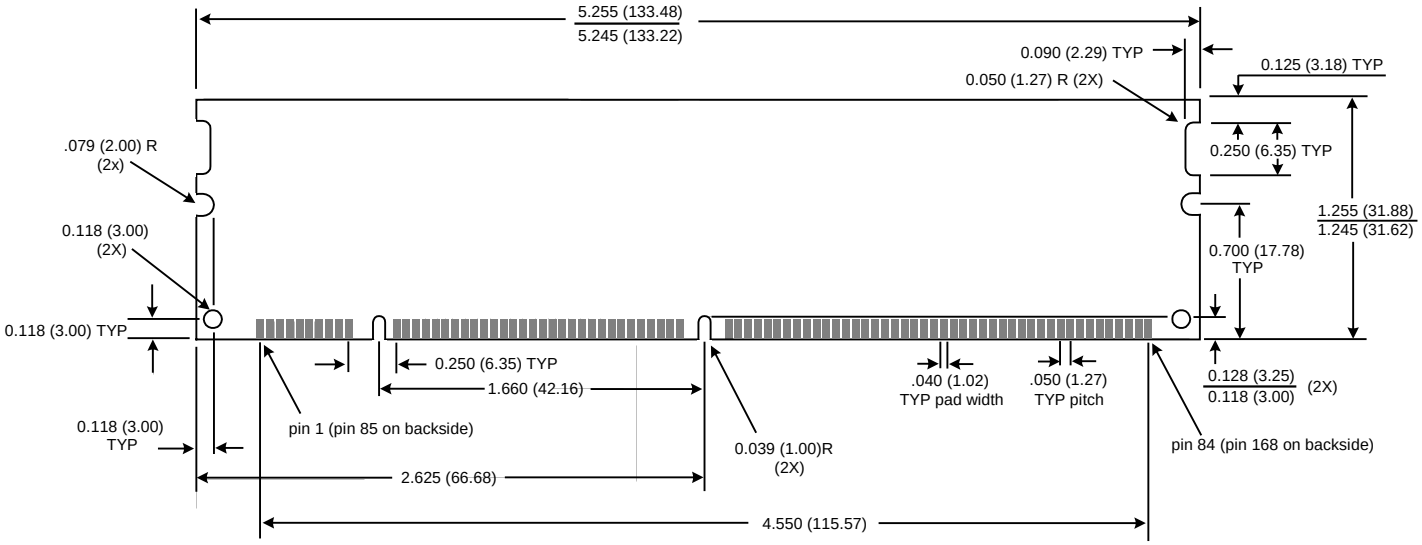
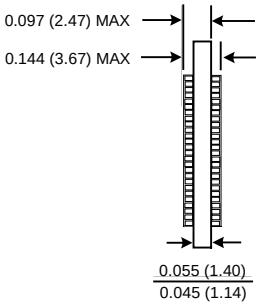
Byte	Description		8MB	16MB	32MB	8MB	16MB	32MB
			SPD Entry			** Hex Code **		
27	Min. Row Precharge Time (tRP)	-7.5	15 ns	15 ns	15 ns	0F	0F	0F
		-10	20 ns	20 ns	20 ns	14	14	14
28	Min. Row-to-Row Delay (tRRD)	-7.5	15 ns	15 ns	15 ns	0F	0F	0F
		-10	20 ns	20 ns	20 ns	14	14	14
29	Min. RAS-to-CAS Delay (tRCD)	-7.5	15 ns	15 ns	15 ns	0F	0F	0F
		-10	20 ns	20 ns	20 ns	14	14	14
30	Min. RAS Pulse Width (tRAS)	-7.5	23 ns	23 ns	23 ns	17	17	17
		-10	30 ns	30 ns	30 ns	1E	1E	1E
31	Density of each bank on module		8MB	16MB	16MB	02	04	04
32	Cmd/Addr input set-up time		2 ns			20	20	20
33	Cmd/Addr input hold time		1 ns			10	10	10
34	Data input set-up time		2 ns			20	20	20
35	Data input hold time		1 ns			10	10	10
36-59	Superset Information		-	-	-	00	00	00
60	ESDRAM Attributes		See Appendix H			03	03	03
61	ESDRAM Superset Information		See Appendix B			01	01	01
62	SPD Rev.		1.2			12	12	12
63	Checksum for bytes 0-62	-7.5				B2	AD	AE
		-10				54	4F	50
64-71	JEDEC ID code		Enhanced Memory Systems			7F32FFFFFFFFFF		
72	Manufacturing Location					00	00	00
73-90	Manufacturer's Part #		SM1M64DT	SM2M64DT	SM4M64DT			
91,92	PCB Rev. Code		-			rrrr	rrrr	rrrr
93,94	Manufacturing Date		yyww code			yyww	yyww	yyww
95-98	Assembly Serial #		serial number			ssss	ssss	ssss
99-125	Manufacturer's Specific Data		open			00	00	00
126	Intel specification frequency		133MHz			85	85	85
127	Intel specification CL and clock support					AF	AF	FF

Mechanical Drawing

168 - pin DIMM

FRONT VIEW





Dimensions: inches (mm)

Ordering Information

Part Number	Capacity	I/O Width	I/O Type	Package	Power Supply	Maximum Operating Frequency (MHz)
SM1M64DT-7.5	8 MB	x64	LVTTL	168-pin DIMM	3.3V	133
SM1M64DT-10	8 MB	x64	LVTTL	168-pin DIMM	3.3V	100
SM2M64DT-7.5	16 MB	x64	LVTTL	168-pin DIMM	3.3V	133
SM2M64DT-10	16 MB	x64	LVTTL	168-pin DIMM	3.3V	100
SM4M64DT-7.5	32 MB	x64	LVTTL	168-pin DIMM	3.3V	133
SM4M64DT-10	32 MB	x64	LVTTL	168-pin DIMM	3.3V	100

Note: Enhanced Memory Systems ESDRAM DIMMs are labeled per the Intel PC SDRAM DIMM Naming Convention. This convention requires identification of the bus speed, latency, clock access time, and SPD revision code. The codes for these DIMM modules is PC133-222-45120 for the –7.5, and PC100-222-50120 for the –10..