CMP-05

HIGH-SPEED PRECISION COMPARATOR (WITH LATCH CIRCUIT)

Precision Monolithics Inc.

FEATURES

- **Precision Input Stage**
  - **Input Offset Voltage 150µV**
  - **Input Offset Current 15nA**
- **Fast Response Time (5mV Overdrive) 38ns**
- **High Voltage Gain 16,000V/V**
- **Latch Function with TTL Compatible Input**
- **TTL Compatible Output**
- **Available in Hermetic Mini-DIP Package**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} (µV)	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	SO 8-PIN	OPERATING TEMPERATURE RANGE
600	CMP05BJ/883	CMP05BZ/883	–	–	MIL
600	CMP05FJ	CMP05FZ	–	–	IND
1000	CMP05CJ/883	CMP05CZ*	–	–	MIL
1000	–	CMP05GZ	CMP05GP	CMP05GS	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

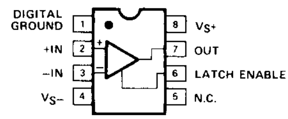
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see 1990/91 Data Book, Section 2.

GENERAL DESCRIPTION

The CMP-05's very high speed and precision input specifications make it the ideal comparator in systems needing 12-bit accuracy along with high speed. An exceptionally fast response time of 60nsec is possible with only 1/2 LSB overdrive (12-bit, 10-volt system).

The CMP-05 design makes it the ideal component in systems requiring high speed with excellent low-level analog signal resolution. High-speed 12-bit successive approximation A/D converters, zero crossing detectors and logic threshold detectors are typical system applications.

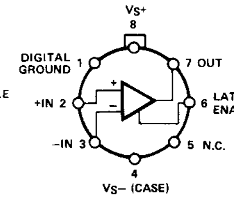
PIN CONNECTIONS



8-PIN HERMETIC MINI-DIP (Z-Suffix)

EPOXY MINI-DIP (P-Suffix)

8-PIN SO (S-Suffix)

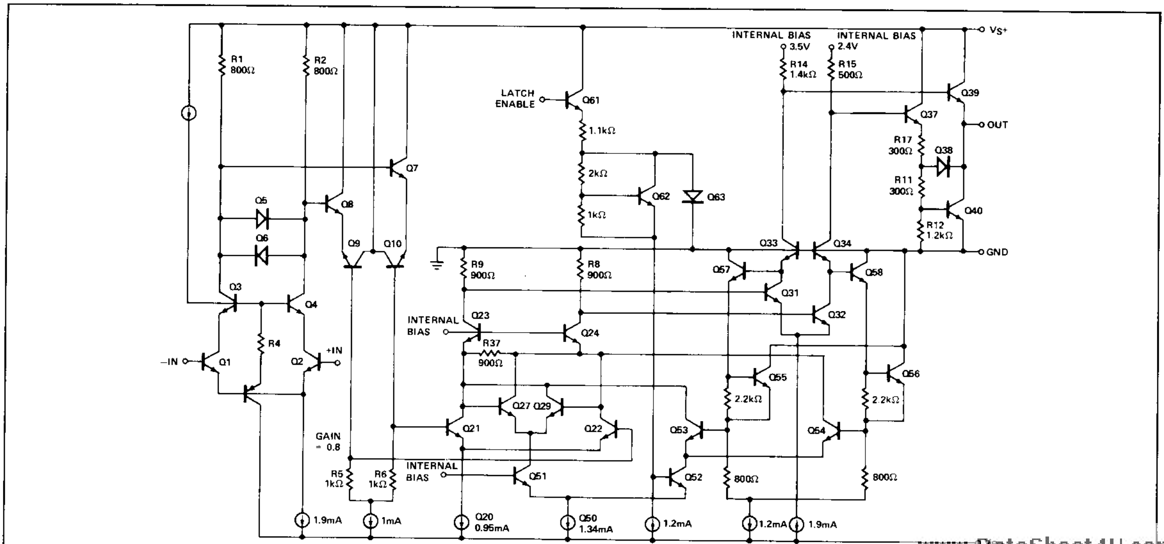


TO-99 (J-Suffix)

LOGIC TABLE

LATCH ENABLE	OUT
0 or NC	Comparing
1	Latched

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Positive Supply Voltage .... +6V
Negative Supply Voltage .... −18V
Differential Input Voltage .... ±5V
Latch Enable Input Voltage .... −0.5V to V+ Supply
Operating Temperature Range
  CMP-05B/C (J, Z) (Note 2) .... −55°C to +125°C
  CMP-05F/G (J, P, S, Z) .... −40°C to +85°C
Junction Temperature (T_j) .... −65°C to +150°C
Storage Temperature Range .... −65°C to +150°V
  P-Suffix .... −65°C to +125°C
Lead Temperature (Soldering, 60 sec) .... 300°C
Output Short-Circuit Duration
  To Ground .... Indefinite
  To V+ = 5.0V .... 1 Minute

PACKAGE TYPE	Θ_{jA} (Note 3)	Θ_{jc}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Latch is functional for $-55°C \le T_A \le +85°C$.
3. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for TO, CerDIP and P-DIP packages; Θ_{jA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_S+ = 5.0V$, $V_S- = -5.0V$, $T_A = 25°C$ and Latch Enable grounded, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-05B/F MIN	CMP-05B/F TYP	CMP-05B/F MAX	CMP-05C/G MIN	CMP-05C/G TYP	CMP-05C/G MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	150	600	—	400	1000	µV
Input Offset Current	I_{OS}		—	15	80	—	30	150	nA
Input Bias Current	I_B		—	0.6	1.2	—	0.8	1.8	µA
Voltage Gain	A_{VO}	(Note 1)	8	16	—	7	14	—	V/mV
Input Voltage Range	CMVR	(Note 1)	±3.0	±3.3	—	±3.0	±3.3	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm3.0V$, (Note 1)	86	91	—	84	89	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm4.75V$ to $V_S = \pm5.25V$	—	51	126	—	64	126	µV/V
		P Package	—	—	—	—	120	360	
		$V_S+ = 5V$, $V_S- = -5V$ to $-15V$	—	15	51	—	18	63	
		P Package	—	—	—	—	36	180	
Output High Voltage	V_{OH}	$V_{IN} \ge 10mV$, $I_O = 0\mu A$	2.4	2.9	—	2.4	2.9	—	V
		$V_{IN} \ge 10mV$, $I_O = 320\mu A$	2.4	2.9	—	—	—	—	
		$V_{IN} \ge 10mV$, $I_O = 200\mu A$	—	—	—	2.4	2.9	—	
Saturation Voltage	V_{SAT}	$V_{IN} \le -10mV$, $I_{SINK} = 0mA$	—	0.13	0.40	—	0.13	0.40	V
		$V_{IN} \le -10mV$, $I_{SINK} = 8mA$	—	—	—	—	0.28	0.40	
		$V_{IN} \le -10mV$, $I_{SINK} = 12.8mA$	—	0.32	0.40	—	—	—	
Positive Supply Current	I_S+	$V_O \le 2.4V$, (Note 1)	—	7.5	11	—	8.0	12	mA
		$V_O \le 0.4V$	—	10	15	—	11	16	
Negative Supply Current	I_S-	$V_O \le 0.4V$	—	11	16	—	12	18	mA
Power Dissipation	P_d	$V_O \le 0.4V$	—	105	155	—	115	170	mW
Latch Input Voltage Logic 1	V_{LH}	Over Operating Temp. Range Latch Enabled, (Note 1)	2.0	—	—	2.0	—	—	V
Logic 0	V_{LL}	Over Operating Temp. Range Latch Disabled, (Note 1)	—	—	0.8	—	—	0.8	
Latch Input Current Logic 1	I_{LH}	$V_{LH} = 3.0V$, (Note 1)	—	10	45	—	10	45	µA
Logic 0	I_{LL}	$V_{LL} = 0.8V$, (Note 1)	—	6	25	—	6	25	
Input to Output High Response Time	t_{pd+}	$V_{OD} = 1.2mV$, (Note 2)	—	60	—	—	60	—	ns
		$V_{OD} = 5.0mV$, (Note 2)	—	41	55	—	41	55	
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 1.2mV$, (Note 2)	—	60	—	—	60	—	ns
		$V_{OD} = 5.0mV$, (Note 2)	—	37	55	—	37	55	
Latch Disable Time	t_{LPD}	(Note 3)	—	50	65	—	50	65	ns

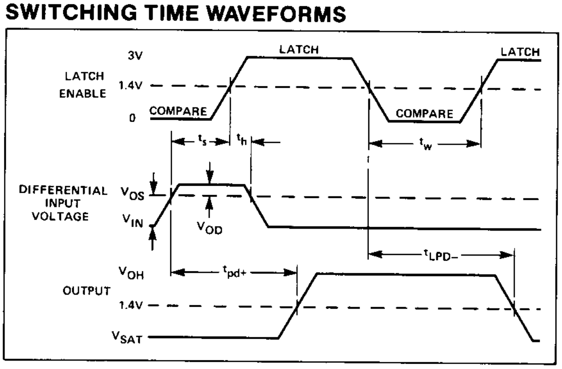
NOTES:
1. Guaranteed by design.
2. Times are for 100mV step inputs. See switching time waveforms.
3. See switching time waveforms.

ELECTRICAL CHARACTERISTICS at $V_S+ = 5.0V$, $V_S- = -5.0V$, and Latch Enable grounded, $-55°C \le T_A \le +125°C$ for CMP-05B/C, $-25°C \le T_A \le +85°C$ for CMP-05F, $-40°C \le T_A \le +85°C$ for CMP-05G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-05B/F MIN	CMP-05B/F TYP	CMP-05B/F MAX	CMP-05C/G MIN	CMP-05C/G TYP	CMP-05C/G MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.3	1.5	—	0.55	2.0	mV
Input Offset Voltage Drift	TCV_{OS}		—	1.5	7.5	—	2.5	15	μV/°C
Input Offset Current	I_{OS}		—	40	250	—	70	400	nA
Input Bias Current	I_B		—	1.1	2.5	—	1.5	3.8	μA
Voltage Gain	A_{VO}	(Note 1)	6	11	—	5	10	—	V/mV
Input Voltage Range	CMVR	(Note 1)	±2.9	±3.2	—	±2.9	±3.2	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 2.9V$, (Note 1)	83	90	—	80	88	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 4.75V \le V_S \le \pm 5.25V$	—	63	178	—	80	252	μV/V
		P Package	—	—	—	—	150	400	
Output High Voltage	V_{OH}	$V_{IN} \ge 10mV$, $I_O = 0\mu A$	2.4	—	—	2.4	—	—	V
		$V_{IN} \ge 10mV$, $I_O = 240\mu A$	2.4	—	—	—	—	—	
		$V_{IN} \ge 10mV$, $I_O = 160\mu A$	—	—	—	2.4	—	—	
Saturation Voltage	V_{SAT}	$V_{IN} \le -10mV$, $I_{SINK} = 0mA$	—	0.18	0.40	—	0.20	0.40	V
		$V_{IN} \le -10mV$, $I_{SINK} = 9.6mA$	—	0.2	0.40	—	—	—	
		$V_{IN} \le -10mV$, $I_{SINK} = 6.4mA$	—	—	—	—	0.30	0.40	
Positive Supply Current	I_S+	$V_O \le 0.4V$	—	11	16	—	12	17	mA
Negative Supply Current	I_S-	$V_O \le 0.4V$	—	12	17	—	13	19	mA
Power Dissipation	P_d	$V_O \le 0.4V$	—	115	165	—	125	180	mW
Latch Input Current Logic 1	I_{LH}	$V_{LH} = 3V$, (Notes 1, 4)	—	18	90	—	18	90	μA
Logic 0	I_{LL}	$V_{LL} = 0.8V$, (Notes 1, 4)	—	10	50	—	10	50	
Input to Output High Response Time	t_{pd+}	$V_{OD} = 1.2mV$, (Note 2)	—	125	—	—	125	—	ns
		$V_{OD} = 5.0mV$, (Note 2)	—	92	—	—	92	—	
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 1.2mV$, (Note 2)	—	115	—	—	115	—	ns
		$V_{OD} = 5.0mV$, (Note 2)	—	88	—	—	88	—	
Latch Disable Time	t_{LPD+}	(Notes 2, 4)	—	56	—	—	56	—	ns
	t_{LPD-}		—	30	—	—	30	—	

NOTES:
1. Guaranteed by design.
2. Times are for 100mV step inputs. See switching time waveforms.
3. A high on the latch enable input will cause the latch to assume the state of the comparator and not follow subsequent inputs.
4. Latch is functional for $-55°C \le T_A \le +85°C$.

SWITCHING TIME WAVEFORMS

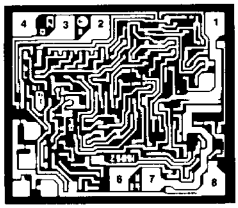


Minimum Input Timing Requirements*

Parameter		Minimum Limit	Units
t_S	Setup Time	35	ns
t_h	Hold Time	10	ns
t_W	Latch Pulse Width	25	ns

*t_S, t_h, t_W are tested with $V_{IN} = 100mV$ and $V_{OD} = 5mV$.

DICE CHARACTERISTICS



DIE SIZE 0.052 × 0.046 inch, 2392 sq. mils
(1.321 × 1.168mm, 1.543 sq. mm)

1. DIGITAL GROUND
2. NONINVERTING INPUT
3. INVERTING INPUT
4. NEGATIVE SUPPLY (SUBSTRATE)
6. LATCH ENABLE
7. OUTPUT
8. POSITIVE SUPPLY

For additional DICE ordering information, refer to 1990/91 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 5V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-05G LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	1000	μV MAX
Input Offset Current	I_{OS}		150	nA MAX
Input Bias Current	I_B		1.8	μA MAX
Voltage Gain	A_{VO}	(Note 1)	7	V/mV MIN
Input Voltage Range	CMVR	(Note 1)	±3.0	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 2.9V$ (Note 1)	80	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 4.75 \leq V_S \leq \pm 5.25$ $V_S+ = 5V$, $V_S- = -5V$ to $-15V$	178 63	μV/V MAX
Positive Output Voltage	V_{OH}	$V_{IN} \geq 10mV$, $I_O = 0\mu A$	2.4	V MIN
Saturation Voltage	V_{SAT}	$V_{IN} \leq 10mV$, $I_O = 0\mu A$	0.4	V MAX
Positive Supply Current	I+	$V_O \leq 0.4V$	16	mA MAX
Negative Supply Current	I–	$V_O \leq 0.4V$	18	mA MAX
Negative Supply Current	I–	$V- = -15V$, $V_O \leq 0.4V$	20	mA MAX
Latch Input Voltage				
Logic 1	V_{LH}	Latch Enabled	2.0	V MIN
Logic 0	V_{LL}	Latch Disabled	0.8	V MAX
Latch Input Current				
Logic 1	I_{LH}	$V_{LH} = 3.0V$, (Notes 1, 4)	45	μA MAX
Logic 0	I_{LL}	$V_{LL} = 0.8V$, (Notes 1, 4)	25	μA MAX
Input to Output High Response Time	t_{pd+}	$V_{OD} = 5.0mV$, (Notes 1, 2)	60	ns MAX
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 5.0mV$, (Notes 1, 2)	60	ns MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

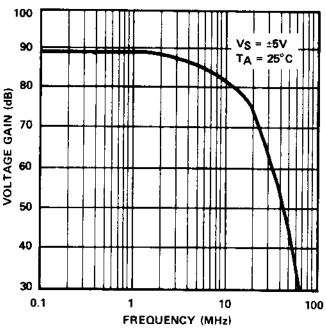
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 5V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-05G TYPICAL	UNITS
Input to Output High Response Time	t_{pd+}	$V_{OD} = 1.2mV$, (Note 2)	41	ns
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 1.2mV$, (Note 2)	37	ns
Latch Disable Time	t_{LPD}	(Notes 3, 4)	50	ns

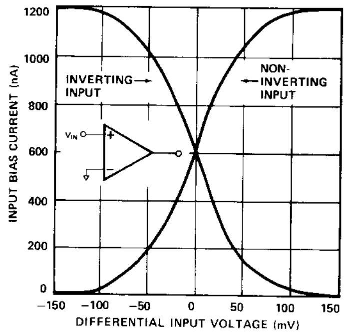
NOTES:
1. Guaranteed by design.
2. Times are for 100mV step inputs.
3. See switching time waveforms.
4. Latch is functional for $-55°C \leq T_A \leq 85°C$.

TYPICAL PERFORMANCE CHARACTERISTICS

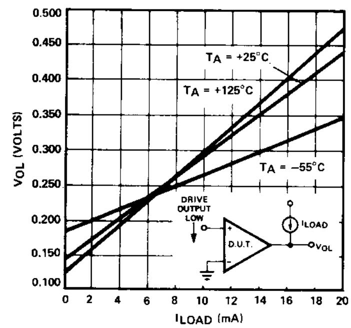
VOLTAGE GAIN vs FREQUENCY



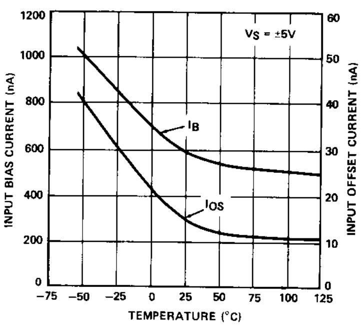
INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



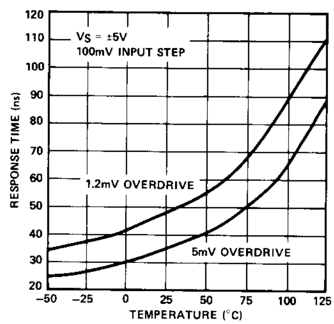
VSAT vs LOAD CURRENT



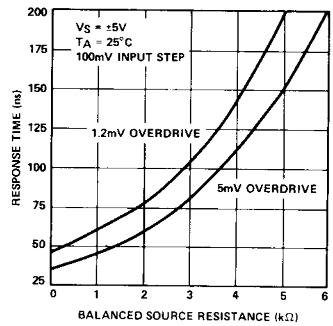
INPUT CURRENTS vs TEMPERATURE



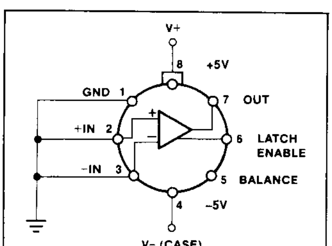
RESPONSE TIME vs TEMPERATURE



RESPONSE TIME vs BALANCED SOURCE RESISTANCE

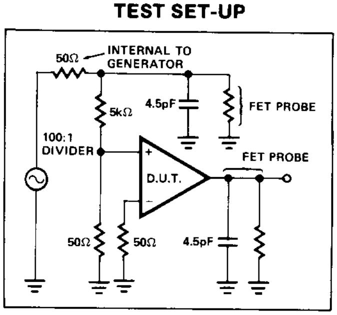


STANDARD BURN-IN CIRCUIT

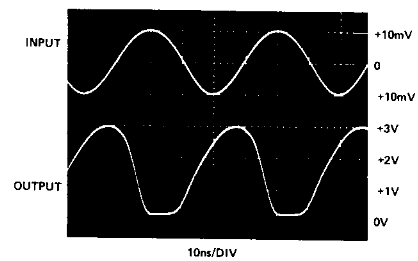


MIL-STD-883, METHOD 1015, CONDITION B

RESPONSE PHOTOGRAPH TEST SET-UP

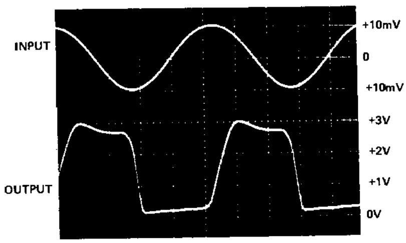


RESPONSE TO 25MHz SINE WAVE

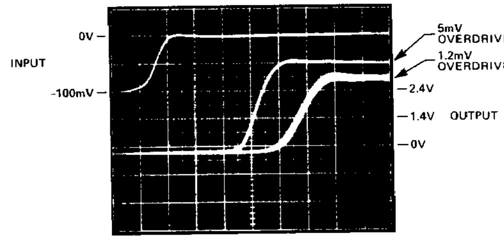


TYPICAL PERFORMANCE CHARACTERISTICS

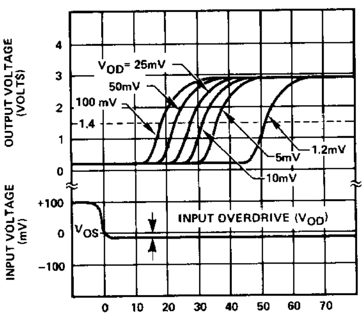
RESPONSE TO 10MHz SINE WAVE



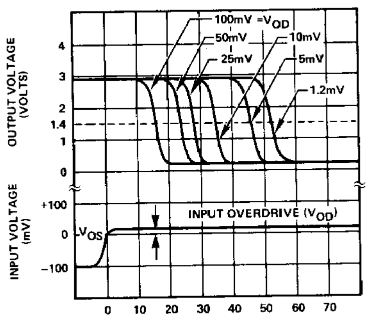
RESPONSE TIME TO 5mV AND 1.2mV (= 1/2 LSB) OVERDRIVES



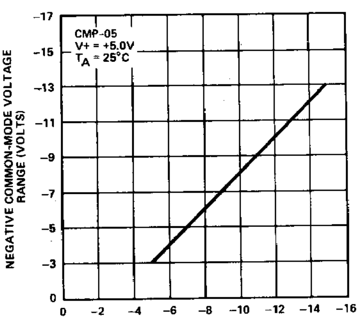
t_{pd+} RESPONSE TIME



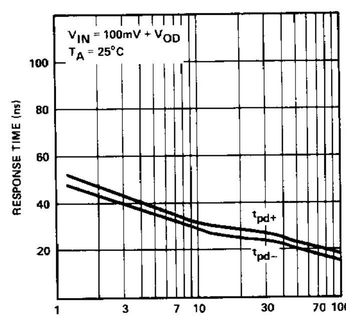
t_{pd-} RESPONSE TIME



CMP-05 NEGATIVE COMMON-MODE INPUT RANGE vs NEGATIVE SUPPLY



RESPONSE TIME vs OVERDRIVE VOLTAGE



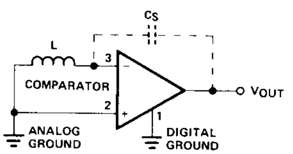
APPLICATION INFORMATION

The CMP-05 is a very accurate device providing fast response time even with small—Microvolt level—overdrives. To achieve this performance requires high gain at high frequencies. As shown in the voltage gain versus frequency curve, the gain—bandwidth product of the CMP-05 is 1.5×10^{11} Hz. It maintains its full gain to approximately 8MHz and rolls off at a very fast rate beyond that frequency due to the fact that five poles occur in the 30 to 60MHz range. At 30MHz the gain of the comparator is still 2000. Therefore, in the transition region small values of source lead inductance and stray feedback capacitance can cause an oscillatory condition.

For example (in the figure below) with $L = 0.1\mu H$, $C_S = 0.15pF$, the closed-loop gain of the circuit at 30MHz is:

$$A_V = \frac{1}{LC_S\omega^2} = \frac{1}{10^{-7} \times 0.15 \times 10^{-12} \times (2\pi \times 30 \times 10^6)^2} = 1880$$

POTENTIAL FEEDBACK SOURCES



With the open-loop gain at 2000 oscillation will occur since the phase shift exceeds 180° C. To minimize these problems power supplies should be decoupled, lead lengths should be kept as short as possible, and a ground plane should be used to reduce the stray feedback capacitance. In addition, a ground plane substantially diminishes the possibility of the output current spike coupling back to the inputs through the ground lead. Keeping a separate digital ground (pin 1) and analog ground (to which the inputs are referenced) also reduces the magnitude of the problem.

Fortunately, in high-speed circuitry the comparator inputs will be driven at a fast rate, in which case no transition region oscillations will occur. As the minimum slew rate versus source resistance curve indicates, if the input is driven at a rate exceeding 6mV/µsec, no oscillations will occur with source resistors of less than 1kΩ. Examples of "clean" transitions can be observed in the photographs of the response time with 5mV and 1.2mV overdrives, and the response to the 10 and 25MHz input signals.

In order to not degrade its speed the CMP-05's inputs are not internally clamped. If large differential voltages are present it is recommended that the inputs be clamped with high speed, low capacitance diodes such as the H.P. 5082-2835, which is a Schottky Diode.

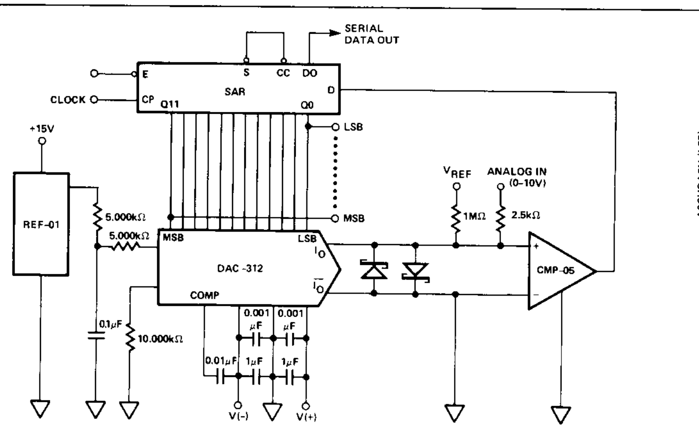
As in all high-speed devices, it is to the user's advantage to keep the source impedances low and matched.

LATCH

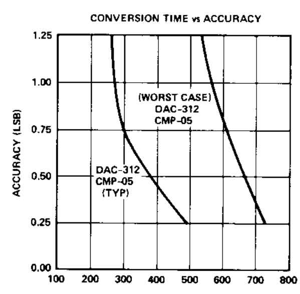
The CMP-05 has a latch feature which functions over −55° C to +85° C. When the latch is enabled, the output stays in its existing logic state regardless of the input signal. The input timing requirements of the latch are presented in the Switching Time Waveforms. The latch opens up a broader applications area at no sacrifice in total system speed. Effectively, the latch allows high speed sampling of comparison decisions. This is important in automatic test equipment limit comparators, in measuring pods used in logic analyzers and other similar synchronous measurement circuitry needing fast clocking frequencies. The latch pulse width t_w allows sampling of input signals to take place in 25nsec.

The latch prevents self oscillation (due to positive feedback) from taking place when slowly-moving high-source-impedance signals pass thru the linear amplification region of the comparator. This is successfully accomplished by rapidly strobing the comparator near its minimum t_w time which prevents self oscillation from making a complete cycle since t_w is shorter than the total response time t_{pd} through the comparator.

12-BIT FAST A/D CONVERTER



NOTE:
DEVICE(S) CONNECTED TO ANALOG INPUT MUST BE CAPABLE OF SOURCING 4.0mA. A BUFFER (eg. BUF-03) MAY BE REQUIRED.



CONVERSION TIME (ns)	TYP	WORST CASE
SAR	33	55
CMP-05	92	125
TOTAL	375ns	680ns
× 13	4.9µs	8.8µs