ITRI ERSO

ES15041

520MHz Frequency Synthesizer

Features

- High Operating Frequency:
  $f_{IN\ MAX}$ = 520MHz
- On-Chip Prescaler: 32/33 or 64/65
- Low Power Supply Voltage: 2.7V to 5.5V
- Low Power Consumption: 30mW
- 2 types of Phase Detector Output:
  On-chip Charge Pump (Bipolar Type)
  Output for External Charge Pump
- Wide Operating Temperature:
  T_A = -40℃ to +85℃

Applications

- Wireless Communication Systems

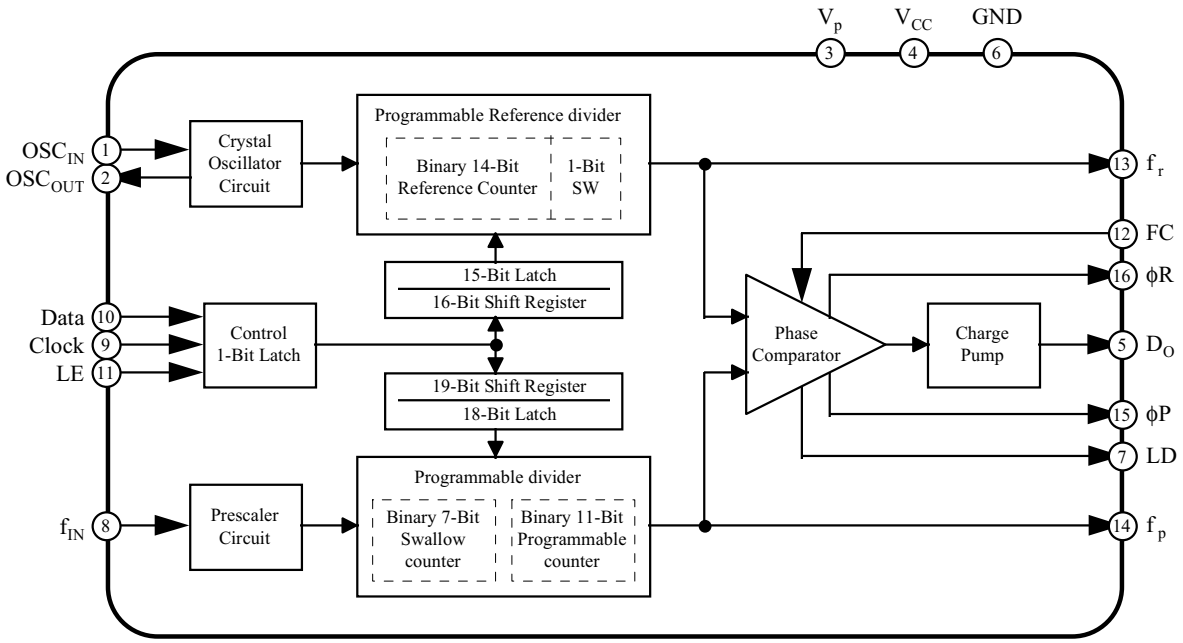
Description

The ES15041 is a high performance frequency synthesizer with pulse-swallow function. It is fabricated by Bi-CMOS technology.

The ES15041 contains dual modulus prescaler which can select either a 32/33 or a 64/65 dividing ratio at input frequency up to 520MHz. Serial data is transferred into the ES15041 via a three line interface (LE, Data, Clock).

The ES15041 operates on a low supply voltage (3V tpy.) and consumes low power (30mW at 520MHz).

Block Diagram



Absolute Maximum Rating (T_A= 25 °C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
	V_P	V_{CC} to 12.0	V
Output Voltage	V_{OUT}	-0.5 to V_{CC}+0.5	V
Open-Drain Output	V_{OOP}	-0.5 to 9.0	V
Output Current	I_{OUT}	±10	mA
Storage Temperature	T_{STG}	-55 to +125	℃

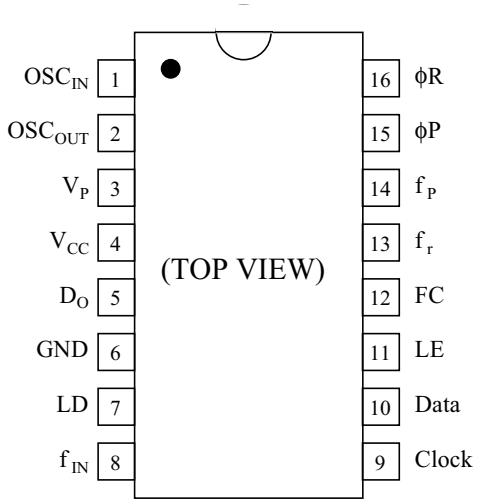
Recommended Operating Conditions

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	2.7	3.0	5.5	V
	V_P	V_{CC}		8.5	V
Open-Drain Output	V_{OOP}	V_{CC}		8.5	V
Input Voltage	V_{IN}	GND		V_{CC}	V
Operating Temperature	T_A	-40		+85	℃

Handling Precautions

- This device should be transported & stored in anti-static containers.
- This device is static charge sensitive; take proper anti-ESD precautions. Ensure that personnel & equipment are properly grounded. Cover workbenches with grounded conductive mats.

Pin Assignment



Pin Description

Pin No.	Pin Name	I/O	Description
1	OSC_{IN}	I	Oscillator input.
2	OSC_{OUT}	O	Oscillator output.
3	V_P	-	Power supply voltage for charge pump.
4	V_{CC}	-	Power supply voltage
5	D_O	O	Charge pump output. Phase characteristic can be reversed depending on FC input.
6	GND	-	Ground.
7	LD	O	Lock Detect. This pin outputs high when the phase is locked, and outputs low when the phase difference of f_r and f_p exits.
8	f_{IN}	I	Prescaler input. It's connected to an external VCO output through a capacitor.
9	Clock	I	Clock input for 19-bit shift register and 16-bit shift register. Each rising edge of the clock shifts one bit of data into the shift registers.
10	Data	I	Serial data of binary code input. The last data bit is a control bit to specify which latch is activated. When the last bit is high level and LE is high level, data is transferred to 15-bit latch. When the last bit is low level and LE is high level, data is transferred to 18-bit latch
11	LE	I	Load enables input (with internal pull-up resistor). When LE is high level (or open), data stored in the shift register is transferred to latch depending on the control data.
12	FC	I	Phase selecting input of phase comparator (with internal pull up resistor). When FC is low level, charge pump and phase detector characteristics can be reversed.
13	f_r	O	Monitor pin of phase comparator input. It is the same as programmable reference divider output.
14	f_P	O	Monitor pin of phase comparator input. It is the same as programmable divider output.
15	ϕP	O	Output for external charge pump. Phase characteristics can be reversed depending on FC input. ϕP pin is an N-channel open-drain output.
16	ϕR	O	Output for external charge pump. Phase characteristics can be reversed depending on FC input.

Electrical Characteristics

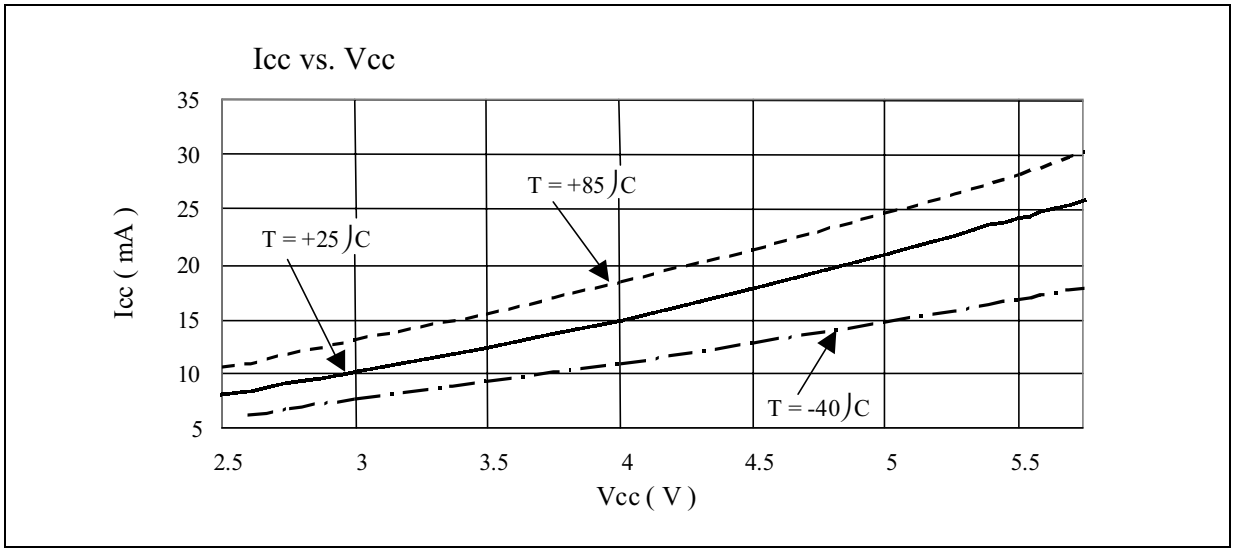
(V_{CC} = 2.7 to 5.5V, T_A = -40 to +85℃)

Parameter	Pin Name	Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current	V_{CC}	I_{CC}	*1	-	10	-	mA
Operating Frequency	f_{IN}	f_{IN}	*2	10	-	520	MHz
	OSC_{IN}	f_{OSC}		-	12	20	MHz
Input Sensitivity	f_{IN}	Pf_{IN1}	V_{CC}=2.7 ~ 4.0V	-10	-	6	dBm
		Pf_{IN2}	V_{CC}=4.0 ~ 5.5V	-4	-	6	dBm
	OSC_{IN}	V_{IN}		0.5	-	-	V_{P-P}
High-level Input Voltage	Except f_{IN} & OSC_{IN}	V_{IH}		0.7× V_{CC}	-	-	V
Low-level Input Voltage		V_{IL}		-	-	0.3× V_{CC}	V
High-level Input Current	Data, Clock	I_{IH}		-	1.0	-	μA
Low-level Input Current		I_{IL}		-	-1.0	-	μA
Input Current	OSC_{IN}	I_{IN}		-	±50	-	μA
	LE, FC	I_{LE}		-	-60	-	μA
N-channel Open-drain Cutoff Current	ϕP	I_{OFF}	$V_{CC} \le V_P \le 8V$	-	-	1.1	μA
High-level Output Current	Except D_O & OSC_{OUT}	I_{OH}	V_{OH}=2.4V	-1.0	-	-	mA
Low-level Output Current		I_{OL}	V_{OL}=0.4V	1.0	-	-	mA
High-level Output Current	D_O	I_{DOH}	V_{CC}=3.0V, V_P=6V, T_A=25℃, V_{DOH}=5.4V	-1.0	-2.5	-	mA
Low-level Output Current		I_{DOL}	V_{CC}=3.0V, V_P=6V, T_A=25℃, V_{DOL}=0.6V	4.0	7.0	-	mA
Leakage Current	D_O, ϕP	D_{OZ}	V_{CC}=3.0V, V_P=8V, T_A=25℃	-	-	1.0	μA

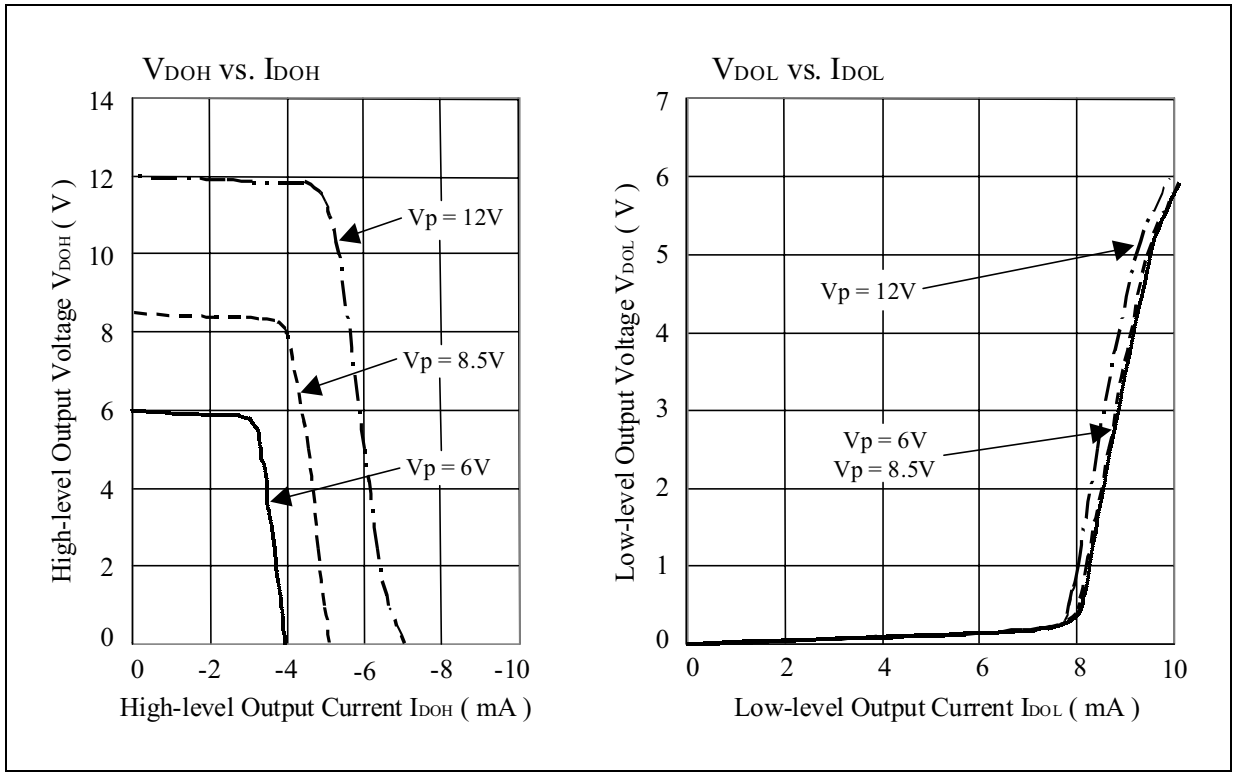
Note: *1. V_{CC} = 3.0V, f_{IN} = 520MHz, f_{OSC} = 12MHz crystal.
Inputs are grounded except f_{IN}, and outputs are open.
*2. Input coupling capacitor 1000pF is connected.

Typical Performance Characteristics

• Power Supply Current



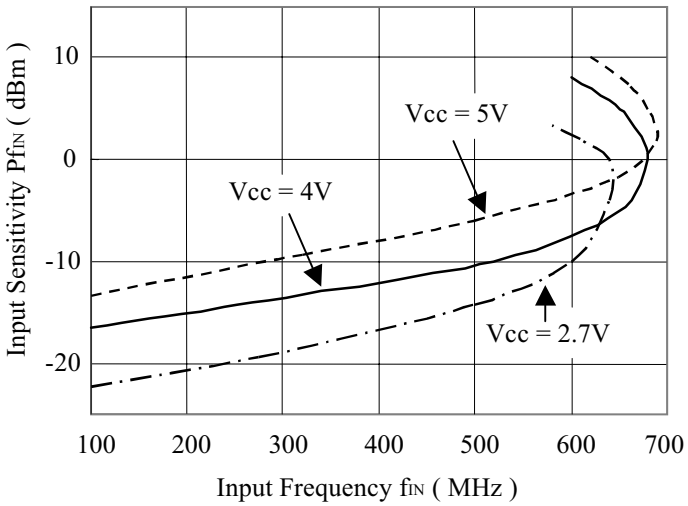
• Do Voltage vs. Charge Pump Current

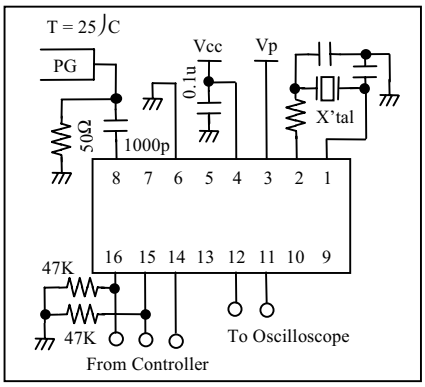


Typical Performance Characteristics (cont.)

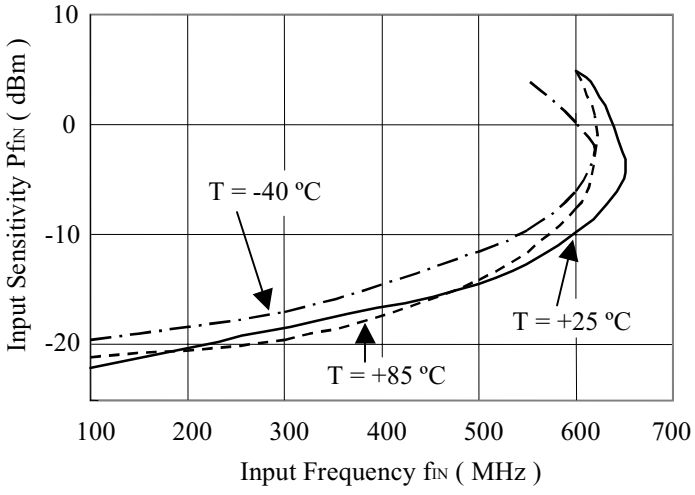
• Input Sensitivity vs. Input Frequency

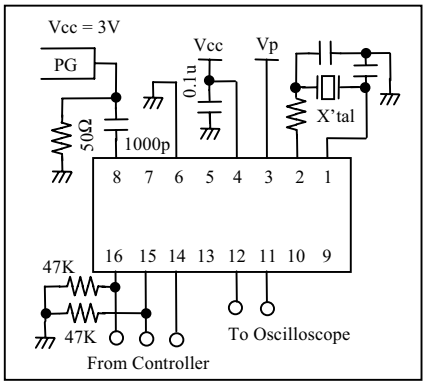
Supply Voltage Dependence





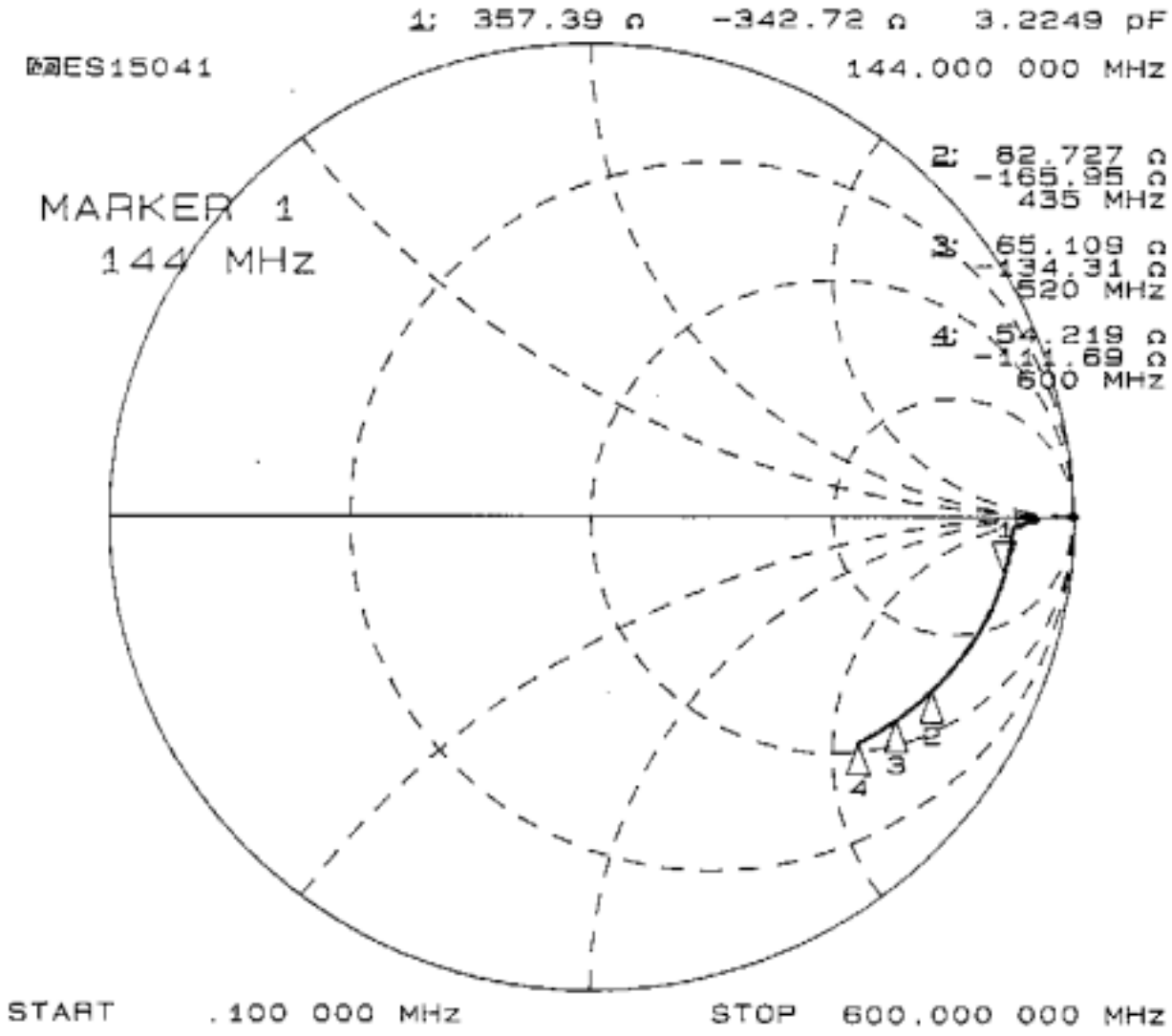
Temperature Dependence





Typical Performance Characteristics (cont.)

• Input Impedance vs. Frequency



Functional Description

• Serial Data Input

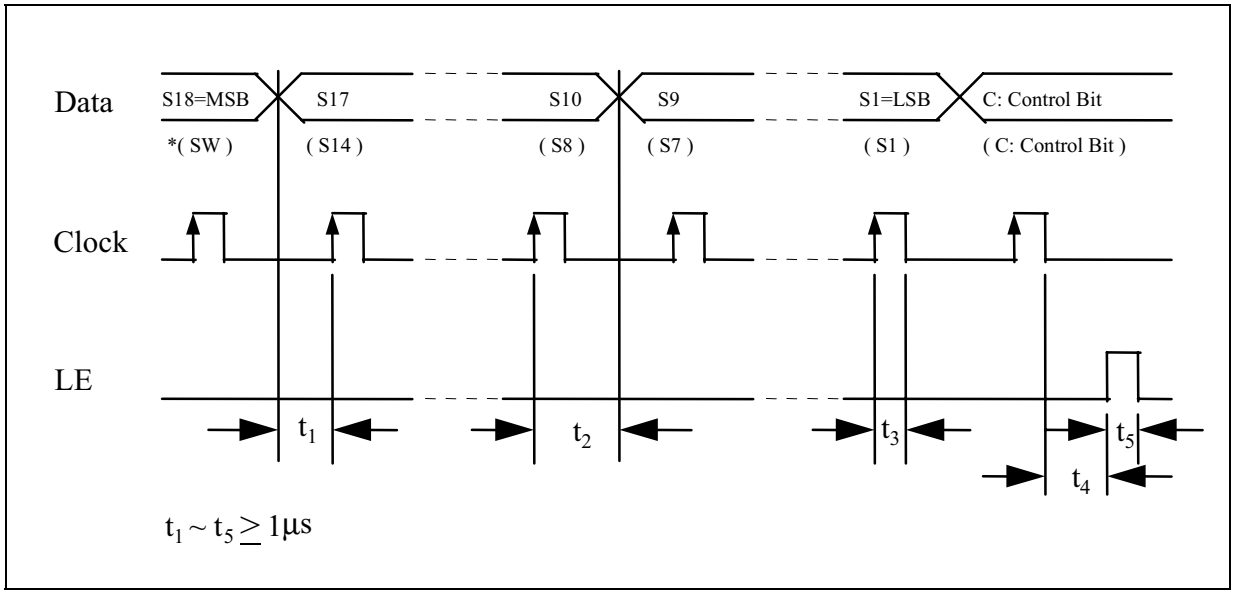
Serial data input is input using Data pin, Clock pin, LE pin.

Each one bit of the data shifted into the internal shift registers on clock rising edge.

When LE is high level (or open), data stored in shift registers is transferred to 15-bit latch or 18-bit latch depending upon the control bit level.

Control data "H" : Data is transferred into 15-bit latch.
Control data "L" : Data is transferred into 18-bit latch.

t_1 : Data setup time t_2 : Data hold time t_3 : Clock pulse width
t_4 : LE setup time t_5 : LE pulse width

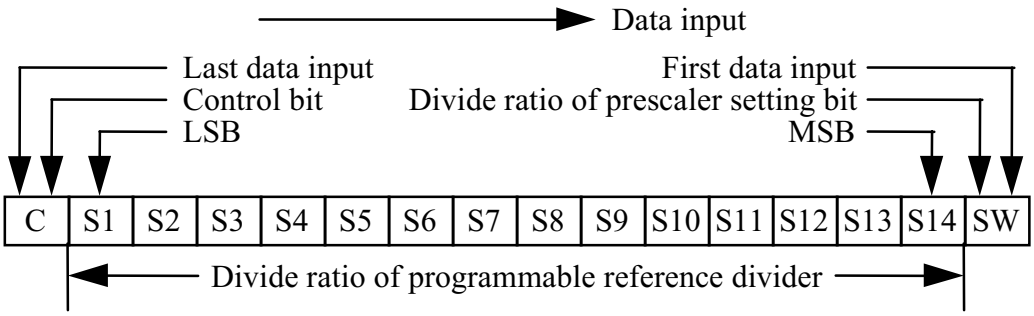


Notes: Parenthesis data indicates programmable reference divider data.
Data Shifted into register on clock rising edge.

Functional Description (cont.)

• Programmable Reference Divider

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.



Data is input from MSB data.
C : Control bit (Control bit is set to high)

⊙14-bit Programmable Reference Counter Divide Ratio (R Counter)

Divide Ratio R	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Divide ratio less than 8 is prohibited.
Divide ratio R : 8 to 16383

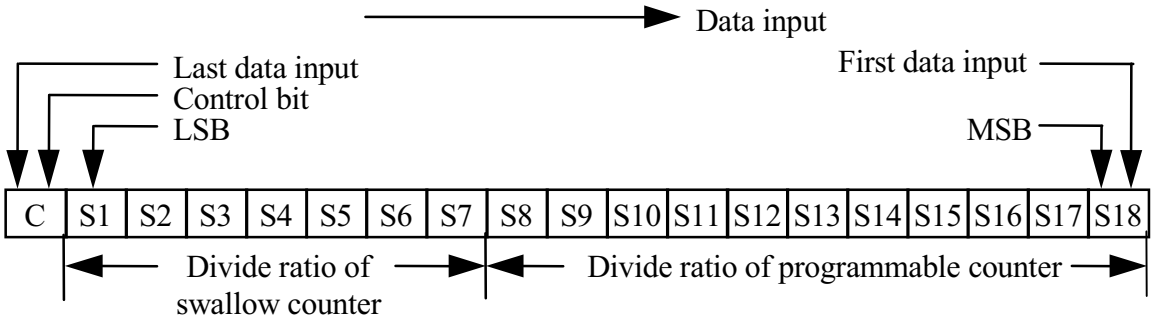
⊙1-bit Prescaler Select (S Latch)

Prescaler Select P	SW
64/65	0
32/33	1

Functional Description (cont.)

• Programmable Divider

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter. Serial 19-bit data format is shown below.



Data is input from MSB data.
C : Control bit (Control bit is set to low)

⊙7-bit Swallow Counter Divide Ratio (A Counter)

Divide Ratio A	S7	S6	S5	S4	S3	S2	S1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Divide ratio A : 0 to 127

⊙11-bit Programmable Counter Divide Ratio (B Counter)

Divide Ratio B	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Divide ratio less than 16 is prohibited
Divide ratio B : 16 to 2047

Functional Description (cont.)

• Pulse Swallow Function

$f_{VCO} = [(P \times B) + A] \times f_{OSC} / R$

f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)

f_{OSC} : Output frequency of the external reference frequency oscillator

P : Prescaler ratio (32 or 64)

B : Divide ratio of 11-bit programmable counter

A : Divide ratio of 7-bit swallow counter ($A \leq B$)

R : Divide ratio of 14-bit programmable reference counter

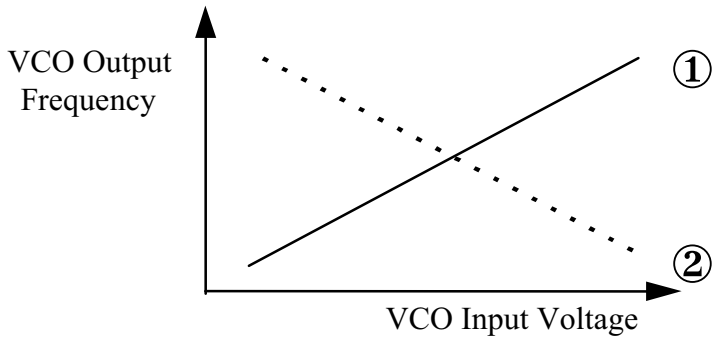
Phase Characteristics

FC pin is provided to reverse the phase comparator characteristics. The characteristics of internal charge pump output (Do), phase detector output (ϕR, ϕP) can be reversed depending on FC input data. Outputs are shown below.

	FC = H (or open)			FC = L		
	Do	ϕR	ϕP	Do	ϕR	ϕP
fr > fp	H	L	L	L	H	Z
fr < fp	L	H	Z	H	L	L
fr = fp	Z	L	Z	Z	L	Z

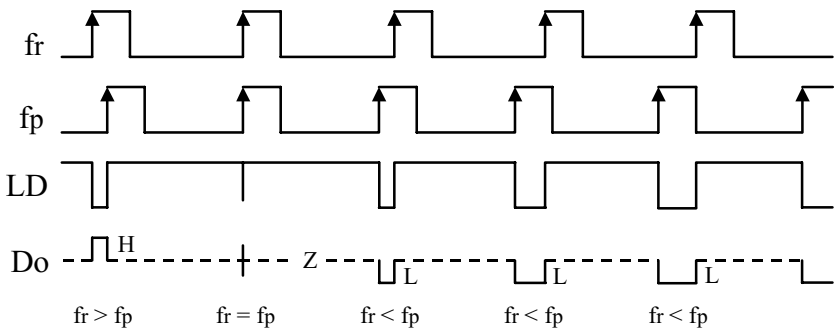
Note : Z=High Impedance

• VCO Characteristics



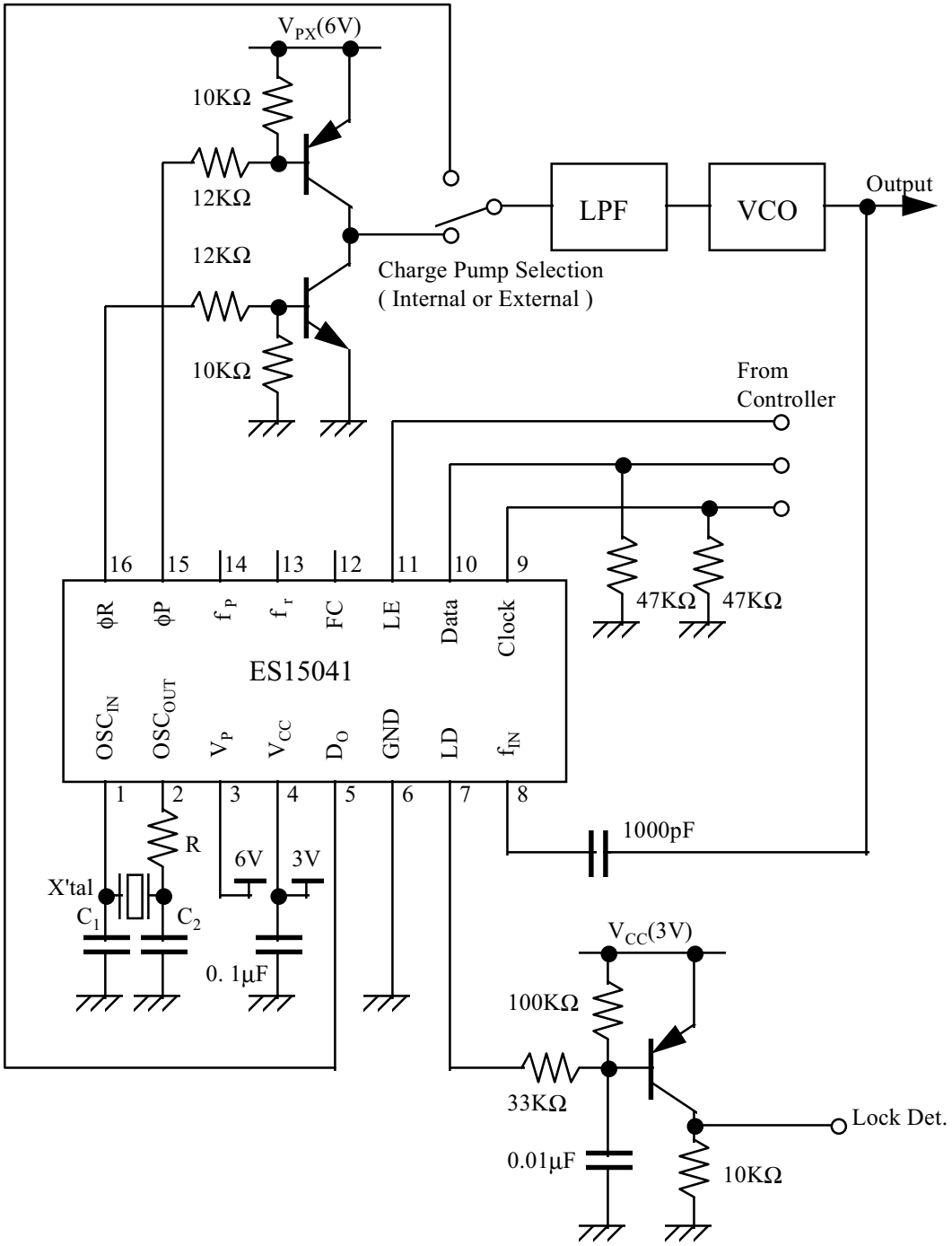
Depending on VCO characteristics, FC pin should be set accordingly:
When VCO characteristics are like ①, FC should be set to high or open circuit.
When VCO characteristics are like ②, FC should be set to low.

• Phase Comparator and Internal Charge Pump Characteristics



Notes: Phase difference detection rage: -2π to +2π
FC = H

Application Circuit



C_1, C_2 & R : Depends on crystal oscillator
V_P, V_{PX} : 8V max

Package Outline Unit: mm

ES15041S 16-pin SOP (Plastic)