HIGH DEFINITION SERIAL DIGITAL INTERFACE (HD-SDI) CHIPSET S8401/S8501

FEATURES

- Micro-Power Bipolor technology
- SMPTE 292M compliant
- 1.485 Gb/s or 1.485/1.001 Gb/s operation
- HD-SDI Serializer transmitter incorporates a Phase Lock Loop (PLL) providing clock synthesis from low-speed reference
- HD-SDI Deserializer receiver PLL configured for clock and data recovery
- 20-bit parallel TTL compatible interface
- Low-jitter serial PECL compatible interface
- Lock detect
- Local loopback
- Continuous downstream clocking from receiver
- Single +3.3V power supply
- Compact 52 PQFP package

APPLICATIONS

Parallel to HD-SDI/HD-SDI to parallel interfacing

- Compressors
- Video graphics
- Video editors
- Disc storage devices
- VTR's
- Cameras
- Monitors
- Frame synchronizers
- Character generators

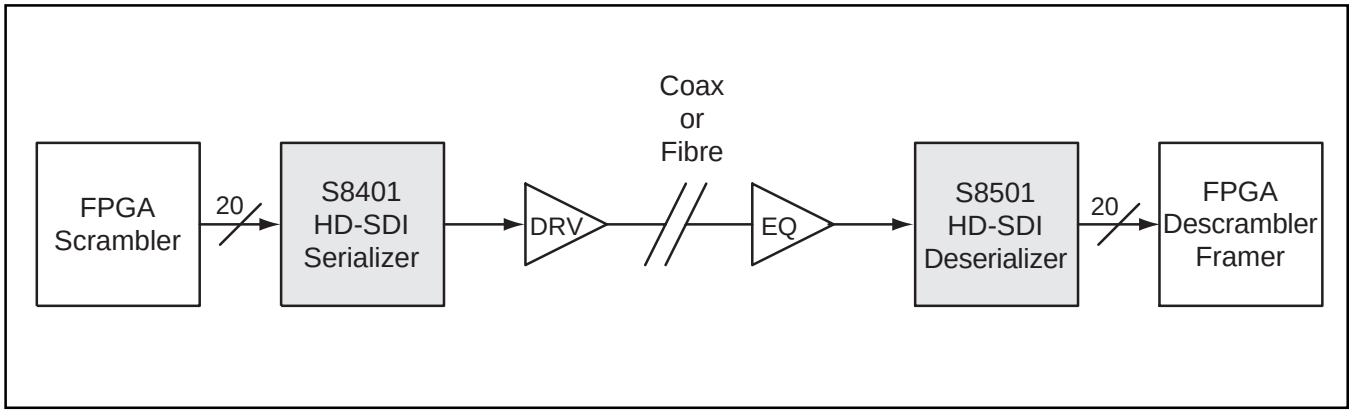
GENERAL DESCRIPTION

The S8401 and S8501 transmitter and receiver pair are designed to perform HD-SDI over fiber optic or coaxial cable interfaces conforming to the requirements of the SMPTE 292M. The chipset supports 1.485 Gb/s with an associated 20-bit data word.

The chipset performs parallel-to-serial and serial-to-parallel conversion for scrambled data. The S8401 on-chip PLL synthesizes the high-speed clock from a low-speed reference. The S8501 on-chip PLL synchronizes directly to incoming digital signals, to receive the data stream. The transmitter and receiver each support differential PECL I/O for fiber optic component interfaces, to minimize crosstalk and maximize data integrity. Local loopback allows for system diagnostics.

The S8401 and S8501 operate from +3.3V power supplies. Each chip typically dissipates only 0.70 and 0.90W respectively. Figure 1 shows a typical network configuration incorporating the chipset.

Figure 1. System Block Diagram



S8401/S8501 OVERVIEW

The S8401 transmitter and S8501 receiver provide serialization and deserialization functions for scrambled data to implement a HD-SDI. Operation of the S8401/S8501 chips is straightforward, as depicted in Figure 2. The sequence of operations is as follows:

Transmitter
1. 20-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver
1. Clock and data recovery from serial input
2. Serial-to-parallel conversion
3. 20-bit parallel output

The 20-bit parallel data handled by the S8401 and S8501 devices should be from a DC-balanced encoding scheme, such as the scrambling as defined by SMPTE-292M.

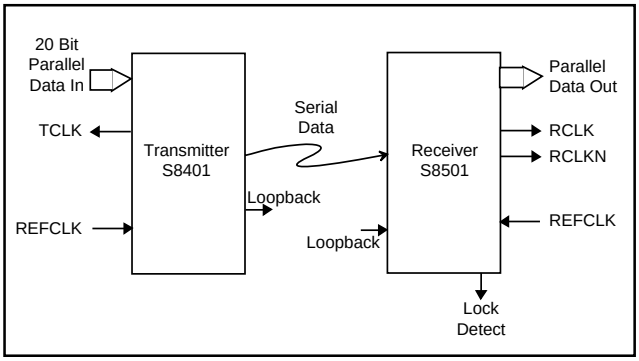
Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figure 5.

A lock detect feature is provided on the receiver, which indicates that the PLL is locked (synchronized) to the data stream.

Loopback

Local loopback is supported by the chipset, and provides a capability for performing offline testing of the interface to ensure the integrity of the serial channel before enabling the transmission medium. It also allows for system diagnostics.

Figure 2. Interface Diagram



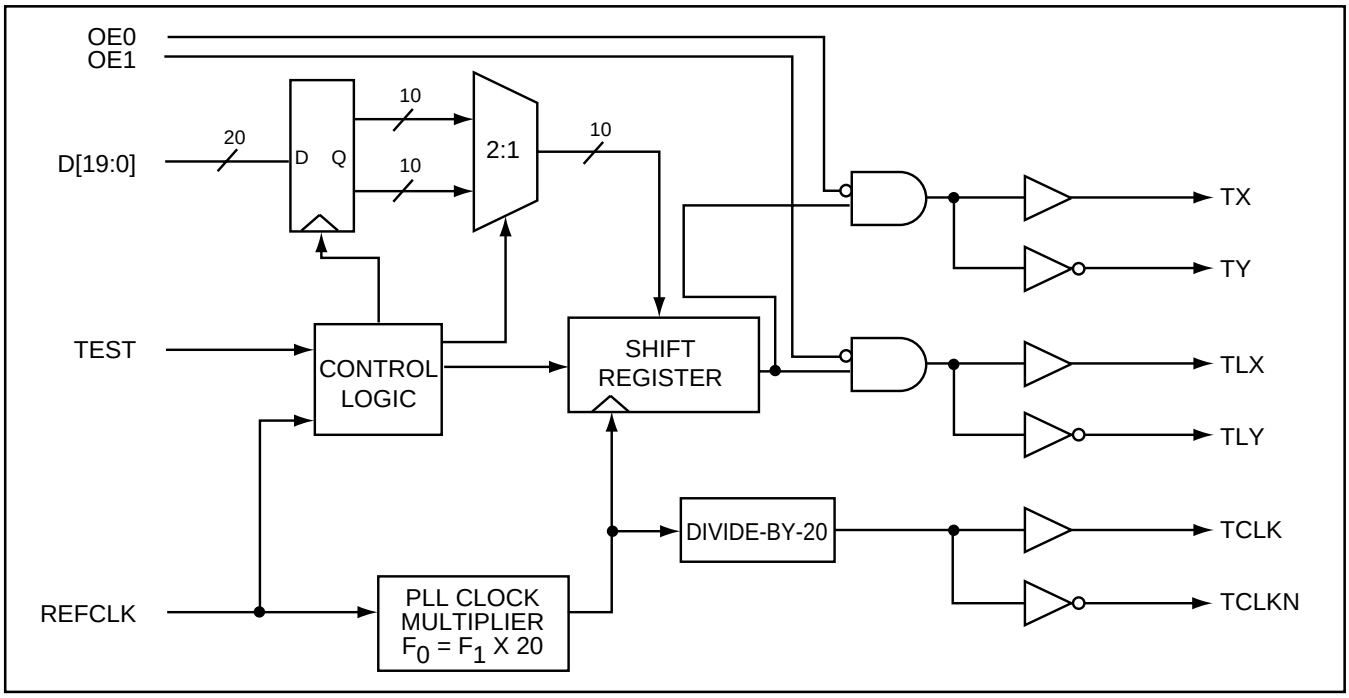
S8401 TRANSMITTER

Architecture/Functional Description

The S8401 transmitter accepts parallel input data and serializes it for transmission over fiber optic or coaxial cable media. The S8401 is compliant with SMPTE 292M Specification, and supports the HD-SDI data rate of 1.485 Gb/s.

The parallel input data word is 20 bits wide. A block diagram showing the basic chip function is shown in Figure 3.

Figure 3. S8401 Functional Block Diagram



Parallel/Serial Conversion

The parallel-to-serial converter takes in 20-bit wide data from the input latch and converts it to a serial data stream. Parallel data is latched into the transmitter on the positive going edge of REFCLK. The data is then clocked synchronous to the clock synthesis unit serial clock into the serial output shift register. The shift register is clocked by the internally generated bit clock which is 20 times the REFCLK input frequency. The state of the serial outputs is controlled by the output enable pins, OE0 and OE1. D[0] is transmitted first.

Reference Clock Input

The reference clock input (REFCLK) must be supplied with a PECL single-ended AC coupled crystal clock source with 100 PPM tolerance to assure that the transmitted data meets the SMPTE 292M Specification frequency limits. The internal serial clock is frequency locked to the reference clock. Refer to Table 1 for reference clock frequency.

Table 1. Transmitter Operating Mode

Data Rate (Mbps)	Word Width (Bits)	Reference Clock Frequency (MHz)	TCLK/TCLKN Frequency (MHz)
1485	20	74.25	74.25

Figure 4. S8501 Functional Block Diagram

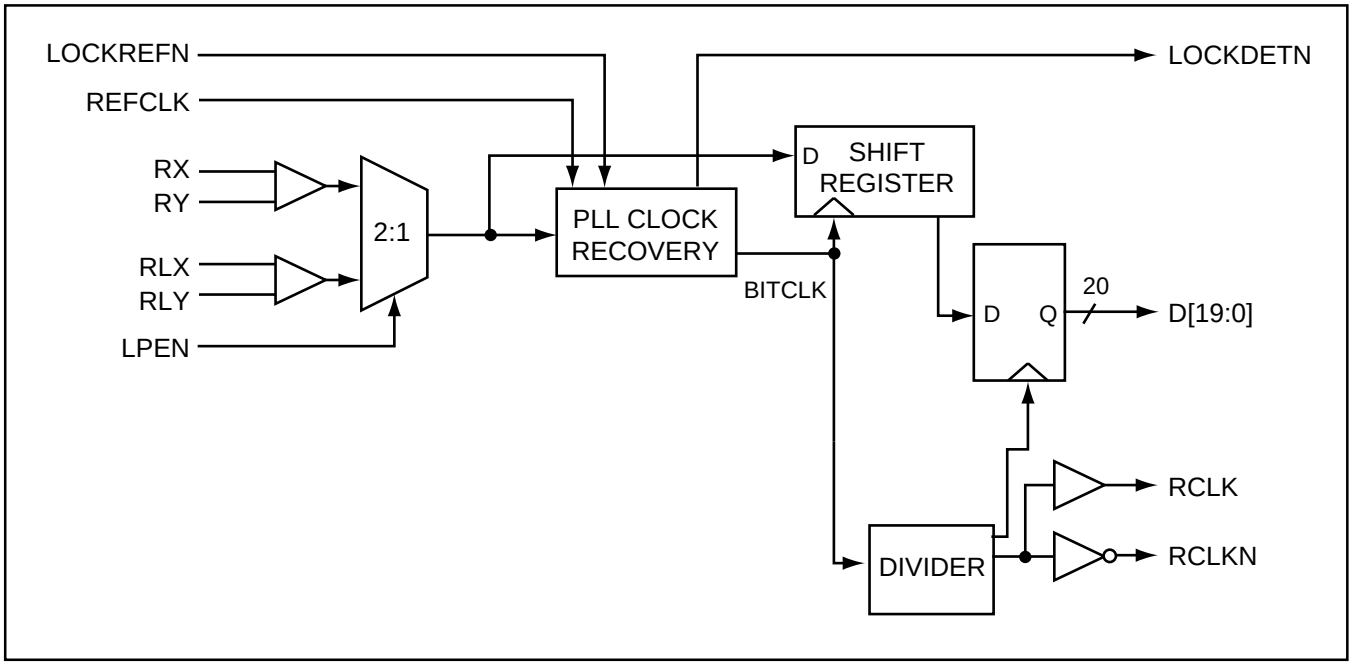
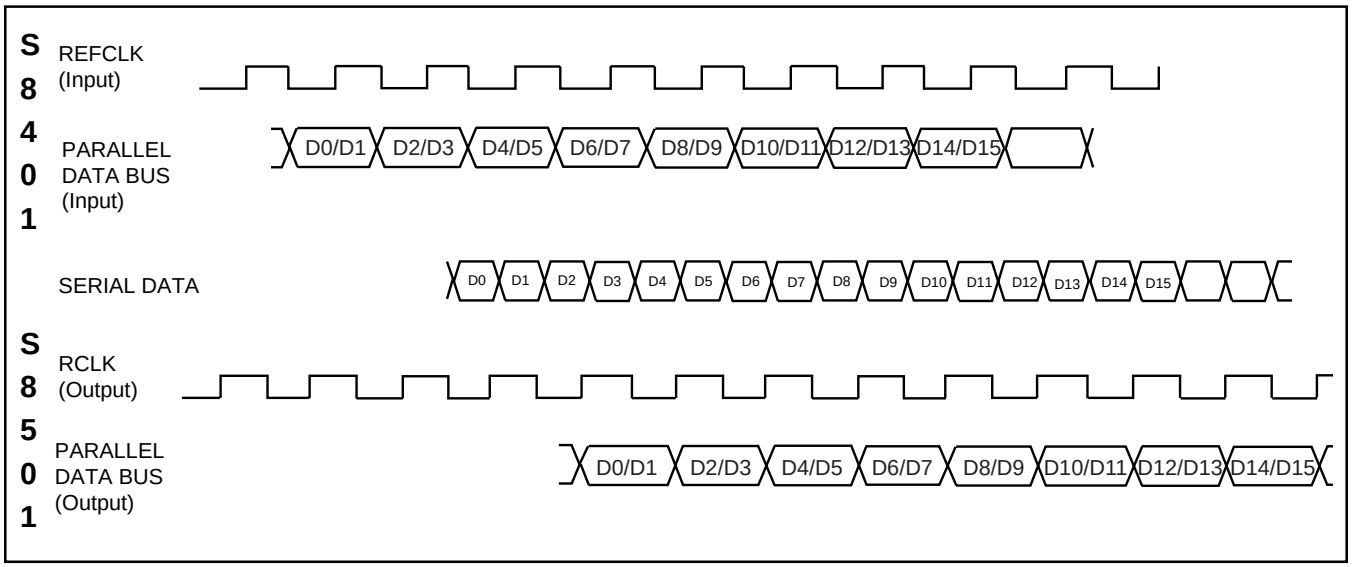


Figure 5. Functional Waveform



S8501 RECEIVER

Architecture/Functional Description

The S8501 receiver is designed to implement SMPTE 292M Specification receiver functions. A block diagram showing the basic chip function is provided in Figure 4.

Whenever a signal is present, the S8501 attempts to achieve bit synchronization of the received encoded bit stream. Received data from the incoming bit stream is provided on the device's parallel data outputs.

The S8501 accepts serial encoded data from a fiber optic or coaxial cable interface. The serial input stream is the result of the serialization of scrambled data by a compatible transmitter. Clock recovery is performed on-chip, with the output data presented to the transmission layer as 20-bit parallel data. The chip operates at the HD-SDI frequency of 1.485Gb/s.

Serial/Parallel Conversion

Serial data is received on the RX, RY pins. The PLL clock recovery circuit will lock to the data stream if the clock to be recovered is within ±100 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The data is then clocked into the serial to parallel output registers.

Reference Clock Input

The reference clock input must be supplied with a PECL single-ended AC coupled crystal clock source at ±100 PPM tolerance. See Table 2 for reference clock frequency.

Framing

Framing is performed off-chip. Typically, an FPGA would be used to implement descrambling and Word/Frame synchronization as required by SMPTE 292M.

Lock Detect

The S8501 lock detect function indicates the state of the phase-locked loop (PLL) clock recovery unit. The PLL will indicate lock within 2.5µs after the start of receiving serial data inputs. If the serial data inputs have an instantaneous phase jump (from a serial switch, for example) the PLL will not indicate an out-of-lock state, but will recover the correct phase alignment within 250 bit times. If a run length of 80-160 bits is exceeded the loop will declare loss of lock. Input data rate variation (compared to REFCLK) can also cause loss of lock. Table 3 shows the response of the PLL loop circuit to input data rate variation. When lock is lost, the PLL will attempt to re-acquire bit synchronization, and will shift from the serial input data to the reference clock so that the correct frequency downstream clocking will be maintained.

The LOCKDETN output will go inactive (High) when no data is present on the serial data inputs. When LOCKDETN is in the inactive (high) state, it indicates that the PLL is locking to the local reference clock to maintain downstream clocking. When LOCKDETN is in the active (low) state, it indicates that the PLL is attempting to lock to the incoming serial data. When serial data is restored, the LOCKDETN output will stay in the active state.

Figure 6. Interface Diagram

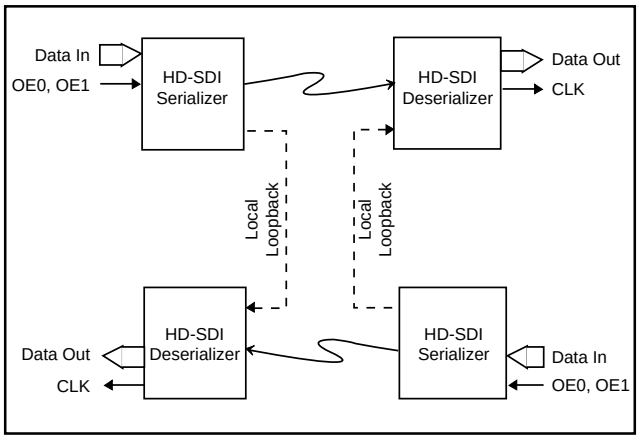


Table 2. Receiver Operating Modes

Data Rate (Mbps)	Word Width (Bits)	Reference Clock Frequency (MHz)	RCLK/RCLKN Frequency (MHz)
1485	20	74.25	74.25

When lock is lost, the PLL will attempt to reacquire bit synchronization, and will shift from the serial input data to the reference clock so that the correct downstream clocking will be maintained. The PLL will continuously shift between the reference clock and the input data until input data has been restored. This will be reflected in the RCLK and the LOCKDETN outputs – RCLK will shift slightly in frequency, and LOCKDETN will toggle to show that the PLL is shifting between input data and REFCLK.

In any transfer of PLL control from the serial data to the reference clock, the RCLK/RCLKN output remains phase continuous and glitch free, assuring the integrity of downstream clocking.

OTHER OPERATING MODES

Loopback

Local loopback requires a S8401 and a S8501 as shown in Figure 6. When enabled, serial data from the S8401 transmitter is sent to the S8501 receiver, where the clock is extracted and the data is deserialized. The parallel data is then sent to the subsystem for verification. This loopback mode provides the capability to perform offline testing of the interface to guarantee the integrity of the serial channel before enabling the transmission medium. It also allows system diagnostics.

Operating Frequency Range

The S8401 and S8501 are optimized for operation at the HD-SDI rate of 1.485 Gb/s. A REFCLK must be selected to be within 100 ppm of the desired byte or word clock rate.

Table 3. Response of PLL Loop Circuit to Input Data Rate Variation

PLL Present State	Input Data Rate Variation (compared to REFCLK)	LOCKDETN	PLL New State
Locked to REFCLK	0 - 244 ppm	H –>L	Locked to input data
	244 - 366 ppm	Indeterminate	Indeterminate
	>366 ppm	H	Locked to REFCLK
Locked to Input Data	0 - 448 ppm	L	Locked to Input Data
	448 - 752 ppm	Indeterminate	Indeterminate
	>752 ppm	L –>H	Locked to REFCLK

Table 4. S8401 Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	TTL	I	50 49 48 47 44 43 42 41 38 37 36 35 31 30 29 28 25 24 23 22	Parallel Input Data. Data is clocked in on the rising edge of REFCLK. D[0] is transmitted first.
—	GND	—	20	This pin must be connected to ground.
OE1	Static TTL	I	1	Output Enable control. Active Low. When active it enables the TLX/TLY outputs. When inactive, TLX/TLY are disabled and remain in the logic low state.
OE0	Static TTL	I	2	Output Enable control. Active Low. When active it enables the TX/TY outputs. When inactive, TX/TY are disabled and remain in the logic low state.
REFCLK	LVPECL	I	16	Reference Clock. (Externally capacitively coupled.) A crystal-controlled reference clock for the PLL clock multiplier.
TCLK TCLKN	Diff. TTL	O	12 11	Transmit Clock. Differential TTL word rate clock true and complement. See Table 1 for frequency.
TLX TLY	Diff. PECL	O	5 4	Transmit Serial Loopback Output. Differential PECL outputs that are functionally equivalent to TX and TY. They are intended to be used for loopback testing. Enabled by OE1.
TY TX	Diff. PECL	O	9 8	Transmit Serial Output. Differential PECL outputs that transmit the serial data and drive 150Ω to ground. Enabled by OE0. TX is the positive output, and TY is the negative output.

Table 4. S8401 Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
ECLVCC	+3.3V	–	21, 39	Core +3.3V.
TTLGND	GND	–	14, 15, 18, 19, 34	TTL Ground.
TTLVCC	3.3V	–	17	TTL Power Supply.
ECLIOVCC	+3.3V	–	3, 10	PECL I/O Power Supply.
ECLIOVEE	GND	–	6, 7	PECL I/O GND.
AVCC	+3.3V	–	27, 32	Analog Power Supply.
AVEE	GND	–	26, 33	Analog Ground.
ECLVEE	GND	–	13, 40, 51, 52	Core Ground.
NC	–	–	45, 46	No Connect.

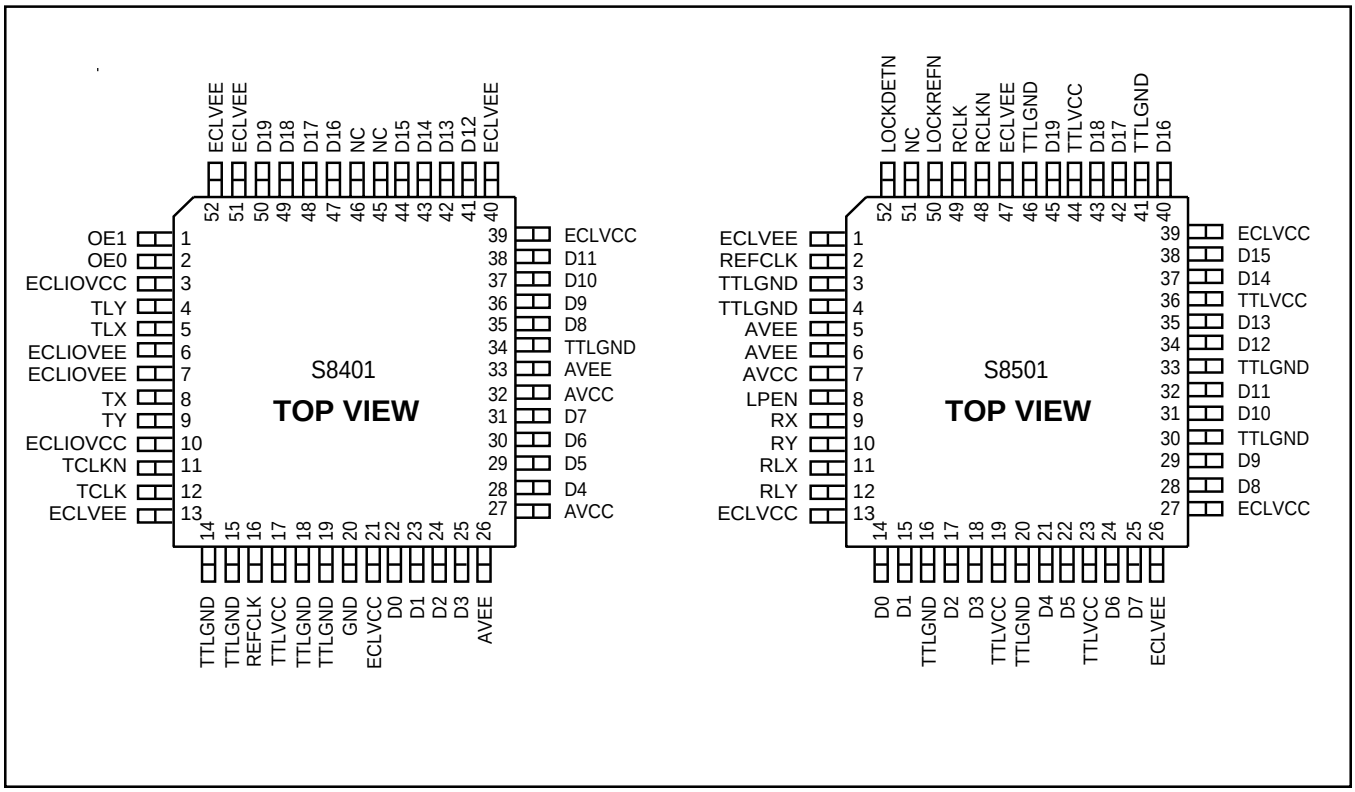
Table 5. S8501 Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	TTL	O	45 43 42 40 38 37 35 34 32 31 29 28 25 24 22 21 18 17 15 14	Outputs parallel data. Parallel data on this bus is clocked out on the falling edge of RCLK. D[0] is the first bit received.
LOCKDETN	TTL	O	52	Lock Detect. When Low, LOCKDETN indicates that the PLL is locked to the incoming data stream. When High, it provides a system flag indicating that the PLL is locked to the local reference clock.
LPEN	TTL	I	8	Loop Enable. Active High. When active, LPEN selects the loopback serial input pins RLX and RLY. When inactive, LPEN selects the received serial data input pins RX and RY (normal operation).
RCLK RCLKN	Diff. TTL	O	49 48	Receive Clock. Parallel data is clocked out on the falling edge of RCLK.
REFCLK	LVPECL	I	2	Reference Clock. (Externally capacitively coupled.) A free-running crystal-controlled reference clock for the PLL clock multiplier. The frequency of REFCLK is shown in Table 2.
RLX RLY	Diff. PECL	I	11 12	Receive Loopback Serial Inputs. (Externally capacitively coupled.) The serial loopback data inputs. RLX is the positive input, and RLY is the negative input. See Figure 16 if not used.
RX RY	Diff. PECL	I	9 10	Receive Serial Inputs. (Externally capacitively coupled.) The received serial data inputs. RX is the positive input, and RY is the negative input. See Figure 16 if not used.

Table 5. S8501 Pin Assignment and Descriptions (Continued)

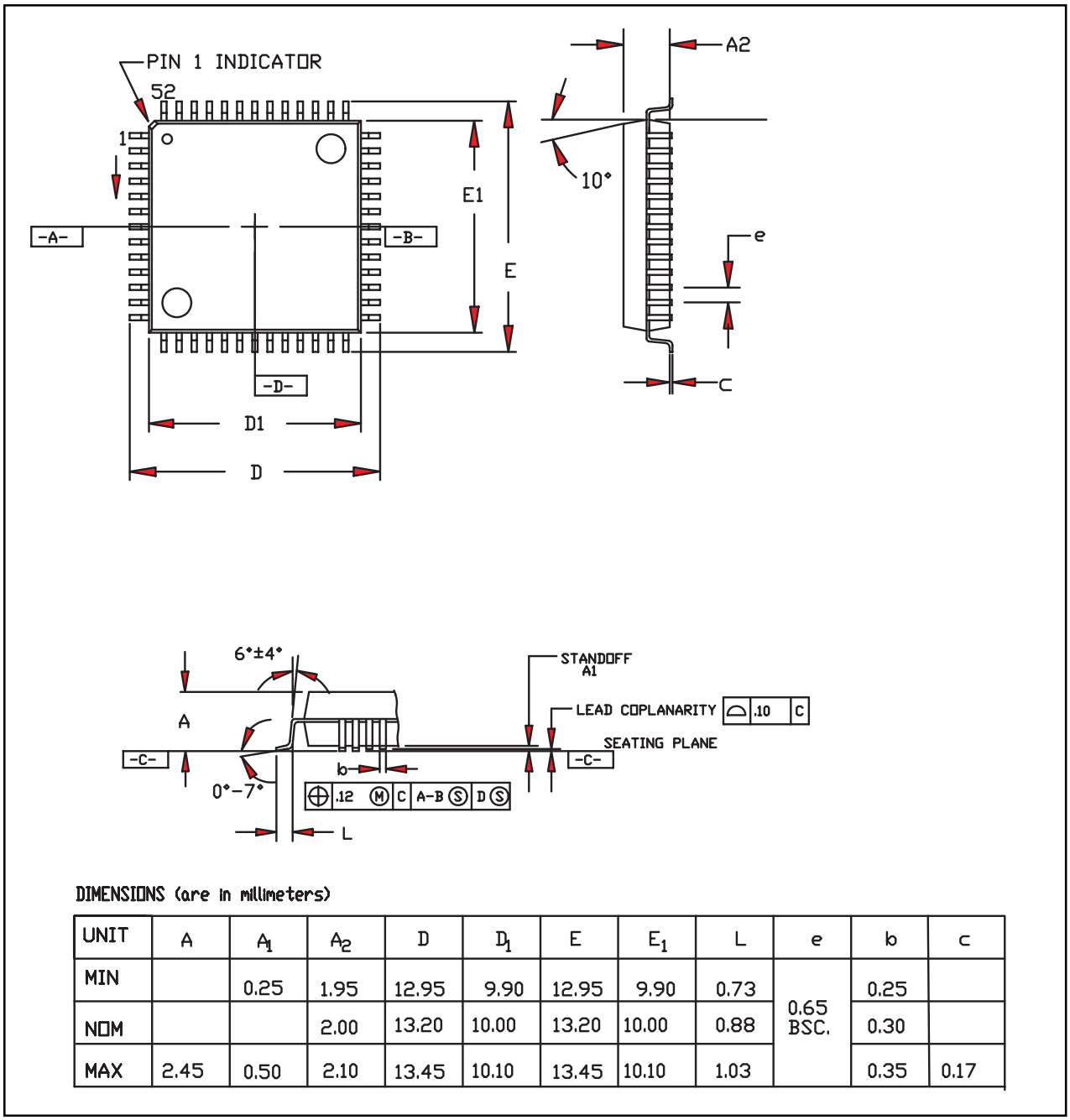
Pin Name	Level	I/O	Pin #	Description
LOCKREFN	TTL	I	50	Active Low. When active, forces the PLL to lock to the REFCLK input and ignore the serial data inputs. When active, PLL locks to the serial data input (normal operation).
TTLVCC	+3.3V	–	19, 23, 36, 44	TTL Power Supply.
TTLGND	GND	–	3, 4, 16, 20, 30, 33, 41, 46	TTL Ground.
ECLVCC	+3.3V	–	13, 27, 39	Core Power Supply.
ECLVEE	GND	–	1, 26, 47	Core Ground.
AVCC	+3.3V	–	7	Analog Power Supply.
AVEE	GND	–	5, 6	Analog Ground.
NC	–	–	51	Not connected.

Figure 7. S8401 and S8501 52 PQFP Pinouts



TTLVCC = +3.3V
AVCC = +3.3V
ECLVCC = +3.3V
ECLIOVCC = +3.3V
ECLIOVEE = 0V
TTLGND = 0V
ECLVEE = 0V
AVEE = 0V

Figure 8. 52 PQFP — (10mm x 10mm) Plastic Quad Flat Pack



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.25	1.95	12.95	9.90	12.95	9.90	0.73	0.65 BSC.	0.25	
NOM			2.00	13.20	10.00	13.20	10.00	0.88		0.30	
MAX	2.45	0.50	2.10	13.45	10.10	13.45	10.10	1.03		0.35	0.17

Thermal Management

Device	Pkg. Max Power	Θja (Still Air)
S8401	1.1W	55° C/W
S8501	1.2W	50° C/W

Note: S8501 package has internal heat spreader resulting in lower Θja.

Table 6. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		150	˚C
Voltage on V_{CC} with respect to Ground	-0.5		3.47	V
Voltage on any TTL Input Pin	-0.7		(V_{CC} +.6V)	V
Voltage on any PECL Input Pin	0		ECL/ V_{CC}	V
TTL Output Sink Current			8	mA
TTL Output Source Current			8	mA
High Speed PECL Output Source Current			24	mA
Electro Static Discharge Voltage		500		V

Table 7. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	0		70	˚C
Junction Temperature Under Bias			130	˚C
Voltage on TTLVCC with respect to Ground 3.3V Operation	3.13	3.3	3.47	V
Voltage on any TTL Input Pin	0		3.47	V
Voltage on ECLVCC with respect to Ground	3.13	3.3	3.47	V
Voltage on any PECL Input Pin	(ECL V_{CC} -2.0)		ECL V_{CC}	V

Table 8. S8401 DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage (TTL) – 3.3V Power Supply – 3.3V Power Supply	 2.1 2.2			 V V	 V_{CC} = min, I_{OH} = -2.4mA V_{CC} = min, I_{OH} = -.1mA
V_{OL}	Output Low Voltage (TTL) – 3.3V Power Supply			.5	V	V_{CC} = min, I_{OL} = 2.4mA
V_{IH}	Input High Voltage (TTL)	2.0	—	—	V	I_{IH} <= 1mA at V_{IH} = 5.5V
V_{IL}	Input Low Voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input High Current (TTL)	—	—	50	µA	V_{IN} = 2.4V
I_{IL}	Input Low Current (TTL)	-500	—	-50	µA	V_{IN} = 0.5V
I_{CC}	Supply Current		123	160	mA	Outputs open, V_{CC} = V_{CC} max
P_D	Power Dissipation		.406	.554	W	Outputs open, V_{CC} = V_{CC} max
ΔV_{INCLK}	Single-ended REFCLK input swing	440	—	1300	mV	AC coupled
ΔV_{OUT}	Serial Output Voltage Swing	600	—	1300	mV	50Ω to V_{CC} -2.0V

Table 9. S8501 DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage (TTL) – 3.3V Power Supply – 3.3V Power Supply	 2.04 2.15			 V V	 V_{CC} = min, I_{OH} = -2.4mA V_{CC} = min, I_{OH} = -.1mA
V_{OL}	Output Low Voltage (TTL) – 3.3V Power Supply			.5	V	V_{CC} = min, I_{OL} = 2.4mA
V_{IH}	Input High Voltage (TTL)	2.0	—	—	V	
V_{IL}	Input Low Voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input High Current (TTL)	—	—	50	µA	V_{IN} = 2.4V
I_{IL}	Input Low Current (TTL)	-500	—	-50	µA	V_{IN} = 0.5V
I_{CC}	Supply Current		213.8	287	mA	Outputs open, V_{CC} = V_{CC} max
P_D	Power Dissipation – 3.3V Supply		0.711	.995	W	Outputs open, V_{CC} = V_{CC} max
ΔV_{INCLK}	Single-ended REFCLK input swing	440	—	1300	mV	AC coupled
V_{DIFF}	Min. differential input voltage swing for differential PECL inputs	100		1300	mV	

Timing

The data on the TX[19:0] data bus will be sampled on every rising edge of REFCLK. The data will be serialized and transmitted onto the serial link. The figure below illustrates the timing requirements of REFCLK with respect to the TX[19:0] signals, minimum high and low durations, and the rising and falling slew rate magnitudes. In addition, this system supplied clock must not have more jitter than ±20% of a baud interval.

Table 10. S8401 Transmitter Timing Table

Parameter	Symbol	Min	Max	Units	Comments[1]
REFCLK Frequency	f	74.24258	74.25743	MHz	
REFCLK Jitter Tolerance 1.485 Gb/s			80	ps pk-pk	While maintaining a 77% eye at serial output.
REFCLK Period	t_p	13.469	13.287	ns	
REFCLK Duty Cycle		40%	60%	90	Measured at 50% level.
Data Setup to REFCLK	t_1	2		ns	Required setup time.
Data Hold from REFCLK	t_2	1		ns	Required hold time.
REFCLK Rise Time	t_r	0.5	3.2	ns	This applies to the REFCLK input (20-80%)
REFCLK Fall Time	t_f	0.5	3.2	ns	This applies to the REFCLK input (20-80%)

Note: All AC measurements are made from the reference voltage level of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Table 11. Serial Data Timing Table (TLX, TLY; TX, TY)

Parameters	Description	Min	Max	Units	Conditions
Total Jitter	Serial data output total jitter (p-p)	—	192	ps	Peak-to-peak, tested on a sample basis. Measured with 2^7-1 pattern.
T_{DJ}	Serial data output deterministic jitter (p-p)	—	80	ps	Peak-to-peak, tested on a sample basis. Measured with IDLE pattern.
T_{RJ}	Serial data output random jitter (p-p)	—	112	ps	Peak-to-peak, calculated from total jitter.
T_{SDR}, T_{SDF}	Serial data rise and fall time	—	300	ps	20% to 80%, tested on a sample basis.

Tested per Figure 9.

Timing

This section will detail the timing requirements of all of the signals on the interface. All timing is measured into a lumped 15pF capacitive load.

RCLK Timing

When LOCKREFN is pulled low, RCLK should be in local phase lock with REFCLK within 500µs. LOCKREFN, when activated, shall stay low for a duration of at least 500µs if receiver frequency lock is to be expected. After local phase lock has been acquired, and when LPEN is high, 2500 baud times after LOCKREFN is driven high, RCLK shall be in phase lock with REFCLK. After local phase lock has been acquired, and when LPEN is low, 250 baud times after LOCKREFN is driven high, RCLK shall be in phase lock with the incoming serial data stream.

When a 74.25 MHz module is in frequency lock (either with REFCLK or a serial data stream) RCLK shall never have a high level duration (>2.0v) which is less than 4.3 ns, nor a low level duration (<0.8v) which is less than 4.3 ns (no clock shivering shall occur). When the S8501 is in frequency lock (either with REFCLK or a serial data stream) and LOCKREFN has been inactive for at least 2500 baud times the minimum instantaneous period shall always be greater that 13.0 ns. When the PLL is adjusting to a new phase or a new frequency, where both the old and new frequencies are valid SMPTE 292M frequencies, RCLK shall never have a period less than 13.0 ns.

Figure 9. Transmitter Timing Diagram

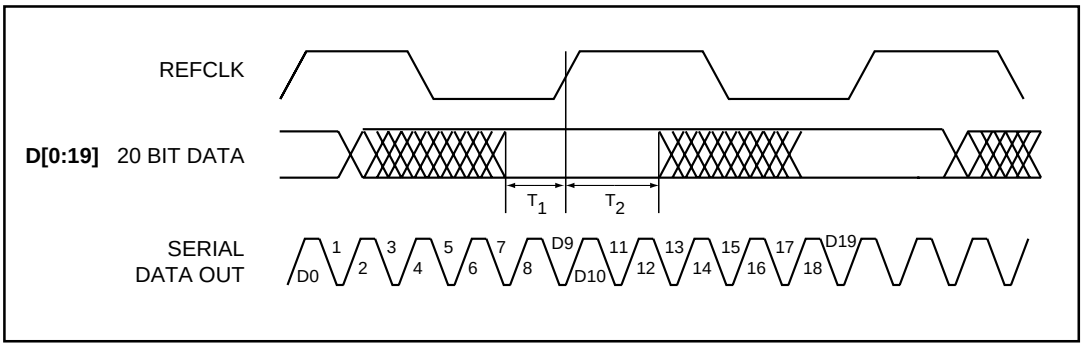


Table 12. Serial Data Input Timing Table (RLX, RLY; RX, RY)

Parameters	Description	Min	Max	Units	Conditions
R_{SDR}, R_{SDF}	Serial data input rise and fall	—	300	ps	20% to 80%.
T_{LOCK}	Data aquisition lock time	—	2.5	µs	
Input Jitter Tolerance	Input data eye opening allocation at receiver input for BER<1E-12	471	—	ps	

Table 13. S8501 Receiver Timing Table

Parameter	Symbol	Min	Max	Units	Comments[1]
RCLK/N Frequency	f	74.24258	74.25743	MHz	
RCLK/N Period in lock		13.46667	13.46936	ns	In frequency lock.[2]
RCLK/N Out of lock period		13.308	13.58415	ns	Not in frequency lock.
RCLK/N Duty Cycle		40%	60%	period	In frequency lock.
RCLK to RCLKN Skew	t_3		1.0	ns	
RX Setup RCLK (rising edge)	t_4	1.55		ns	Provided setup time.
RX Setup RCLKN (falling edge)	t_6	1.55		ns	Provided setup time.
RX Hold RCLK (rising edge)	t_5	2.0		ns	Provided hold time.
RX Hold RCLKN (falling edge)	t_7	2.0		ns	Provided hold time.
RCLK/RCLKN Rise Time	t_r	0.40	2.4	ns	
RCLK/RCLKN Fall Time	t_f	0.7	3.0	ns	

1. All parameters are for outputs driven into a 15pF lumped capacitive load.
2. This is the absolute minimum RCLKN period while in frequency lock and must account for any adjustments to the clock to allow for a change in phase or frequency on the received serial link.

Figure 10. Receiver Timing Diagram

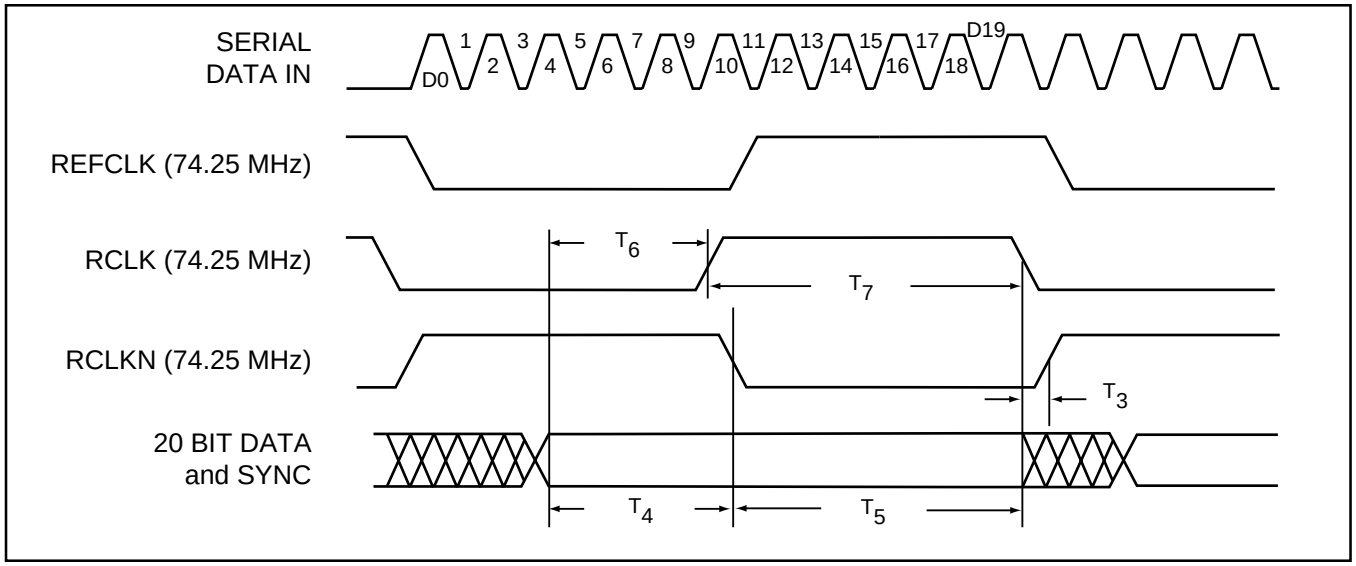


Figure 11. Serial Input Rise and Fall Time

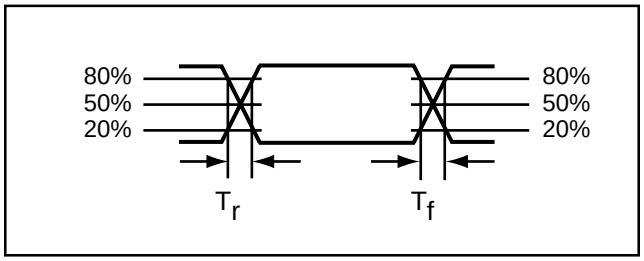


Figure 12. S8401 Serial Output Load

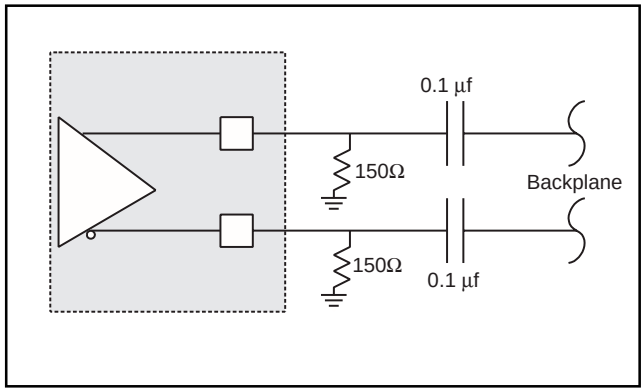


Figure 13. S8501 High Speed Differential Inputs

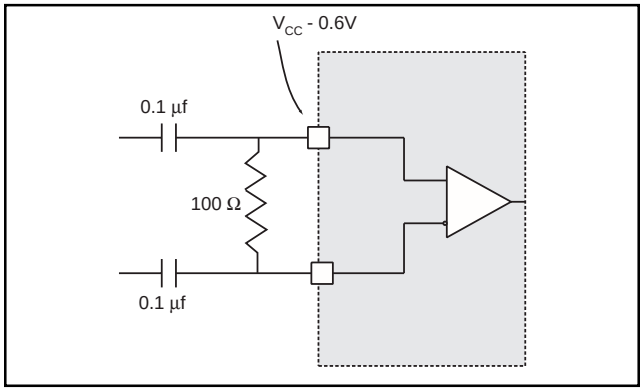


Figure 14. TTL Input Rise and Fall Time

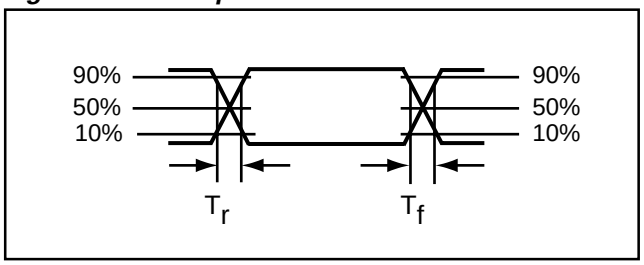


Figure 15. S8501 Receiver Input Eye Diagram Jitter Mask

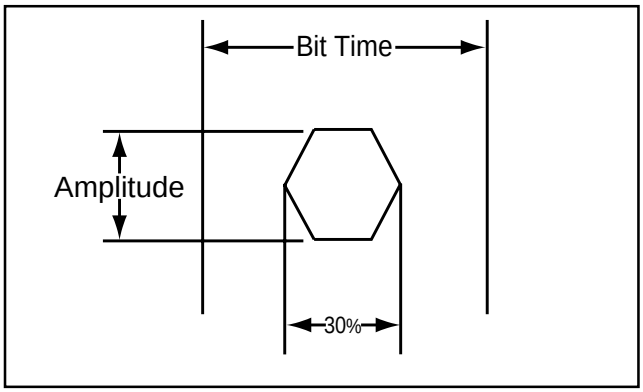
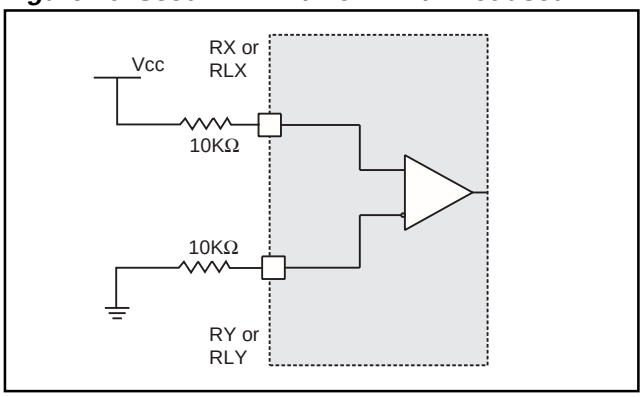


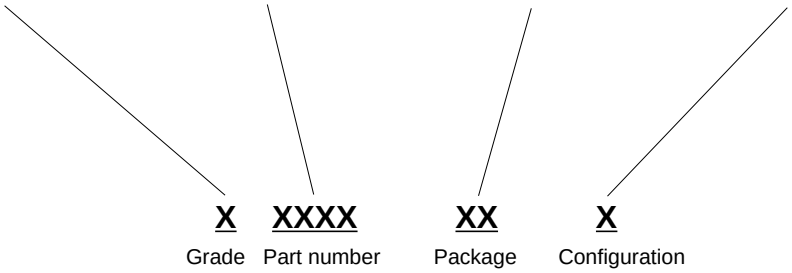
Figure 16. S8501 – If RY/X or RLY/X not used



Ordering Information

GRADE	TRANSMITTER	PACKAGE	SHIPPING CONFIGURATION
S – commercial	8401	QF = 52 PQFP	Blank = trays /D = dry pack /TD = tape, reel, and dry pack

GRADE	RECEIVER	PACKAGE	SHIPPING CONFIGURATION
S – commercial	8501	QF = 52 PQFP	Blank = trays /D = dry pack /TD = tape, reel, and dry pack



Example: S8401QF—S8401 in a 52 PQFP package shipped in trays.

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