S3092

DEVICE SPECIFICATION

SONET/SDH/ATM OC-192 1:16 Receiver with CDR and Postamp

FEATURES

- Silicon Germanium BiCMOS technology
- Complies with Telcordia, ITU-T, and G.709 specifications
- Integrated Phase Lock Loop
- OC-192 with FEC and Digital Wrapper (DW) (9.953 to 10.709 Gbps)
- Reference frequency of 155.52 MHz (or equivalent FEC or DW rate)
- 16-bit parallel, 622.08 Mbps (or equivalent FEC or DW rate) LVDS data path
- Lock detect
- Low jitter CML differential serial interface
- Dual +3.3 V and -5.2 V power supply
- Performs clock recovery for 9.953 Gbps (or equivalent FEC or DW rate) serial NRZ data
- Synthesizes parallel output clock during loss-of-signal conditions
- Postamp on serial input
- 148-pin CBGA package
- Typical power dissipation 2.2 W

APPLICATIONS

- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

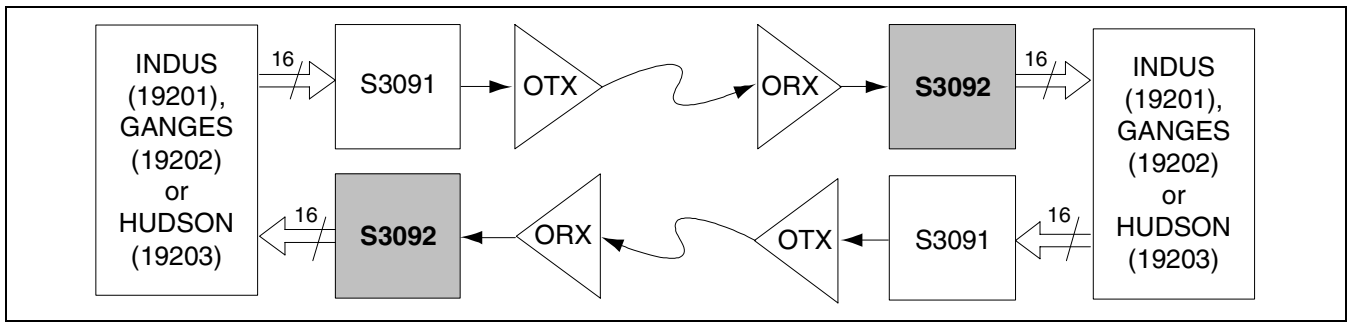
GENERAL DESCRIPTION

The S3092 SONET/SDH receiver chip is a fully integrated deserializer/CDR with SONET OC-192 with FEC and Digital Wrapper (9.953 Gbps to 10.709 Gbps) rate capability. The S3092 receives an OC-192 scrambled NRZ signal and recovers the clock from the data. The chip performs all necessary serial-to-parallel functions in conformance with SONET/SDH/Digital Wrapper transmission standards. The device is suitable for SONET-based ATM applications. Figure 1 shows a typical network application.

The S3092 is a fully integrated OC-192/STM-64 Clock and Data Recovery (CDR) and demultiplexer (DeMUX). The S3092 recovers a synchronous signal from the incoming 9.953 Gbps to 10.709 Gbps serial NRZ data stream and re-times and demultiplexes the serial data into 16 parallel 622.08 Mbps (or equivalent FEC or DW rate) lines. The IC detects a Loss-of-Signal condition, outputs a stable 622.08 MHz (or equivalent FEC or DW rate) clock when the serial data is lost, and provides 1:16 demultiplexing. It also has a limiting postamp on the serial input for small signal gain.

The chip can be used with a 155.52 MHz (or equivalent FEC or DW rate) reference clock. The low jitter LVDS interface guarantees compliance with the bit-error rate requirements of the Bellcore and ITU-T standards.

Figure 1. System Block Diagram



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SONET OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, forms a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

- Photonic
- Section
- Line
- Path

Figure 2 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Data Rates and Signal Hierarchy

Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-N signal is made up of N byte-interleaved STS-1 signals. The optical counterpart of each STS-N signal is an optical carrier level-N signal (OC-N). The chip supports OC-192 with FEC and Digital Wrapper (9.95328 Gbps to 10.709 Gbps) rates.

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for STS-192 consists of 576 transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 576 overhead and 16,704 SPE bytes is repeated nine times in each frame. Frame and byte boundaries are detected using the A1 and A2 bytes found in the transport overhead. (See Figure 3.) The S3092 does not provide A1/A2 detection or alignment to.

For more details on SONET operations, refer to the Bellcore SONET standard document.

Figure 2. SONET Structure

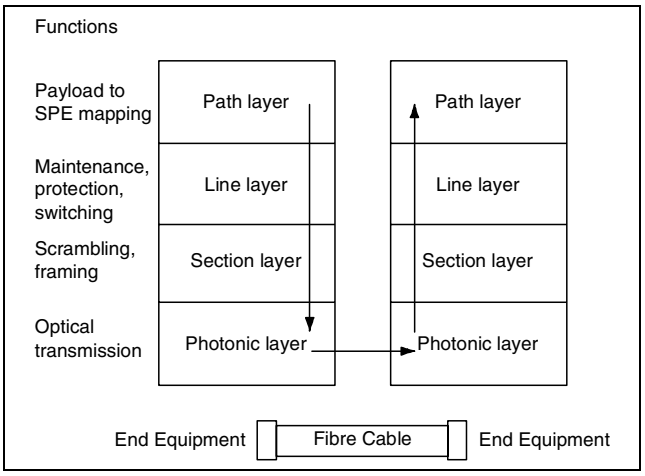
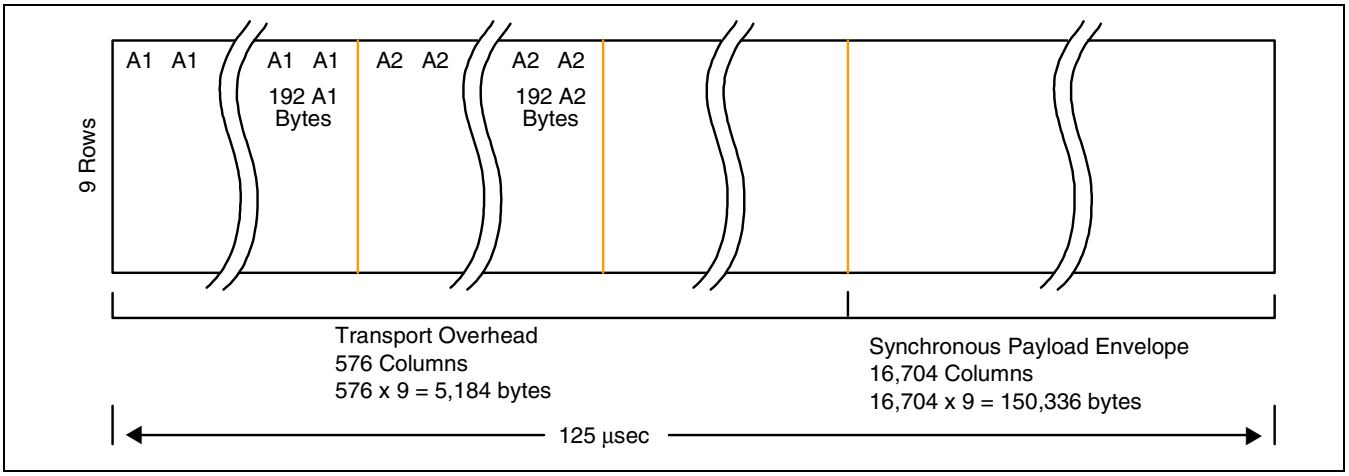


Table 1. SONET Signal Hierarchy

Elec.	ITU-T	Optical	Data Rate (Mbps)
STS-1		OC-1	51.84
STS-3	STM-1	OC-3	155.52
STS-12	STM-4	OC-12	622.08
STS-24	STM-8	OC-24	1244.16
STS-48	STM-16	OC-48	2488.32
STS-192	STM-64	OC-192	9953.28

Figure 3. STS-192 Frame Format



S3092 OVERVIEW

The S3092 CDR with DeMUX implements SONET/SDH deserialization functions. The block diagram in Figure 4 shows the basic operation of the chip. This chip can be used to implement the front end of the SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip includes clock and data recovery, serial-to-parallel conversion and system timing. The sequence of operations of the S3092 is as follows:

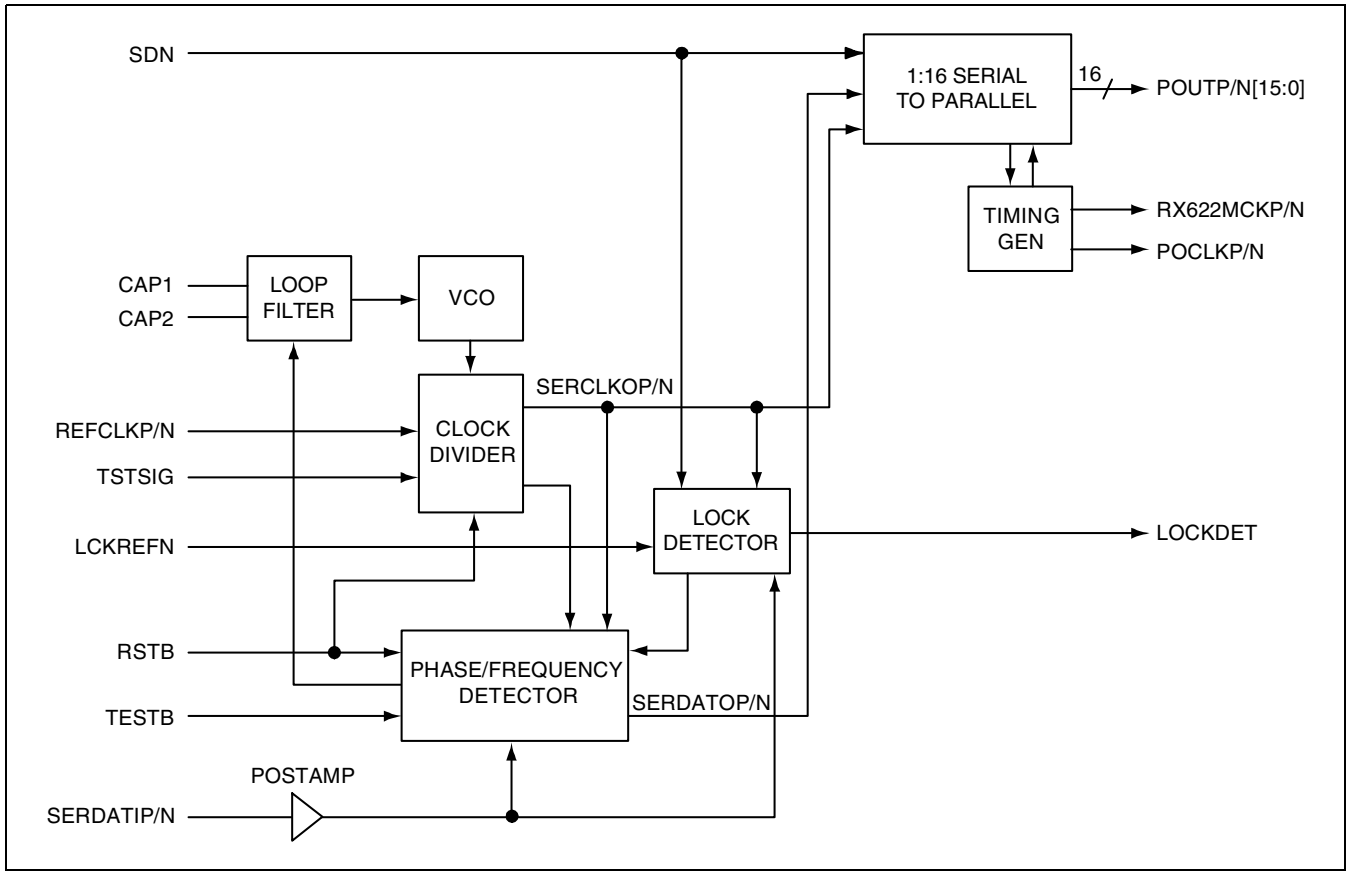
Receiver operations:

1. Serial input to limiting postamp
2. Clock and data recovery
3. Serial-to-parallel conversion
4. 16-bit parallel output

Suggested Interface Devices

AMCC	S3091	OC-192 Transmitter
AMCC	S19201	OC-192 to OC-48 MUX/DeMUX
AMCC	S19202	OC-192 SONET/SDH Mapper
AMCC	S3196	OC-192 Postamp
AMCC	S3090	OC-192 TIA
AMCC	S19203	OC-192 Digital Wrapper

Figure 4. Functional Block Diagram



S3092 ARCHITECTURE/FUNCTIONAL DESIGN

Receiver Description

The S3092 receiver chip provides the first stage of the digital processing of a receive SONET STS-192 bit-serial stream. It converts the bit-serial 9.953 Gbps to 10.709 Gbps data stream into a 622.08 Mbps to 669.33 Mbps 16-bit parallel data format. See Table 17 for Reference Clock (REFCLK) required.

Postamp

The S3092 limiting postamp takes the differential serial data from the SERDATIP/N pins and provides 36 dB small signal gain. The input to the postamp can be either AC or DC coupled.

Clock Recovery

Clock recovery, as shown in the block diagram in Figure 4, generates a clock that is the same frequency as the incoming data bit rate at the serial data input. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The Clock and Data Recovery (CDR) extracts a synchronous signal from the serial data input using a frequency and Phase Lock Loop (PLL). The PLL consists of a Voltage Controlled Oscillator (VCO), Phase/Frequency Detectors (PFD), and a loop filter.

The frequency detector ensures predictable lock-up conditions. It is used during acquisition, and serves as a means of pulling the VCO into the range of the data rate where the phase detector is capable of acquiring lock.

The phase detector used in the CDR is designed to give minimum static phase error of the PLL. When a transition has occurred, the value of the sample in the vicinity of the transition indicates whether the VCO clock leads or lags the incoming data. The phase detector then produces a binary output accordingly.

When a loss-of-signal condition exists, SDN goes inactive, and the PLL locks onto the Reference Clock (REFCLK) to provide a steady output clock. There are two pins (CAP1 and CAP2) to connect the external capacitors and resistors in order to adjust the PLL loop performance.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal.

The total loop dynamics of the clock recovery PLL yield a jitter tolerance that exceeds the minimum tolerance proposed for SONET equipment by the Bellcore TA-NWT-000253 standard.

Lock Detect

The S3092 contains a lock detect circuit that monitors the integrity of the serial data inputs. If the received serial data fails the frequency test, the PLL will be forced to lock to the local reference clock. This will maintain the correct frequency of the recovered clock output under loss-of-signal or loss-of-lock conditions. If the recovered clock frequency deviates from the local reference clock frequency by more than the typical value stated in Table 6, the PLL will be declared out of lock. The lock detect circuit will poll the input data stream in an attempt to reacquire lock to data. If the recovered clock frequency is determined to be within the typical value stated in Table 6, the PLL will be declared in lock, and the lock detect output will go active. An inactive SDN will also cause an out-of-lock condition.

Serial-to-Parallel Converter

The serial-to-parallel converter consists of three 16-bit registers. The first is a serial-in, parallel-out shift register, which performs serial to parallel conversion. The second is a 16-bit internal holding register, which transfers data from the serial to parallel register. On the falling edge of the POCLK, the data in the holding register is transferred to an output holding register which drives POUTP/N[15:0].

Power Sequencing

In order to avoid latch up, it is required that the -5.2 V power be applied to the S3092 for a minimum of 50 ms before the application of 3.3 V power.

Table 2. Input Pin Description and Assignment

Pin Name	Level	I/O	Pin #	Description
SERDATIP SERDATIN	Diff.CML	I	G1 J1	Receive Serial Data Input. Differential high frequency serial data input to limiting postamp for small signal gain. Use Coplanar Waveguide Structure for best results. See Layout Recommendation application note. See Characterization Report for S_{11} plot. See Characterization Report for Differential Input Voltage vs. BER plot.
REFCLKP REFCLKN	Diff.ECL	I	B1 C1	Reference Clock. Differential reference clock input at 155.52 MHz. The PLL will lock onto this reference in the absence of serial input data. Internally biased and terminated.
CAP1 CAP2	Analog	I	B4 C4	Loop Filter Capacitors. The external loop filter capacitor and resistors are connected to these pins. Used to adjust the loop filter performance. See Figure 12.
LCKREFN	LVTTL	I	C14	Lock to Reference. Active Low. When active, the PLL will be forced to lock to the local reference clock input [REFCLK]. RX622MCK remains locked to the VCO.
SDN	ECL	I	A9	Signal Detect. Active Low. A single-ended 10K ECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDN is inactive, the data on the Serial Data In (SERDATIP/N) pins will be internally forced to a constant zero, and the PLL will be forced to lock to the REFCLK inputs. When SDN is active, data on the SERDATIP/N pins will be processed normally. If not used, leave open.
RSTB	LVTTL	I	A7	Master Reset. Active Low. Reset input for the device. For correct reset, this input must be asserted Low for 100 ns.
TESTB	LVTTL	I	C6	Test Enable. Active Low. Used during production test to bypass the VCO in the PLL. Pull High for normal operation.
TSTSIG	LVTTL	I	A6	Test Input Signal. Active Low. Signal used for production test. Pull High for normal operation.

Table 3. Output Pin Description and Assignment

Pin Name	Level	I/O	Pin #	Description
POCLKP POCLKN	LVDS	O	B10 B9	Parallel Clock Output. Regenerated 622.08 MHz (or equivalent FEC or DW rate) differential output clock, synchronized to the parallel output data (see Figure 7). Note that in order to comply with Optical Internetworking Forum (OIF) specifications, POCLKP and POCLKN should be exchanged on the module board.
POUTP0 POUTN0 POUTP1 POUTN1 POUTP2 POUTN2 POUTP3 POUTN3 POUTP4 POUTN4 POUTP5 POUTN5 POUTP6 POUTN6 POUTP7 POUTN7 POUTP8 POUTN8 POUTP9 POUTN9 POUTP10 POUTN10 POUTP11 POUTN11 POUTP12 POUTN12 POUTP13 POUTN13 POUTP14 POUTN14 POUTP15 POUTN15	LVDS	O	N2 N3 P3 P4 N4 N5 P5 P6 N6 N7 P7 P8 N8 N9 P9 P10 M11 M12 N12 N13 N14 M14 L13 K13 K14 J14 H14 G14 G13 F13 F14 E14	Parallel Data Output. Re-timed data from the DeMUX at a rate of 622.08 Mbps (or equivalent FEC or DW rate). Bit 15 is the first bit received. POUTP/N[15] is the most significant bit (corresponding to bit 1 of each word, the first bit transmitted). POUTP/N[0] is the least significant bit corresponding to bit 16 of each word, the last bit transmitted).
LOCKDET	LVTTL	O	C12	Lock Detect. Clock recovery indicator. Active High. Set High when the internal clock recovery has locked onto the incoming data stream after an internal delay. LOCKDET is an asynchronous output.
RX622MCKP RX622MCKN	LVDS	O	B11 A11	622.08 MHz (or equivalent FEC or DW rate) clock output. This clock is derived from the VCO clock.

Table 4. Common Pin Description and Assignment

Pin Name	Level	Pin Number	Description
VCCDIG	+3.3 V	M9	Digital V_{CC}
VCCLVDS	+3.3 V	C9, H13, M3, M6, M13	LVDS V_{CC}
DGND	GND = 0 V	A8, A10, A13, A14, B7, B14, C10, E13, L14, M4, M7, M10, N1, N10, P1, P2, P11, P12, P13, P14	Digital Ground
VCCLVTTL	+3.3 V	C7, C13	LVTTL V_{CC}
NC		A12	Not Connected
AGND	GND = 0 V	A1, A2, A4, B2, B3, B5, B6, C2, C3, C5, D2, D14, E1, F1, F2, H1, H2, K1, K2, L1, M1	Analog Ground
AVEE	-5.2 V	E2, L2, M2	Analog V_{EE}
VEEDIG	-5.2 V	B8, B12, B13, C8, D13, J13, M5, M8, N11	Digital V_{EE}
THERMALGND	GND = 0 V	E6, E7, E8, E9, E10, F5, F6, F7, F8, F9, F10, G5, G6, G7, G8, G9, G10, H5, H6, H7, H8, H9, H10, J5, J6, J7, J8, J9, J10, K5, K6, K7, K8, K9, K10	Thermal Grounds
VEE_FILTER	-5.2 V	A3	Analog V_{EE} for Filter
VEE_VCO	-5.2 V	A5	Analog V_{EE} for VCO
VEE_REFCLK	-5.2 V	D1	Analog V_{EE} for REFCLK

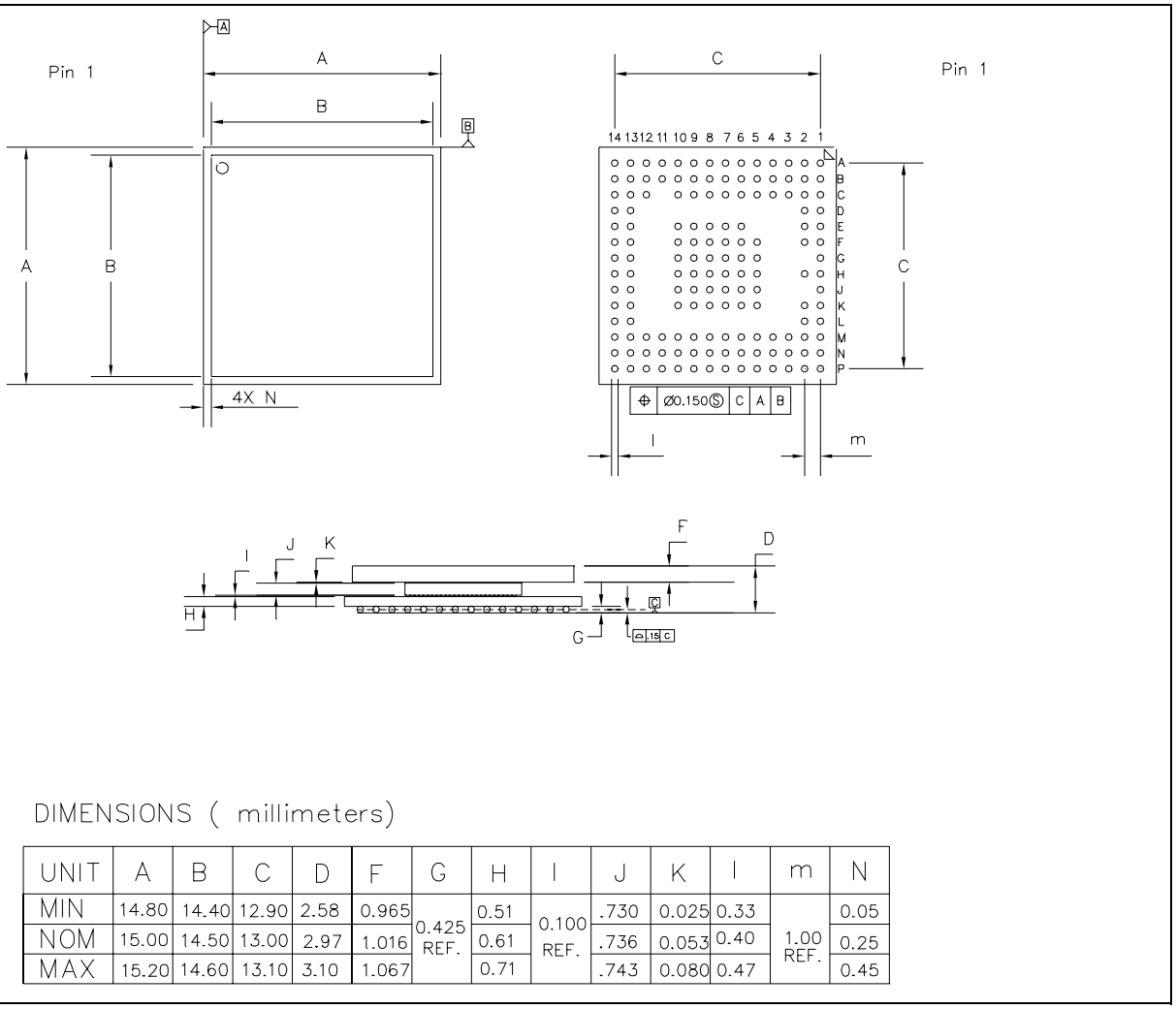
Note: All digital, analog, and thermal grounds are connected together on the package.

Figure 5. S3092 Pinout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	AGND	AGND	VEE FILTER	AGND	VEE VCO	TSTSIG	RSTB	DGND	SDN	DGND	RX622MCKN	NC	DGND	DGND
B	REFCLKP	AGND	AGND	CAP1	AGND	AGND	DGND	VEEDIG	POCLKN	POCLKP	RX622MCKP	VEEDIG	VEEDIG	DGND
C	REFCLKN	AGND	AGND	CAP2	AGND	TESTEN	VCCLVTTL	VEEDIG	VCCLVDS	DGND		LOCKDET	VCCLVTTL	LCKREFN
D	VEE REFCLK	AGND											VEEDIG	AGND
E	AGND	AVEE				THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND			DGND	POUT15N
F	AGND	AGND			THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND			POUT14N	POUT15P
G	SERDATIP				THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND			POUT14P	POUT13N
H	AGND	AGND			THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND			VCCLVDS	POUT13P
J	SERDATIN				THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND			VEEDIG	POUT12N
K	AGND	AGND			THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND			POUT11N	POUT12P
L	AGND	AVEE											POUT11P	DGND
M	AGND	AVEE	VCCLVDS	DGND	VEEDIG	VCCLVDS	DGND	VEEDIG	VCCDIG	DGND	POUT8P	POUT8N	VCCLVDS	POUT10N
N	DGND	POUT0P	POUT0N	POUT2P	POUT2N	POUT4P	POUT4N	POUT6P	POUT6N	DGND	VEEDIG	POUT9P	POUT9N	POUT10P
P	DGND	DGND	POUT1P	POUT1N	POUT3P	POUT3N	POUT5P	POUT5N	POUT7P	POUT7N	DGND	DGND	DGND	DGND

S3092
(Package TOP View)
(Die BOTTOM View)

Figure 6. S3092 Package



DIMENSIONS (millimeters)

UNIT	A	B	C	D	F	G	H	I	J	K	I	m	N
MIN	14.80	14.40	12.90	2.58	0.965	0.425 REF.	0.51	0.100 REF.	.730	0.025	0.33	1.00 REF.	0.05
NOM	15.00	14.50	13.00	2.97	1.016		0.61		.736	0.053	0.40		0.25
MAX	15.20	14.60	13.10	3.10	1.067		0.71		.743	0.080	0.47		0.45

Table 5. Thermal Management

Device	Package Max Power (70°C Ambient)	Θja	Θjc
S3092	2.68 W	20.5 °C/W	3.0 °C/W

Note: See Application Note for simulation results, thermal management suggestions, and thermal profile for package attachment.

Table 6. Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
Nominal VCO Center Frequency	9.953		10.709	GHz	
Reference Clock Frequency Tolerance	-100		+100	ppm	± 20 ppm is required to meet SONET output frequency specification.
SERDATIP/N Input Return Loss (S_{11}) (when driven differentially)			-10	dB	DC – 10 GHz
Capture Range	-220		+220	ppm	With respect to fixed reference frequency.
Acquisition Lock Time		16	25	µsec	Minimum transition density of 50%. Guaranteed but not tested. With device already powered up and valid REFCLK.
Reference Clock Input Duty Cycle	40		60	% of UI	
Reference Clock Rise and Fall Times	0.2		0.8	ns	20% to 80% of amplitude.
Frequency difference at which the PLL goes out of lock (REFCLK compared to the divided down VCO clock).	440	600	732	ppm	
Frequency difference at which receive PLL goes into lock (REFCLK compared to the divided down VCO clock).	220	300	366	ppm	

Table 7. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-55		150	°C
V_{CC} 3.3 V Supply	-0.5		3.6	V
V_{EE} -5.2 V Supply	0.5		-7.0	V
LVTTL Input Voltage	-0.5		V_{CC} + 0.5	V
LVTTL Output Voltage	-0.5		V_{CC} + 0.5	V
LVDS Output Voltage	0		V_{CC}	V
ECL Input Voltage	V_{EE} - 0.25		AGND	V
CML Input Voltage	V_{EE} - 0.25		AGND	V
LVTTL Input Current per pin	-450		1000	µA
LVTTL Output Current per pin			2	mA

Electrostatic Discharge (ESD) Ratings

The S3092 is rated to the following voltages based on the human body model:

1. All pins are rated at 100 Volts.

Standards for ESD protection should be adhered to when handling the devices to ensure that they are not damaged. The standards to be used are defined in ANSI standard ANSI/ESD S20.20-1999, “Protection of Electrical and Electronic Parts, Assemblies and Equipment.” Contact your local FAE or sales representative for ESD application notes.

Table 8. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias (Commercial)	0		+70	°C
Junction Temperature Under Bias	40		125	°C
Voltage on V_{CC} with Respect to GND	3.135	3.3	3.465	V
Voltage on V_{EE} with Respect to GND	-4.94	-5.2	-5.46	V
I_{CC} Supply Current, includes bias resistors		320	375	mA
I_{EE} Supply Current		230	275	mA

Table 9. Internally Biased Differential CML Input DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Comments
ΔV_{INDIFF}	Differential Input Voltage Swing	15		1400	mV	See Figure 13.
$\Delta V_{INSINGLE}$	Single-Ended Input Voltage Swing (while driven differentially)	7.5		700	mV	See Figure 13.
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	
V_{IH}	Input High Voltage			AGND - 0.2	V	
V_{IL}	Input Low Voltage	AGND - 2.0			V	

Table 10. Single-Ended ECL Input DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IL}	ECL Input Low Voltage	AGND - 2		AGND - 1.4	V	
V_{IH}	ECL Input High Voltage	AGND - 1.225		AGND - 0.525	V	

Table 11. LVDS Output DC Characteristics[1, 2] (See Figure 9)

Symbol	Description	Min	Typ	Max	Unit	Conditions
V_{OH}	Output High Voltage	1.25		1.8	V	Output loading is 100 Ω line-to-line. Over process, voltage and temperature range.
V_{OL}	Output Low Voltage	0.85		1.4	V	Output loading is 100 Ω line-to-line. Over process, voltage and temperature range.
$V_{OUTDIFF}$	Output Differential Voltage	500	740	1100	mV	Output loading is 100 Ω line-to-line. Over process, voltage and temperature range.
$V_{OUTSINGLE}$	Output Single-ended Voltage	250	370	550	mV	Output loading is 100 Ω line-to-line. Over process, voltage and temperature range.

1. Output loading in 100 Ω line-to-line.
2. 330 Ω pull-down resistor per line to ground.

Table 12. LVTTL Input DC Characteristics

Symbol	Description	Min	Typ	Max	Unit	Conditions
V_{IH}	Input High Voltage	2.0		3.47	V	LVTTL V_{CC} = Max
V_{IL}	Input Low Voltage	0.0		0.8	V	LVTTL V_{CC} = Min
I_{IH}	Input High Current			50	µA	V_{IN} = 2.4 V
I_{IL}	Input Low Current	-500			µA	V_{IN} = 0.5 V

Table 13. LVTTL Output DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Condition
V_{OH}	Output High Voltage	2.4			V	V_{CC} = Min I_{OH} = -30 µA
V_{OL}	Output Low Voltage			0.5	V	V_{CC} = Min I_{OL} = 1 mA

Table 14. AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
J_{TOL}	Jitter Tolerance			15	UI (p-p)	10 Hz - 2.4 kHz (Sinusoidal). See Figure 14.
				15/(f ÷ 2400)	UI (p-p)	2.4 kHz - 24 kHz (Sinusoidal). See Figure 14.
				1.5	UI (p-p)	24 kHz - 400 kHz (Sinusoidal). See Figure 14.
				15/(f ÷ 400 x 10^3)	UI (p-p)	400 kHz - 4 MHz (Sinusoidal). See Figure 14.
				0.15	UI (p-p)	4 MHz - 1 GHz (Sinusoidal). See Figure 14.
L_{CID}	Consecutive Identical Digits RX622MCK			80	bits	Number of bits with no transitions.
C_{DUTY}	POCLKP/N / RX622MCKP/N Duty Cycle	47		53	%	100 Ω line-to-line, SONET spec is 45/55.
T_{TLH}	POCLKP/N Rise Time	100		250	ps	20% – 80%, 100 Ω line-to-line.
	POUTP/N Rise Time	100		250		
T_{THL}	POCLKP/N Fall Time	100		250	ps	20% – 80%, 100 Ω line-to-line.
	POUTP/N Fall Time	100		250		
T_{PD}	POUTP/N Delay from POCLKP/N	600		1000	ps	See Figure 7.
T_{SU}	POCLKP/N to POUTP/N	600			ps	See Figure 7.
T_H	POCLKP/N to POUTP/N	600			ps	See Figure 7.
T_{CQ_MIN} T_{CQ_MAX}	Data Invalid Window with respect to Falling Edge of POCLKP.			200	ps	See Figure 8.
t_{pw}	RSTB Minimum Pulse Width[1]	100			ns	

1. Guaranteed by design.

Table 15. Internally Biased Differential ECL Input DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Comments
ΔV_{INDIFF}	Differential Input Voltage Swing	300		1600	mV	See Figure 13.
$\Delta V_{INSINGLE}$	Single-ended Input Voltage Swing	150		800	mV	See Figure 13.
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	
V_{IH}	Input High Voltage			AGND - 0.2	V	
V_{IL}	Input Low Voltage	AGND - 2.0			V	

Table 16. External Loop Filter Components

Symbol	Description	Value	Unit
R_1, R_2	Resistor, Surface Mount, 0402	10	Ω
C_2	Capacitor, Surface Mount, 0603 or larger	1	µF

Figure 7. Parallel Data Output Delay from POCLK

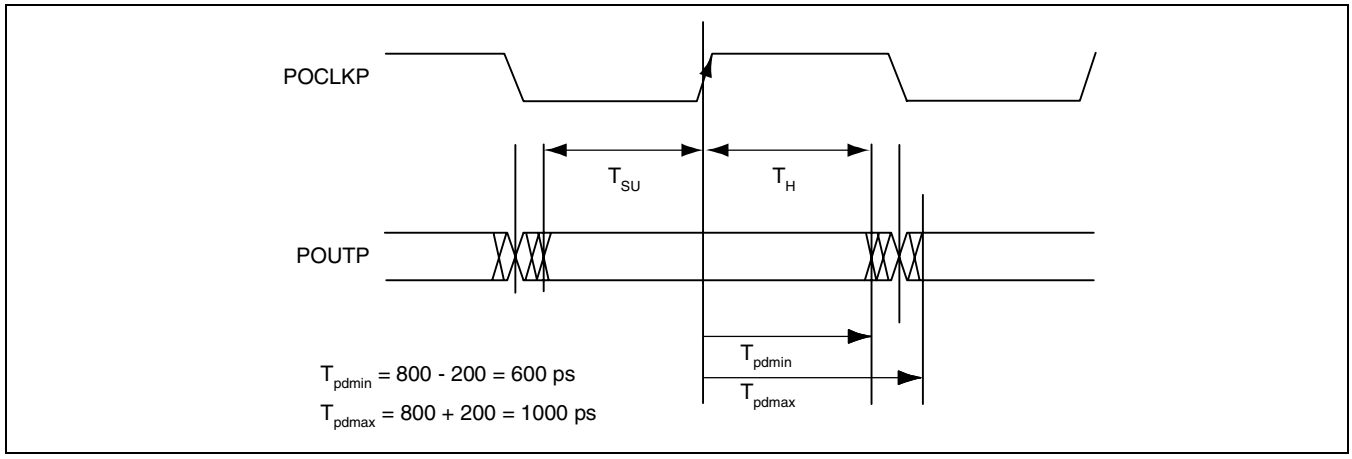
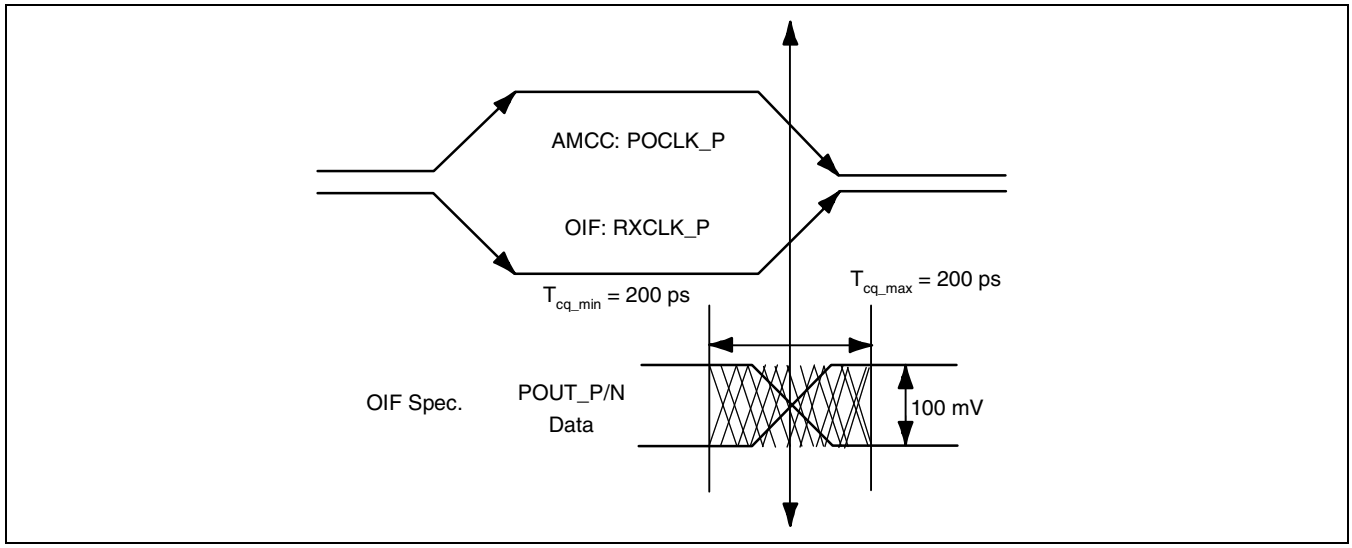


Figure 8. Data Invalid Window



Note: See OIF Specs for SERDES outputs.

Table 17. FEC Modes

Error Correcting Capability	Code Rate Showing Bandwidth Expansion Due to Code Words and FSB	Increased SERDATIN Frequency	Increased Input Clock (REFCLK) Frequency
0 bytes per 255-byte block	0% Increase	9.953 Gbps	155.52 MHz
3 bytes per 255-byte block	2.82% Increase	10.234 Gbps	159.90 MHz
4 bytes per 255-byte block	3.66% Increase	10.317 Gbps	161.21 MHz
5 bytes per 255-byte block	4.51% Increase	10.402 Gbps	162.53 MHz
6 bytes per 255-byte block	5.37% Increase	10.488 Gbps	163.87 MHz
7 bytes per 255-byte block	6.25% Increase	10.575 Gbps	165.24 MHz
8 bytes per 255-byte block	7.14% Increase	10.664 Gbps	166.62 MHz
Digital Wrapper (OTU2)	7.59% Increase	10.709 Gbps	167.32 MHz

Figure 9. S3092 LVDS Driver to LVDS Input, Reference Only

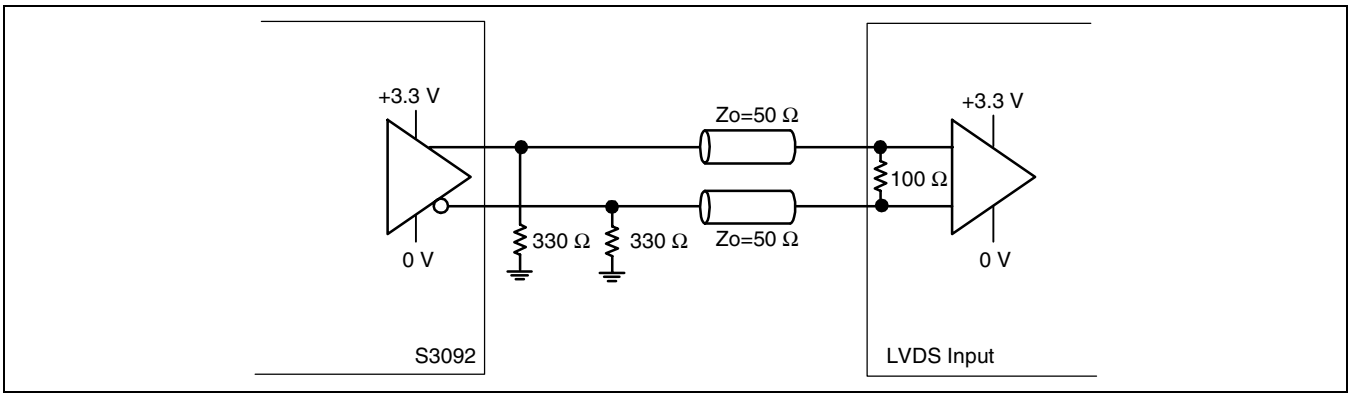


Figure 10. -5.2 V ECL Post Amp to S3092 Input DC Coupled Termination, Reference Only

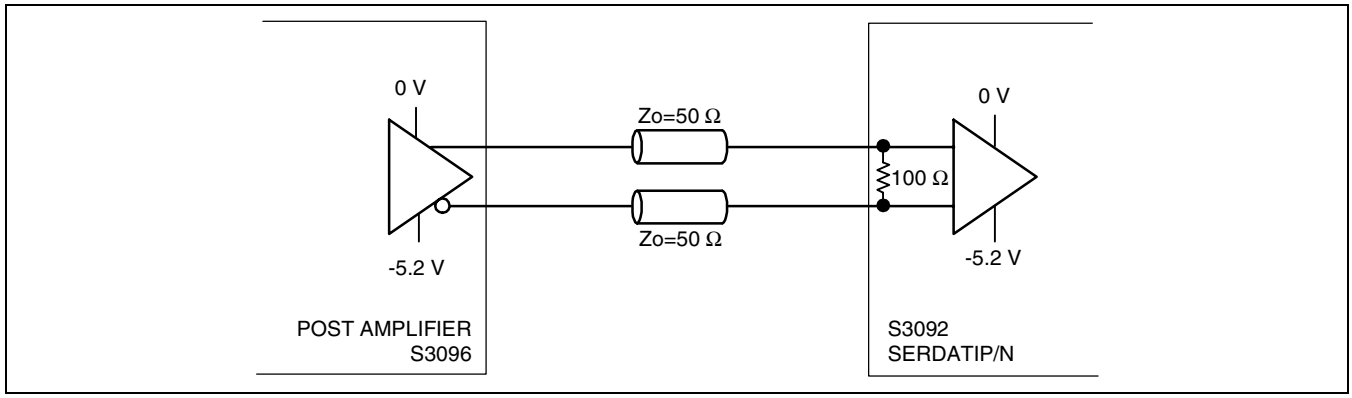


Figure 11. -5.2 V ECL Post Amp to S3092 Input AC Coupled Termination, Reference Only

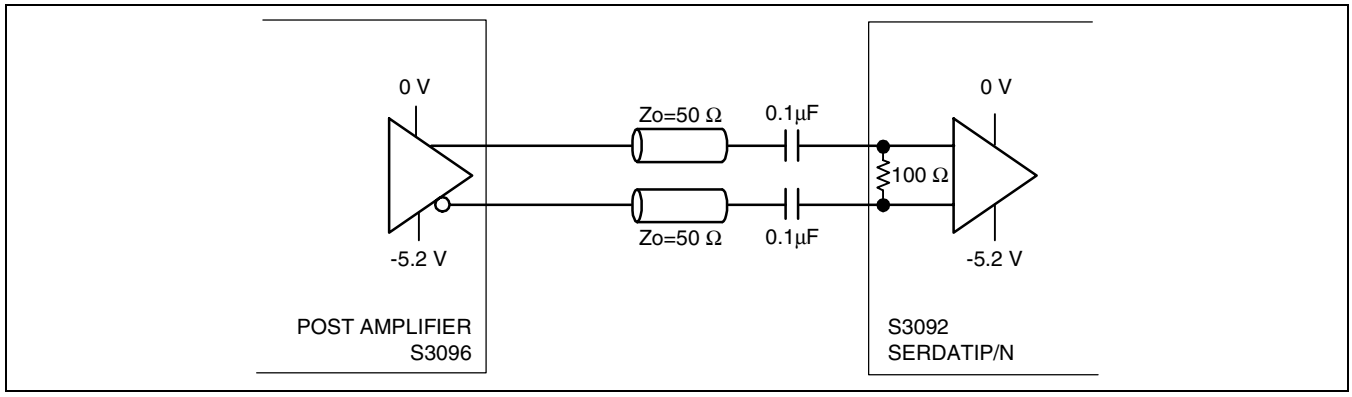


Figure 12. External Loop Filter

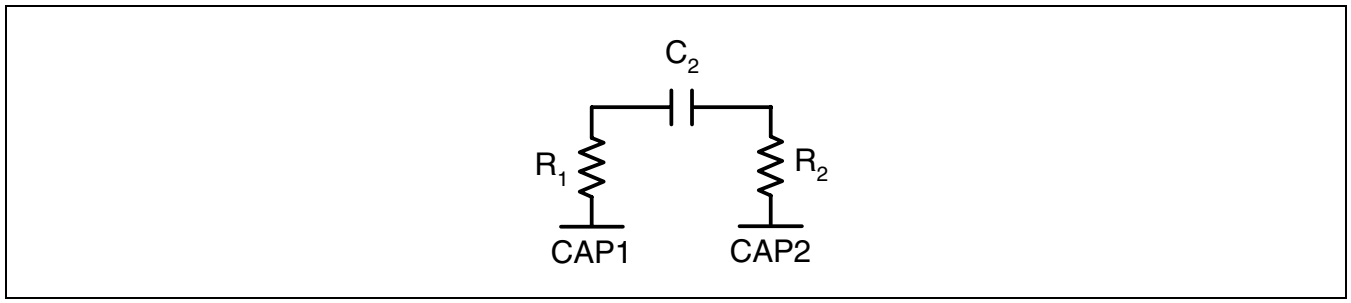


Figure 13. Differential Voltage Measurement

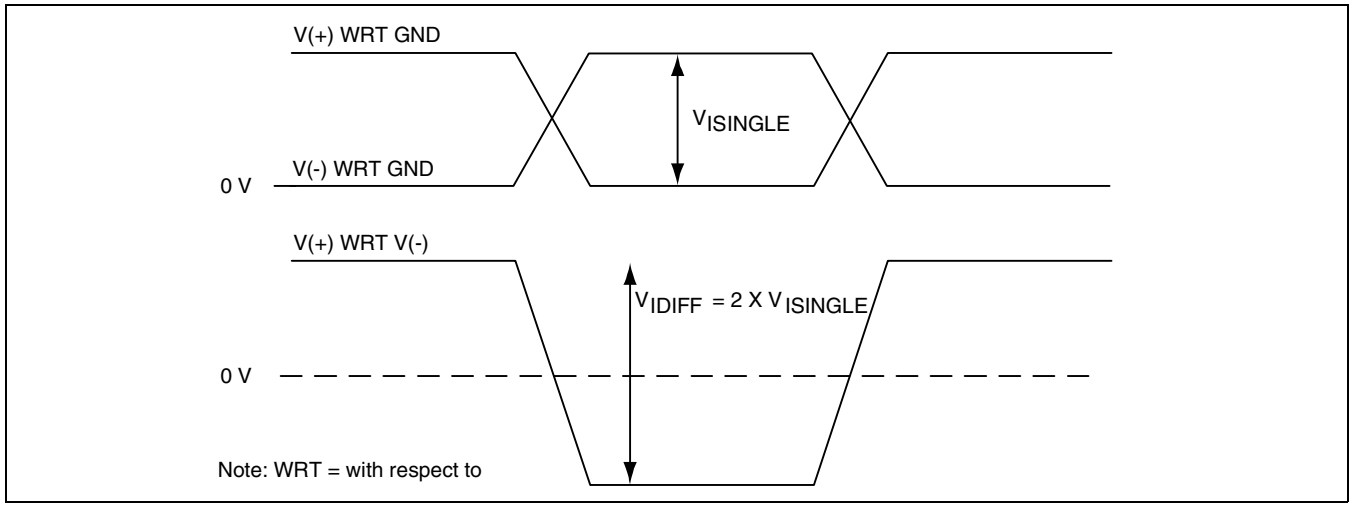
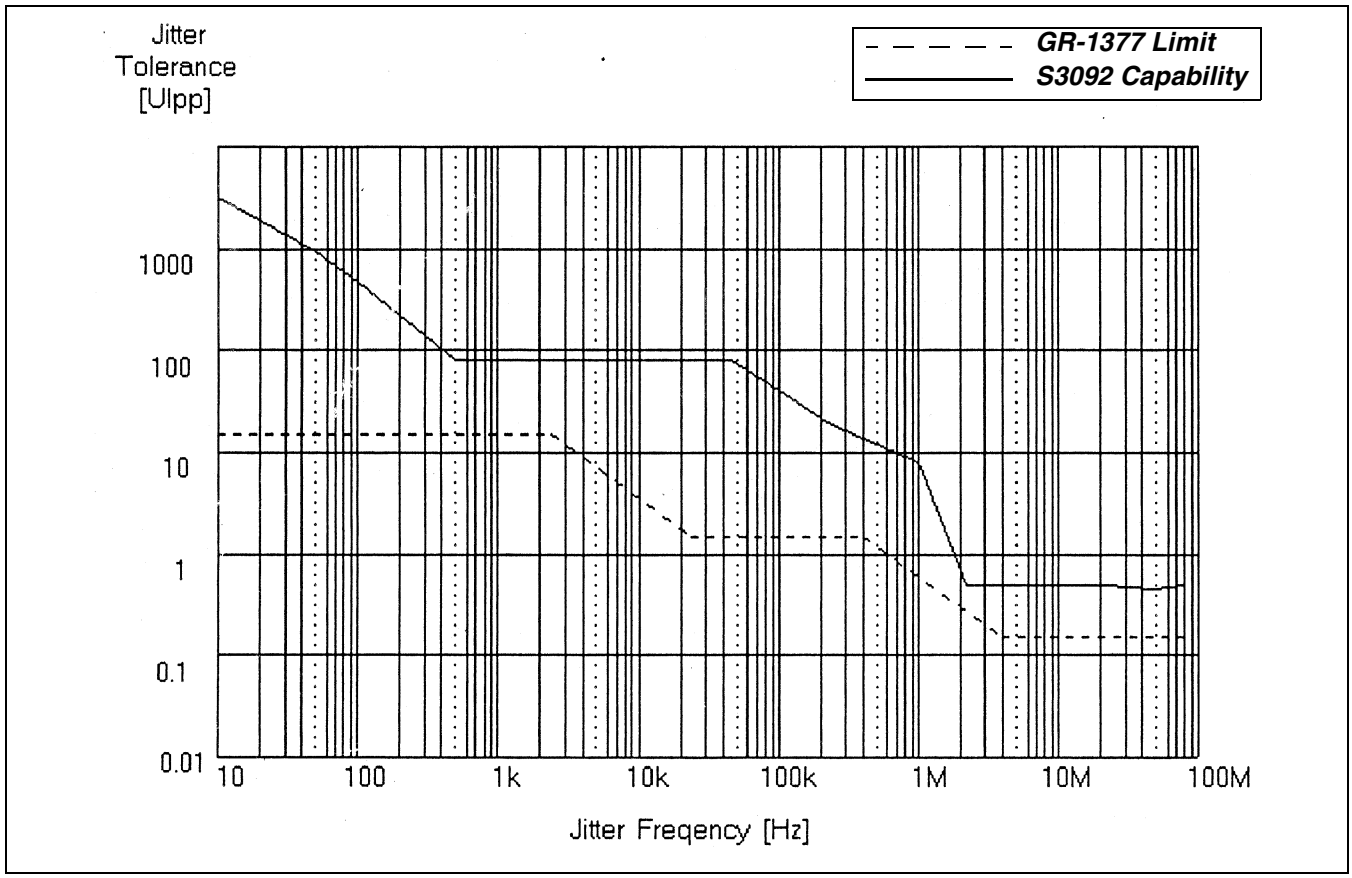
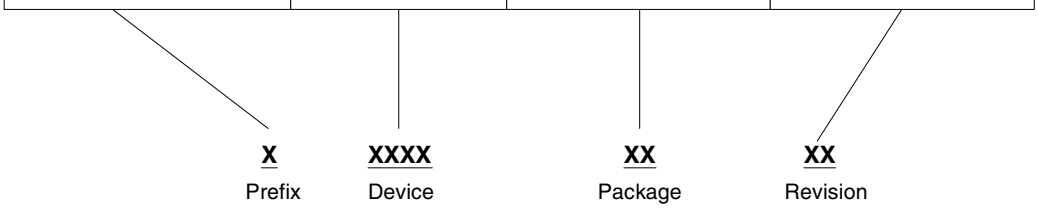


Figure 14. Jitter Tolerance UIpp



Ordering Information

Prefix	Device	Package	Revision
S - Integrated Circuit	3092	CB - 148 CBGA	20



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