

S3091

SONET/SDH/ATM OC-192 16:1 Transmitter

DEVICE SPECIFICATION

FEATURES

- Silicon Germanium BiCMOS technology
- Complies with Telcordia, ITU-T, and G.709 specifications
- On-chip high-frequency PLL for clock generation
- OC-192 with FEC and Digital Wrapper (DW) (9.953 to 10.709 Gbps)
- Reference frequency of 155.52 or 622.08 MHz (or equivalent FEC or DW rate)
- 16-bit parallel, 622.08 Mbps LVDS data path
- Lock detect/Phase error indicator
- Low jitter CML differential or single-ended serial interface
- Dual +3.3 V and -5.2 V power supply
- Supports line timing
- Internal FIFO to decouple transmit clocks
- 311.04 MHz or 622.08 MHz parallel input clock
- Programmable skew on 311.04 MHz parallel clock mode
- 148-pin CBGA package
- Typical power dissipation 2.3 W

APPLICATIONS

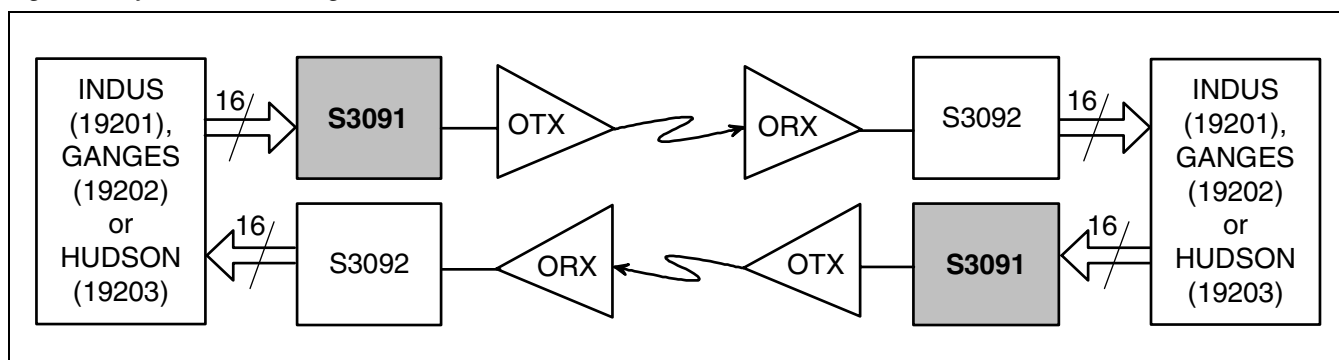
- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

GENERAL DESCRIPTION

The S3091 SONET/SDH MUX chip is a fully integrated serializer with SONET OC-192 with FEC and Digital Wrapper (9.953 to 10.709 Gbps) rate capability. The chip performs all necessary parallel-to-serial functions in conformance with SONET/SDH/Digital Wrapper transmission standards. The device is suitable for SONET-based ATM applications. Figure 1 shows a typical network application.

On-chip clock synthesis PLL components are contained in the S3091 MUX chip, allowing the use of a slower external transmit clock reference. The chip can be used with a 155.52 or 622.08 MHz reference clock (or equivalent FEC or DW rate), in support of existing system clocking schemes.

Figure 1. System Block Diagram



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SONET OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, forms a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

- Photonic
- Section
- Line
- Path

Figure 2 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Data Rates and Signal Hierarchy

Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal, referred to as the synchronous transport signal level-1 (STS-1). An STS-N signal is made up of N byte-interleaved STS-1 signals. The optical counterpart of each STS-N signal is an optical carrier level-N signal (OC-N). The chip supports OC-192 with FEC and Digital Wrapper (9.95328 to 10.709 Gbps) rates.

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for STS-192 consists of 576 transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 576 overhead and 16,704 SPE bytes is repeated nine times in each frame. Frame and byte boundaries are detected using the A1 and A2 bytes found in the transport overhead. (See Figure 3.)

For more details on SONET operations, refer to the Bellcore SONET standard document.

Figure 2. SONET Structure

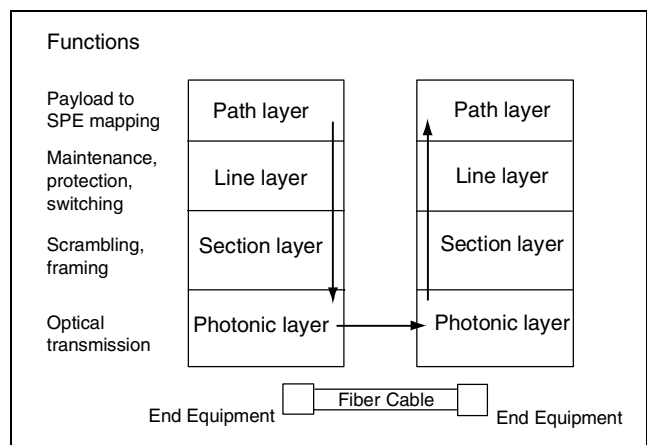
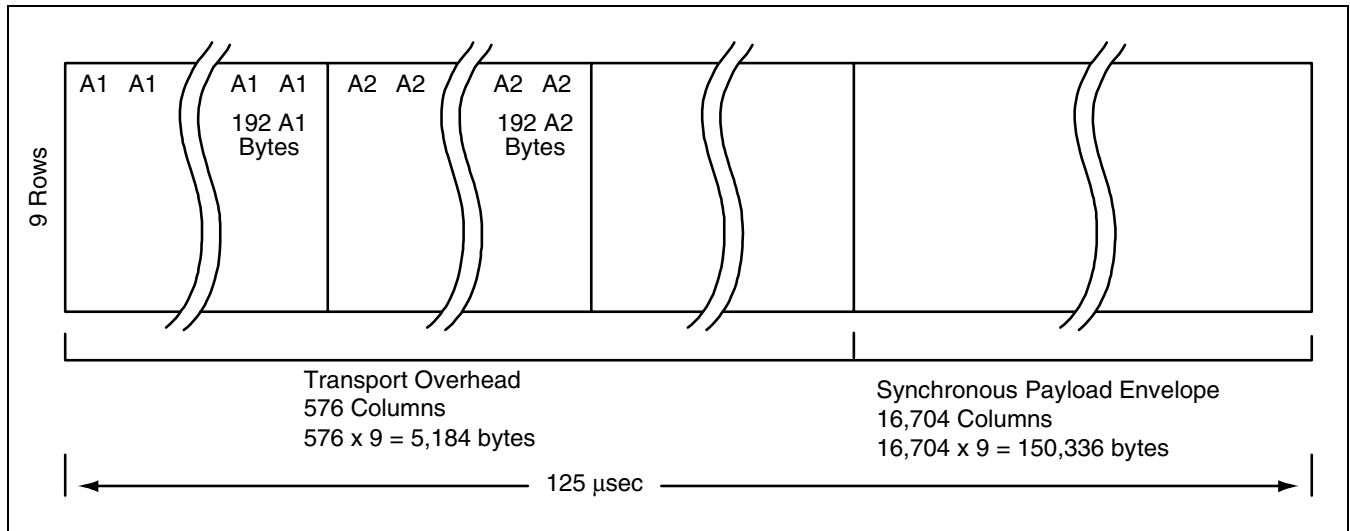


Table 1. SONET Signal Hierarchy

| Elec. | ITU-T | Optical | Data Rate (Mbps) |
|---------|--------|---------|------------------|
| STS-1 | | OC-1 | 51.84 |
| STS-3 | STM-1 | OC-3 | 155.52 |
| STS-12 | STM-4 | OC-12 | 622.08 |
| STS-24 | STM-8 | OC-24 | 1244.16 |
| STS-48 | STM-16 | OC-48 | 2488.32 |
| STS-192 | STM-64 | OC-192 | 9953.28 |

Figure 3. STS-192 Frame Format



S3091 OVERVIEW

The S3091 transmitter implements SONET/SDH serialization and transmission functions. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip includes parallel-to-serial conversion and system timing. The system timing circuitry consists of a high-speed phase detector, clock dividers, and clock distribution throughout the front end.

The sequence of transmitter operations is as follows:

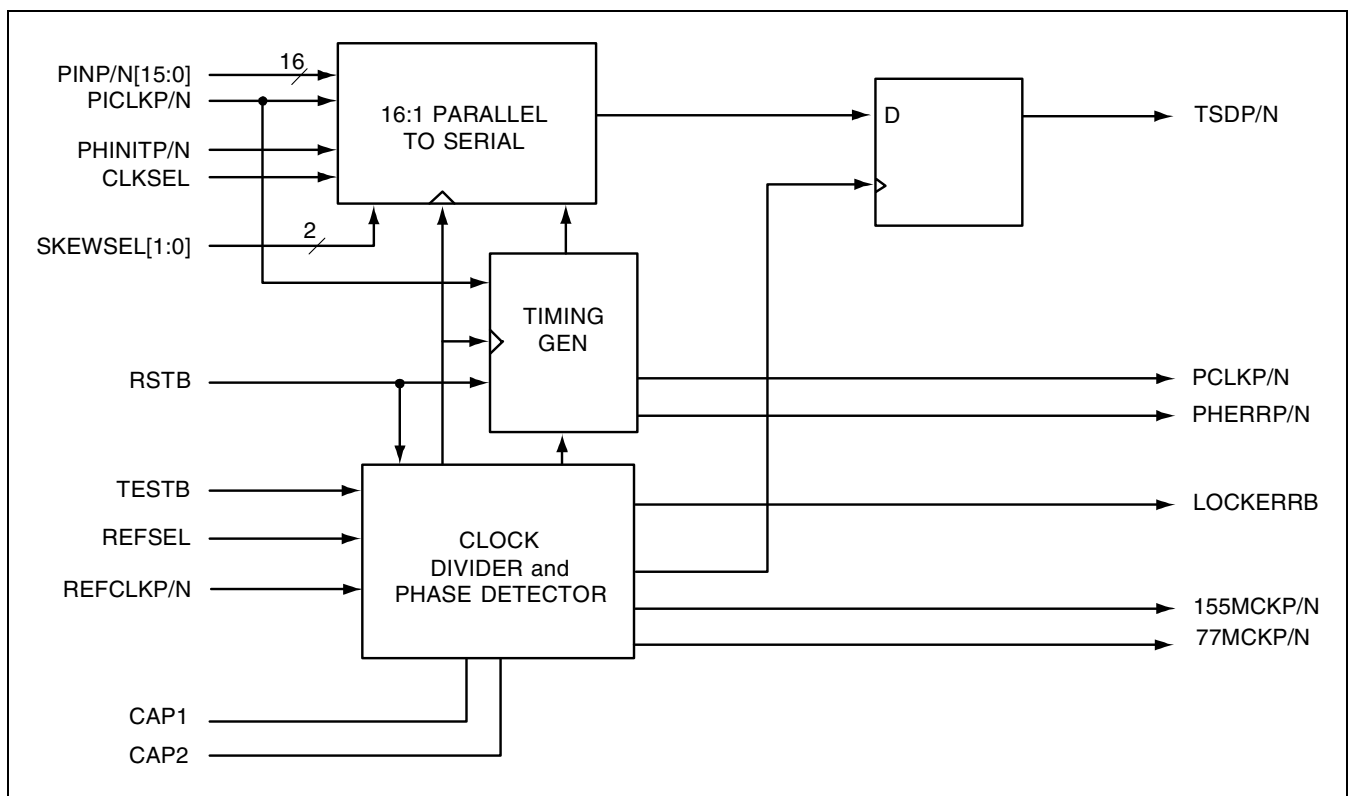
1. 16-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figures 7 and 8.

Suggested Interface Devices

| | | |
|------|-------|---------------------------|
| AMCC | S3092 | OC-192 CDR+DeMUX |
| AMCC | 19201 | OC-192 to OC-48 MUX/DeMUX |
| AMCC | 19202 | OC-192 SONET/SDH Mapper |
| AMCC | 19203 | OC-192 Digital Wrapper |

Figure 4. Functional Block Diagram



S3091 ARCHITECTURE/FUNCTIONAL DESIGN

MUX OPERATION

The S3091 performs serialization in the processing of a transmit SONET STS-192 bit serial data stream. It converts the 16-bit parallel 622.08 Mbps data stream to bit serial format at 9.953 Gbps.

A high-frequency bit clock is generated from a 155.52 or 622.08 MHz (or equivalent FEC or DW rates) frequency reference by using a frequency synthesizer that consist of an on-chip phase-lock loop circuit with a divider, VCO and loop filter.

Clock Divider and Phase Detector

The clock divider and phase detector, shown in the block diagram in Figure 4, contains monolithic PLL components that generate signals required to drive the loop filter. See Table 2 for REFCLK required.

In order for the VCO clock frequency to meet the accuracy required for operation in a SONET system, the REFCLK input must be generated from a differential ECL crystal oscillator in which the frequency accuracy equals the value stated in Table 10.

Oscillator phase noise allowable can be defined best by looking at plots of oscillators that allow the part to meet SONET jitter generation specifications of 100 mUIpp. As can be seen from Figures 16 and 17, two different vendors' oscillators can yield similar results. For 622 MHz REFCLK, the 82 mUIpp graph is at the noise floor of the part.

For best jitter generation, use a 622.08 MHz oscillator with a phase noise that meets or exceeds the phase noise plots shown in Figure 16, or a 155.52 MHz oscillator with a phase noise that meets or exceeds the phase noise plots in Figure 17.

Timing Generator

The timing generator function, shown in Figure 4, provides two separate functions. It provides a 16-bit parallel rate clock and a mechanism for aligning the phase between the incoming clock and the clock that loads the parallel-to-serial shift register.

The PCLK output is a 16-bit parallel rate clock. For STS-192, the PCLK frequency is 622.08 MHz. PCLK is intended for use as a 16-bit parallel speed clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3091 device.

In the parallel-to-serial conversion process, the incoming data is passed from the PCLK clock timing domain to the internally generated byte clock timing domain using an internal FIFO.

The timing generator also produces a feedback reference clock to the clock synthesizer. A counter divides the synthesized clock down to the same frequency as the reference clock (REFCLK). The PLL in the clock synthesizer maintains the stability of the synthesized clock by comparing the phase of the feedback clock to that of the reference clock (REFCLK). The modulus of the counter is a function of the reference clock frequency and the operating frequency.

Table 2. FEC Modes

| Error Correcting Capability | Code Rate showing Bandwidth Expansion due to code words and FSB | Increased TSD Frequency | Increased Input Clock (REFCLK) Frequency |
|------------------------------------|--|--------------------------------|---|
| 0 bytes per 255-byte block | 0% Increase | 9.953 Gbps | 622.08 MHz |
| 3 bytes per 255-byte block | 2.82% Increase | 10.234 Gbps | 639.62 MHz |
| 4 bytes per 255-byte block | 3.66% Increase | 10.317 Gbps | 644.84 MHz |
| 5 bytes per 255-byte block | 4.51% Increase | 10.402 Gbps | 650.13 MHz |
| 6 bytes per 255-byte block | 5.37% Increase | 10.488 Gbps | 655.48 MHz |
| 7 bytes per 255-byte block | 6.25% Increase | 10.575 Gbps | 660.96 MHz |
| 8 bytes per 255-byte block | 7.14% Increase | 10.664 Gbps | 666.51 MHz |
| Digital Wrapper (OTU2) | 7.59% Increase | 10.709 Gbps | 669.33 MHz |

Parallel-to-Serial Converter

The parallel-to-serial converter shown in Figure 4 is comprised of two byte-wide registers. The PCLK (622.08 MHz or 311.04 MHz dual edge clock) clocks in the data from the PINP/N[15:0] bus to the first register of the parallel-to-serial register. The second register is a parallel loadable shift register, which takes its parallel input from the first register.

An internally generated byte clock activates the parallel data transfer between registers. The serial data is shifted out of the second register.

If the 311.04 MHz dual edge PCLK mode is selected, PCLK skew relative to PINP/N[15:0] may be introduced to optimize data and clock setup and hold times. SKEWSEL[1:0] may be used to control the skew which is nominally 815 ps. See Table 5 for skew selections.

FIFO

A FIFO is added to decouple the internal and external parallel clocks. The internally generated divide-by-16 clock is used to clock out data from the FIFO. PHINIT and LOCKERRB are used to center or reset the FIFO. The PHINIT and LOCKERRB signals will center the FIFO after the third PCLK pulse. (See Figure 9.) This ensures that PCLK is stable. This scheme allows the user to have an infinite PCLK to PCLK delay through the ASIC. Once the FIFO is centered, the PCLK to PCLK delay can have a maximum drift as specified in Table 20.

FIFO Initialization

The FIFO can be initialized in one of the following three ways:

1. During power up, once the PLL has locked to the reference clock provided on the REFCLK pins, the LOCKERRB will go active and initialize the FIFO.
2. When RSTB goes active, the entire chip is reset. This causes the PLL to go out of lock, and thus the LOCKERRB goes inactive. When the PLL reacquires the lock, the LOCKERRB goes active and initializes the FIFO. Note that PCLK does not toggle when RSTB is active.
3. The user can also initialize the FIFO by raising PHINIT.

During normal running operation, the incoming data is passed from the PCLK timing domain to the internally generated divide-by-16 clock timing domain. Although the frequency of PCLK and the internally generated clock is the same, their phase relationship is arbitrary.

Table 3. Reference Frequency

| REFSEL | REFCLK |
|--------|---|
| 0 | 155.52 MHz (or equivalent FEC or DW rate) |
| 1 | 622.08 MHz (or equivalent FEC or DW rate) |

To prevent errors caused by short setup or hold times between the two timing domains, the timing generator circuitry monitors the phase relationship between PCLK and the internally generated clock. When a potential setup or hold time violation is detected, Phase Error (PHERR) goes High. If the condition persists, PHERR will remain High. When PHERR conditions occur, PHINIT should be activated to recenter the FIFO (at least 10 ns). This can be done by connecting PHERR to PHINIT. When realignment occurs, four to ten bytes of data will be lost. The user can also take in the PHERR signal, process it, and send an output to PHINIT in such a way that idle bytes are lost during the realignment process. PHERR will go inactive when the realignment is complete. (See Figure 9, *Phase Adjust Timing*.)

Power Sequencing

In order to avoid latchup, it is required that the -5.2 V power be applied to the S3091 for a minimum of 50 ms before 3.3 V power is applied.

Table 4. Clock Select

| CLKSEL | PCLK Frequency |
|--------|---|
| 0 | 622.08 MHz (or equivalent FEC or DW rate) |
| 1 | 311.04 MHz (or equivalent FEC or DW rate) |

Table 5. Skew Select

| SKEWSEL[1] | SKEWSEL[0] | 311 PCLK Target Skew |
|------------|------------|----------------------|
| 0 | 0 | 915 ps |
| 0 | 1 | 1015 ps |
| 1 | 0 | 715 ps |
| 1 | 1 | 815 ps |

Table 6. Input Pin Assignment and Descriptions

| Pin Name | Level | I/O | Pin # | Description |
|--|--------------|-----|---|---|
| PINP0 PINN0 PINP1 PINN1 PINP2 PINN2 PINP3 PINN3 PINP4 PINN4 PINP5 PINN5 PINP6 PINN6 PINP7 PINN7 PINP8 PINN8 PINP9 PINN9 PINP10 PINN10 PINP11 PINN11 PINP12 PINN12 PINP13 PINN13 PINP14 PINN14 PINP15 PINN15 | LVDS | I | N2 N3 P3 P4 N4 N5 P5 P6 N6 N7 P7 P8 N8 N9 P9 P10 M11 M12 N12 N13 N14 M14 L13 K13 K14 J14 H14 G14 G13 F13 F14 E14 | Parallel Data Input. A 16-bit parallel, 622.08 Mbps, aligned to the PCLK parallel input clock. PINP/N[15] is the most significant bit (corresponding to bit 1 of each word, the first bit transmitted). PINP/N[0] is the least significant bit (corresponding to bit 16 of each word, the last bit transmitted). PINP/N[15:0] is sampled on the rising edge of PCLK (when CLKSEL = 0) or on the rising and falling edge of PCLK (when CLKSEL = 1). Internally biased and terminated. |
| PICLKP PICLKN | LVDS | I | D14 C14 | Parallel Input Clock. A 622.08 MHz or dual edge 311.04 MHz nominally 50% duty cycle input clock, to which PINP/N[15:0] is aligned. PCLK is used to transfer the data on the PIN inputs into a holding register in the parallel-to-serial converter. Internally biased and terminated. |
| TESTB | LVTTL | I | C6 | Test Clock Enable. Active Low. Set Low to provide access to the PLL during production tests. (Pull High for normal operation.) |
| REFCLKP REFCLKN | Diff. ECL | I | B1 C1 | Reference Clock. Input used as the reference for the internal bit clock frequency synthesizer. Internally terminated and biased. |
| RSTB | LVTTL | I | A7 | Master Reset. Active Low. Reset input for the device. For correct reset, this input must be asserted Low for 100 ns. During reset, PCLK does not toggle. |
| CAP1 CAP2 | Analog | I | B4 C4 | Loop Filter Capacitors. Connections for external loop filter capacitor and resistors. (See Figure 15.) |

Table 6. Input Pin Assignment and Descriptions (Continued)

| Pin Name | Level | I/O | Pin # | Description |
|----------------------|--------|-----|------------|---|
| REFSEL | LVTTTL | I | M2 | Reference Select. Used to select the reference clock frequency. See Table 3. |
| PHINITP PHINITN | LVDS | I | C13 B13 | Phase Initialization. Asynchronous input that initializes the phase adjust circuit. (See Figure 9.) |
| CLKSEL | LVTTTL | I | A6 | Clock Select. Used to select between the 622.08 MHz or 311.04 MHz dual edge clock on the P1CLKP/N. See Table 4. |
| SKEWSEL1 SKEWSEL0 | LVTTTL | I | J13 D13 | Allows magnitude error in delaying the 311 P1CLK to compensate for the variations in the data valid window due to Inter-Symbol Interference (ISI) and static skew. See Table 5. |

Table 7. Output Pin Assignment and Descriptions

| Pin Name | Level | I/O | Pin # | Description |
|--------------------|--------------|-----|------------|---|
| TSDP TSDN | Diff. CML | O | G1 J1 | Transmit Serial Data. Serial data stream signals, normally connected to an optical transmitter module. Use Coplanar Waveguide Structure for best results. See Layout Recommendation application note. See Characterization Report for S ₂₂ plot. |
| P1CLKP P1CLKN | LVDS | O | B11 A11 | Parallel Clock. A 622.08 MHz clock. It is normally used to coordinate transfers between upstream logic and the S3091 device. |
| 155MCKP 155MCKN | LVDS | O | B10 B9 | 155.52 MHz Clock Output. 155.52 MHz clock output from the clock synthesizer. The output should be connected to the reference clock input of the external clock recovery function (such as the S3092). Pull-down resistors may be removed to minimize power. |
| 77MCKP 77MCKN | LVDS | O | A10 A9 | 77.76 MHz Clock Output. 77.76 MHz clock output from the clock synthesizer. For test purposes only. Pull-down resistors may be removed to minimize power. |
| LOCK- ERRB | LVTTTL | O | C12 | Lock Error/Phase Error. Active Low. Goes inactive after an internal delay and the PLL has locked to the clock provided on the REF-CLK pins. LOCKERRB goes active for at least 100 ns when PHERR goes active. LOCKERRB stays active as long as PHERR is active. LOCKERRB is an asynchronous output. |
| PHERRP PHERRN | LVDS | O | B12 A12 | Phase Error. Pulses High during each P1CLK cycle for which there is a potential set-up/hold timing violation between the internal byte clock and P1CLK timing domains. |

Table 8. Common Pin Assignment and Descriptions

| Pin Name | Level | Pin # | Description |
|------------------|-----------|--|-----------------------------------|
| A _{VEE} | -5.2 V | B8, C8, D1, E2, L2, M5, M8, N11 | Analog V _{EE} |
| VEE_FILTER | -5.2 V | A3 | Analog V _{EE} for Filter |
| VEE_VCO | -5.2 V | A5 | Analog V _{EE} for VCO |
| DGND | GND = 0 V | A8, A13, A14, B7, B14, C10, E13, L14, M4, M7, M10, N1, N10, P1, P2, P11, P12, P13, P14 | Digital Ground |
| AGND | GND = 0 V | A1, A2, A4, B2, B3, B5, B6, C2, C3, C5, D2, E1, F1, F2, H1, H2, M1, K1, K2, L1 | Analog GND |
| THERMALGND | GND = 0 V | E6, E7, E8, E9, E10, F5, F6, F7, F8, F9, F10, G5, G6, G7, G8, G9, G10, H5, H6, H7, H8, H9, H10, J5, J6, J7, J8, J9, J10, K5, K6, K7, K8, K9, K10 | Thermal Ground |
| VCCLVDS | +3.3 V | C9, H13, M3, M6, M9, M13 | LVDS V _{CC} |
| VCCLVTTL | +3.3 V | C7 | LVTTTL V _{CC} |

Note: All digital, analog, and thermal grounds are connected together on the package.

Figure 5. S3091 Pinout

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|----------|------------|--------|------------|-------|---------|-------------|-------------|-------------|-------------|-------------|-------|----------|----------|--------|
| A | AGND | AGND | VEE FILTER | AGND | VEE VCO | CLKSEL | RSTB | DGND | 77MCKN | 77MCKP | PCLKN | PHERRN | DGND | DGND |
| B | REFCLKP | AGND | AGND | CAP1 | AGND | AGND | DGND | AVEE | 155MCKN | 155MCKP | PCLKP | PHERRP | PHINITN | DGND |
| C | REFCLKN | AGND | AGND | CAP2 | AGND | TESTB | VCCLVTTL | AVEE | VCCLVDS | DGND | | LOCKERRB | PHINITP | PICKLN |
| D | VEE REFCLK | AGND | | | | | | | | | | | SKEWSEL0 | PICKLP |
| E | AGND | AVEE | | | | THERMAL GND | THERMAL GND | THERMAL GND | THERMAL GND | THERMAL GND | | | DGND | PIN15N |
| F | AGND | AGND | | | | THERMAL GND | THERMAL GND | THERMAL GND | THERMAL GND | THERMAL GND | | | PIN14N | PIN15P |
| G | TSDP | | | | | THERMAL GND | THERMAL GND | THERMAL GND | THERMAL GND | THERMAL GND | | | PIN14P | PIN13N |
| H | AGND | AGND | | | | THERMAL GND | THERMAL GND | THERMAL GND | THERMAL GND | THERMAL GND | | | VCCLVDS | PIN13P |
| J | TSDN | | | | | THERMAL GND | THERMAL GND | THERMAL GND | THERMAL GND | THERMAL GND | | | SKEWSEL1 | PIN12N |
| K | AGND | AGND | | | | THERMAL GND | THERMAL GND | THERMAL GND | THERMAL GND | THERMAL GND | | | PIN11N | PIN12P |
| L | AGND | AVEE | | | | | | | | | | | PIN11P | DGND |
| M | AGND | REFSEL | VCCLVDS | DGND | AVEE | VCCLVDS | DGND | AVEE | VCCLVDS | DGND | PIN8P | PIN8N | VCCLVDS | PIN10N |
| N | DGND | PIN0P | PIN0N | PIN2P | PIN2N | PIN4P | PIN4N | PIN6P | PIN6N | DGND | AVEE | PIN9P | PIN9N | PIN10P |
| P | DGND | DGND | PIN1P | PIN1N | PIN3P | PIN3N | PIN5P | PIN5N | PIN7P | PIN7N | DGND | DGND | DGND | DGND |

**S3091
(Package TOP View)
(Die BOTTOM View)**

Figure 6. S3091 148-Pin CBGA Package

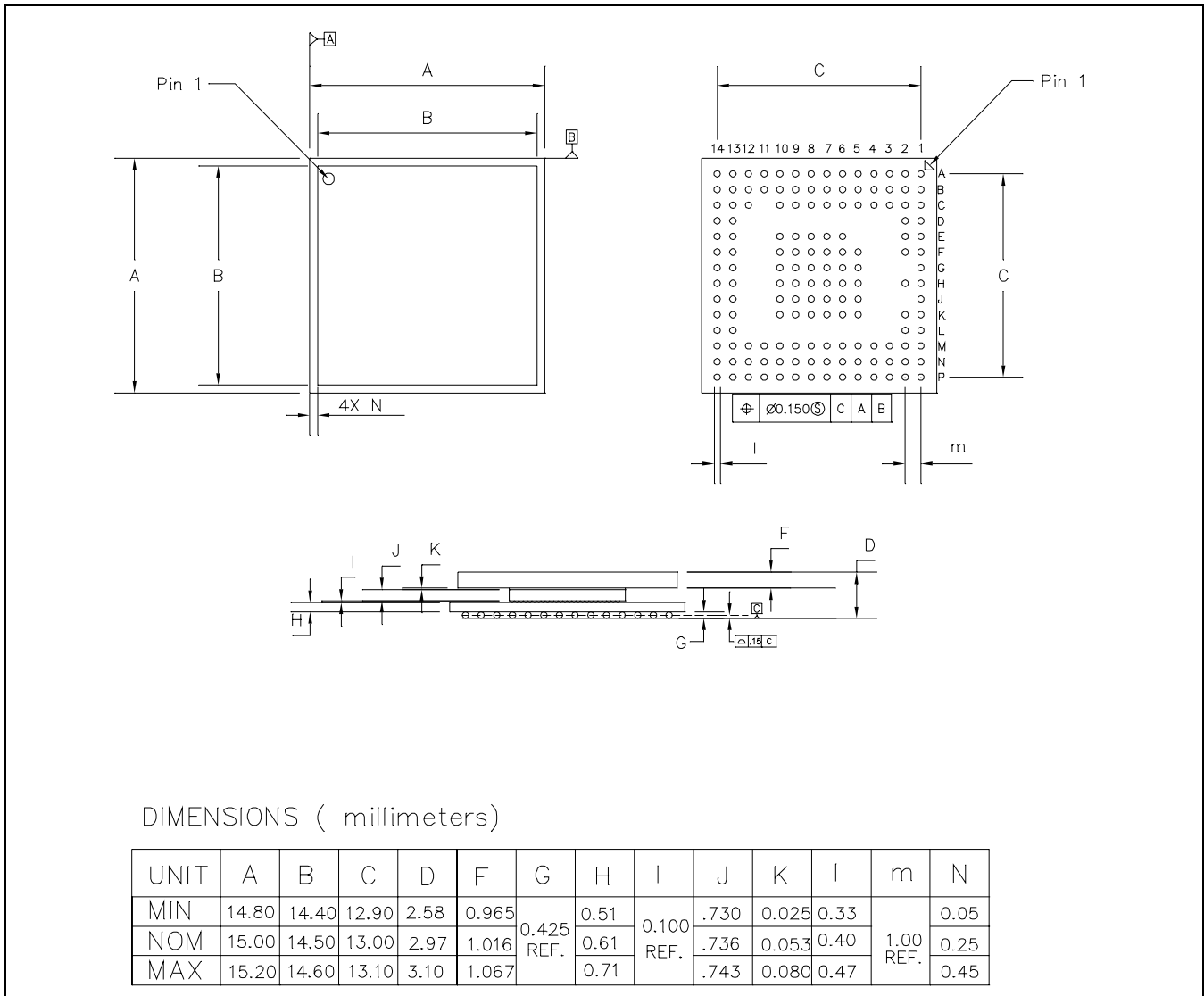


Table 9. Thermal Management

| Device | Package Max Power (70°C Ambient) | θ_{ja} | θ_{jc} |
|--------|----------------------------------|---------------|---------------|
| S3091 | 2.68 W | 20.5°C/W | 3.0°C/W |

Note: See application note for simulation results, thermal management suggestions and thermal profile for attachment.

Table 10. Performance Specifications

| Parameter | Min | Typ | Max | Units | Conditions |
|--|-------|-----|--------|---------|--|
| Nominal VCOCLK Center Frequency | 9.953 | | 10.709 | GHz | |
| Data Output Jitter STS-192 with 622.08 MHz REFCLK. | | | 82 | mUIpp | Limited B.W., 50 kHz to 80 MHz, BER = 1E-12. |
| Data Output Jitter STS-192 with 155.52 MHz REFCLK. | | 100 | | mUIpp | Limited B.W., 50 kHz to 80 MHz, 49/51 duty cycle REFCLK. |
| TSDP/N Output Return Loss (S_{22}) | | | -12 | dB | DC – 10 GHz |
| Reference Clock Frequency Tolerance | -100 | | +100 | ppm | ± 20 ppm is required to meet SONET output frequency specification. |
| Reference Clock Input Duty Cycle (622.08 MHz) (or equivalent FEC or DW rate) | 45 | | 55 | % | |
| Reference Clock Input Duty Cycle (155.52 MHz) (or equivalent FEC or DW rate) | 49 | | 51 | % | Required for best jitter performance. |
| Reference Clock Rise and Fall Times for 155.52 MHz Clk. (or equivalent FEC or DW rate) | 0.2 | | 0.8 | ns | 20% to 80% of amplitude. |
| Reference Clock Rise and Fall Times for 622.08 MHz Clk. (or equivalent FEC or DW rate) | 0.1 | | 0.5 | ns | 20% to 80% of amplitude. |
| Acquisition Lock Time (phase lock) | | 16 | 25 | μ s | After the release of RSTB, with device already powered up and with a valid REFCLK. Guaranteed, but not tested. |

Table 11. Absolute Maximum Ratings

| Parameter | Min | Typ | Max | Units |
|------------------------------|-----------------------|-----|----------------------|-------|
| Storage Temperature | -55 | | 150 | °C |
| VCC 3.3 V Supply | -0.5 | | 3.6 | V |
| VEE -5.2 V Supply | 0.5 | | -7.0 | V |
| LVTTL Input Voltage | -0.5 | | V _{CC} +0.5 | V |
| LVDS Input Voltage | 0 | | V _{CC} | V |
| LVDS Output Voltage | 0 | | V _{CC} | V |
| ECL Input Voltage | V _{EE} -0.25 | | AGND | V |
| CML Output Voltage | V _{EE} -0.25 | | AGND | V |
| LVTTL Output Voltage | AGND -0.5 | | V _{CC} +0.5 | V |
| CML Output Current per pin | | | 13 | mA |
| LVDS Input Current per pin | | | 10 | mA |
| LVTTL Input Current per pin | -450 | | 1000 | µA |
| LVTTL Output Current per pin | | | 2 | mA |
| LVDS Output Current per pin | | | 15 | mA |
| ECL Input Current per pin | | | 15 | mA |

Electrostatic Discharge (ESD) Ratings

The S3091 is rated to the following voltages based on the human body model:

1. All pins are rated at 100 Volts.

Standards for ESD protection should be adhered to when handling the devices to ensure that they are not damaged. The standards to be used are defined in ANSI standard ANSI/ESD S20.20-1999, "Protection of Electrical and Electronic Parts, Assemblies and Equipment." Contact your local FAE or sales representative for ESD application notes.

Table 12. Recommended Operating Conditions

| Parameter | Min | Typ | Max | Units |
|--|-------|------|-------|-------|
| Ambient Temperature Under Bias (Commercial) | 0 | | +70 | °C |
| Junction Temperature Under Bias | 40 | | 125 | °C |
| Voltage on V _{CC} with Respect to GND | 3.135 | 3.3 | 3.465 | V |
| Voltage on V _{EE} with Respect to GND | -4.94 | -5.2 | -5.46 | V |
| I _{CC} Supply Current | | 290 | 360 | mA |
| I _{EE} Supply Current | | 260 | 320 | mA |

Table 13. LVTTTL Input DC Characteristics

| Parameters | Description | Min | Typ | Max | Units | Condition |
|------------|--------------------|------|-----|-------|---------------|---------------------------|
| V_{IH} | Input High Voltage | 2.0 | | 3.465 | V | TTL $V_{CC} = \text{Max}$ |
| V_{IL} | Input Low Voltage | 0.0 | | 0.8 | V | TTL $V_{CC} = \text{Min}$ |
| I_{IH} | Input High Current | | | 20 | μA | $V_{IN} = 2.4 \text{ V}$ |
| I_{IL} | Input Low Current | -500 | | | μA | $V_{IN} = 0.5 \text{ V}$ |

Table 14. LVTTTL Output DC Characteristics

| Parameters | Description | Min | Typ | Max | Units | Condition |
|------------|---------------------|-----|-----|-----|-------|---|
| V_{OH} | Output High Voltage | 2.4 | | | V | $V_{CC} = \text{Min}$ $I_{OH} = -30 \mu\text{A}$ |
| V_{OL} | Output Low Voltage | | | 0.5 | V | $V_{CC} = \text{Min}$ $I_{OL} = 1 \text{ mA}$ |

Table 15. Differential CML Output DC Characteristics

| Parameters | Description | Min | Typ | Max | Units | Condition |
|--------------------------------|--|-------------|-----|-------------|----------|--|
| V_{OL} | Output Low Voltage | AGND - 1.25 | | AGND - 0.80 | V | 100 Ω line-to-line. |
| V_{OH} | Output High Voltage | AGND - 0.55 | | AGND - 0.25 | V | 100 Ω line-to-line. |
| $\Delta V_{OUTDIFF}$ Data | Serial Output Differential Voltage Swing | 1000 | | 1500 | mV | 100 Ω line-to-line. See Figure 10. |
| $\Delta V_{OUTSINGLE}$ Data | Serial Output Single-ended Voltage Swing | 500 | | 750 | mV | 100 Ω line-to-line. See Figure 10. |
| R_{SINGLE} | Single-ended Resistance | 40 | | 60 | Ω | Over process, voltage and temperature range. |

Table 16. Internally Biased Differential ECL Input DC Characteristics

| Parameters | Description | Min | Typ | Max | Units | Comments |
|-----------------------|----------------------------------|------------|-----|------------|----------|----------------|
| ΔV_{INDIFF} | Differential Input Voltage Swing | 300 | | 1600 | mV | See Figure 10. |
| $\Delta V_{INSINGLE}$ | Single-ended Input Voltage Swing | 150 | | 800 | mV | See Figure 10. |
| R_{DIFF} | Differential Input Resistance | 80 | 100 | 120 | Ω | |
| V_{IH} | Input High Voltage | | | AGND - 0.2 | V | |
| V_{IL} | Input Low Voltage | AGND - 2.0 | | | V | |

Table 17. Internally Biased LVDS Input Characteristics

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|-----------------------|-------------------------------|------|-----|------|------|---|
| V _{IH} | Input High Voltage | 1.16 | | 2.9 | V | Over process, voltage and temperature range |
| V _{IL} | Input Low Voltage | 0.6 | | 2.8 | V | Over process, voltage and temperature range |
| V _{INDIFF} | Input Voltage Differential | 200 | | 2600 | mV | Over process, voltage and temperature range |
| V _{INSINGLE} | Input Single-ended Voltage | 100 | | 1300 | mV | Over process, voltage and temperature range |
| R _{DIFF} | Differential Input Resistance | 80 | 100 | 120 | Ω | Over process, voltage and temperature range |

Table 18. LVDS Output DC Characteristics^{1,2} (See Figure 12)

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|------------------------|-----------------------------|------|-----|------|------|---|
| V _{OH} | Output High Voltage | 1.25 | | 1.8 | V | Over process, voltage and temperature range |
| V _{OL} | Output Low Voltage | 0.85 | | 1.45 | V | Over process, voltage and temperature range |
| V _{OUTDIFF} | Output Differential Voltage | 500 | 740 | 1100 | mV | Over process, voltage and temperature range |
| V _{OUTSINGLE} | Output Single-ended Voltage | 250 | 370 | 550 | mV | Over process, voltage and temperature range |

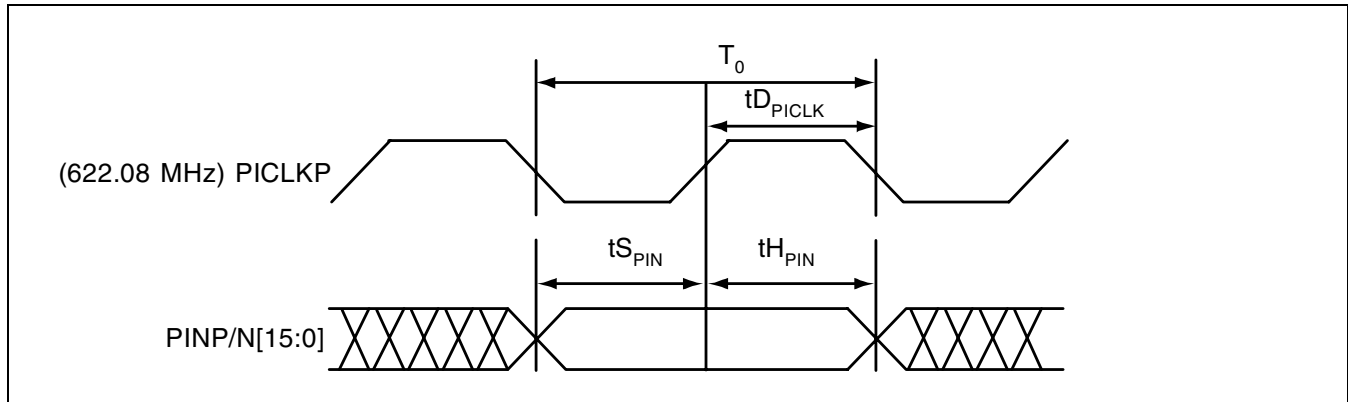
1. Output loading is 100 Ω line-to-line.
2. 330 Ω pull-down resistor per line to ground.

Table 19. AC Transmitter Timing Characteristics (PICKLP/N = 622.08 MHz)

| Symbol | Description | Min | Typ | Max | Units |
|------------|--|-----|-----|-----|-------|
| | PICKLP/N Duty Cycle = tD_{PICKLP}/T_0 | 40 | | 60 | % |
| tS_{PIN} | PINP/N[15:0] Set-up Time w.r.t. rising edge of PICKLP (622.08 MHz PICKLP) | 200 | | | ps |
| tH_{PIN} | PINP/N[15:0] Hold Time w.r.t. rising edge of PICKLP (622.08 MHz PICKLP) | 200 | | | ps |
| | PCLKP/N Duty Cycle | 45 | | 55 | % |
| | CML Output Rise and Fall Time (20% - 80%), Pattern 27 – 1 | | | 35 | ps |
| | LVDS Output Rise and Fall Time (20% - 80%) | 100 | | 250 | ps |
| t_{PW} | PHINIT Minimum Pulse Width (See Figure 9) | 10 | | | ns |
| t_{PW} | RSTB Minimum Pulse Width ¹ | 100 | | | ns |
| | 155MCKP/N Duty Cycle | 45 | | 55 | % |
| | PCLK to PICKLP drift after FIFO is centered | | | 2 | ns |

1. Guaranteed by design.

Figure 7. AC Input Timing (PICKLP/N = 622.08 MHz)



1. When a set-up time is specified on LVDS signals between an input and a clock, the set-up time in picoseconds, is from the 50% point of the input to the 50% point of the clock.
2. When a hold time is specified on LVDS signals between an input and a clock, the hold time in picoseconds, is from the 50% point of the clock to the 50% point of the input.

Table 20. AC Transmitter Timing Characteristics (PICKLP/N = 311.04 MHz)

| Symbol | Description | Min | Typ | Max | Units |
|------------|---|------|-----|-----|-------|
| | PICKLP/N Duty Cycle = tD_{PICKLP}/T_0 | 48 | | 52 | % |
| T_R, T_F | LVDS output rise and fall times (20% - 80%) | 100 | | 250 | ps |
| tS_{PIN} | PINP/N[15:0] setup time w.r.t. next edge of PICKLP (311.04 MHz PICKLP) | 1000 | | | ps |
| tH_{PIN} | PINP/N[15:0] hold time w.r.t. next edge of PICKLP (311.04 MHz PICKLP) | | | 600 | ps |
| | PCLK to PICKLP drift after the FIFO is centered | | | 2 | ns |

Figure 8. AC Input Timing (PICKLP/N = 311.04 MHz)

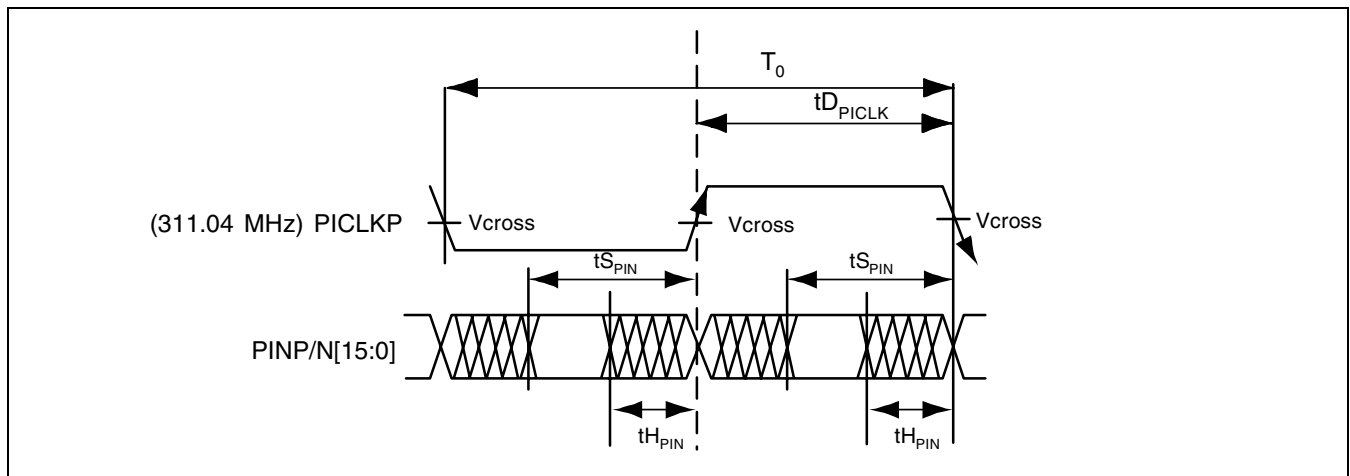
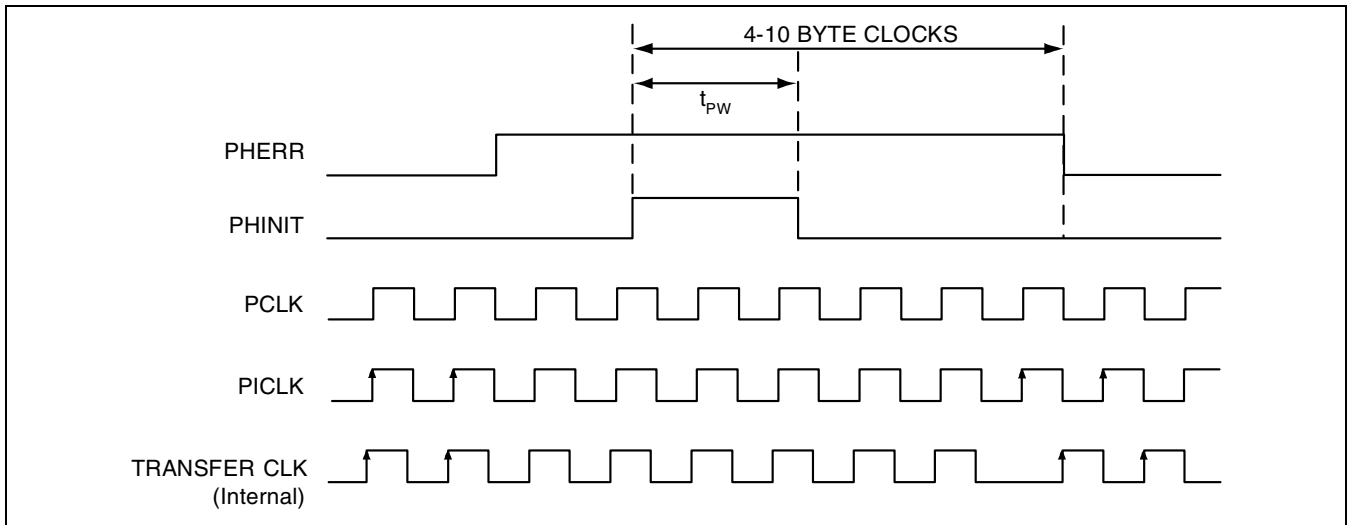


Table 21. External Loop Filter Components

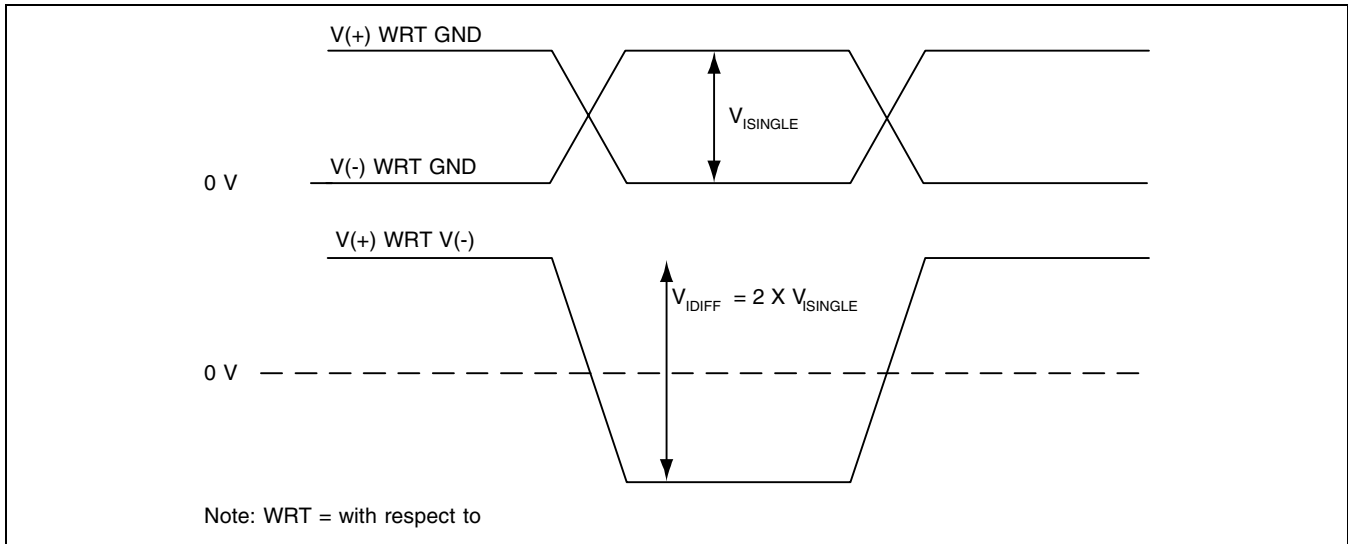
| Symbol | Description | Value | Unit |
|------------|--|-------|----------|
| R_1, R_2 | Resistor, Surface Mount, 0402 | 150 | Ω |
| C_2 | Capacitor, Surface Mount, 0603 or larger | 1.0 | μF |

Figure 9. Phase Adjust Timing



Note: The byte clock = 622.08 MHz to 669.33 MHz.

Figure 10. Differential Voltage Measurement



Note: $V(+)$ - $V(-)$ is the algebraic difference of the input signals.

Figure 11. CML Output to -5.2 V ECL Input DC Coupled Termination, Reference Only

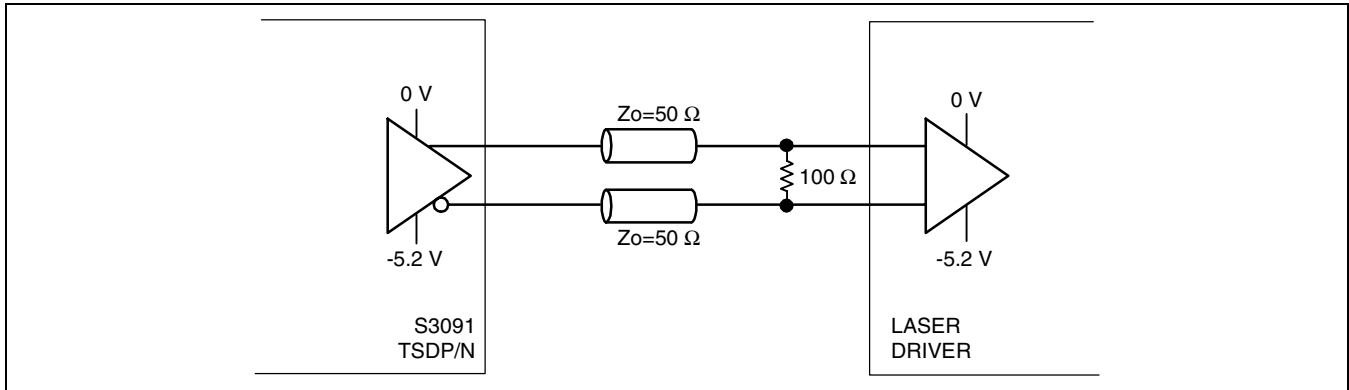


Figure 12. S3091 LVDS Driver to LVDS Input, Reference Only

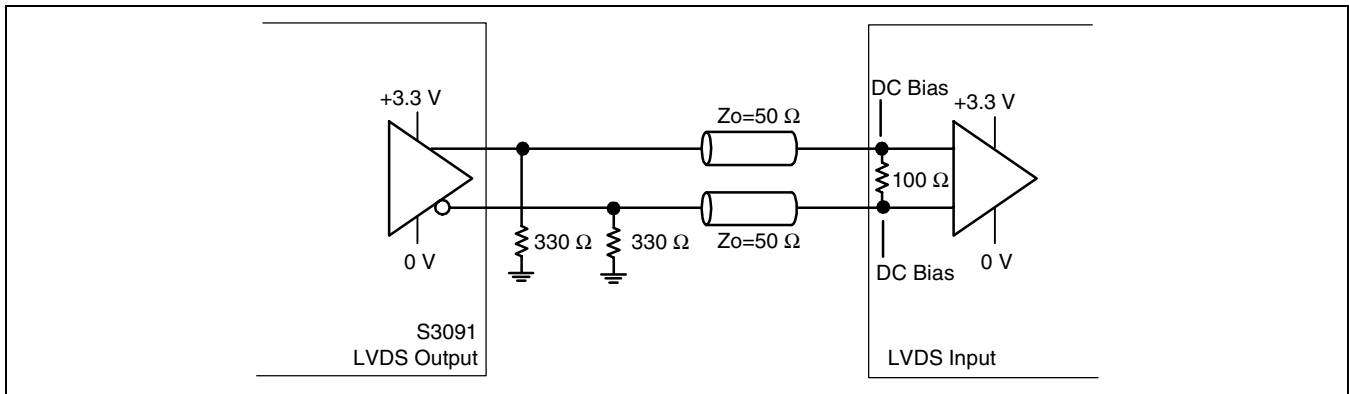


Figure 13. LVDS Driver to S3091 LVDS Input Direct Coupled Termination, Reference Only

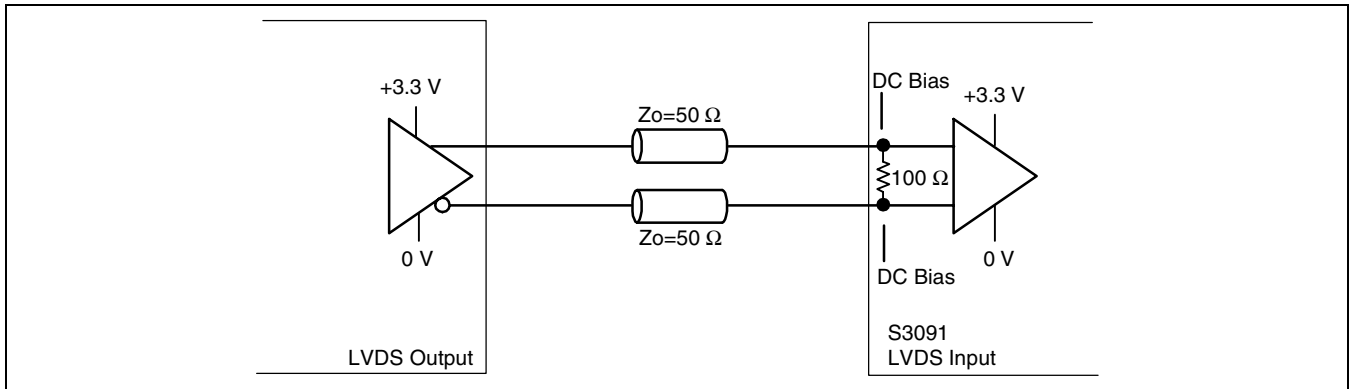


Figure 14. LVDS Driver to S3091 LVDS Input AC Coupled Termination, Reference Only

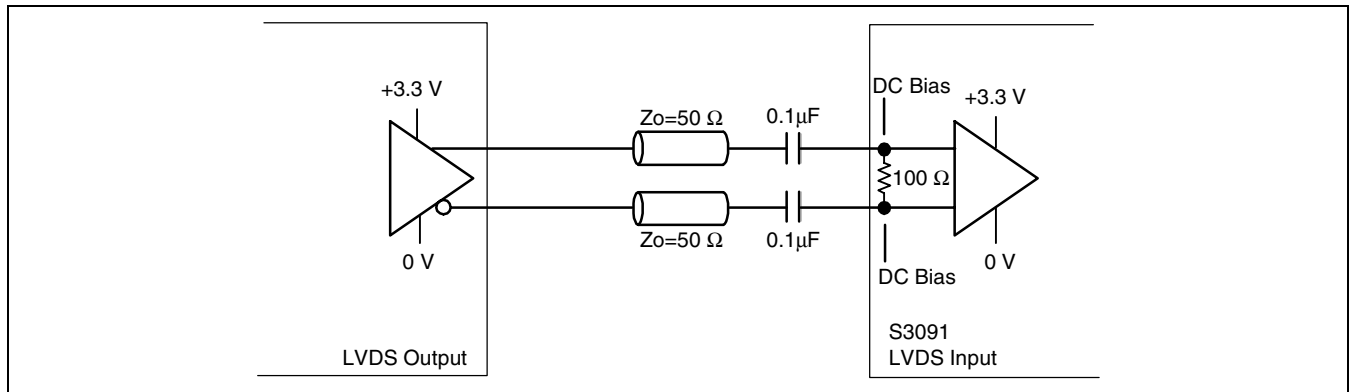


Figure 15. External Loop Filter

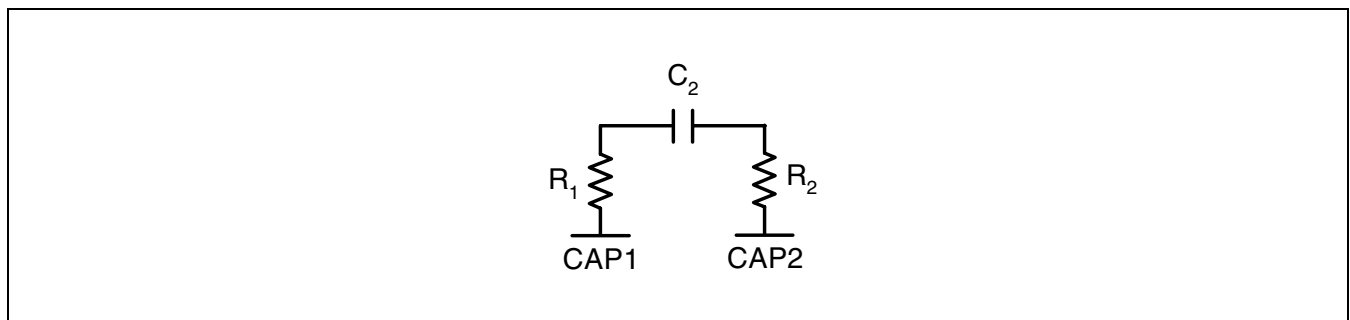
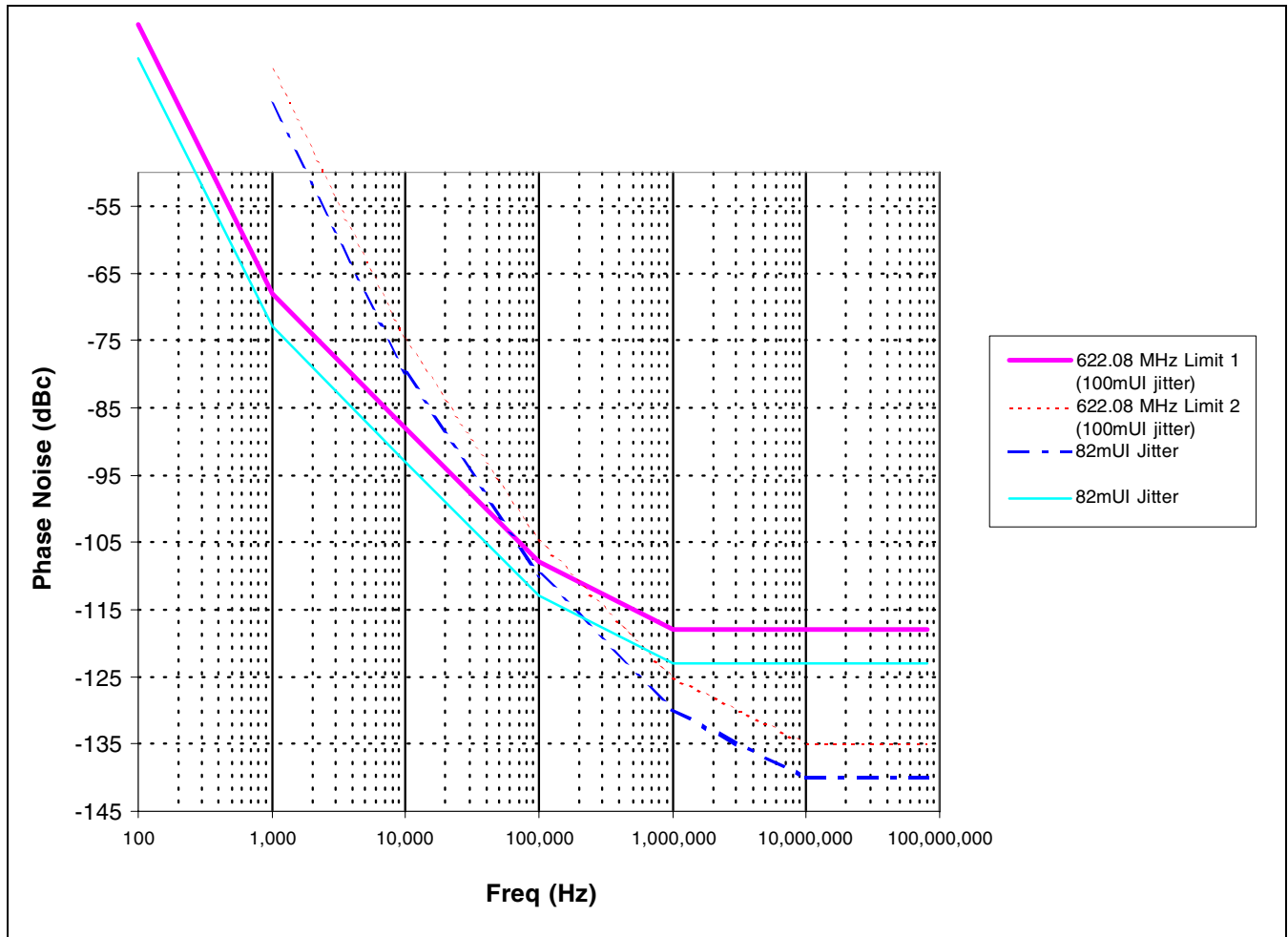
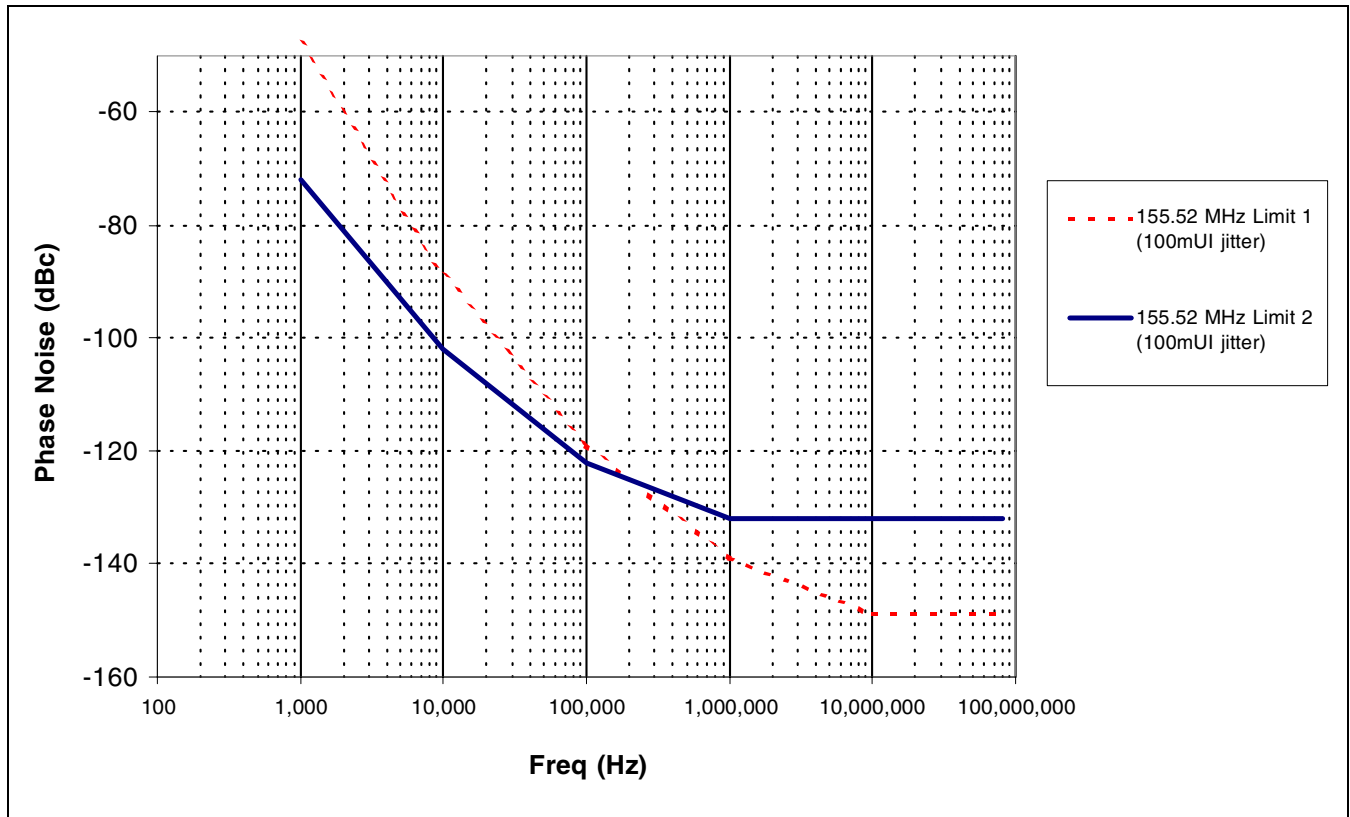


Figure 16. S3091 622.08 MHz REFCLK Phase Noise Limit



Note: Using an oscillator with one of the phase noise spectrums shown above, will yield the respective jitter generation numbers associated with each phase noise plot.

Figure 17. S3091 155.52 MHz REFCLK Phase Noise Limit



Note: Using an oscillator with either phase noise spectrum shown above, will yield similar jitter generation as the integrated phase noise under each mask is similar.

Ordering Information

| Prefix | Device | Package | Revision |
|------------------------|--------|---------------|----------|
| S - Integrated Circuit | 3091 | CB - 148 CBGA | 20 |

X
Prefix

XXXX
Device

XX
Package

XX
Revision



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