AMCC®

MULTI-RATE (OC-48/24/12/3/GBE) SONET/SDH/ATM TRANSCEIVER   S3059

FEATURES

- SiGe BiCMOS technology
- Complies with Bellcore and ITU-T specifications
- On-chip high-frequency PLL for clock generation
- Supports OC-48 (2488.32 Mbps)
  OC-24 (1244.16 Mbps)
  Gigabit Ethernet (1250 Mbps)
  OC-12 (622.08 Mbps)
  OC-3 (155.52 Mbps)
- Reference frequency of 155.52 MHz
- Interface to LVPECL and LVTTL logic
- 16-bit differential LVPECL datapath
- Compact 218 TBGA package
- Diagnostic loopback mode
- Supports line timing
- Lock detect
- Signal detect input
- Low jitter LVPECL interface
- Internal FIFO to decouple transmit clocks
- Single 3.3 V supply
- Typical power 1.7 W

APPLICATIONS

- Wavelength Division Multiplexing (WDM) equipment
- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

GENERAL DESCRIPTION

The S3059 SONET/SDH transceiver chip is a fully integrated serialization/deserialization SONET OC-48 (2488.32 Mbps), OC-24 (1244.16 Mbps), Gigabit Ethernet (1250 Mbps), OC-12 (622.08 Mbps) and OC-3 (155.52 Mbps) interface device. The chip performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based WDM applications. Figure 1 shows a typical network application.

On-chip clock synthesis is performed by the high-frequency Phase Locked Loop (PLL) on the S3059 transceiver chip allowing the use of a slower external transmit clock reference. The chip can be used with a 155.52 MHz reference clock in support of existing system clocking schemes.

The low jitter LVPECL interface guarantees compliance with the bit-error rate requirements of the Bellcore and ITU-T standards. The S3059 is packaged in a 218 TBGA, offering designers a small package outline.

Figure 1. System Block Diagram
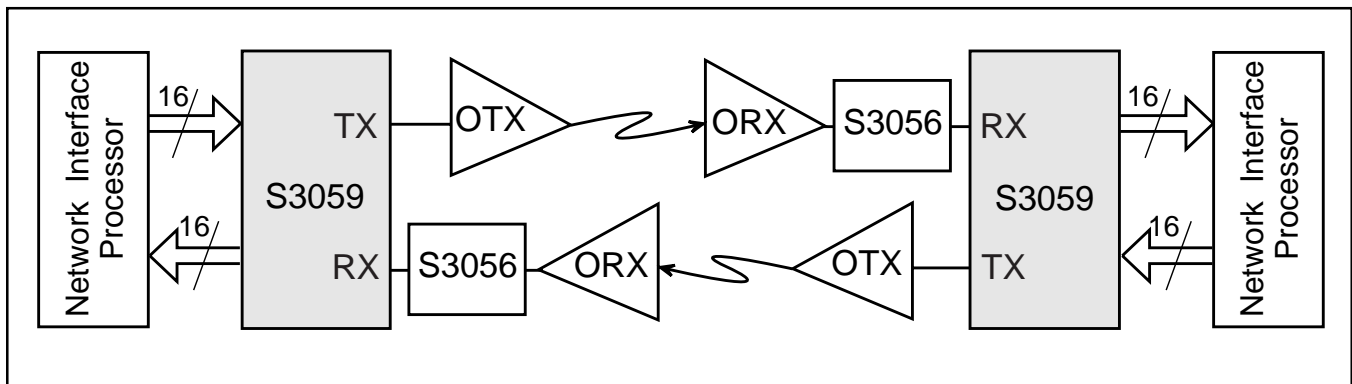
S3059 OVERVIEW

The S3059 transceiver implements SONET/SDH serialization/deserialization, and transmission functions. The block diagram in Figure 2 shows the basic operation of the chip. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation, and system timing. The system timing circuitry consists of management of the data stream and clock distribution throughout the front end. The suggested interface devices are given in Table 2.

Table 1. Data Rate Select

RATESEL0	RATESEL1	Operating Mode
0	0	OC-3
0	1	OC-12
1	0	OC-24/GBE
1	1	OC-48

The S3059 is divided into a transmitter section and a receiver section. The sequence of operations is as follows:

Transmitter Operations:
1. 16-bit parallel input
2. Parallel-to-serial conversion
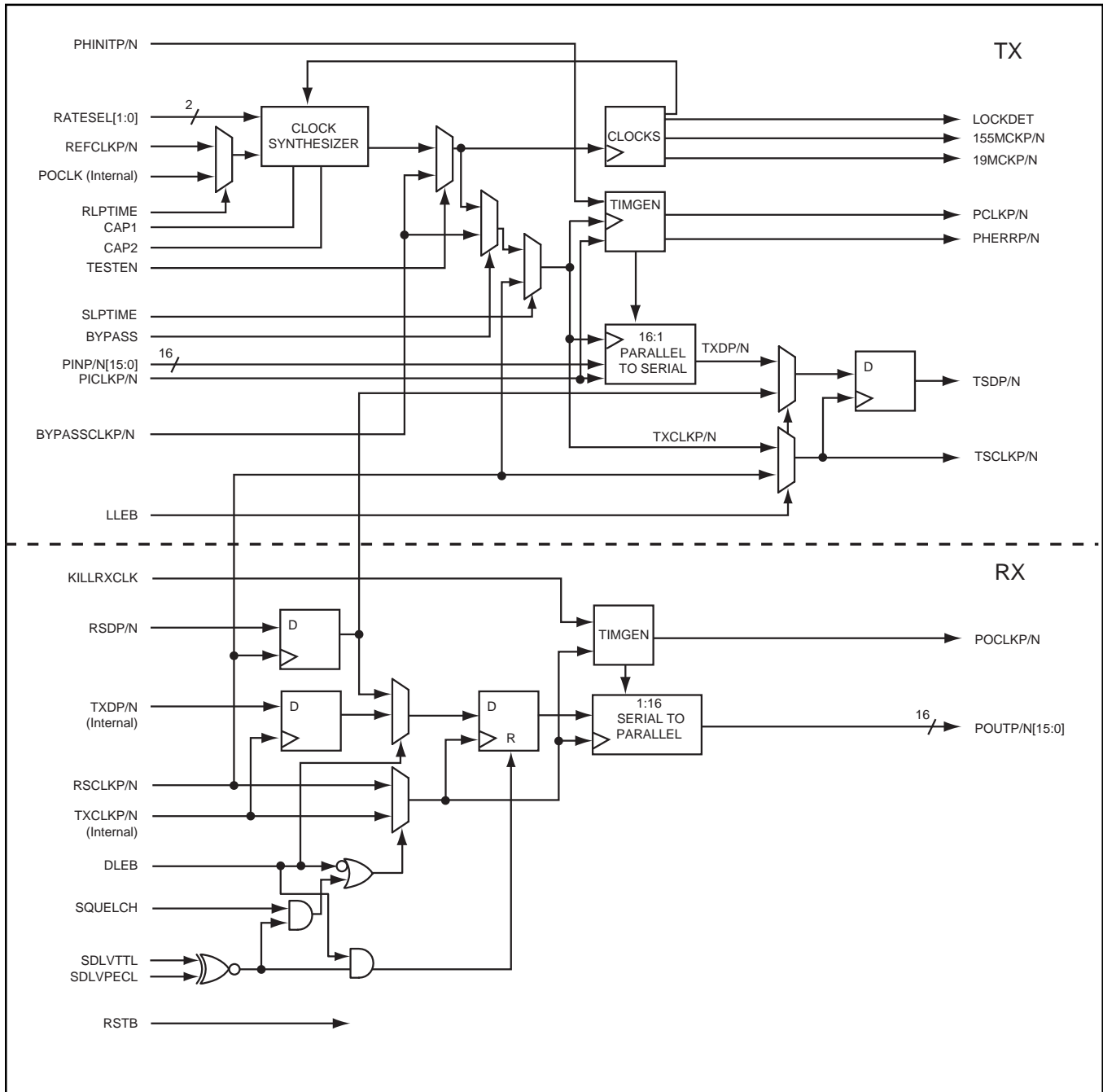3. Serial output

Receiver Operations:
1. Serial input
2. Serial-to-parallel conversion
3. 16-bit parallel output

Internal clocking and control functions are transparent to the user.

Table 2. Suggested Interface Devices

AMCC	S3056	OC-48 Clock Recovery Device
AMCC	S4801	STS-48C POS/ATM SONET Mapper

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Figure 2. S3059 Transceiver Functional Block Diagram

S3059 TRANSCEIVER FUNCTIONAL DESCRIPTION

TRANSMITTER OPERATION

The S3059 transceiver chip performs the serialization stage in the processing of a transmit SONET STS-48/STS-24/STS-12/STS-3/GBE data stream depending on the data rate selected. It converts 16-bit parallel data into bit-serial format at 2488.32/1244.16/622.08/155.52/1250 Mbps.

A high-frequency bit clock can be generated from a 155.52 MHz frequency reference by using an integral frequency synthesizer consisting of a phase-locked loop circuit with a divider in the loop.

Diagnostic loopback (transmitter to receiver) and line loopback (receiver to transmitter) is provided. See Other Operating Modes.

Clock Synthesizer

The clock synthesizer, shown in the block diagram in Figure 2, is a monolithic PLL that generates the serial output clock frequency locked to the input Reference Clock (REFCLKP/N).

The REFCLKP/N input must be generated from a crystal oscillator which has a frequency accuracy of better than the value stated in Table 8 in order for the Transmit Serial Clock (TSCLK) frequency to have the same accuracy required for operation in a SONET system. Lower accuracy crystal oscillators may be used in applications less demanding than SONET/SDH.

The on-chip PLL consists of a phase detector, which compares the phase relationship between the VCO output and the REFCLKP/N input, a loop filter which converts the phase detector output into a smooth DC voltage, and a VCO, whose frequency is varied by this voltage.

The loop filter generates a VCO control voltage based on the average DC level of the phase discriminator output pulses. A single external clean-up capacitor is utilized as part of the loop filter. The loop filter's corner frequency is optimized to minimize output phase jitter.

Timing Generation

The timing generation function, seen in Figure 2, provides a divide by 16 rate version of the transmit serial clock. This circuitry also provides an internally generated load signal, which transfers the PINP/N[15:0] data from the FIFO to the serial shift register.

The PCLK output is a divide by 16 rate version of transmit serial clock (divide by 16). PCLK is intended for use as a divide by 16 clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3059 device.

The timing generator also produces a feedback reference clock to the clock synthesizer. A counter divides the synthesized clock down to the same frequency as the REFCLK. The PLL in the clock synthesizer maintains the stability of the synthesized clock by comparing the phase of the internal clock with that of the REFCLK.

Table 3. Reference Jitter Limits

Operating Mode	Band Width	RMS Jitter
STS-48	12 kHz to 20 MHz	-61 dBc
STS-24	12 kHz to 10 MHz	2 ps
STS-12	12 kHz to 5 MHz	4 ps
STS-3	12 kHz to 1 MHz	16 ps

Parallel-to-Serial Converter

The parallel-to-serial converter shown in Figure 2 is comprised of a FIFO and a parallel-to-serial register. The FIFO input latches the data from the PINP/N[15:0] bus on the rising edge of PICLK. The parallel-to-serial register is a loadable shift register which takes its parallel input from the FIFO output.

An internally generated divide by 16 clock, which is phase aligned to the transmit serial clock as described in the timing generator description, activates the parallel data transfer between registers. The serial data is shifted out of the parallel-to-serial register at the TSCLK rate.

FIFO

A FIFO is added to decouple the internal and external (PICLK) clocks. The internally generated divide by 16 clock is used to clock out data from the FIFO. Phase Initialization (PHINIT) and Lock Detect (LOCKDET) are used to center or reset the FIFO. The PHINIT and LOCKDET signals will center the FIFO after the third PICLK pulse. This is in order to insure that PICLK is stable. This scheme allows the user to have an infinite PCLK to PICLK delay through the ASIC. Once the FIFO is centered, the PCLK to PICLK delay can have a maximum drift specified by Table 18.

FIFO Initialization

The FIFO can be initialized in one of the following three ways:

1. During power up, once the PLL has locked to the reference clock provided on the REFCLK pins, the LOCKDET will go active and initialize the FIFO.

2. When RSTB goes active, the entire chip is reset. This causes the PLL to go out of lock and thus the LOCKDET goes inactive. When the PLL reacquires the lock, the LOCKDET goes active and initializes the FIFO. Note: PCLK is held reset when RSTB is active.

3. The user can also initialize the FIFO by raising PHINIT.

During the normal running operation, the incoming data is passed from the PICLK timing domain to the internally generated divide by 16 clock timing domain. Although the frequency of PICLK and the internally generated clock is the same, their phase relationship is arbitrary. To prevent errors caused by short setup or hold times between the two timing domains, the timing generator circuitry monitors the phase relationship between PICLK and the internally generated clock. When a potential setup or hold time violation is detected, the phase error goes High. When PHERR conditions occur, PHINIT should be activated to recenter the FIFO (at least 2 PCLK periods). This can be done by connecting PHERR to PHINIT. When realignment occurs up to 10 bytes of data will be lost. The user can also take in the PHERR signal, process it and send an output to PHINIT in such a way that idle bytes are lost during the realignment process. PHERR will go inactive when the realignment is complete.

RECEIVER OPERATION

The S3059 receiver chip provides the first stage of the digital processing of a receive SONET STS-48/STS-24/STS-12/STS-3/GBE bit-serial stream. It converts the bit-serial 2.488 Gbps, 1.244 Gbps, 622.08 Mbps, 155.52 Mbps, 1.25 Gbps data stream into a 16-bit parallel data format. A loopback mode is provided for diagnostic loopback (transmitter to receiver). A line loopback (receiver to transmitter) is also provided. Both line and local loopback modes can be active at the same time.

Serial-to-Parallel Converter

The serial-to-parallel converter consists of two 16-bit registers. The first is a serial-in, parallel-out shift register, which performs the serial-to-parallel conversion clocked by the clock recovery block. On the falling edge of the POCLK, the data in the parallel register is transferred to an output parallel register which drives POUTP/N[15:0].

OTHER OPERATING MODES

Diagnostic Loopback

When the Diagnostic Loopback Enable (DLEB) input is active, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes. The differential serial output data from the transmitter is routed to the serial-to-parallel block in place of the normal Receive Serial Data (RSD). TSD/TSCLK outputs are active. DLEB takes precedence over SDLVPECL and SDLVTTL.

Line Loopback

The line loopback circuitry selects the source of the data and clock which is output on TSD and TSCLK. When the Line Loopback Enable (LLEB) input is inactive, it selects data and clock from the parallel to serial converter block. When LLEB is active, it forces the output data multiplexer to select data and clock from the RSD and RSCLK inputs, and a receive-to-transmit loopback can be established at the serial data rate. Diagnostic loopback and line loopback can be active at the same time.

Loop Timing

In Serial Loop Timing (SLPTIME) mode, the clock synthesizer PLL of the S3059 is bypassed, and the timing of the entire transmitter section is controlled by the Receive Serial Clock (RSCLKP/N). This mode is entered by setting the SLPTIME input to an LVTTL high level.

In this mode the REFCLKP/N input is not used. It should be carefully noted that the internal PLL continues to operate in this mode, and continues as the source for the 19MCK and 155MCKP/N, and if these signals are being used (e.g. as the reference for an external S3056 clock recovery device), the REFCLKP/N inputs must be properly driven.

In Reference Loop Timing (RLPTIME) mode, the parallel clock from the receiver (POCLK) is used as the reference clock to the transmitter. In this mode, the REFCLKP/N input is not used. The 19MCK and 155MCKP/N are generated from the POCLK in this operating mode. When operating the S3059 in RLPTIME mode, the 19MCK and 155MCKP/N outputs should not be used as the back-up reference clock for a clock and data recovery device (S3056, S3040). When performing loopback testing (DLEB), the S3059 must not be in RLPTIME.

"Squelched Clock" Operation

Some integrated optical receiver/clock recovery modules force their recovered serial receive clock output to the logic zero state if the optical signal is removed or reduced below a fixed threshold. This condition is accompanied by the expected deassertion of the signal detect output.

The S3059 has been designed for operation with clock recovery devices that provide a continuous serial clock for seamless downstream clocking in the event of optical signal loss.

For operation with an optical transceiver that provides the "squelched clock" behavior as described above, the S3059 can be operated in the "squelched clock" mode by activating the SQUELCH pin.

In this condition, the RSCLKP/N is used for all receiver timing when the SDLVPECL/SDLVTTL inputs are in the active state. When the SDLVPECL/SDLVTTL inputs are placed in the inactive state (usually by the deassertion of LOCKDET or signal detect from the optical transceiver/clock recovery unit) the transmitter serial clock will be used to maintain timing in the receiver section. This will allow the POCLK to continue to run and the parallel outputs to flush out the last received characters and then assume the all zero state imposed at the serial data input.

It is important to note that in this mode there will be a one time shortening or lengthening of the POCLK cycle, resulting in an apparent phase shift in the POCLK at the deassertion of the SD condition. Another similar phase shift will occur when the SD condition is reasserted.

In the normal operating mode with SQUELCH inactive, there will be no phase discontinuities at the POCLK output during signal loss or reacquisition (assuming operation with continuous clocking from the CRU device such as the AMCC S3040, S3050, or S3056).

Table 4. S3059 Transmitter Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
PINP0 PINN0 PINP1 PINN1 PINP2 PINN2 PINP3 PINN3 PINP4 PINN4 PINP5 PINN5 PINP6 PINN6 PINP7 PINN7 PINP8 PINN8 PINP9 PINN9 PINP10 PINN10 PINP11 PINN11 PINP12 PINN12 PINP13 PINN13 PINP14 PINN14 PINP15 PINN15	Internally Biased Differential LVPECL	I	B5 A5 B4 A4 C4 B3 C2 C3 D4 C1 D1 D2 E3 E4 E1 E2 F3 F4 G4 F1 G2 G3 H4 G1 H2 H3 J3 J4 J1 J2 K3 K4	Parallel Input Data, aligned to the PICLK parallel input clock. PINP/N15 is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PINP/N0 is the least significant bit (corresponding to bit 16 of each PCM word, the last bit transmitted). PINP/N[15:0] is sampled on the rising edge of PICLK.
PICLKP PICLKN	Internally Biased Differential LVPECL	I	A6 A7	Parallel Input Clock, a divide by 16, nominally 50% duty cycle input clock, to which PINP/N[15:0] is aligned. PICLK is used to transfer the data on the PINP/N inputs into a holding register in the parallel-to-serial converter. The rising edge of PICLKP samples PINP/N[15:0].
CAP1 CAP2	Analog	I	V7 W7	Loop Filter Capacitor. The external loop filter capacitor and resistors are connected to these pins. See Figure 20.
PHINITP PHINITN	Internally Biased Differential LVPECL	I	K1 K2	Phase Initialization. Rising edge will realign internal timing.

Table 4. S3059 Transmitter Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
TSDP TSDN	Differential CML	O	V13 V14	Transmit Serial Data. Serial data stream signals, normally connected to an optical transmitter module.
TSCLKP TSCLKN	Differential CML	O	V10 V11	Transmit Serial Clock that can be used to retime the TSD signal. This clock frequency will depend on RATESEL.
PCLKP PCLKN	Differential LVPECL	O	B8 B9	A reference clock generated by dividing the internal bit clock by 16. It is normally used to coordinate 16 bit parallel transfers between upstream logic and the S3059 device.
PHERRP PHERRN	Differential LVPECL	O	A8 C8	Phase Error. Pulses High during each PCLK cycle for which there is a potential setup/hold timing violation between the internal byte clock and PICLK timing domains.

Table 5. S3059 Receiver Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
RSDP RSDN	Differential CML	I	M17 L17	Receive Serial Data stream signals normally connected to an optical receiver module. Internally biased and terminated.
RSCLKP RSCLKN	Differential CML	I	P17 N17	Receive Serial Clock. Used to supply a clock input for the RSDP/N inputs. Internally biased and terminated.
SDLVPECL	Single Ended LVPECL	I	R19	LVPECL Signal Detect. LVPECL with internal pull-down. Active High when SDLVTTL is held at logic 0. A single-ended 10K LVPECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDLVPECL is inactive, the data on the Receive Serial Data in (RSDP/N) pins will be internally forced to a constant zero. When SDLVPECL is active, data on the RSDP/N pins will be processed normally. When SDLVTTL is to be connected to the optical receiver module instead of SDLVPECL, then SDLVPECL should be tied High to implement an active Low signal detect, or left unconnected to implement an active High signal detect.
SDLVTTL	LVTTL	I	R18	LVTTL Signal Detect. Active High when SDLVPECL is unconnected (logic 0). Active Low when SDLVPECL is held at logic 1. A single-ended LVTTL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDLVTTL is inactive, the data on the RSDP/N pins will be internally forced to a constant zero. When SDLVTTL is active, data on the RSDP/N pins will be processed normally.

Table 5. S3059 Receiver Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
POUTP0 POUTN0 POUTP1 POUTN1 POUTP2 POUTN2 POUTP3 POUTN3 POUTP4 POUTN4 POUTP5 POUTN5 POUTP6 POUTN6 POUTP7 POUTN7 POUTP8 POUTN8 POUTP9 POUTN9 POUTP10 POUTN10 POUTP11 POUTN11 POUTP12 POUTN12 POUTP13 POUTN13 POUTP14 POUTN14 POUTP15 POUTN15	Differential LVPECL	O	K17 K16 K19 K18 J17 J16 H19 J18 H18 H17 G18 G19 F19 G17 F17 F18 E18 E19 E16 E17 D16 D17 C17 C18 B15 C15 C14 A15 C13 A14 A13 B13	Parallel Data Output bus, aligned to the Parallel Output Clock (POCLK). POUTP/N15 is the most significant bit (corresponding to bit 1 of each PCM word, the first bit received). POUTP/N0 is the least significant bit. POUTP/N[15:0] is updated on the falling edge of POCLKP.
POCLKP POCLKN	Differential LVPECL	O	B11 B12	Parallel Output Clock. A divide by 16, nominally 50% duty cycle, parallel output clock that is aligned to POUTP/N[15:0] word serial output data. POUTP/N[15:0] is updated on the falling edge of POCLKP.

Table 6. S3059 Common Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
SQUELCH	LVTTL	I	T18	RSCLK Clock Squelch. Active High. When SQUELCH is active and SD is inactive, the transmit clock will be used in place of the RSCLK.
REFCLKP REFCLKN	Internally Biased Differential LVPECL	I	R3 R2	Reference Clock input. Used as the reference for the internal bit clock frequency synthesizer.
DLEB	LVTTL	I	R17	Diagnostic Loopback Enable. Active Low. Selects diagnostic loopback. When DLEB is inactive, the S3059 device uses the primary data (RSD) and clock (RSCLK) inputs. When active, the S3059 device uses the diagnostic loopback clock and data from the transmitter. TSD/TSCLK is active in DLEB.
LLEB	LVTTL	I	T16	Line Loopback Enable. Active Low. Selects line loopback. When LLEB is active, the S3059 will route the data from the RSD/RSCLK inputs to the TSD/TSCLK outputs.
KILLRXCLK	LVTTL	I	R16	Kill Receive Clock Input. For normal operation, KILLRXCLK is High. When this input is Low, it will force POCLK output to a logic "0" state.
SLPTIME	LVTTL	I	U4	Serial Clock Loop Time Select input. Active High. When active, SLPTIME enables the recovered clock from the receive section to be used in place of the synthesized transmit clock.
RLPTIME	LVTTL	I	W4	Reference Clock Loop Time Select input. Active High. When active, RLPTIME enables POCLK from the receiver to be used as the reference clock input to the transmitter.
RSTB	LVTTL	I	T17	Master Reset. Reset input for the device, Active Low. During Reset, all clocks are disabled.
TESTEN	LVTTL	I	T3	Test Enable. Used for production testing. Low for normal operation.
155MCKP 155MCKN	Differential LVPECL	O	V16 W17	155.52 MHz Clock output from the clock synthesizer. This output should be connected to the reference clock input of the external clock recovery function (such as the S3040, S3050 or S3056).
19MCK	Single Ended LVPECL	O	U16	19.44 MHz Clock output from the clock synthesizer. This output should be connected to the reference clock input of the external clock recovery function.
LOCKDET	LVTTL	O	L1	Lock Detect. Active High. Goes active after the PLL has locked to the clock provided on the REFCLK pins. LOCKDET is an asynchronous output.

Table 6. S3059 Common Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
RATESEL0 RATESEL1	LVTTL	I	V4 U5	Selects the operating mode. (See Table 1.)
BYPASSCLKP BYPASSCLKN	Differential CML	I	N2 M2	Provides an alternative serial clock bypassing the internal VCO. Internally biased and terminated.
BYPASS	LVTTL	I	T2	Bypass Clock Select. Active High. Selects between BYPASS clock and the VCO clock. REFCLKP/N must not be floating in BYPASS mode. It should be tied to High or Low.
AGND	GND		U6, U7, V8	Ground (0 V)
AVCC	+3.3 V		U8, W5, W6	Power Supply
TXCOREVCC	+3.3 V		A9, P2, U15	Power Supply
TXCOREGND	GND		A10, P1, W15	Ground (0 V)
TTLVCC	+3.3 V		T1, U17	Power Supply
TTLGND	GND		P18, V5	Ground (0 V)
GND	GND		L2, L18, T4, U2, U9, V6, V9, W8, W16	Ground (0 V)
TSCLKGND	GND		W9, W11	Ground (0 V)
TSCLKVCC	+3.3 V		U10, U11	Power Supply
TSDGND	GND		V12, W14	Ground (0 V)
TSDVCC	+3.3 V		U12, U14	Power Supply
RSCLKVCC	+3.3 V		P16	Power Supply
RSCLKGND	GND		N16	Ground (0 V)
RSDVCC	+3.3 V		L16	Power Supply
RSDGND	GND		M16	Ground (0 V)
RXCOREVCC	+3.3 V		A11, M18	Power Supply
RXCOREGND	GND		C10, N18	Ground (0 V)
POUTVCC	+3.3 V		A12, A16, F16, H16, L19	Power Supply

Table 6. S3059 Common Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
POUTGND	GND		B14, D18, G16, J19	Ground (0 V)
PINVCC	+3.3 V		B6, D3, H1	Power Supply
PINGND	GND		C5, C7, F2, L4	Ground (0 V)
PCLKVCC	+3.3 V		C9, C11	Power Supply
PCLKGND	GND		B7, C12	Ground (0 V)
REFCLKVCC	+3.3 V		R4	Power Supply
REFGND	GND		R1	Ground (0 V)
BYPCLKVCC	+3.3 V		N3	Power Supply
BYPCLKGND	GND		M3	Ground (0 V)
VCC	+3.3 V		M4, U3, V17	Power Supply
NC			A1, A2, A3, A17, A18, A19, B1, B2, B10, B16, B17, B18, B19, C6, C16, C19, D19, L3, M1, M19, N1, N4, N19, P3, P4, P19, T19, U1, U13, U18, U19, V1, V2, V3, V15, V18, V19, W1, W2, W3, W10, W12, W13, W18, W19	Not Connected

Figure 3. S3059 Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	NC	NC	NC	PINN1	PINN0	PICLKP	PICLKN	PHERRP	TXCORE VCC	TXCORE GND	RXCORE VCC	POUTVCC	POUTP15	POUTN14	POUTN13	POUTVCC	NC	NC	NC
B	NC	NC	PINN2	PINP1	PINP0	PINVCC	PCLKGND	PCLKP	PCLKN	NC	POCLKP	POCLKN	POUTN15	POUTGND	POUTP12	NC	NC	NC	NC
C	PINN4	PINP3	PINN3	PINP2	PINGND	NC	PINGND	PHERRN	PCLKVCC	RXCORE GND	PCLKVCC	PCLKGND	POUTP14	POUTP13	POUTN12	NC	POUTP11	POUTN11	NC
D	PINP5	PINN5	PINVCC	PINP4												POUTP10	POUTN10	POUTGND	NC
E	PINP7	PINN7	PINP6	PINN6												POUTP9	POUTN9	POUTP8	POUTN8
F	PINN9	PINGND	PINP8	PINN8												POUTVCC	POUTP7	POUTN7	POUTP6
G	PINN11	PINP10	PINN10	PINP9												POUTGND	POUTN6	POUTP5	POUTN5
H	PINVCC	PINP12	PINN12	PINP11												POUTVCC	POUTN4	POUTP4	POUTP3
J	PINP14	PINN14	PINP13	PINN13												POUTN2	POUTP2	POUTN3	POUTGND
K	PHINITP	PHINITN	PINP15	PINN15												POUTN0	POUTP0	POUTN1	POUTP1
L	LOCKDET	GND	NC	PINGND												RSDVCC	RSDN	GND	POUTVCC
M	NC	BYPASS CLKN	BYPCLK GND	VCC												RSDGND	RSDP	RXCORE VCC	NC
N	NC	BYPASS CLKP	BYPCLK VCC	NC												RSCLK GND	RSCLKN	RXCORE GND	NC
P	TXCORE GND	TXCORE VCC	NC	NC												RSCLK VCC	RSCLKP	TTL GND	NC
R	REFGND	REFCLKN	REFCLKP	REFCLK VCC												KILLRX CLK	DLEB	SDLVTTL	SDLVPECL
T	TTLVCC	BYPASS	TESTEN	GND												LLEB	RSTB	SQUELCH	NC
U	NC	GND	VCC	SLPTIME	RATESEL1	AGND	AGND	AVCC	GND	TSCLK VCC	TSCLK VCC	TSDVCC	NC	TSDVCC	TXCORE VCC	19MCK	TTLVCC	NC	NC
V	NC	NC	NC	RATESEL0	TTLGND	GND	CAP1	AGND	GND	TSCLKP	TSCLKN	TSDGND	TSDP	TSDN	NC	155MCKP	VCC	NC	NC
W	NC	NC	NC	RLPTIME	AVCC	AVCC	CAP2	GND	TSCLK GND	NC	TSCLK GND	NC	NC	TSDGND	TXCORE GND	GND	155MCKN	NC	NC

Figure 4. S3059 Pinout (Bottom View)

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
NC	NC	NC	POUTVCC	POUTN13	POUTN14	POUTP15	POUTVCC	RXCORE VCC	TXCORE GND	TXCORE VCC	PHERRP	PICLKN	PICLKP	PINNO	PINN1	NC	NC	NC	A
NC	NC	NC	NC	POUTP12	POUTGND	POUTN15	POCLKN	POCLKP	NC	PCLKN	PCLKP	PCLKGND	PINVCC	PINP0	PINP1	PINN2	NC	NC	B
NC	POUTN11	POUTP11	NC	POUTN12	POUTP13	POUTP14	PCLKGND	PCLKVCC	RXCORE GND	PCLKVCC	PHERRN	PINGND	NC	PINGND	PINP2	PINN3	PINP3	PINN4	C
NC	POUTGND	POUTN10	POUTP10												PINP4	PINVCC	PINN5	PINP5	D
POUTN8	POUTP8	POUTN9	POUTP9												PINN6	PINP6	PINN7	PINP7	E
POUTP6	POUTN7	POUTP7	POUTVCC												PINN8	PINP8	PINGND	PINN9	F
POUTN5	POUTP5	POUTN6	POUTGND												PINP9	PINN10	PINP10	PINN11	G
POUTP3	POUTP4	POUTN4	POUTVCC												PINP11	PINN12	PINP12	PINVCC	H
POUTGND	POUTN3	POUTP2	POUTN2												PINN13	PINP13	PINN14	PINP14	J
POUTP1	POUTN1	POUTP0	POUTN0												PINN15	PINP15	PHINITN	PHINITP	K
POUTVCC	GND	RSDN	RSDVCC												PINGND	NC	GND	LOCKDET	L
NC	RXCORE VCC	RSDP	RSDGND												VCC	BYPCLK GND	BYPASS CLKN	NC	M
NC	RXCORE GND	RSCLKN	RSCLK GND												NC	BYPCLK VCC	BYPASS CLKP	NC	N
NC	TTL GND	RSCLKP	RSCLK VCC												NC	NC	TXCORE VCC	TXCORE GND	P
SDLVPECL	SDLVTTL	DLEB	KILLRX CLK												REFCLK VCC	REFCLKP	REFCLKN	REFGND	R
NC	SQUELCH	RSTB	LLEB												GND	TESTEN	BYPASS	TTLVCC	T
NC	NC	TTLVCC	19MCK	TXCORE VCC	TSDVCC	NC	TSDVCC	TSCLK VCC	TSCLK VCC	GND	AVCC	AGND	AGND	RATESEL1	SLPTIME	VCC	GND	NC	U
NC	NC	VCC	155MCKP	NC	TSDN	TSDP	TSDGND	TSCLKN	TSCLKP	GND	AGND	CAP1	GND	TTLGND	RATESEL0	NC	NC	NC	V
NC	NC	155MCKN	GND	TXCORE GND	TSDGND	NC	NC	TSCLK GND	NC	TSCLK GND	GND	CAP2	AVCC	AVCC	RLPTIME	NC	NC	NC	W

Figure 5. 218 TBGA Package

DIMENSIONS (are in millimeters)

UNIT	A	A₁	D	D₁	E	E₁	P	b	c	e
MIN	1.45	0.60	24.80		24.80			0.65	0.85	
NOM	1.55	0.65	25.00	22.86 BSC.	25.00	22.86 BSC.		0.75	0.90	1.27 BSC.
MAX	1.65	0.70	25.20		25.20		0.25	0.85	0.95	
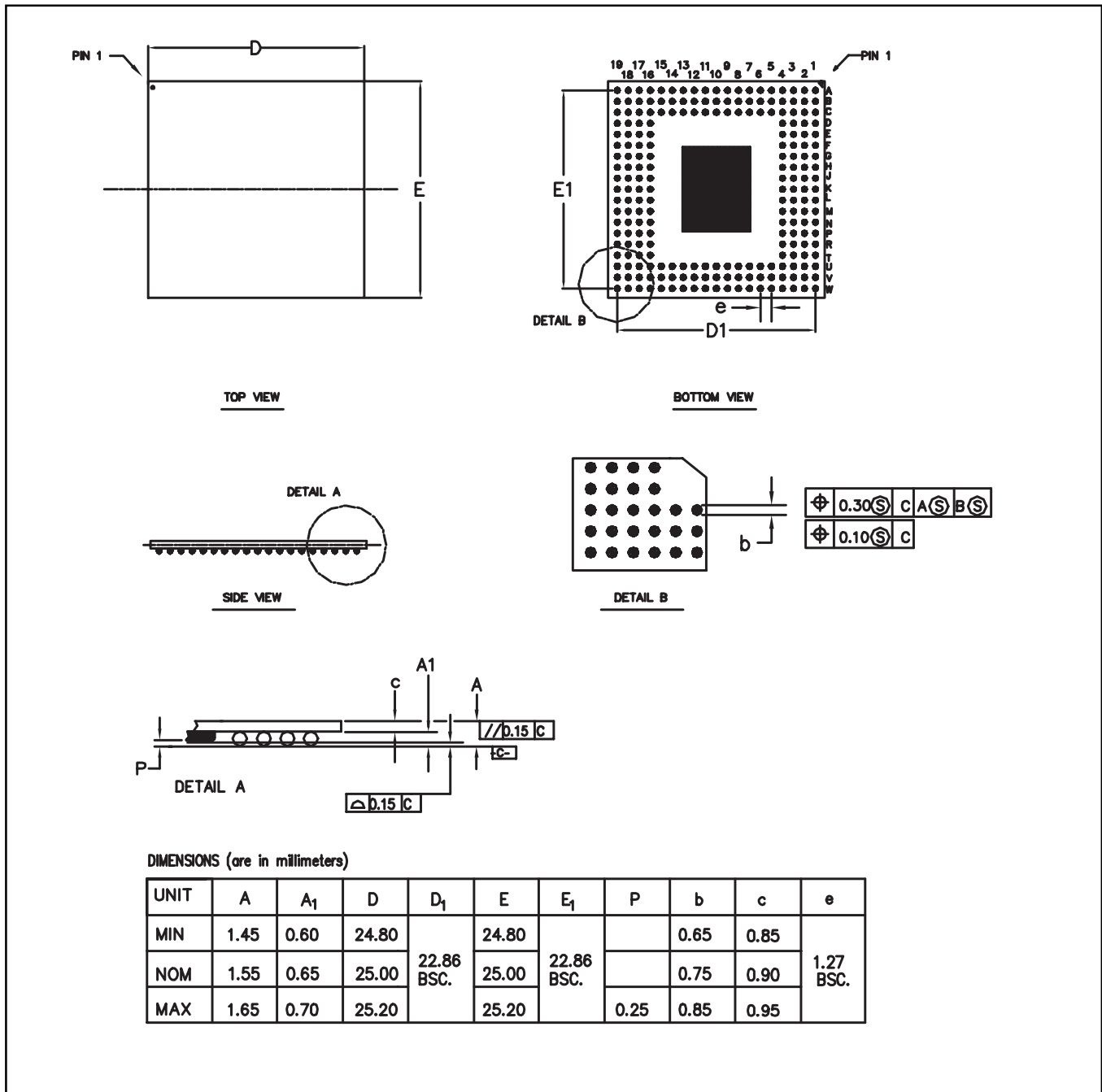
Table 7. Thermal Management

Device	Package Max Power	Θja (Still Air)	Θjc
S3059	2.8 W	16 ˚C/W	1.8 ˚C/W

Table 8. Performance Specifications

Parameter	Min	Typ	Max	Units	Conditions
Nominal VCO Center Frequency		2.488		GHz	
Output Jitter STS-48 STS-24/Gigabit Ethernet (not tested) STS-12 STS-3			0.007 0.006 0.005 0.004	UI (rms)	Note: Output jitter measured at SONET operating rate using appropriate filter. rms jitter, in lock.
Reference Clock Frequency Tolerance	−100		+100	ppm	± 20 is required to meet SONET output frequency specification.
Reference Clock Input Duty Cycle	45		55	%	
Reference Clock Rise and Fall Times			1.5	ns	10% to 90% of amplitude.
REFCLK to PCLK Delay	0		6.4	ns	Guaranteed by design. Not Tested.
Bit Latency. Number of clock cycles after PINP/N[X] appears at TSDP/N.		5		PICLK Cycles	Guaranteed by design. Not Tested.

Table 9. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		150	˚C
Voltage on V_{CC} with respect to GND	-0.5		+3.6	V
Voltage on any LVPECL Input Pin	0		V_{CC}	V
High Speed LVPECL Output Source Current			24	mA

Electrostatic Discharge (ESD) Ratings
The S3059 is rated to the following voltages based on the human body model:
1. All pins are rated 100 Volts except pin # V7(CAP1), W7(CAP2), N17(RSCLKN), P17(RSCLKP), R2(REFCLKN), R3(REFCLKP), M2(BYPASSCLKN), N2(BYPASSCLKP), M17(RSDP), and L17(RSDN).

Adherence to standards for ESD protection should be taken during the handling of the devices to ensure that the devices are not damaged. The standards to be used are defined in ANSI standard ANSI/ESD S20.20-1999, "Protection of Electrical and Electronic Parts, Assemblies and Equipment." Contact your local FAE or sales representative for appliable ESD application notes.

Table 10. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	-20		85	˚C
Junction Temperature Under Bias			130	˚C
Voltage on V_{CC} with respect to GND	3.135	3.3	3.465	V
Voltage on any LVPECL Input Pin	V_{CC}-2		V_{CC}	V
Voltage on any LVTTL Input Pin	0		V_{CC}	V
ICC[1]		515	610	mA

1. Outputs unterminated.

Table 11. LVTTL Input/Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input High Voltage	2.0		TTL V_{CC}	V	TTL V_{CC} = Max
V_{IL}	Input Low Voltage	0.0		0.8	V	TTL V_{CC} = Max
I_{IH}	Input High Current			50	µA	V_{IN} = 2.4 V
I_{IL}	Input Low Current	-500			µA	V_{IN} = 0.5 V
V_{OH}	Output High Voltage	2.4			V	V_{CC} = Min I_{OH} = -100 µA
V_{OL}	Output Low Voltage			0.5	V	V_{ICC} = Min I_{oL} = 1.5 mA

Table 12. Internally Biased Differential LVPECL Input DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IL}	LVPECL Input Low	V_{CC}-2		V_{CC}-1.4	V	
V_{IH}	LVPECL Input High	V_{CC}-1.25		V_{CC}-0.55	V	
$\Delta V_{INSINGLE}$	Single Ended Input Voltage Swing	200		1200	mV	See Figure 10.
ΔV_{INDIFF}	Diff. Input Voltage Swing	400		2400	mV	See Figure 10.
V_{BIAS}	Input DC Bias	V_{CC}-0.65	V_{CC}-0.5	V_{CC}-0.35	V	

Table 13. Differential LVPECL Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
$\Delta V_{OUTSINGLE}$	Single Ended Output Voltage Swing	500		950	mV	51 Ω to V_{CC} –2V See Figure 10.
$\Delta V_{OUTDIFF}$	Diff. Output Voltage Swing	1000		1900	mV	51 Ω to V_{CC} –2V See Figure 10.
V_{OH}	Output High Voltage	V_{CC}-1.2		V_{CC}-0.65	V	51 Ω to V_{CC} –2V
V_{OL}	Output Low Voltage	V_{CC}-1.95		V_{CC}-1.50	V	51 Ω to V_{CC} –2V

Table 14. Single-Ended LVPECL Input DC Characteristics[1]

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IL}	PECL Input Low Voltage	V_{CC} -2.0		V_{CC} -1.5	V	Guaranteed at -20˚ C.
V_{IL}	PECL Input Low Voltage	V_{CC} -2.0		V_{CC} -1.441	V	Guaranteed at 85˚ C.
V_{IH}	PECL Input High Voltage	V_{CC} -1.2		V_{CC} -0.75	V	Guaranteed at -20˚ C.
V_{IH}	PECL Input High Voltage	V_{CC} -1.023		V_{CC} -0.55	V	Guaranteed at 85˚ C.
I_{IL}	Input Low Current	-100		0	µA	$V_{IL} = V_{CC}$ -2
I_{IH}	Input High Current	+50		350	µA	$V_{IH} = V_{CC}$ -0.5

1. The AMCC LVPECL inputs (V_{IL} AND V_{IH}) are non-temperature compensated I/O which vary at 1.3mV/˚C

Table 15. Single-Ended LVPECL Output DC Characteristics[1]

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OL}	PECL Output Low Voltage	V_{CC} -1.98		V_{CC} -1.63	V	Guaranteed at -20 ˚ C.
V_{OL}	PECL Output Low Voltage	V_{CC} -1.98		V_{CC} -1.57		Guaranteed at 85 ˚ C.
V_{OH}	PECL Output High Voltage	V_{CC} -1.1		V_{CC} -0.850	V	Guaranteed at -20 ˚ C.
V_{OH}	PECL Output High Voltage	V_{CC} -0.95		V_{CC} -0.673		Guaranteed at 85 ˚ C.

1. The AMCC LVPECL outputs are non-temperature compensated I/O which vary at 1.3 mV/˚C

Table 16. CML Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OL} (Data)	CML Output Low Voltage	V_{CC} -1.0		V_{CC} -0.65	V	100 Ω line-to-line.
V_{OH} (Data)	CML Output HighVoltage	V_{CC} -0.35		V_{CC} -0.2	V	100 Ω line-to-line.
$\Delta V_{OUTDIFF}$ (Data)	CML Serial Output Differential Voltage Swing	800		1600	mV	100 Ω line-to-line. See Figure 10.
$\Delta V_{OUTSINGLE}$ (Data)	CML Serial Output Single-ended Voltage Swing	400		800	mV	100 Ω line-to-line at 2.5 Gbps. See Figure 10.
V_{OL} (Clock)	CML Output Low Voltage	V_{CC} -1.5		V_{CC} -0.85	V	100 Ω line-to-line.
V_{OH} (Clock)	CML Output High Voltage	V_{CC} -0.5		V_{CC} -0.25	V	100 Ω line-to-line.
$\Delta V_{OUTDIFF}$ (Clock)	CML Serial Output Differential Voltage Swing	800		1800	mV	100 Ω line-to-line. See Figure 10.
$\Delta V_{OUTSINGLE}$ (Clock)	CML Serial Output Single-ended Voltage Swing	400		900	mV	100 Ω line-to-line at 2.5 GHz. See Figure 10.

Table 17. CML Input DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IL}	CML Input Low	V_{CC} -1.7		V_{CC} -0.6	V	
V_{IH}	CML Input High	V_{CC} -0.55		V_{CC} -0.15	V	
ΔV_{INDIFF}	Differential Input Voltage Swing	300		2400	mV	See Figure 10.
$\Delta V_{INSINGLE}$	Single-Ended Input Voltage Swing	150		1200	mV	See Figure 10.
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	

Table 18. Transmitter AC Timing Characteristics

Parameter	Description	Min	Max	Units
	TSCLK Frequency		2.488	GHz
	TSCLK Duty Cycle	45	55	%
	TSCLK Duty Cycle Distortion w.r.t. RSCLK or BYPASSCLK (In SLPTIME, LLEB or BYPASS modes)		5.0	%
	PICLK Duty Cycle	35	65	%
tS_{PIN}	PINP/N[15:0] Set-up Time w.r.t. PICLK (See Figure 6)	1.5		ns
tH_{PIN}	PINP/N[15:0] Hold Time w.r.t. PICLK (See Figure 6)	0.5		ns
tP_{TSD}	TSCLKP Low to TSDP/N Valid Propagation Delay (See Figure 7)		± 100	ps
tS_{TSD}	TSDP/N Set-up Time w.r.t. TSCLKP Rising (See Figure 7)	100		ps
tH_{TSD}	TSDP/N Hold Time w.r.t. TSCLKP Rising (See Figure 7)	100		ps
	PCLK to PICLK drift after FIFO is centered		5.2	ns
	PCLK Duty Cycle	45	55	%
	PHINIT Pulse Width	2 PICLK Cycles		

Figure 6. Transmitter Input Timing
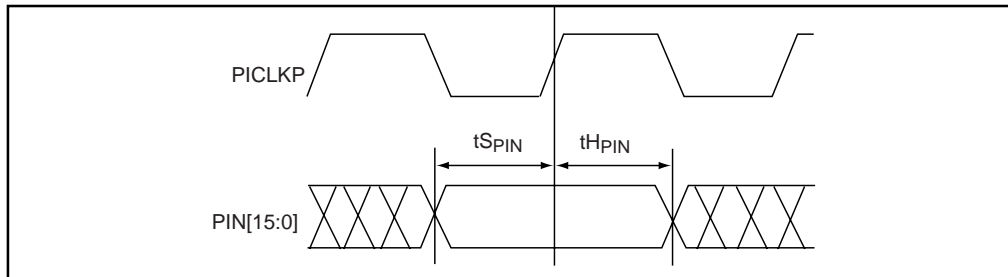
Figure 7. Transmitter Output Timing
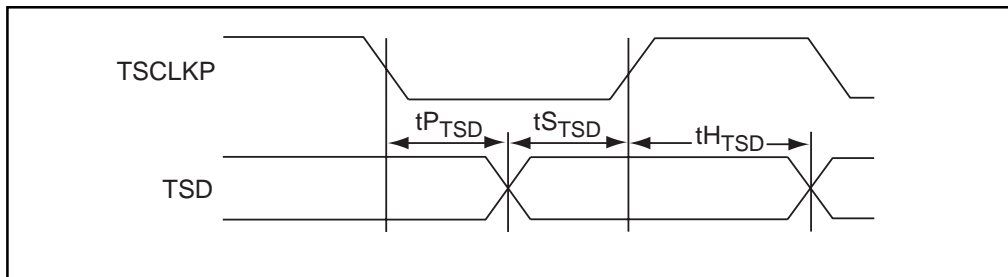
1. When a setup time is specified between an input and a clock, the setup time is from the crossover point of the input to the crossover point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is from the crossover point of the clock to the crossover point of the input.

Table 19. AC Receiver Timing Characteristics

Parameter	Description	Min	Max	Units
	POCLK Duty Cycle	45	55	%
tS_{POUT}	POUTP/N[15:0] Set-up Time w.r.t. POCLKP (See Figure 9)	2.25		ns
tH_{POUT}	POUTP/N[15:0] Hold Time w.r.t. POCLKP (See Figure 9)	2		ns
tS_{RSD}	RSDP/N Set-up Time w.r.t. RSCLKP (See Figure 8)	75		ps
tH_{RSD}	RSDP/N Hold Time w.r.t. RSCLKP (See Figure 8)	75		ps
	RSCLK Duty Cycle	40	60	%
	RSCLK Frequency		2.488	GHz

Figure 8. Receiver Input Timing Diagram
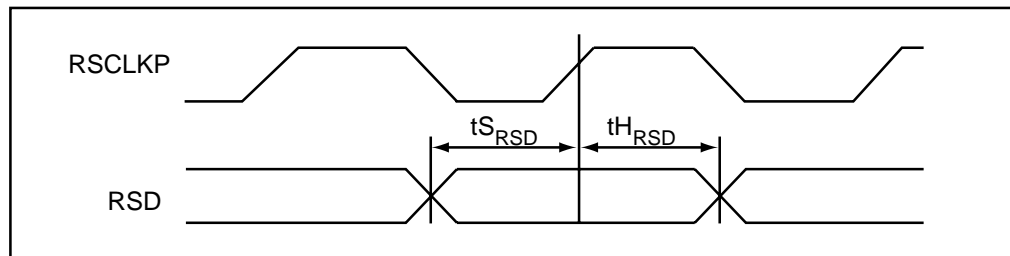
Figure 9. Receiver Output Timing Diagram
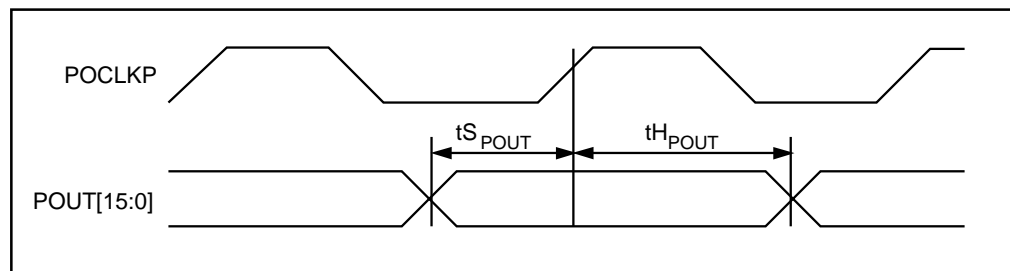
1. When a setup time is specified between an input and a clock, the setup time is from the crossover point of the input to the crossover point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is from the crossover point of the clock to the crossover point of the input.

Figure 10. Differential Voltage Measurement
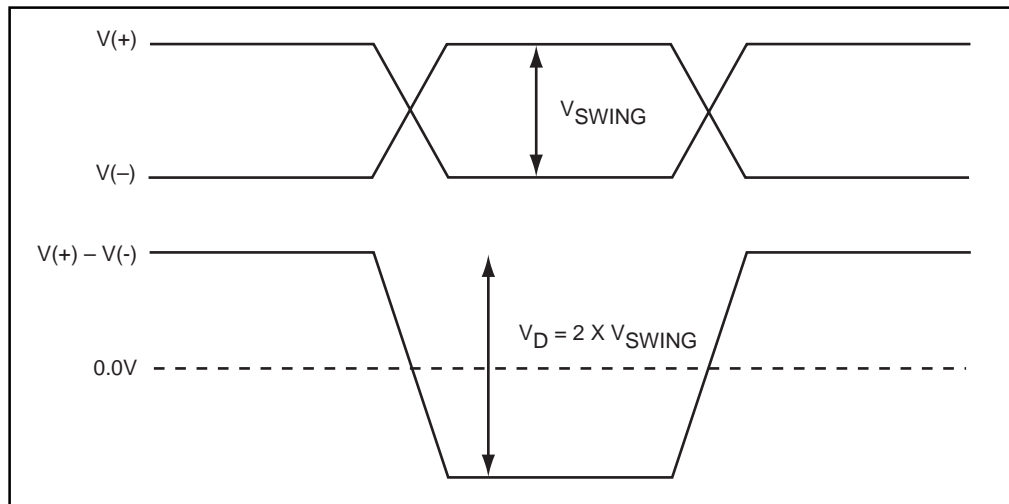
Note: V(+) – V(-) is the algebraic difference of the input signals.

Figure 11. Phase Adjust Timing[1]
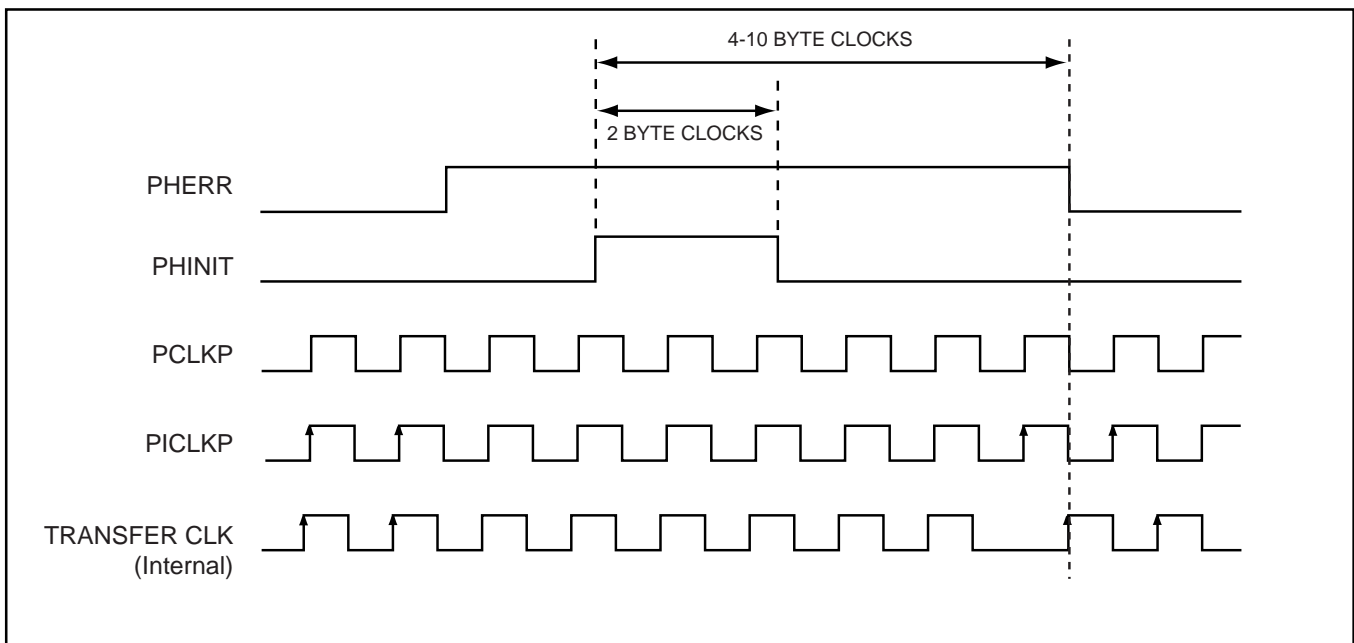
1. Byte clock = 155.52 MHz.

Figure 12. S3056 to S3059 Differential CML Input Termination
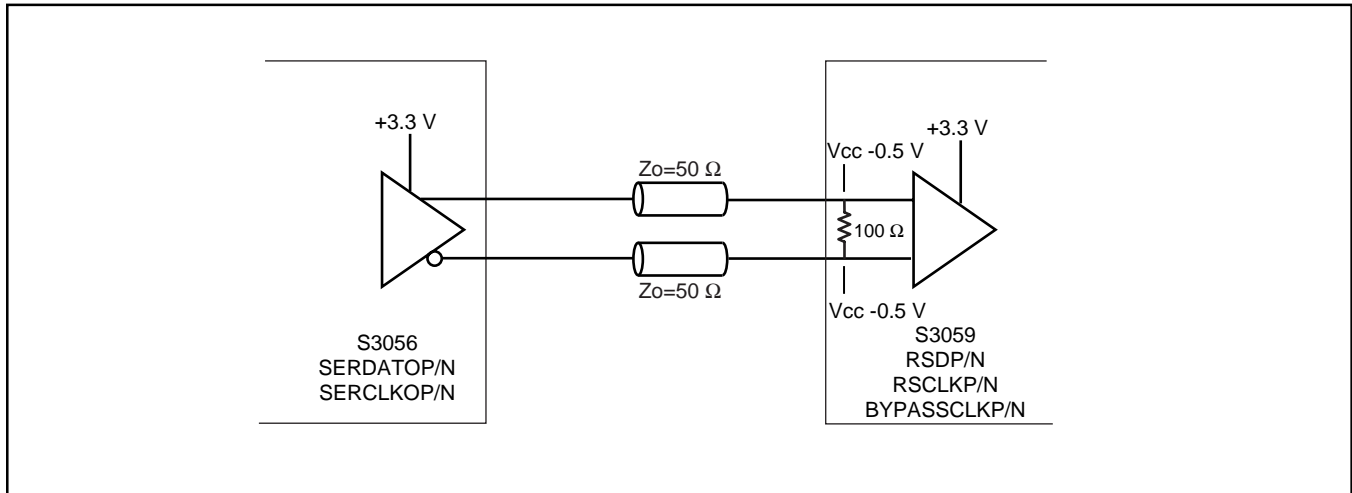
Figure 13. +5V Differential CML Driver to S3059 Differential CML Input AC Coupled Termination
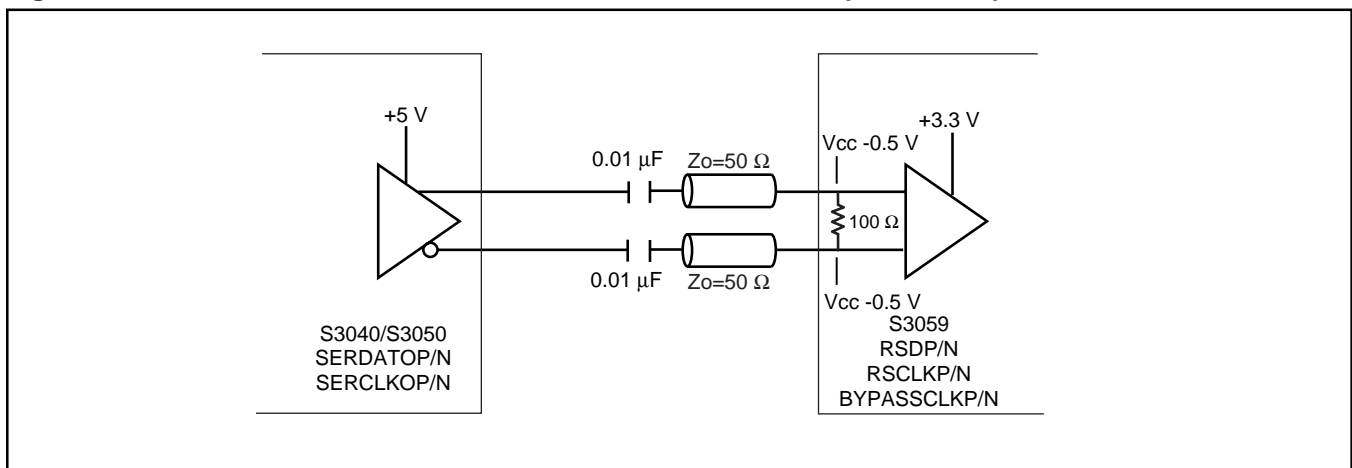
Figure 14. Differential CML Output to +5V PECL Input AC Coupled Termination

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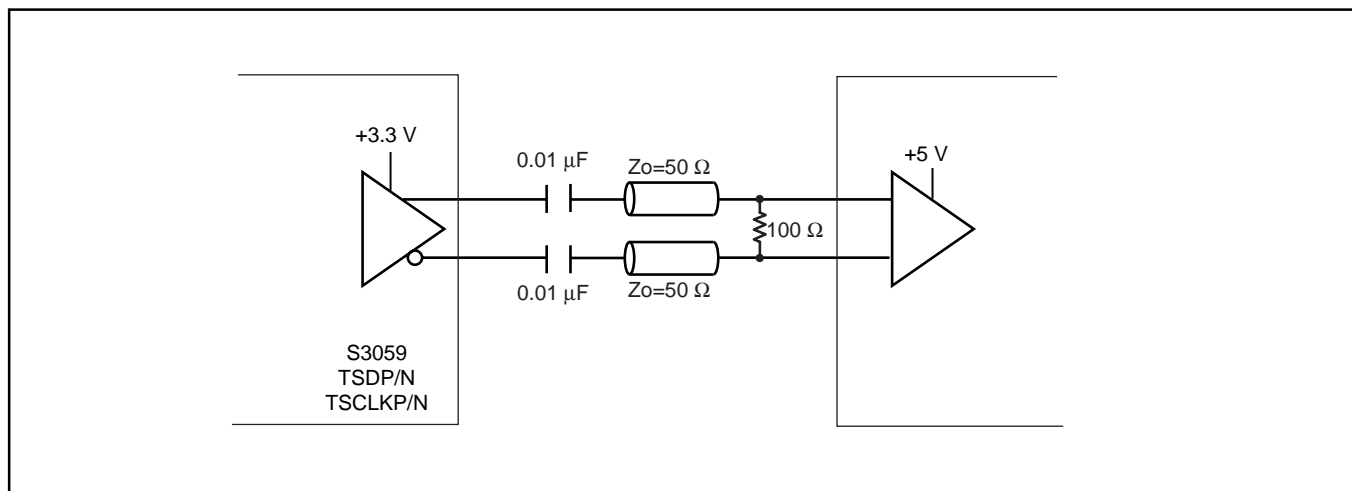
Figure 15. Differential CML Output to +3.3 V PECL Input DC Coupled Termination
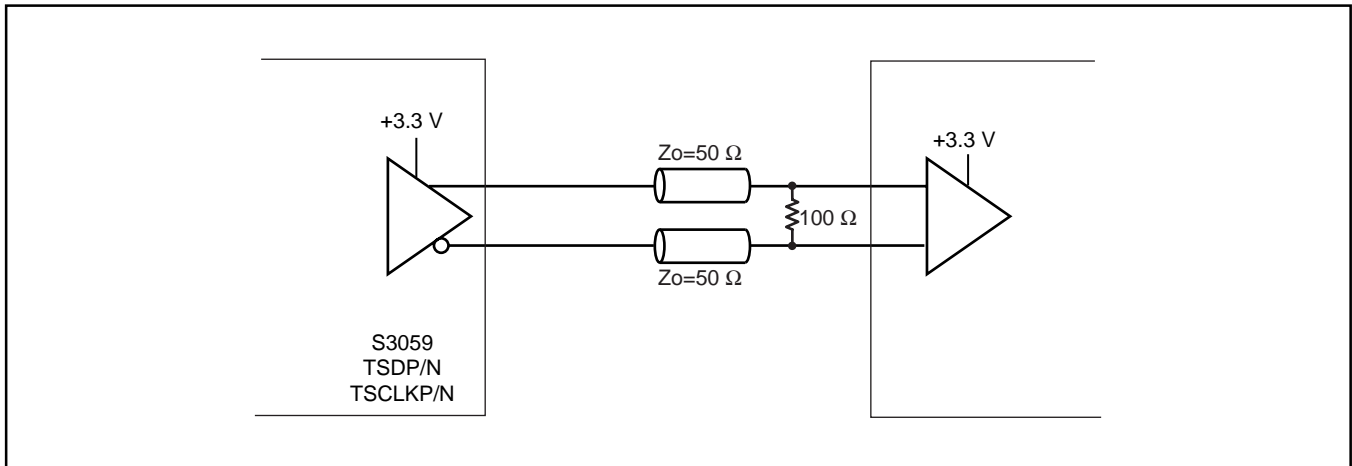
Figure 16. S3059 Differential LVPECL Driver to Differential LVPECL Input Termination
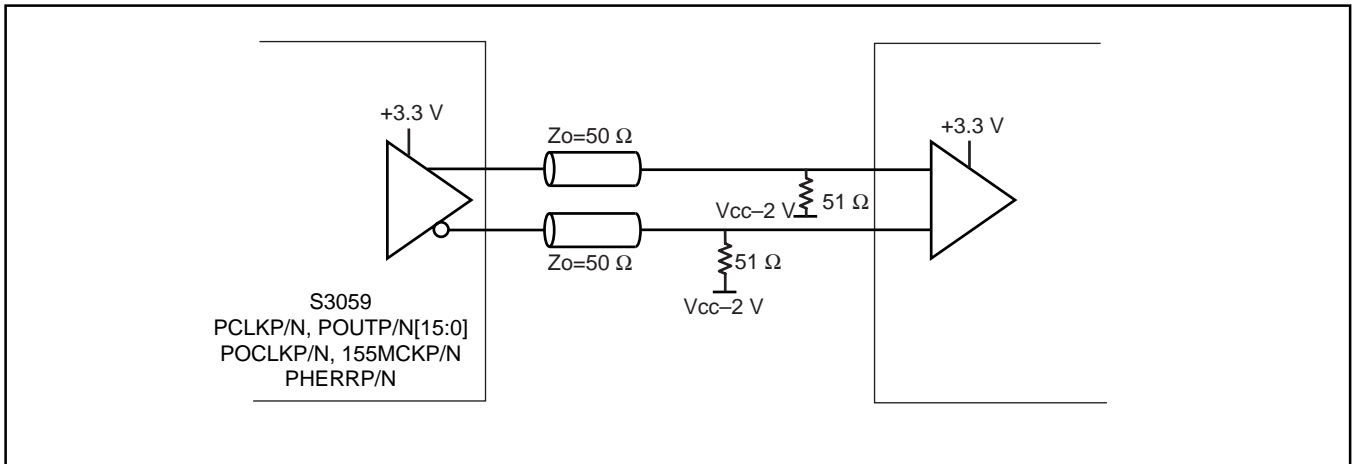
Figure 17. S3059 Differential LVPECL Driver to Differential LVPECL Input Termination
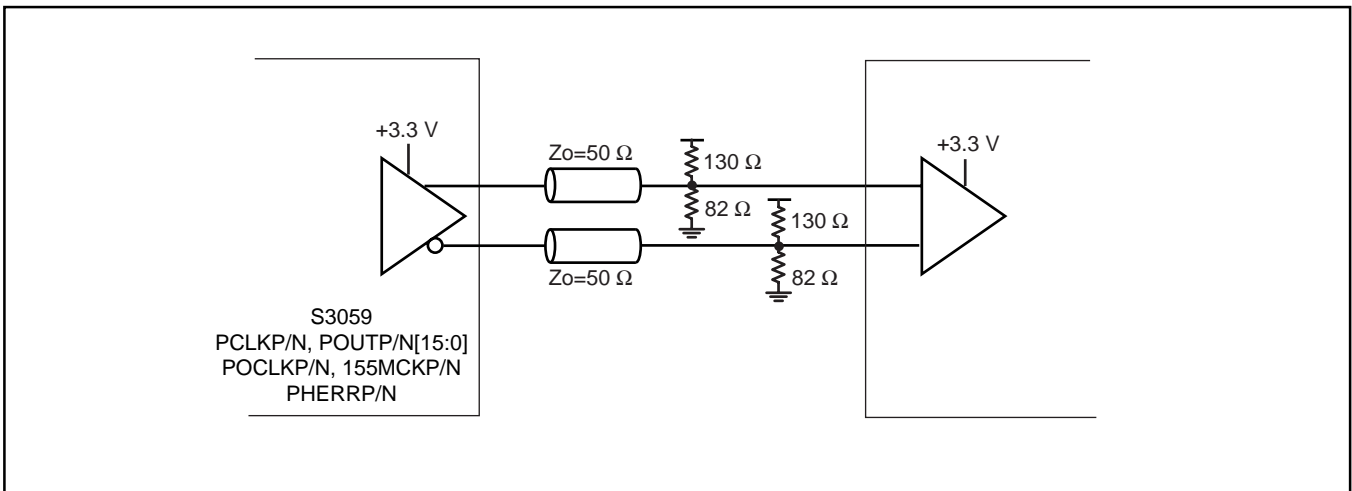
Figure 18. S3059 Differential LVPECL Driver to Differential LVPECL Input Termination[1]
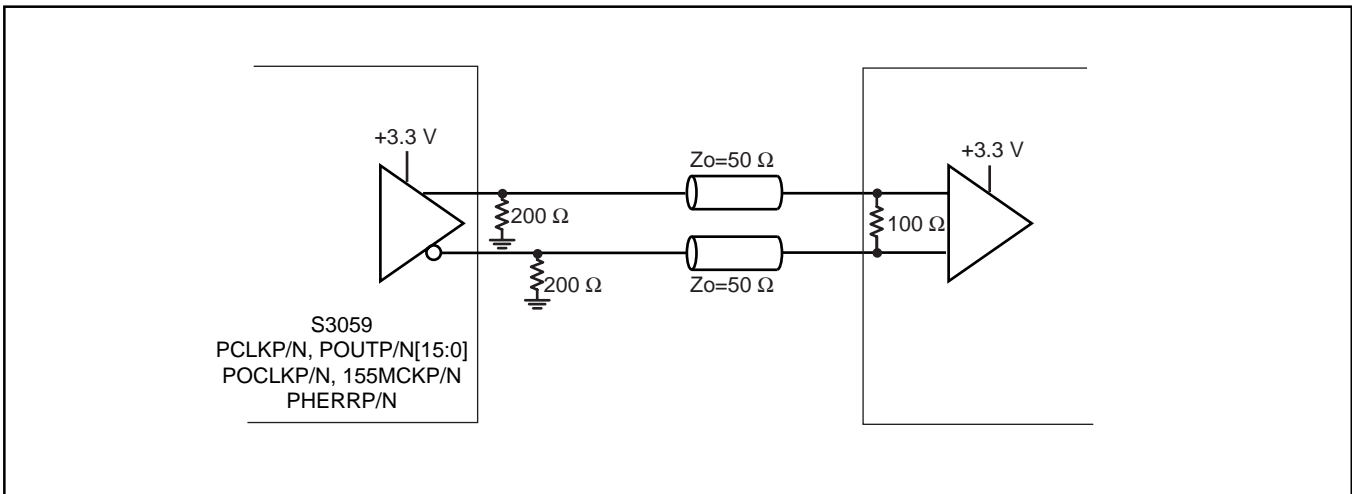
1. With 100 Ω line-to-line, V_{OL} Max increases by 100 mV .

Figure 19. Differential LVPECL Driver to S3059 Internally Biased Differential LVPECL Inputs
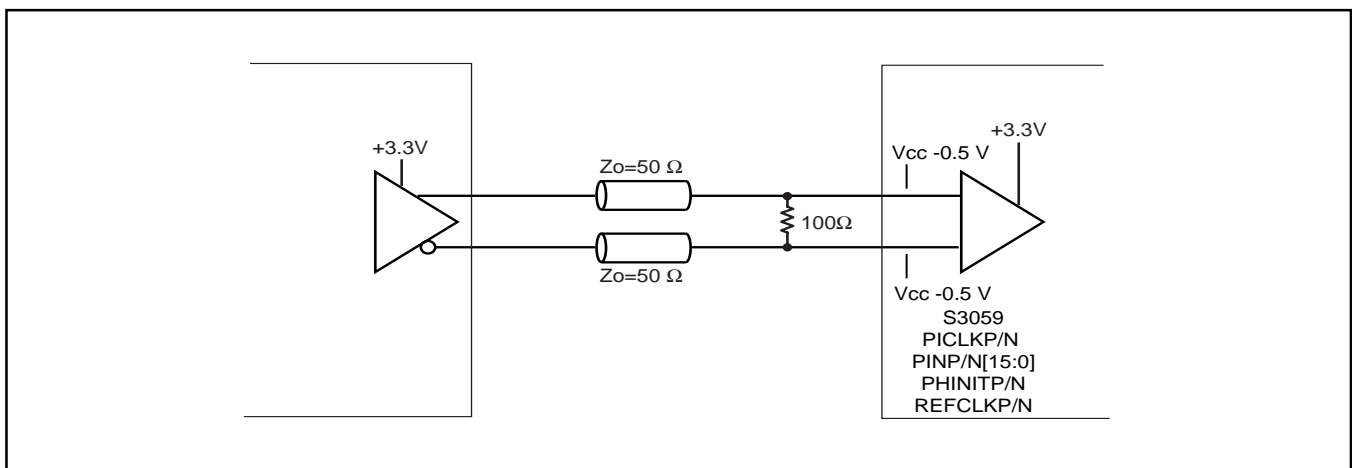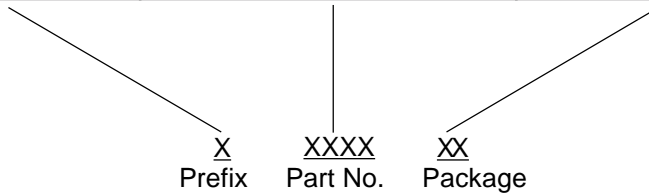
Figure 20. External Loop Filter Components
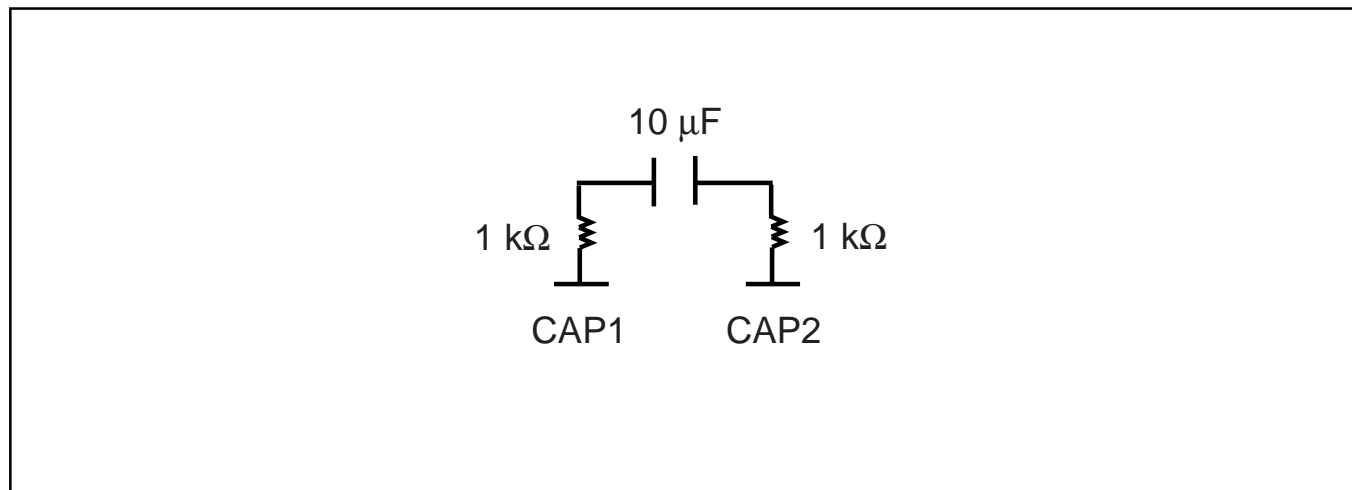
Ordering Information

PREFIX	DEVICE	PACKAGE
S – Integrated Circuit	3059	TB – 218 TBGA

<u>X</u>   <u>XXXX</u>   <u>XX</u>
Prefix   Part No.   Package

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