2.5 GBIT 2 X 2 DUAL CROSSPOINT SWITCH S3054

FEATURES

- Supports 2.5 Gbit/sec Data Rates
- Fully differential for minimum jitter accumulation
- High speed 50Ω source terminated outputs
- 0.83 W Typical power dissipation
- 3.3 V power supply
- 52 Pin TQFP/TEP

GENERAL DESCRIPTION

The S3054 is a high performance 2 x 2 crosspoint switch. It is designed to minimize jitter accumulation by providing a high bandwidth fully differential signal path. A 2 x 2 crosspoint can be used to switch OC-48 data signals in Dense Wavelength Division Multiplexer designs and other high speed serial switch designs.

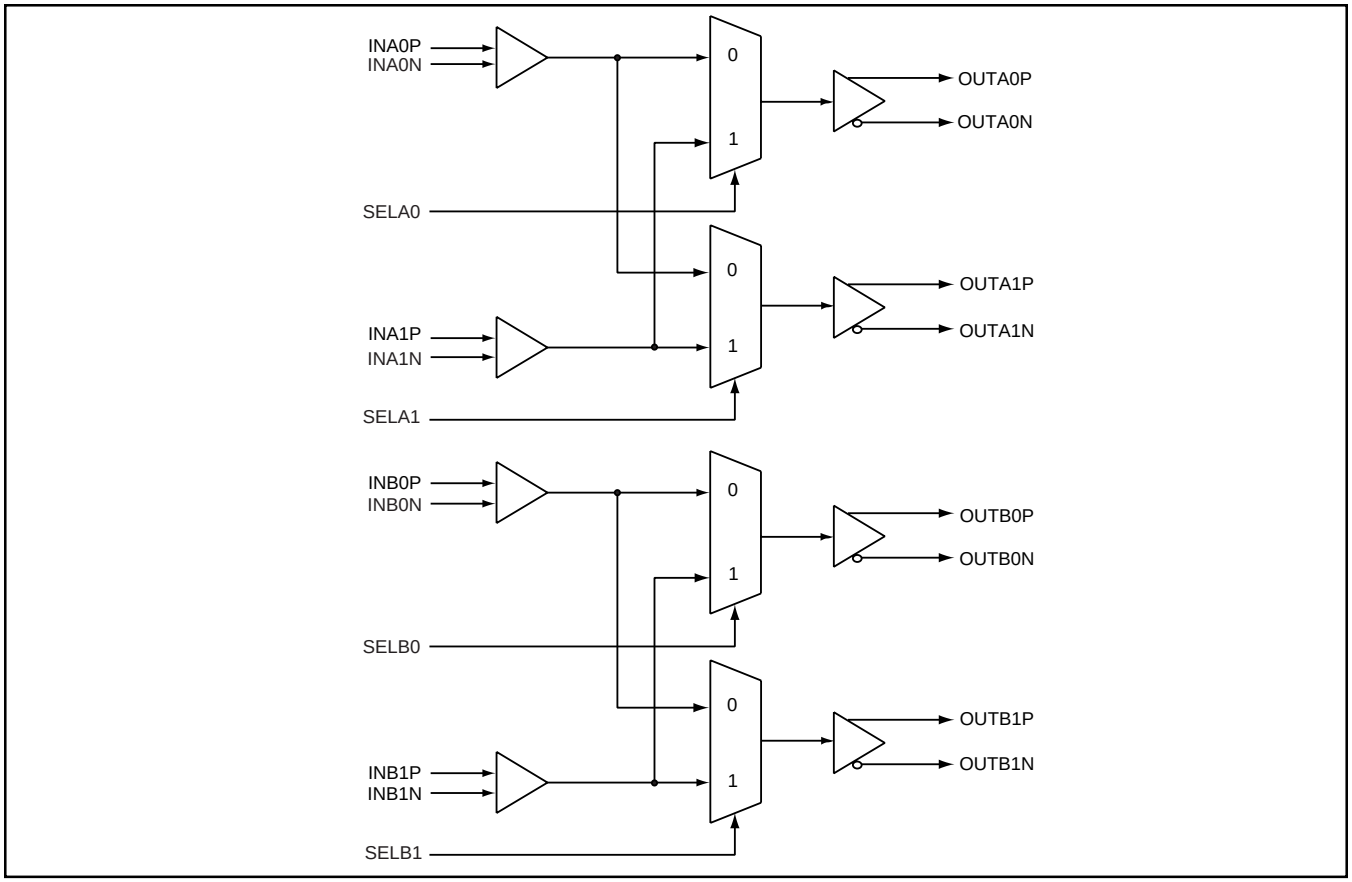
The 2 x 2 crosspoint is designed using two 2:1 multiplexers. It can be used to fan out and/or multiplex high speed data signals. The S3054 is compatible with the AMCC OC-48 clock recovery, MUX/DEMUX and Crosspoint Switch products. This allows signal integrity to be maintained throughout the system design.

Table 1 is a truth table detailing the control of flow through the S3054. The primary AC parameter of importance is the deterministic jitter or data eye degradation inserted by the crosspoint. The design minimizes jitter accumulation by using high bandwidth, low skew fully differential circuits. This provides for symmetric rise and fall delays as well as noise rejection.

Table 1. Truth Table

SELA0/B0	SELA1/B1	OUTA0/B0	OUTA1/B1
0	0	INA0/B0	INA0/B0
0	1	INA0/B0	INA1/B1
1	0	INA1/B1	INA0/B0
1	1	INA1/B1	INA1/B1

Figure 1. S3054 Block Diagram



Programable Swing Control

An external resistor can be connected across adjacent pins, VSWx to VEEx, where x is A0, A1, B0 and B1. This will result in a decreased Vswing for the specified output and a decrease in chip power dissipation. For example, if a 700 Ohm resistor is used, the Vswing will decrease from its full scale swing of approximately 570mV to 250mV and that specific output will draw approximately 13mA less. All four outputs can be independently set. If no external resistor is used, the output swing will default to its full scale value.

The 700 Ohm value is only used as an example. The power conscious user could use as small a resistor value as the application can handle.

Figure 2. Timing Waveforms

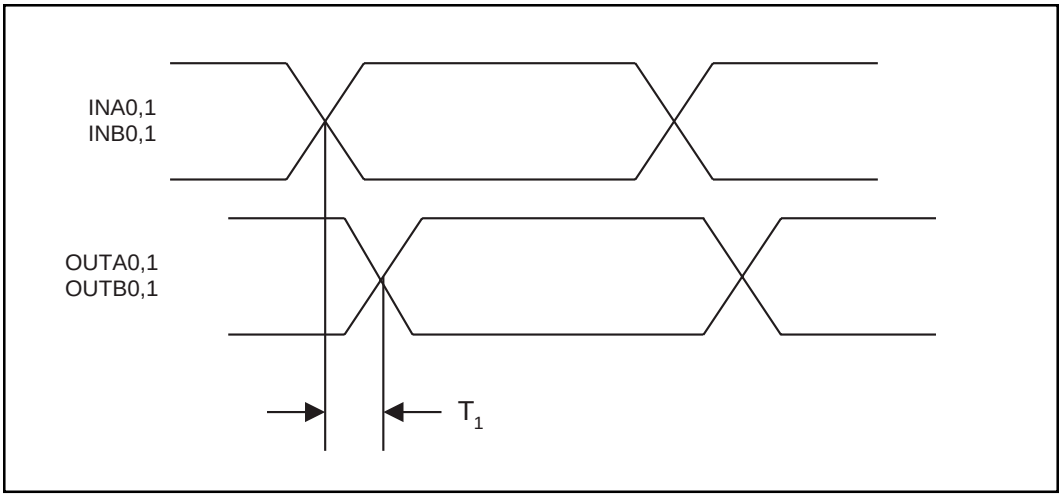


Figure 3. Differential Voltage

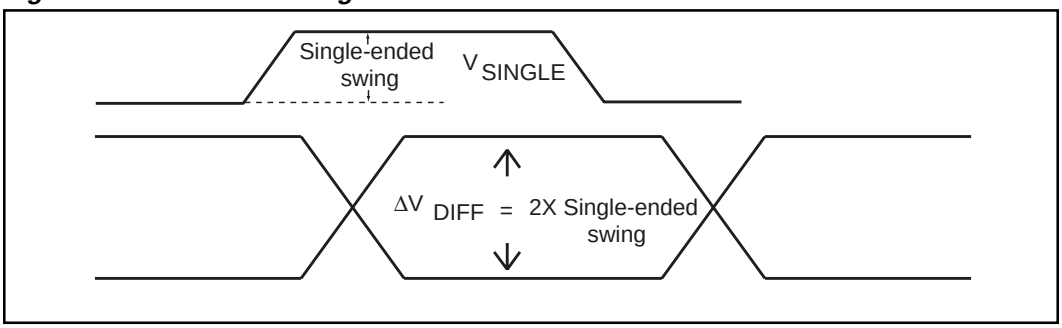


Table 2. Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin#	Description
INA0P INA0N	Diff. LVPECL	I	42 41	Differential input from the downstream PBC port.
INA1P INA1N	Diff. LVPECL	I	50 51	Serial input from the local disk drive.
INB0P INB0N	Diff. LVPECL	I	37 38	Differential input from the downstream PBC port.
INB1P INB1N	Diff. LVPECL	I	29 28	Serial input from the local disk drive.
SELA0	LVTTL	I	43	A Low level selects INA0P/N.
SELA1	LVTTL	I	49	A High level selects INA1P/N.
SELB0	LVTTL	I	36	A Low level selects INB0P/N.
SELB1	LVTTL	I	30	A High level selects INB1P/N.
OUTA0P OUTA0N	Diff. CML	O	23 22	Channel A0 serial output.
OUTA1P OUTA1N	Diff. CML	O	17 18	Channel A1 serial output.
OUTB0P OUTB0N	Diff. CML	O	4 5	Channel B0 serial output.
OUTB1P OUTB1N	Diff. CML	O	10 9	Channel B1 serial output.
VCC			6,8,19 20,21,32 34,45,46 47	Power Supply, 3.3V Nominal.

Table 2. Pin Assignment and Descriptions *(Continued)*

Pin Name	Level	I/O	Pin#	Description
VSWA0 VSWA1 VSWB0 VSWB1	Analog	I	25 15 2 12	Voltage Swing Control.
VEE			1 7 13 14 26 27 31 33 35 39 40 44 48 52	Ground.
VEEA0	Output GND		24	Ground for A0.
VEEA1	Output GND		16	Ground for A1.
VEEB0	Output GND		3	Ground for B0.
VEEB1	Output GND		11	Ground for B1.

Figure 4. S3054 Pinout Package

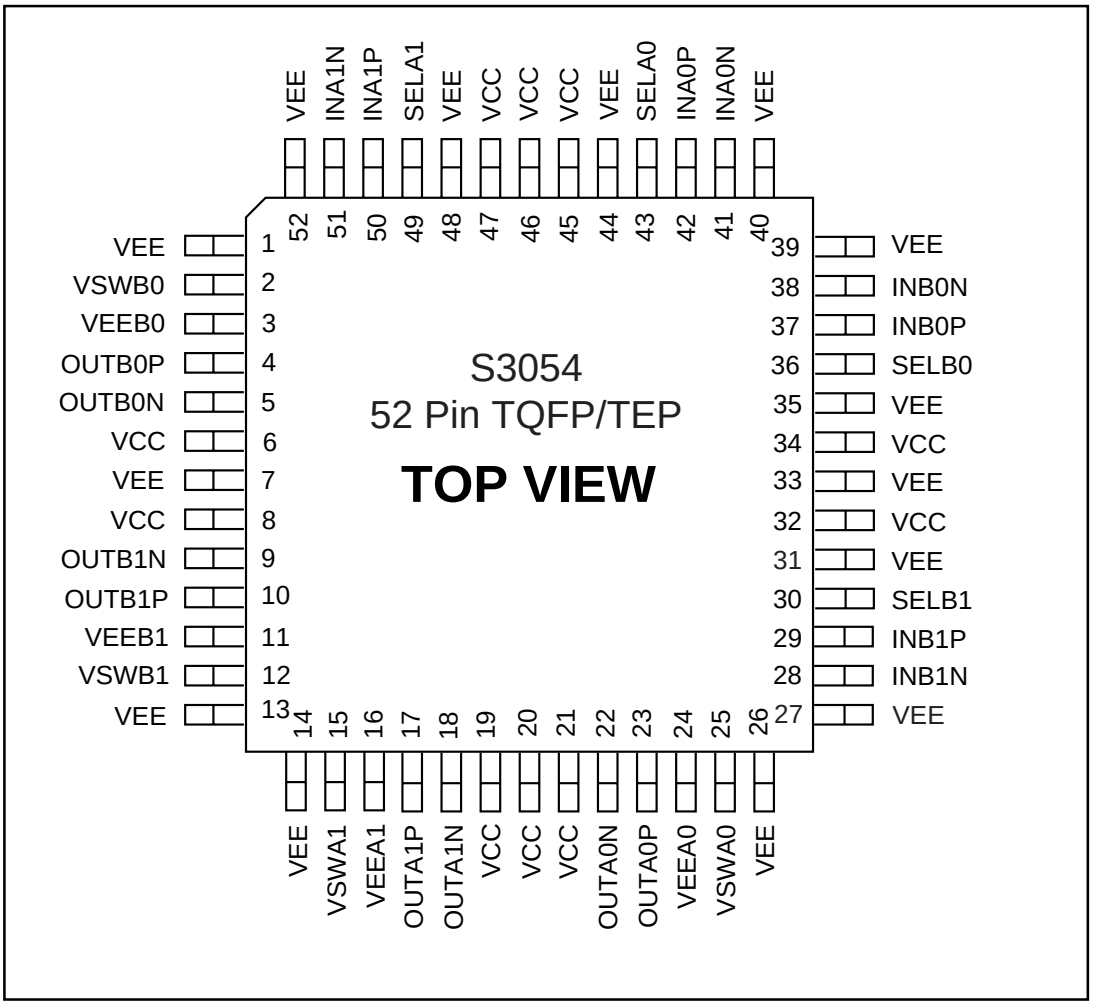
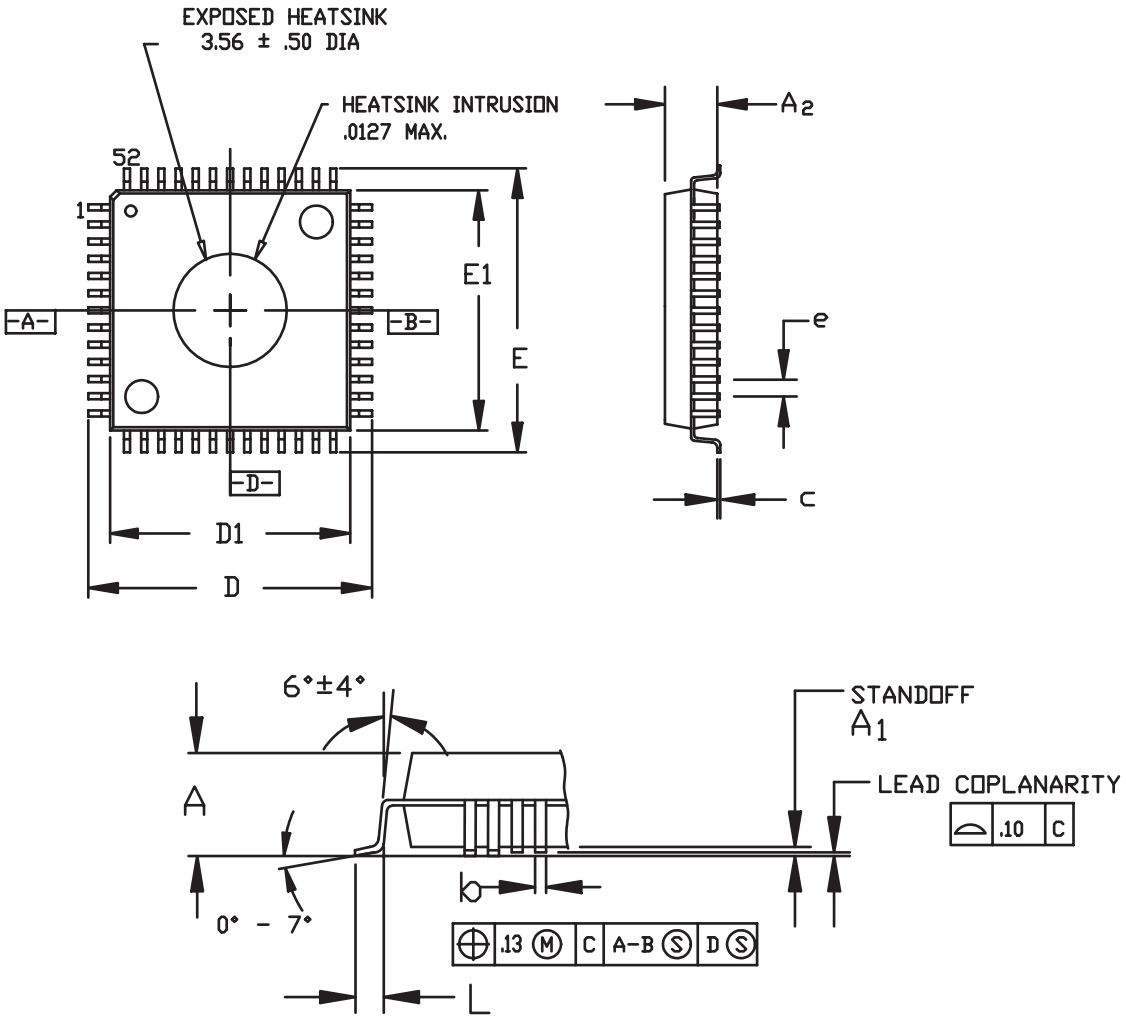


Figure 5. S3054 52 Pin TQFP/TEP Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.05	1.35	11.75	9.90	11.75	9.90	0.50	0.65 BSC.	0.25	0.127
NOM			1.40	12.00	10.00	12.00	10.00	0.60		0.30	
MAX	1.60	0.15	1.45	12.25	10.10	12.25	10.10	0.75		0.35	0.17

Table 3. Thermal Management

Device	Power	Θja Still Air	Θjc Still Air
S3054	1.1W	45.6° C/W	4.2° C/W

Table 4. AC Characteristics *(Over recommended operating conditions.)*

Parameter	Description	Min	Typ	Max	Units	Conditions
T_R	Serial Data rise and fall time. (OUT0, OUT1).			175	ps	20% to 80% tested on a sample basis. (100Ω line-to-line.)
T_F				150	ps	
T1	Flow through propagation delay IN to OUT.			2.0	ns	100Ω line-to-line.
R_J	Random jitter		2	4	ps	
D_J	Deterministic jitter		20		ps	
	Output skew		25		ps	

Table 5. Internally Biased LVPECL Input DC Characterisitics

Symbol	Description	Min	Typ	Max	Units	Conditions
ΔV_{INDIFF}	Differential Input Voltage Swing	300		1200	mV	See Figure 3.
$\Delta V_{INSINGLE}$	Single-ended Input Voltage Swing	150		600	mV	See Figure 3.
R_{DIFF}	Differential Input Resistance	75	100	125	Ω	

Table 6. LVTTL Input DC Characteristics

Symbol	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input High Voltage	2.0			V	Vcc = Max
V_{IL}	Input Low Voltage	0.0		0.8	V	Vcc = Max
V_{IH}	Input High Current			50	µA	V_{IN} = 2.4V
I_{IL}	Input Low Current	-500			µA	V_{IN} = 0.5V

Table 7. CML Output DC Characteristics

Symbol	Description	Min	Typ	Max	Units	Conditions
V_{OL}	Output Low Voltage	VCC -1.0		VCC -.55	V	100Ω line-to-line.
V_{OH}	Output High Voltage	VCC -.35		VCC -.1	V	100Ω line-to-line.
ΔVout Diff	Output Diff Voltage Swing	900		1460	mV	100Ω line-to-line. See Figure 3. Rext = open.
ΔVout Single	Output Single Ended Voltage Swing	450		730	mV	100Ω line-to-line. See Figure 3. Rext = open.

Table 8. Absolute Maximum Ratings[1]

Parameter	Min	Typ	Max	Units
Power Supply Voltage (V_{CC})	0.5		+4	V
Voltage on any LVPECL Input Pin	0		V_{CC}	V
Voltage on any TTL Input Pin	-0.5		V_{CC}+0.5	V
Case Temperature Under Bias (T_C)	-55		125	C°
Storage Temperature (T_{STG})	-65		150	C°
Static Discharge Voltage		500		V

1. CAUTION: Stresses listed under “Absolute Maximum Ratings” may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 9. Recommended Operating Conditions [1]

Parameter	Min	Typ	Max	Units
Power Supply Voltage (V_{CC})	+3.14	3.3	+3.47	V
Ambient Operating Temperature Range (T)	-40		+85	C°
Voltage on any LVPECL Input Pin	Vcc-2		Vcc	V
ICC Supply Current		260	330	mA

1. AMCC guarantees the functional and parametric operation of the part under “Recommended Operating Conditions” (except where specifically noted in the AC and DC Parametric tables).

Input Structures

Two input structures exist in this part; TTL and High Speed, Differential Inputs. The LVTTL Inputs will interface with any LVTTL outputs. The High Speed, Differential Inputs can be AC Coupled. Therefore, the High Speed, differential Input buffers are biased at Vcc -0.5V. Refer to Figure 6 for High Speed Differential Input termination.

Figure 6. Input Termination

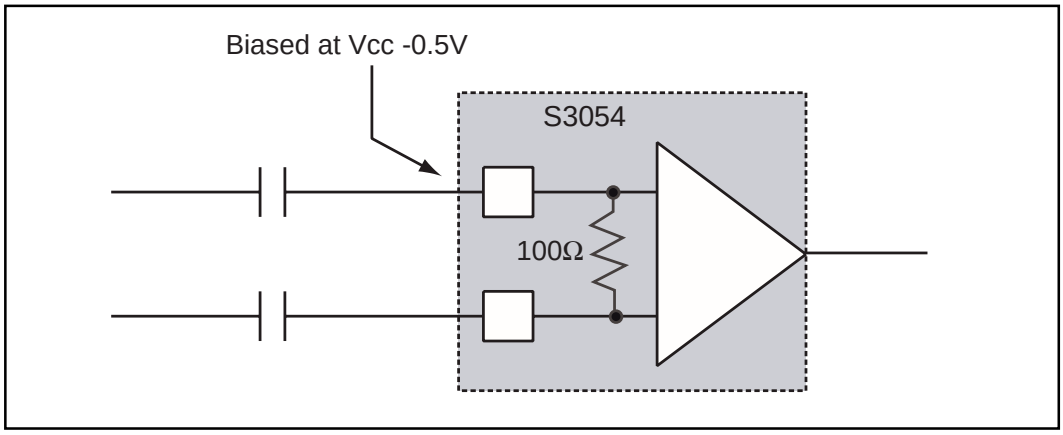
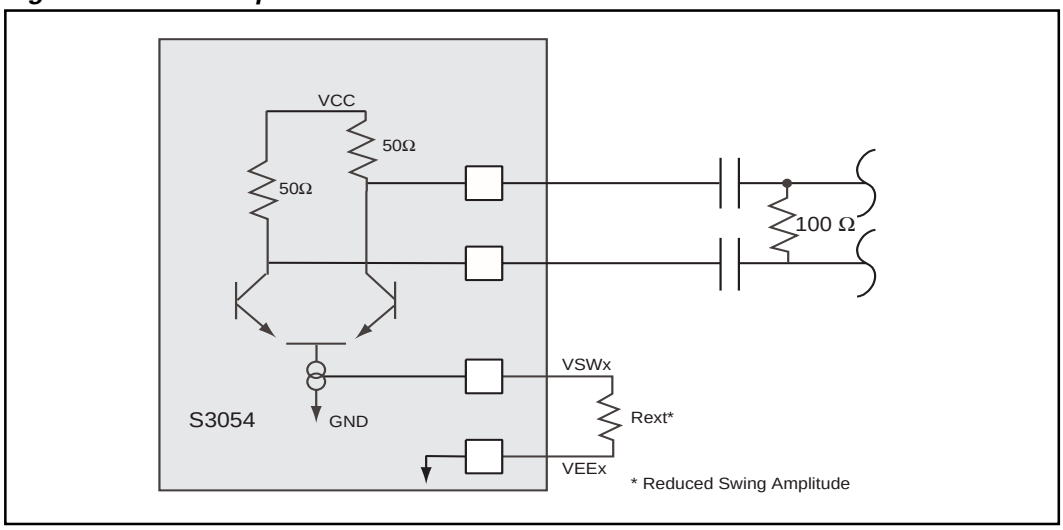
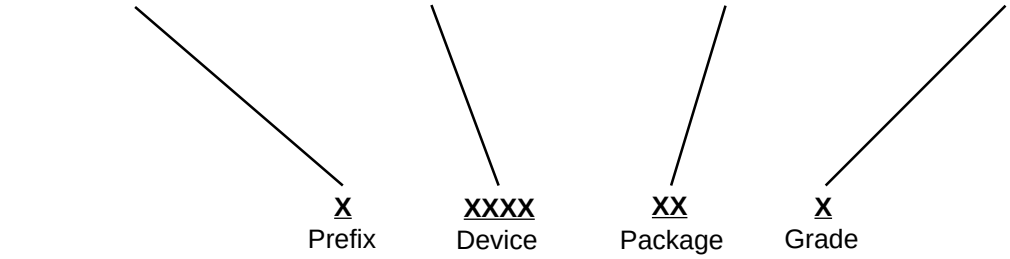


Figure 7. S3054 Output Termination



Ordering Information

PREFIX	DEVICE	PACKAGE	GRADE
S- Integrated Circuit	3054	TT – 52 TQFP/TEP	(blank) – Commercial I – Industrial



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