DESCRIPTION

The S3045 Evaluation Board provides a flexible platform for verifying the operation of the S3045 with a SONET tester. This user's manual provides information on the board contents.

Figure 1 shows the outline of the S3045 Evaluation Board. In Figure 2, the block diagram of how the S3045 Evaluation Board should be connected to the test equipment for SONET/SDH testing is shown. The four possible test configurations are:

1. Use both the input/output on board clock recovery devices (S3040 #1, #2).
2. Use the input on board clock recovery device (S3040 #1).
3. Use the output on board clock recovery device (S3040 #2).
4. Do not use any of the on board clock recovery devices.

Figures 4-7, show the wiring connections for these four test setups.

The SONET network tester compares the received data with the transmitted data to determine whether an error has occurred. The SONET tester can also demonstrate the SONET protocol features of the chipset. In addition, most SONET testers should be able to manipulate any bits being transmitted to the S3045 test board to verify the operation of SONET overhead and alarm functionality.

Required Parts:

The tests can be conducted using a SONET Tester and the Unit Under Test (the S3045 Evaluation Board). The following is a parts list of the items that will be needed.

1. Power cable between the power source and the S3045.
2. S3045 Test Board.
3. One 5 volt power supply (Current rating 2 Amps).
4. SONET/SDH network tester.
5. 50 Ohm SMA terminated test cables.
6. Optional: –5.2V DC supply for VBB as required for SONET termination pulldowns.

Power Connections

Terminal posts are provided at the top edge of the board for VCC (+5V), and GND. The required +5V power supply connected to the board provides the 5 volts for the S3040's. The board contains two power regulators with one providing the 3.3 volts for the S3045, and the other supplying the 3.3 volts for the S3041 and S3042. Figure 3 demonstrates the input and output LVPECL waveforms that the S3045 Evaluation Board will output. (Note that in the final design of the S3045 Evaluation Board, the regulator providing 3.0V and 4.1V will be modified to supply 3.3V by replacing R2 and R12.)

Figure 1. Test Board Layout

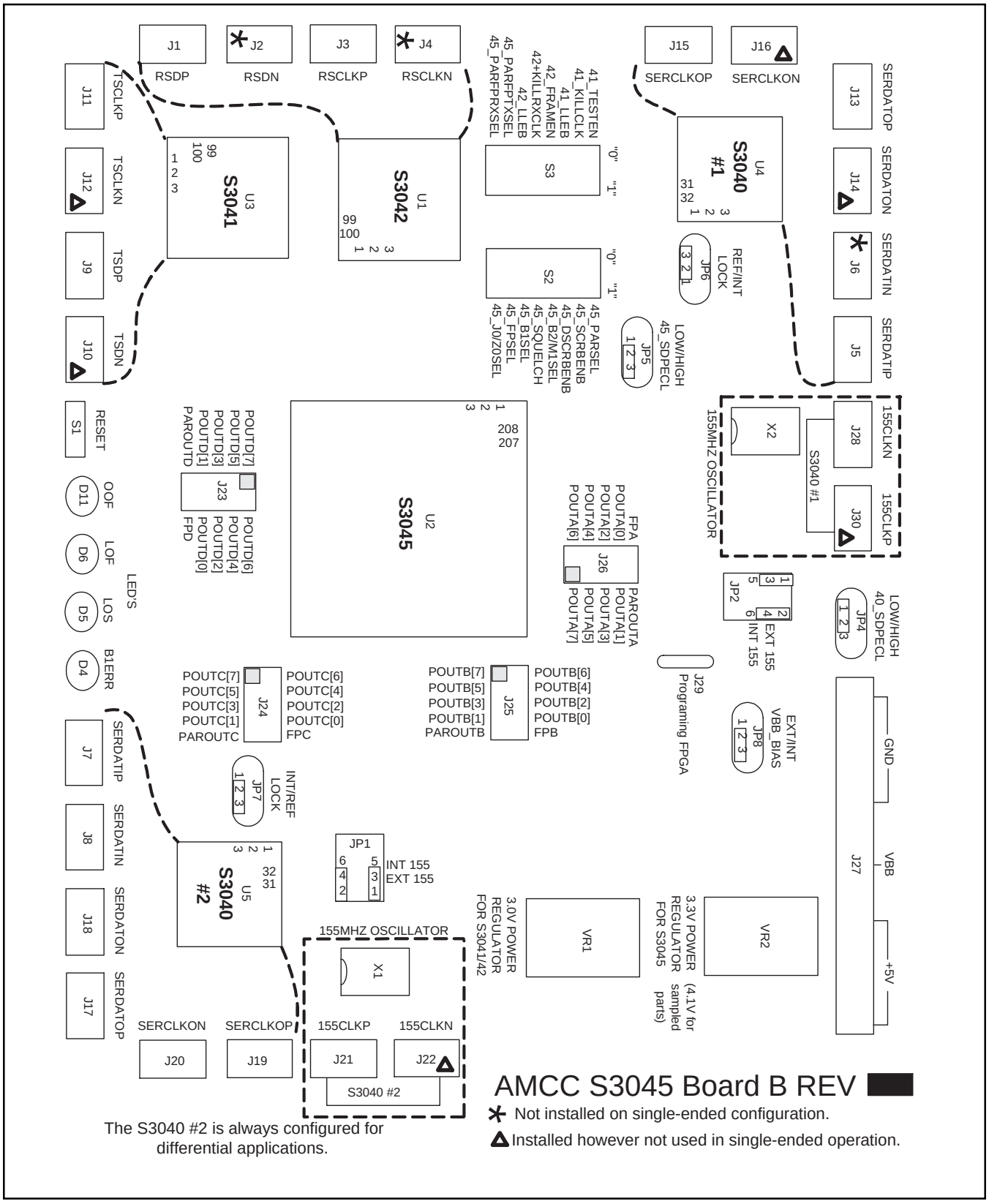
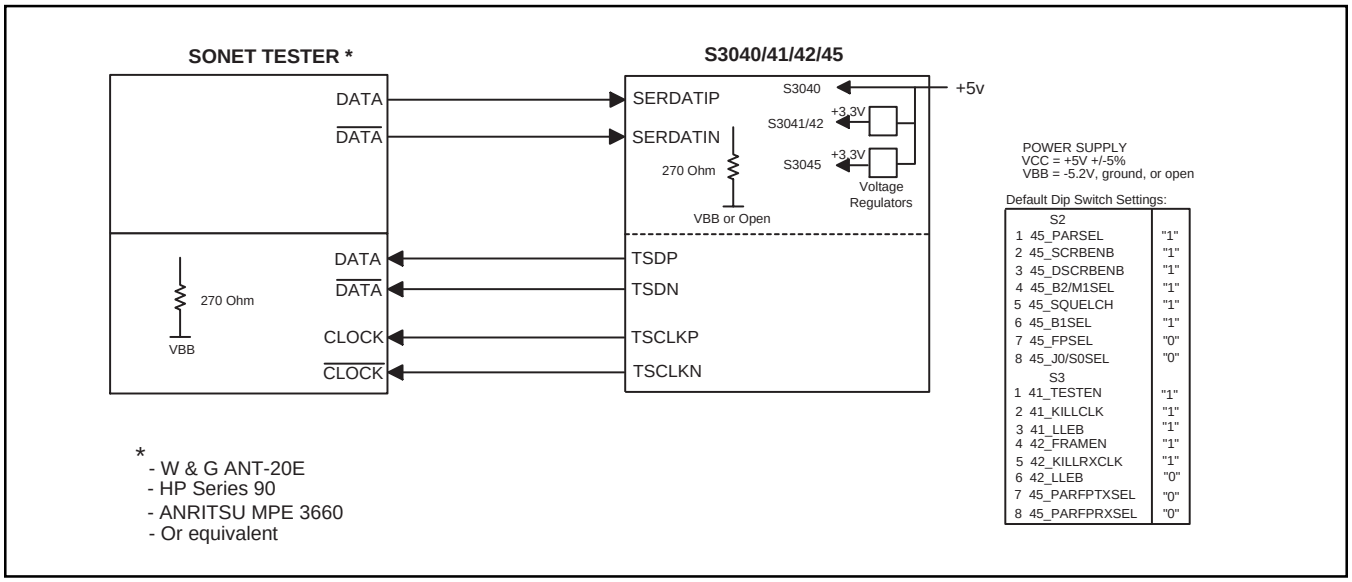


Figure 2. Test Setup (Differential Version Shown)



VBB should be –5.2V for tester outputs that require DC pulldown for activation. Otherwise, VBB should remain open, or connected to ground as shown in Table 2, jumper JP8. Figure 2 depicts how the S3045 Evaluation Board can be connected for SONET/SDH measurements, and shows all of the DIP switch settings, and the LVPECL power supply requirements. This is accomplished by setting the VBB Bias voltage from an external voltage supply. For SONET testers that need 50 Ohm's to –2V, set VBB Bias to -5.2V. External test equipment with standard LVPECL or PECL may interface to the S3045 Evaluation Board, as indicated in Figure 3.

Figure 3. LVPECL and PECL Voltage Swing

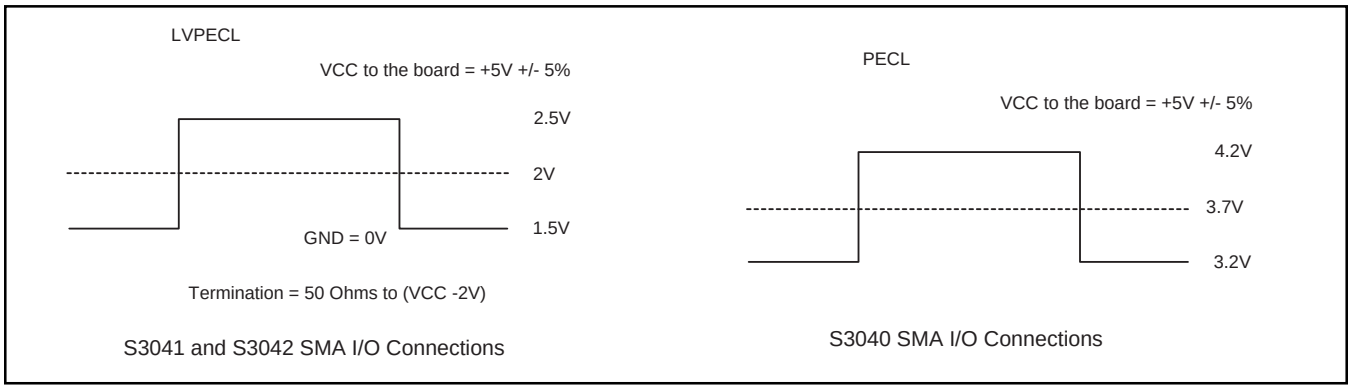


Table 1. Power Connections for DUT and Test Equipment Interface

Power Supply	Nominal Input Voltage
VCC	+5V
GND	0V
VBB (optional)	-5.2V/GND/OPEN

The user may vary VBB Bias (JP8) to terminate the S3045 Evaluation Board to different bias levels (VBB or ground) as shown in Table 2. AC termination is part of the S3042 and S3040 inputs.

The user has the option of using one, both, or none of the on board clock recovery units (S3040).

The user can choose one of the following reference clock options for the S3040's:

1. An external single ended 155MHz (Default factory configuration).
2. An external differential 155 MHz (Must be configured at the factory for this option).
3. The on board 155MHz oscillator (Must be configured at the factory for this option).

JP1 and JP2 of the S3045 Evaluation Board must be configured as in Table 2 for the desired clock option.

SMA Edge Connectors.

SMA edge connectors are provided for the differential serial input/output signals and output clock. All interfaces to the S3045 Evaluation Board are AC coupled, 50 Ohms.

S3040 #1

Serial Data In [SERDATIP/N] (J5, J6) – (Internal Termination.) Clock is recovered from the transitions on these inputs. J6 is not installed for a single-ended configuration.

Serial Data Out [SERDATOP/N] (J13, J14) – This signal is the delayed version of the incoming data stream (SERDATIP/N) updated on the falling edge of Serial Clock Out (SERCLKOP).

Serial Clock Out [SERCLKOP/N] (J15, J16) –This signal is phase aligned with Serial Data Out (SERDATOP/N).

S3040 #2

Serial Data In [SERDATIP/N] (J7, J8) – (Internal Termination.) Clock is recovered from the transitions on these inputs.

Serial Data Out [SERDATOP/N] (J17, J18) – This signal is the delayed version of the incoming data stream (SERDATIP/N) updated on the falling edge of Serial Clock Out (SERCLKOP).

Serial Clock Out [SERCLKOP/N] (J19, J20) – This signal is phase aligned with Serial Data Out (SERDATOP/N).

S3041

Transmit Clock Output [TSCLKP/N] (J11, J12) – Transmit serial clock that can be used to retime the TSD signal. An optical transmitter can use the rising edge of TSCLK to retime the TSD data.

Transmit Serial Data [TSDP/N] (J9, J10) – Serial data stream signals, normally connected to an optical transmitter module.

S3042

Receive Serial Data [RSDP/N] (J1, J2) – Serial data streams normally connected to an optical module. These inputs are clocked by the rising edge RSCLKP inputs. The RSD will be frame aligned and demultiplexed to an 8-bit parallel output <7:0>. J2 is not installed for a single-ended configuration.

Receive Serial Clock [RSCLKP/N] (J3, J4) – Recovered clock signal that is synchronous with the RSDP/N inputs. This clock is used by the receive section as the master clock to perform framing and deserialization functions. J4 is not installed for a single-ended configuration.

Dip Switch Settings

The S3045 Evaluation Board is equipped with two DIP switch modules (S2 and S3), to control the static control functions of the on-board devices. For these DIP switches the OFF (open = "1") condition asserts a logic low on the assigned signal, and the ON (closed = "0") condition asserts a logic high.

S1:

RESET Toggle Switch – This momentary contact switch controls the master reset for the S3041/42/45.

S2:

Parity Select [45_PARSEL] – When high selects even parity. When low selects odd parity.

Scramble Enable [45_SCRBENB] – When low the frame synchronous scrambler is enabled. When high the scrambler is disabled.

Descrambler Enable [45_DSCRBENB] – When low the frame synchronous descrambler is enabled. When high the frame synchronous descrambler is disabled.

B2/M1 Parity Byte and Parity count select [45_B2/M1SEL] – When high the B2/M1 byte calculations and insertions are disabled. When low B2 and M1 calculations and insertions are enabled.

Squelch Clock Mode [45_SQUELCH] – Active low. Set inactive when a clock recovery device used provides a continuous clock during signal loss or reacquisition. Set active when the clock recovery device used does not provide a continuous clock during signal loss or signal acquisition. When active and SDLVPECL/SDLVTTL is inactive, the transmitter serial clock (311TCLK) will be used to maintain timing in the receiving section. When active and SDLVPECL/SDLVTTL is also active, the 311CLKIN is used for all receiver timing. When active there is a 3.2 ns shortening or lengthening of the POCLK cycle.

B1 Parity Byte Select [45_B1SEL] – When low B1 calculation and insertion is enabled. When high B1 calculation and insertion is disabled.

Frame Pulse Select [45_FPSEL] – For normal board operation set low. When low the FRAME input is used to generate the FP A,B,C,D pulse when the third A2 byte is output. When high the FP A,B,C,D output is internally generated using the A1A2 frame boundary. The FP A,B,C,D is asserted high when the third A2 (28h) byte is output.

Section-Trace Insertion Select [45_J0/Z0SEL] – Select pins, select section-trace bytes J0/Z0 options. When low the J0/Z0 bytes are passed through with no modification. When high byte 1 of 48 (J0 bytes) is passed through with no modification (transparent) and bytes 2 through 48 (Z0 bytes) are filled with the values of 02hex to 30hex (48 decimal) respectively.

S3:

Test Clock Enable [41_TESTEN] – For normal board operation set high. When high this input will select the LLCLK input instead of the internally generated 2.4 GHz clock as the system clock. When this input is Low it will select the internally generated 2.4 GHz clock from the LLCLK input.

Kill Transmit Clock Input [41_KILLTXCLKN] – For normal board operation set high. When low this input will force the PCLKP/N and PULSE0P/N outputs low.

Line Loopback Enable [41_LLEB] – For normal board operation set high. Selects Line Loopback when low. When LLEB is low the S3041 will force the data from the LLD/LLCLK inputs from the S3042 to the TSD/TSCLK outputs of the S3042.

Frame Enable Input [42_FRAMEN] – For normal board operation set FRAMEN high. This enables the frame detector circuit to detect A1 A2 alignment and lock to word boundary. When this input is low it will disable the frame detector circuit and it will lock on the last byte alignment state.

Kill Receive Clock Input [42_KILLRXCLK] – For normal board operation set KILLRXCLK "high." When this input is low it will force RX311MCK and POCLK outputs to a logic "0" state.

Line Loopback Enable [42_LLEB] – Active low. For normal board operation set low. Selects Line Loopback. When active the S3042 will enable the data on the LLD/LLCLK outputs.

Parity Frame Pulse Select [45_PARFPTXSEL] – Default setting for the board is low. When low parity is calculated over the data bus PIN <7:0> A,B,C,D. When high parity is calculated over the PIN <7:0> A,B,C,D data bus and the Transmit Input Frame Pulse (TIFP A,B,C,D).

Parity Frame Pulse Receive Select [45_PARFPRXSEL] – Default setting for the board is low. When low parity is calculated over the data POUT <7:0> A,B,C,D. When high parity is calculated over the data POUT <7:0> A,B,C,D and the frame pulse (FP A,B,C,D) output.

LED'S

The static status pins such as LOF (D6), OOF (D11), B1ERR (D4), LOS (D5) are available as LED indictors and as test points. The LED versions of the alarms are held in the active state longer than the actual alarms last so that the LED'S are able to turn on.

Parallel Output Header Terminals

The parallel outputs POUTA,B,C,D[7:0] (J23, J24, J25, J26) from the S3045 are available at the 2 x 5 pin header arrays.

Signal Detect - The SD line should be tied to a static value. Table 2 shows how the signal detect can be configured.

J29 – This connector is used at the factory for FPGA programming.

JP2 and JP1 – These jumpers are for the External or internal clock for the S3040's as described in Table 2.

JP6 – When strapped for logic "0" the S3040 (U4) serial clock output is forced to lock to REFCLK. Strapped for logic "1", the S3040 (U4) locks to the incoming data stream SERDATIP/N.

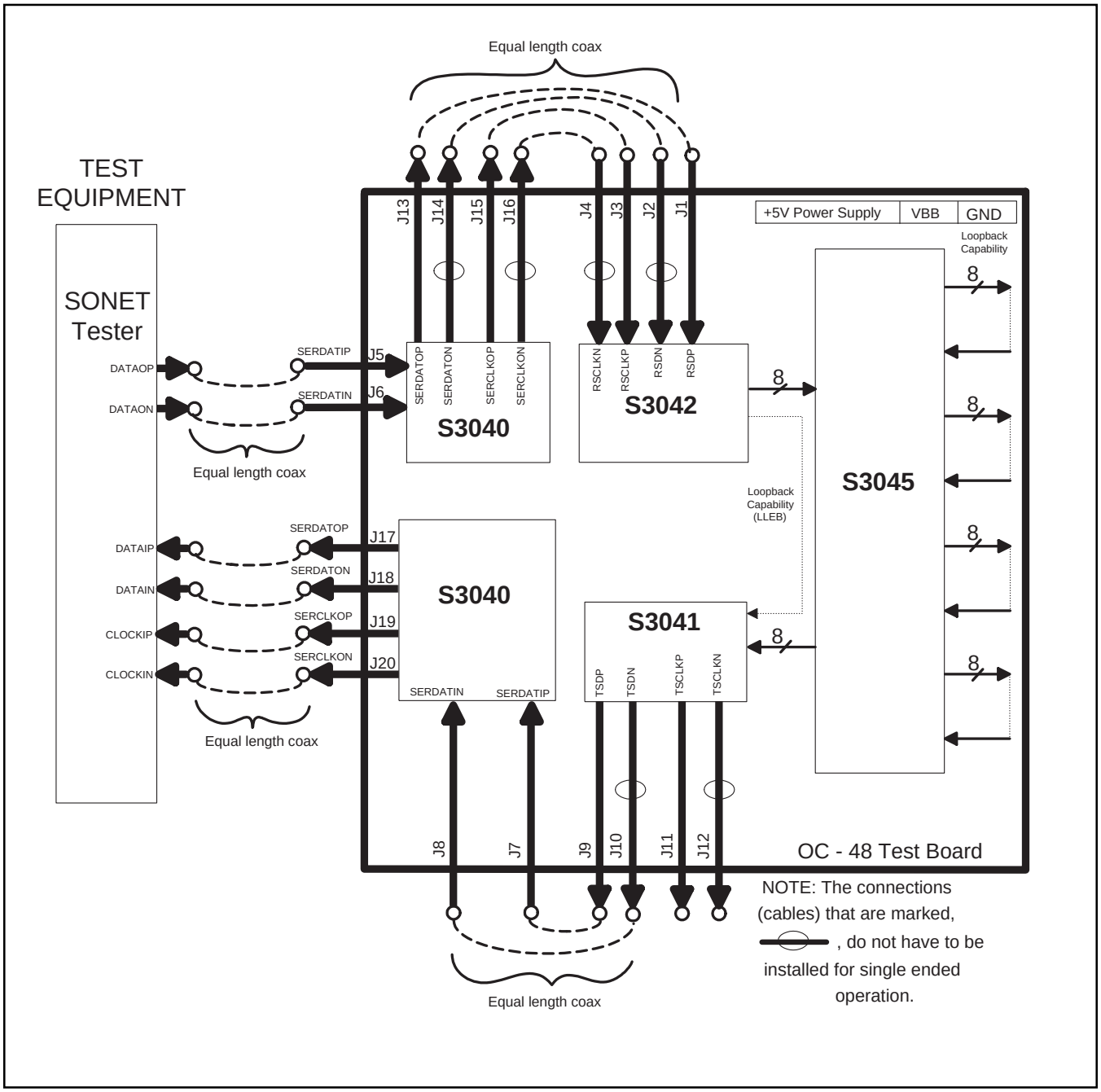
JP7 – When strapped for a logic "0" the S3040 (U5) serial clock output is forced to lock to REFCLK. Strapped for a logic "1", the S3040 (U5) locks to the incoming data stream SERDATIP/N.

Table 2. Jumper Positions and Functions

Jumper	Description	Option	Jumper Position
JP1	Selects between the on board oscillator or the external source for U4 (S3040 #1). J22 is not installed for single-ended configuration. For normal operation, the board is configured for single-ended operation.	External Clock (balanced/unbalanced)	1~3 and 2~4
		On board reference oscillator X1	3~5 and 4~6
JP2	Selects between the on board oscillator or the external source for U5 (S3040 #2). J28 is not installed for single-ended configuration. For normal operation, the board is configured for single-ended operation.	External Clock (balanced/unbalanced)	1~3 and 2~4
		On board reference oscillator X2	3~5 and 4~6
JP4	SDN control for U4 (S3040 #1), and U5 (S3040 #2).	Dataout all zeros with synthesized clock output	2~3 (logic "1")
		Normal CDR function	1~2 (logic "0")
JP5	SDLVPECL control for U1 (S3042) Pin 52.	Normal operation of S3042 (U1)	2~3 (logic "1")
		All zeros for dataout	1~2 (logic "0")
JP6	U4 LCKREFN control (S3040 #1).	Normal CDR function	2~3 (logic "1")
		PLL locks to reference	1~2 (logic "0")
JP7	U5 LCKREFN control (S3040 #2).	Normal CDR function	2~3 (logic "1")
		PLL locks to reference	1~2 (logic "0")
JP8	EXT/INT VBB_BIAS	VBB_BIAS = GND	2~3
		VBB_BIAS = external voltage	1~2

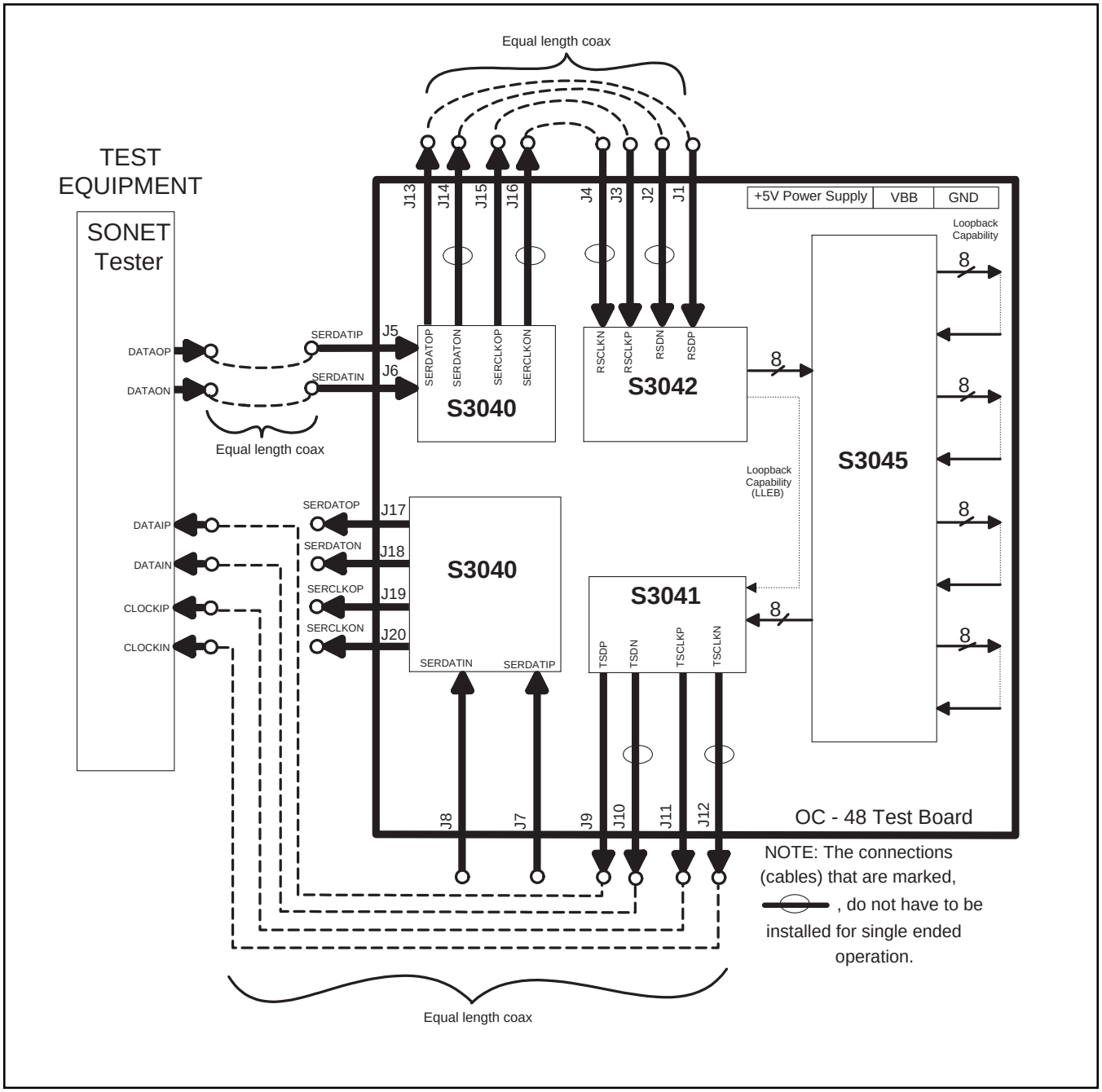
Differential and Single-Ended configurations for 2.5Gbps I/O are determined by component stuffing options at the factory. The factory default is single-ended.

Figure 4. Coax Connections Required When Using Both Clock Recovery Devices (S3040)



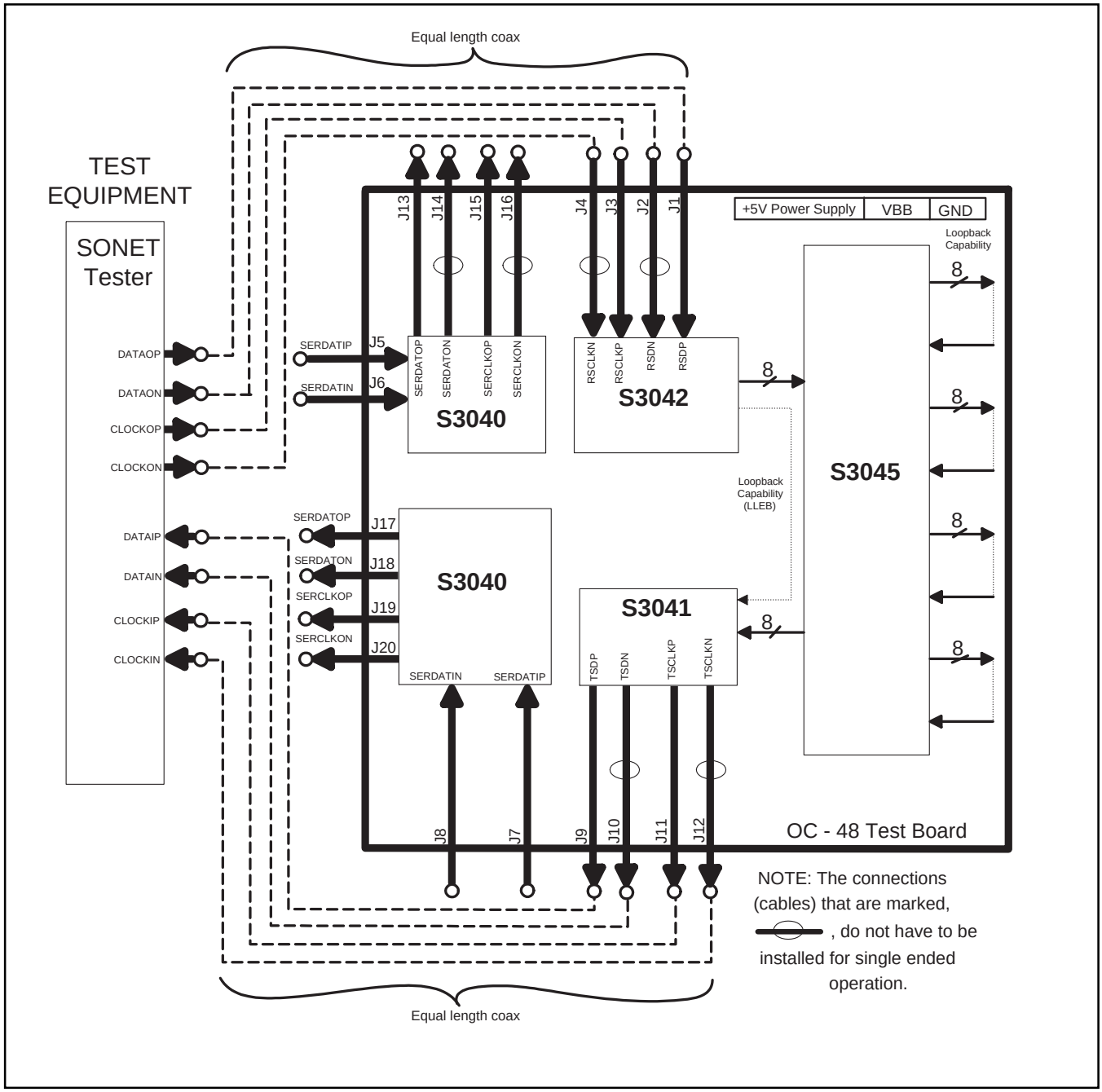
Note that the dotted lines are 50 Ohm SMA coax connections. Equal length coax cable must be used for the P and N signal connections. For example, the coax cable between TSDP and SERDATIP must be the same length as the cable between TSDN and SERDATIN.

Figure 5. Coax Connections Required When Using the On Board Input Clock Recovery Device (S3040)



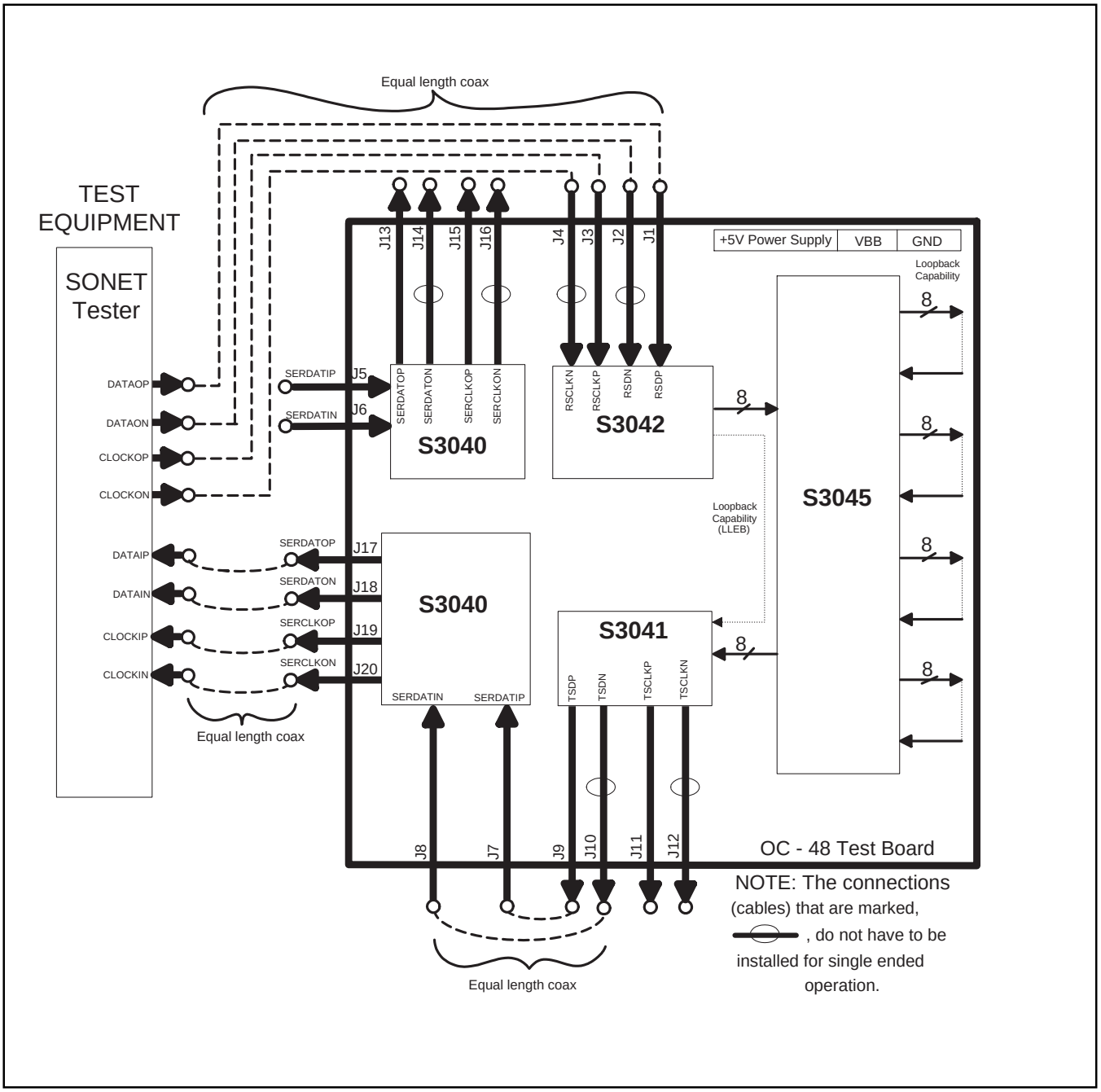
Note that the dotted lines are 50 Ohm coax connections. Equal length coax cable must be used for the P and N signal connections. For example, the coax cable between TSDP and DATAIP must be the same length as the cable between TSDN and DATAIN.

Figure 6. Coax Connections Required When Not Using the On Board Input Clock Recovery Devices (S3040)



Note that the dotted lines are 50 Ohm coax connections. Equal length coax cable must be used for the P and N signal connections. For example, the coax cable between TSDP and DATAIP must be the same length as the cable between TSDN and DATAIN.

Figure 7. Coax Connections Required When Using the On Board Output Clock Recovery Device (S3040)



Note that the dotted lines are 50 Ohm coax connections. Equal length coax cable must be used for the P and N signal connections. For example, the coax cable between TSDP and SERDATIP must be the same length as the cable between TSDN and SERDATIN.

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