2.5 GBPS LASER DRIVER S3049

FEATURES

- 2.5 Gbps data rate
- Automatic Laser Power Control
- Laser Bias Enable Input
- Differential PECL Inputs
- Temperature Compensated Reference Voltage
- Laser Fault and Fail indicators
- Selectable on-chip Re-Clocking
- 60 mA Modulation Current, 90 mA Bias Current
- 32 Pin TQFP Package

APPLICATIONS

- WDM for SONET OC-48
- OC-48 Fiber optic modules
- OC-48 Line termination equipment

GENERAL DESCRIPTION

The S3049 has three main sections: a reference generator, a high speed current modulation driver, and a laser bias block with automatic power control.

The reference generator generates a temperature stabilized reference voltage, V_{REF}, which can be used to program the bias and the modulation currents.

The high-speed modulation driver can switch up to 60 mA swing through the laser. The CLKSEL pin can be used to select whether or not to re-clock the input data.

The laser bias block sets the bias current of the laser and has an Automatic Power Control (APC) system, which keeps the current through the laser constant by monitoring the current through the monitor photo-diode.

The APC loop is also used to detect excessive laser power and low laser power. These conditions are flagged on the LSFAULT and LSFAIL output pins respectively.

Figure 1. Typical Operating Circuit

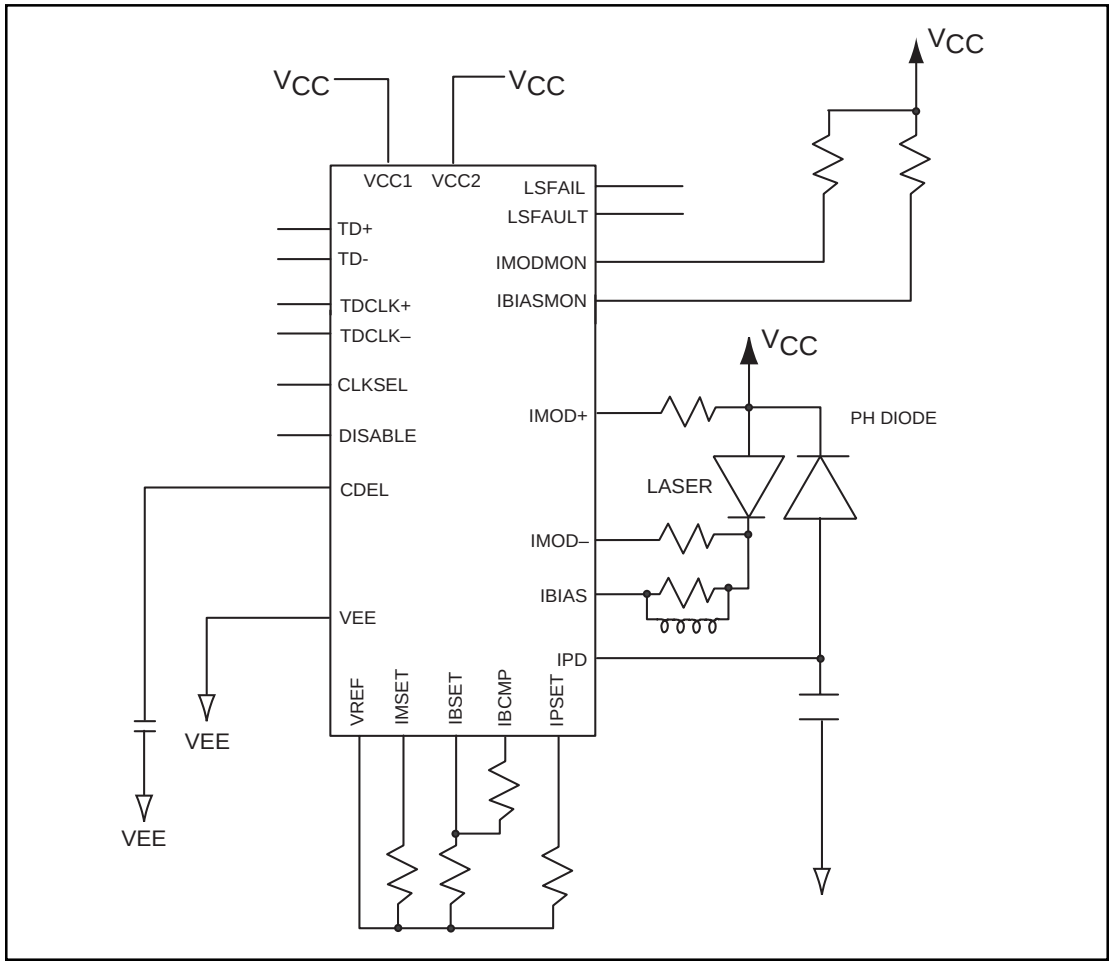
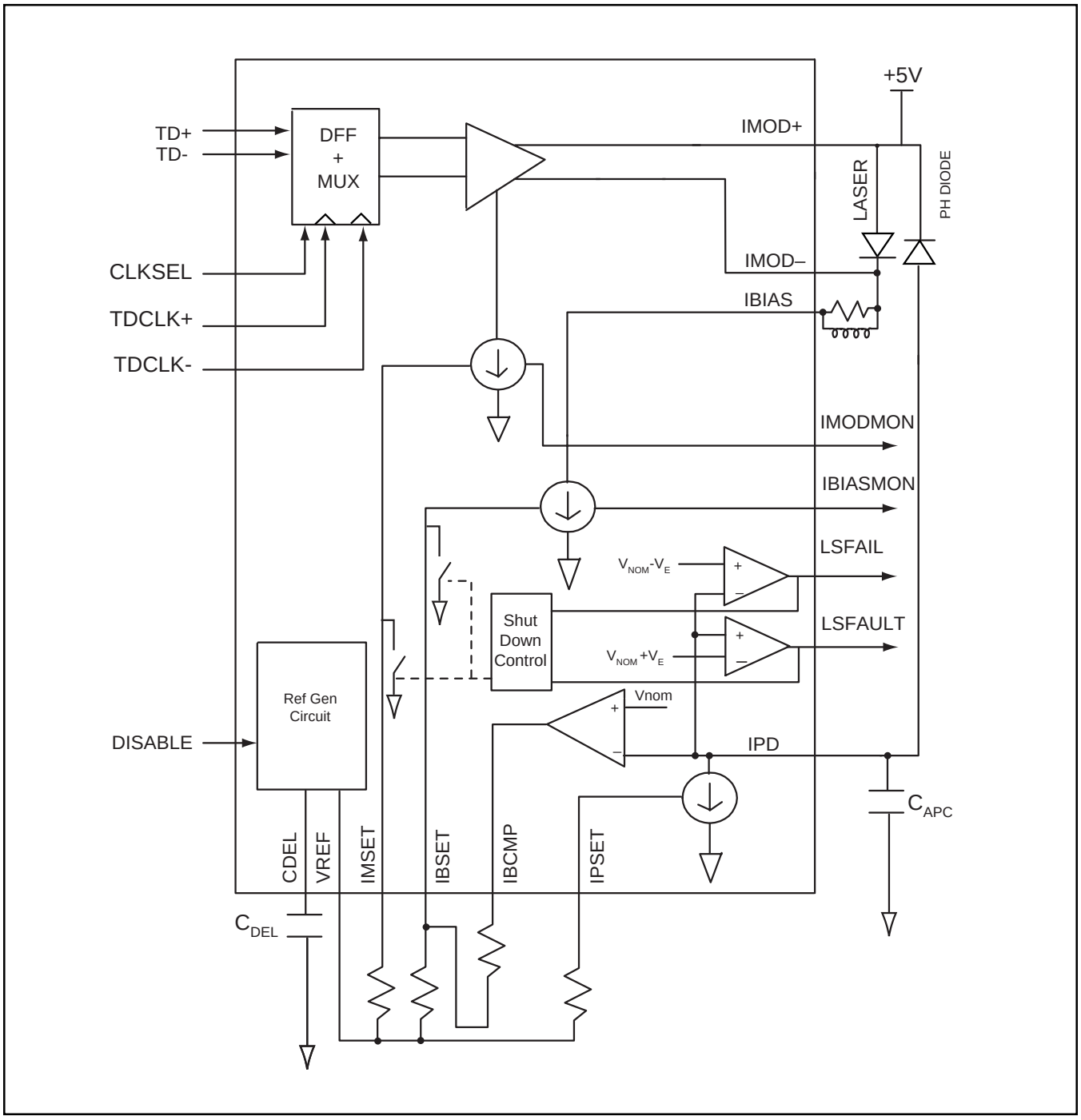


Figure 2. Functional Block Diagram



DETAILED DESCRIPTION

Reference Generator

The reference generator provides temperature compensated reference voltage, VREF, which is used to program the laser diode bias current, I_{BIAS} , the modulation current, I_{MOD}, and the photo-diode reference current, I_{PD}. The currents are set by connecting a resistor between VREF and the respective current source pin.

Laser Bias Block with Automatic Power Control

The laser bias current, I_{BIAS}, is set by connecting a resistor between the IBSET pin and VREF. The current through the resistor is amplified by a gain factor, A_{IBSET}, to generate I_{BIAS}.

There is a feedback configuration to adjust the laser bias current to maintain constant laser power as laser efficiency changes with temperature and age. Light produced by the laser diode produces an average current in the monitor photo-diode. This current flows into the IPD pin. The IPSET current source, whose current is set by the IPSET resistor, draws current away from the IPD node. When the two currents are equal, the voltage at that node is set by the nominal reference voltage, $V_{NOM,}$ of a differential amplifier. When the currents are not equal a voltage change is generated across the capacitor, $C_{APC,}$ which the differential amplifier translates to a voltage which generates a current through the IBCMP resistor. This current is summed with current through the IBSET resistor which adjusts I_{BIAS} until the monitor photo-diode current equals the nominal monitor photo-diode current, I_{PD}.

Modulation Driver

The modulation driver consists of a high speed input buffer and a differential output stage. The modulation current, I_{MOD}, is programmed by connecting a resistor between the IMSET pin and VREF.

The current through the resistor is amplified by a gain factor, A_{IMSET} , to generate I_{MOD}.

If the CLKSEL input is set Low, the data input, TD+/TD–, is clocked at the input by TDCLK to provide low jitter. If CLKSEL is High, TD+/TD– will be passed through to the modulation driver with no re-clocking.

Monitor Pins

I_{BIAS} and I_{MOD} are mirrored and brought out on the IBIASMON and IMODMON pins respectively. The monitor currents are a specified fraction of the actual currents and are converted to a voltage by connecting the pins to VCC through a resistor.

FAULT Detection

If the monitor photo-diode current increases beyond the point which can be controlled by the APC loop, the LSFAULT signal is asserted, indicating excessive laser power (a FAULT condition). This condition occurs when the voltage at the IPD node exceeds V_{NOM} by more than 400mv.

LSFAULT is also asserted if V_{REF} is detected to exceed 3.8V, as this will generate excessively high laser current.

FAIL Detection

If the monitor photo-diode current decreases beyond the point which can be controlled by the APC loop, LSFAIL is asserted, indicating low laser power (FAIL condition). This condition occurs when the voltage at the IPD pin drops below V_{NOM} by more than 400mv.

Laser Shutdown

If a FAULT or FAIL condition is detected the laser bias and modulation currents will be turned off.

The laser can be enabled only by toggling the DISABLE input or by initiating a power-on cycle. LSFAULT and LSFAIL will be reset on DISABLE de-assert or V_{CC} > 4.4V.

If the CDEL pin is grounded, the shutdown of the laser currents on a FAULT or FAIL detection is disabled, and LSFAIL or LSFAULT will de-assert when the FAULT or FAIL condition no longer exists.

Start-up Sequence

The laser bias and modulation currents are turned on within a time t_{ON} from when V_{CC} exceeds 4.4V or from when the DISABLE input is de-asserted. During the period t_{DELAY}, set by the capacitor C_{DEL}, the shutdown of the laser is disabled in order to allow the APC loop time to settle. During this time if a FAULT or FAIL condition is detected the laser will not be shut down as it could be caused by the APC loop transient state. C_{DEL} should be chosen such that t_{DELAY} is much longer than the APC loop settling time. LSFAULT and LSFAIL will not assert during t_{DELAY}.

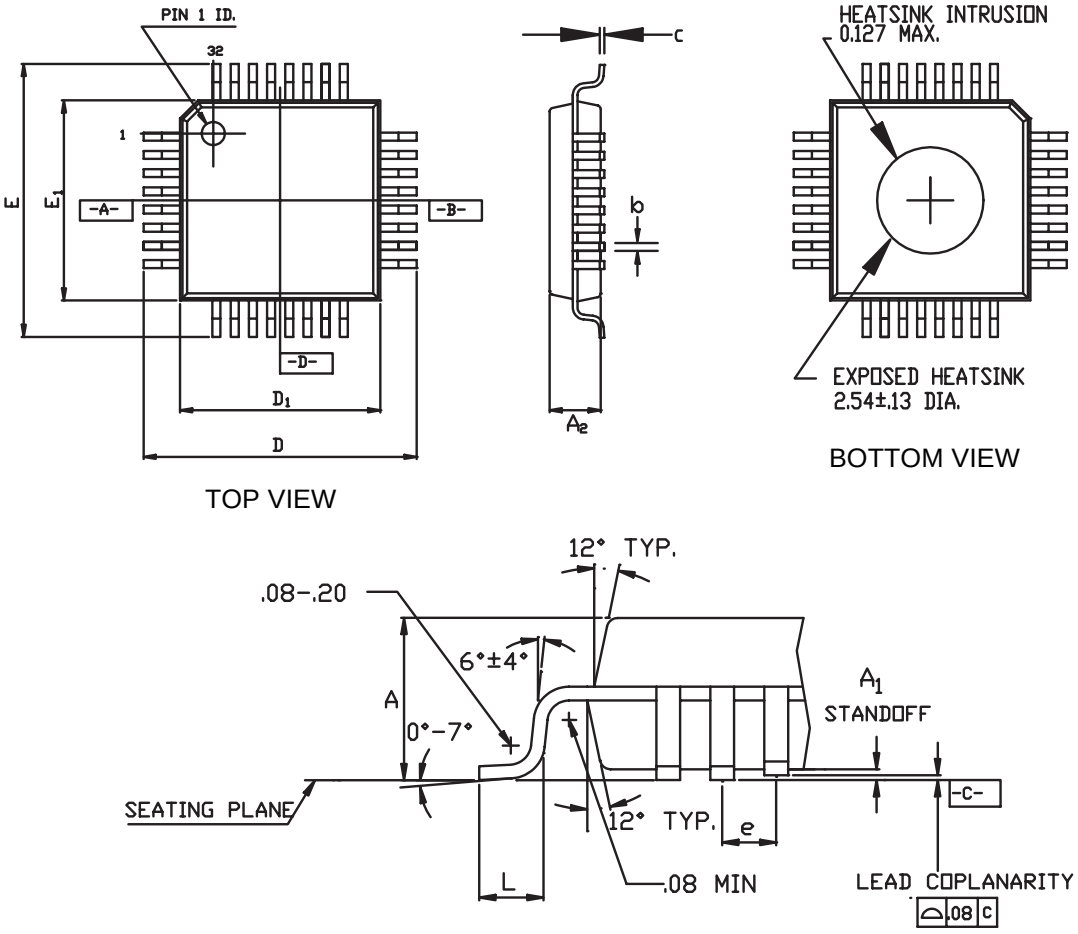
Table 1. Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
TD+	Diff. PECL	I	10	Positive PECL Data Input.
TD-	Diff. PECL	I	12	Negative PECL Data Input.
TDCLK+	Diff. PECL	I	14	Positive clock input.
TDCLK-	Diff. PECL	I	16	Negative clock input.
CLKSEL	TTL	I	9	A Low selects re-clocking of TD+, TD-. A High will pass the data through without re-clocking.
DISABLE	TTL	I	17	High level disables bias and modulation currents. If left open it will default to a low state.
CDEL			3	A capacitor to ground sets the time for $t_{DELAY,}$, the time during which laser shutdown is disabled after Disable is de-asserted or V_{CC} > 4.4V. If this pin is grounded, laser shutdown is disabled.
IMSET			24	A resistor to VREF sets the modulation current. (See Figure 7.)
IBSET			23	A resistor to VREF sets the bias current. (See Figure 6.)
IPSET			6	A resistor to VREF sets the monitor photo-diode reference current. (See Figure 8.)
IBCMP			22	A resistor to IBSET pin sets the maximum APC loop compensation bias current. (See Figure 9.)
IPD	Current	I	2	Monitor photo-diode current input.
IMOD-	Current	O	27	Secondary Laser Modulation Current output. When TD+ is High, current is driven through this pin.
IMOD+	Current	O	29	Primary Laser Modulation Current output. When TD+ is Low, current is driven through this pin.

Table 1. Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
IBIAS	Current	O	25	Laser Bias Current output.
LSFAULT	Open Collector	O	8	Active High output. Asserts when excessively high laser power is detected or V_{REF} exceeds 3.8V.
LSFAIL	Open Collector	O	7	Active High output. Asserts when excessively low laser power is detected.
IMODMON	Open Collector	O	20	Modulation current monitor output. It can be used to monitor I_{MOD} by connecting it to V_{CC} through a resistor.
IBIASMON	Open Collector	O	19	Bias current monitor output. It can be used to monitor I_{BIAS} by connecting it to V_{CC} through a resistor.
VREF		O	5, 21	Temperature compensated reference.
VCC1			18	Positve supply for low frequency circuitry.
VCC2			31, 32	Positve supply for high frequency circuitry.
VEE1			4	Ground for low frequency circuitry.
VEE2			1, 28, 30	Ground for high frequency circuitry.
VEE3			26	Ground for I_{BIAS} circuitry.
VEE4			11, 13, 15	Ground for high frequency input shield.

Figure 3. 32 TQPF Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	b	e	c
MIN		0.05	1.35	6.80	4.90	6.80	4.90	0.50	0.17	0.50 BSC.	0.127 BSC.
NOM			1.40	7.00	5.00	7.00	5.00	0.60	0.22		
MAX	1.60	0.15	1.45	7.20	5.10	7.20	5.10	0.75	0.27		

Thermal Management

Device	Max Power	Θja
S3049	0.64 W	70° C/W

Figure 4. S3049 Pinout

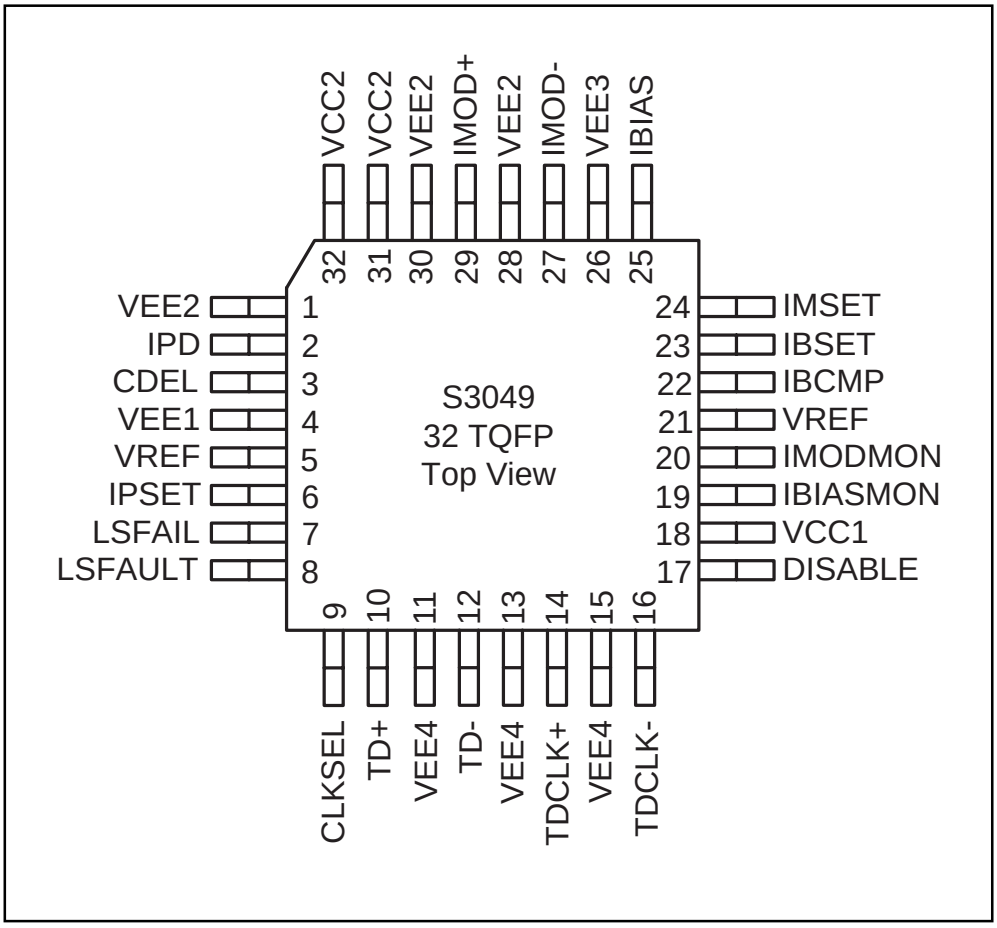


Figure 5. Bonding Pad Location

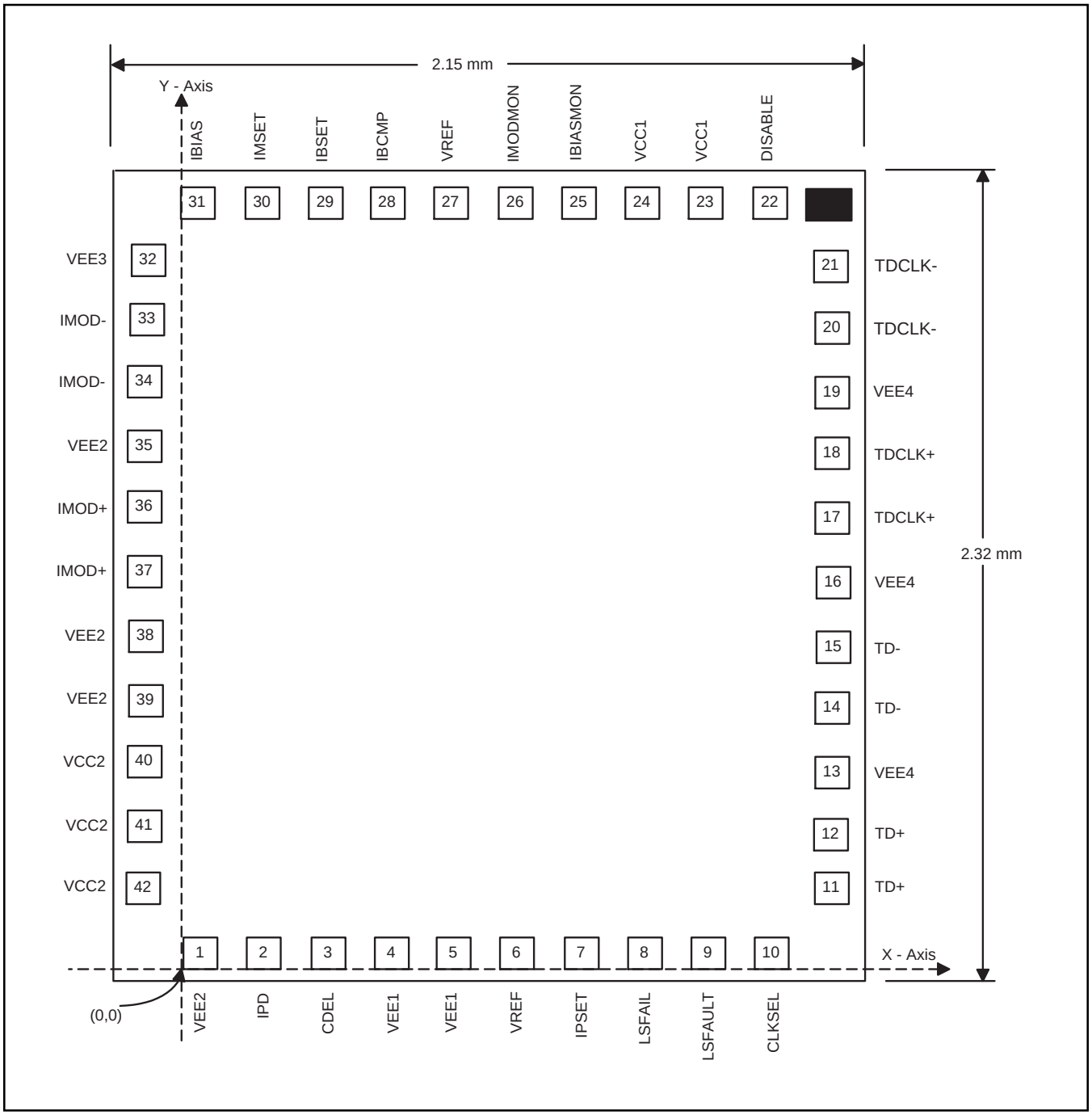


Table 2. Pad Assignment and Description

Pin Name	Level	I/O	Pad #	Coordinates [X,Y] [1]	Description
TD+	Diff. PECL	I	11 12	[1772.5, 247.375] [1775.5, 419.375]	Positive PECL Data Input.
TD-	Diff. PECL	I	14 15	[1772.5, 763.375] [1772.5, 935.375]	Negative PECL Data Input.
TDCLK+	Diff. PECL	I	17 18	[1772.5, 1279.375] [1772.5, 1451.375]	Positve Clock Input.
TDCLK-	Diff. PECL	I	20 21	[1772.5, 1795.375] [1772.5, 1967.375]	Negative Clock Input.
CLKSEL	TTL	I	10	[1592.375, 45]	A Low selects re-clocking of TD+, TD-. A High will pass the data through without re-clocking.
DISABLE	TTL	I	22	[1592.625, 2170]	High level disables Bias and Modulation currents. If left open it will default to a low state.
CDEL			3	[388.375, 45]	A capacitor ground sets the time for t_{DELAY}, the time during which laser shutdown is disabled after DISABLE is de-asserted, or V_{CC} > 4.4V. If this pin is grounded, laser shutdown is disabled.
IMSET			30	[216.625, 2170]	A resistor to VREF sets the Modulation current. (See Figure 7.)
IBSET			29	[388.625, 2170]	A resistor to VREF sets the Bias current. (See Figure 6.)
IPSET			7	[1076.375, 45]	A resistor to VREF sets the monitor photo-diode reference current. (See Figure 8.)
IBCMP			28	[560.625, 2170]	A resistor to IBSET pin sets the maximum APC loop compensation bias current. (See Figure 9.)
IPD	Current	I	2	[216.375, 45]	Monitor photo-diode current input.
IMOD-	Current	O	33 34	[-180.5, 1795.625] [-180.5, 1623.625]	Secondary Laser Modulation Current output. When TD+ is High, current is driven through this pin.
IMOD+	Current	O	36 37	[-180.5, 1279.625] [-180.5, 1107.625]	Primary Laser Modulation Current output. When TD+ is Low, current is driven through this pin.
IBIAS	Current	O	31	[44.625, 2170]	Laser Bias Current output.
LSFAULT	Open Collector	O	9	[1420.375, 45]	Active High output. Asserts when excessively high laser power is detected or V_{REF} exceeds 3.8V.

Table 2. Pad Assignment and Description *(Continued)*

Pin Name	Level	I/O	Pad #	Coordinates [X,Y] [1]	Description
LSFAIL	Open Collector	O	8	[1248.375, 45]	Active High output. Asserts when excessively low laser power is detected.
IMODMON	Open Collector	O	26	[904.625, 2170]	Modulation current monitor output. It can be used to monitor I_{MOD} by connecting it to V_{CC} through a resistor.
IBIASMON	Open Collector	O	25	[1076.625, 2170]	Bias current monitor output. It can be used to monitor I_{BIAS} by connecting it to V_{CC} through a resistor.
VREF		O	6 27	[904.375, 45] [732.625, 2170]	Temperature compensated reference.
VCC1			23 24	[1420.625, 2170] [1248.625, 2170]	Positive supply for low frequency circuitry.
VCC2			40 41 42	[-180.5, 591.625] [-180.5, 419.625] [-180.5, 247.625]	Positive supply for high frequency circuitry.
VEE1			4 5	[560.375, 45] [732.375, 45]	Ground for low frequency circuitry.
VEE2			1 35 38 39	[44.375, 45] [180.5, 1451.625] [180.5, 935.625] [180.5, 763.625]	Ground for high frequency circuitry.
VEE3			32	[-180.5, 1967.625]	Ground for I_{BIAS} circuitry.
VEE4			13 16 19	[1772.5, 591.375] [1772.5, 1107.375] [1772.5, 1623.375]	Ground for high frequency input shield.

Notes
1. The coordinates represent the position of the center of the pad, in μm, with respect to the lower left corner of Pad 1.
2. Pad size: 90 x 90 μm.

Table 3. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage temperature range	-55		+175	˚C
Processing temperature			+400	˚C
Voltage on V_{CC} with respect to GND	-0.5		+5.5	V
Voltage on any TTL input pin	-0.5		+5.5	V
Voltage on any PECL input pin	V_{CC} -2		V_{CC}	V
ESD Sensitivity [1]	300			V

1. Human body model.

Table 4. Power and References
(VCC-VEE = 5V±5%, TA = -40˚C to 85˚C, 25˚ C for die)

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{CC}	Supply Current			76	mA	I_{MOD} = 0, I_{BIAS} = 0, R_{LOAD} = 25
V_{REF}	Reference Voltage		3.3		V	

Table 5. Laser Modulation (R_{LOAD} = 25Ω)
(VCC-VEE = 5V±5%, TA = -40˚C to 85˚C, 25˚ C for die)

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{MOD}	Range of programmable Laser Modulation Current	1		60	mA	
$T_{r,}$ T_f	Modulation Current Rise and Fall Time			150	ps	I_{MOD} = 30mA, I_{BIAS} = 50mA, 20% to 80%
F_{max}	Maximum Operating Frequency	2.5			Gbps	
PWD	Modulation current pulse width distortation			40	ps	I_{MOD} = 30mA, I_{BIAS} = 50mA
V_{IMSET}	IMSET Pin Voltage		1.5			T_A = 25˚ C
A_{IMSET}	I_{MOD} Current Source Gain		32			
V_{IMOD}	IMOD, IMOD- Pin minimum voltage requirement	V_{CC} -2.5			V	
$I_{MOD}V$	Modulation current drift over full voltage range			4	%	
$I_{MOD}T$	Modulation current drift over temperature			4	%	
$V_{IMODMON}$	IMODMON Pin minimum voltage requirement	V_{CC} -3			V	
$I_{MOD/}$ I_{MODMON}	Ratio I_{MOD} to I_{MODMON}		32			

Table 6. Laser Bias

(VCC-VEE = 5V±5%, TA = -40˚C to 85˚C, 25˚C for die)

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{BIAS}	Range of programmable Laser Bias current	1		50	mA	
V_{IBSET}	IBSET pin voltage		1.5		V	T_A = 25˚ C
A_{IBIAS}	I_{BIAS} Current Source gain		50			
V_{IBIAS}	I_{BIAS} pin minimum voltage requirement	1			V	
V_{IBIASM}	$I_{BIASMON}$ pin minimum voltage requirement	V_{CC} -3			V	
I_{BIAS}/ $I_{BIASMON}$	Ratio I_{BIAS} to $I_{BIASMON}$		50			

Table 7. Automatic Power Control

(VCC-VEE = 5V±5%, TA = -40˚C to 85˚C, 25˚C for die)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IPSET}	IPSET Pin Voltage		1.5		V	T_A = 25˚ C
A_{IPD}	I_{PD} Current Souce Gain		1			
I_{PD}	Range of monitor photo diode current	20		900	µA	
I_{BCMP}	Maximum Compensation Bias current generated by APC circuit (up or down)	40			mA	

Table 8. Power Initialization and Latched Shutdown

(VCC-VEE = 5V±5%, TA = -40˚C to 85˚C, 25˚C for die)

Parameter	Description	Min	Typ	Max	Units	Conditions
$VCCI_{ON}$	Internal power turn-on threshold		4.4		V	
$VCCI_{OFF}$	Internal power turn-off threshold		4.3		V	
t_{DELAY}	Programmable delay for disabling laser shutdown after Vcc > 4.4V or Disable deasserted	1		20	ms	
t_{ON}	Laser currrent turn on delay from DISABLE de-assert			1	µS	
t_{RESET}	Minimum DISABLE assert time (or power-off time) required to discharge C_{DEL} cap	100			µS	C_{DEL} = 0.1 µF.

Table 9. PECL and TTL Input/Outputs

(VCC-VEE = 5V±5%, TA = -40˚C to 85˚C, 25˚C for die)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IN}	Single-ended Input Voltage Swing (TD ±, TDCLK ±)	250		1400	mv	
V_{CM}	Differential Input Common Mode range (TD ±, TDCLK ±)	V_{CC} -1.5		V_{CC} -1.1	V	
V_{IL}	TTL Input Low Voltage			VEE +0.8	V	
V_{IH}	TTL Input High Voltage	V_{CC} -3			V	
V_{OC}	Open Collector Outputs, Low Voltage			0.5	V	10kΩ pull-up I_{OUT} = 1 mA
tS_{TD}	TD+/TD- Setup time w.r.t. clock	70			ps	
tH_{TD}	TD+/TD- Hold time w.r.t. clock	10			ps	

Resistor and Capacitor Values

The resistors and capacitors can be selected using the following plots and formula.

Figure 6. Bias Current vs. IBSET Resistor Value

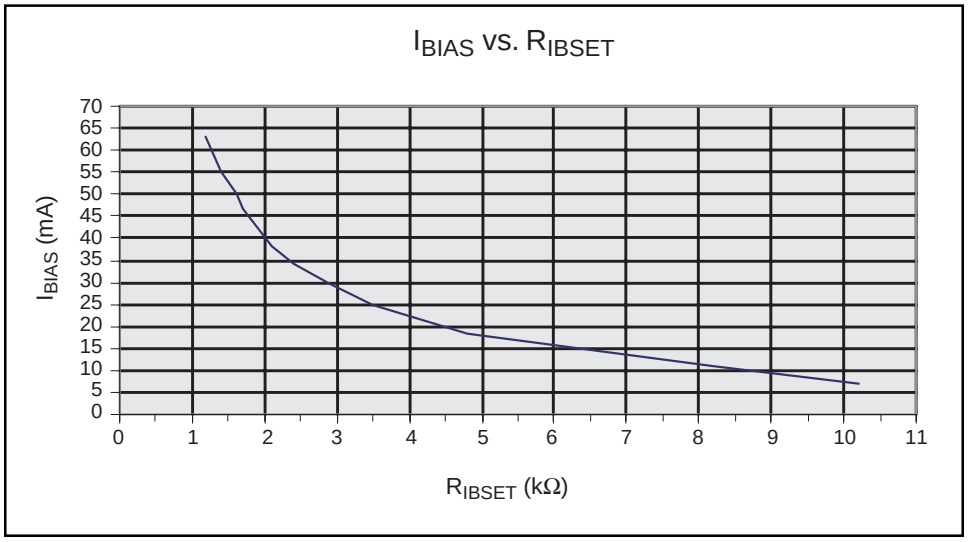


Figure 7. Modulation Current vs. IMSET Resistor Value

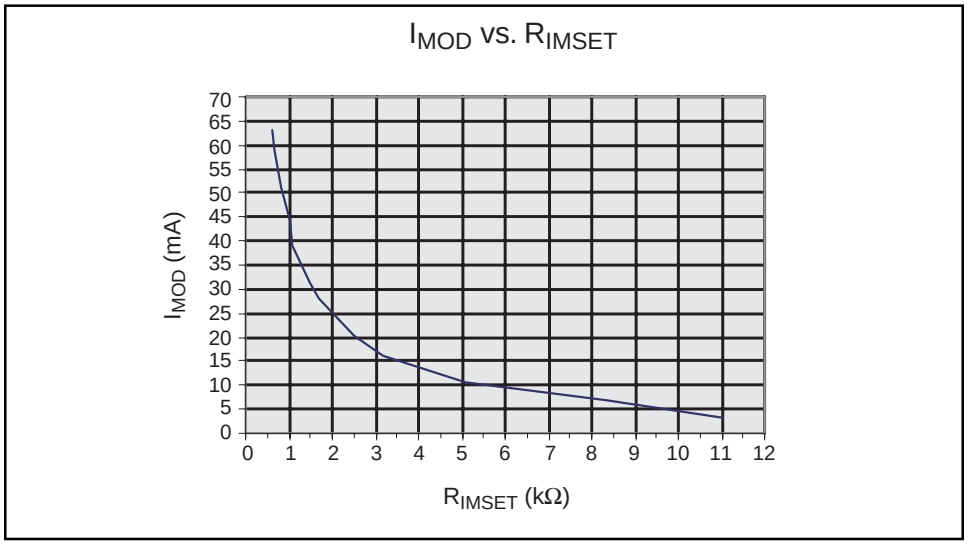


Figure 8. Photo Diode Current vs. IPSET Resistor Value

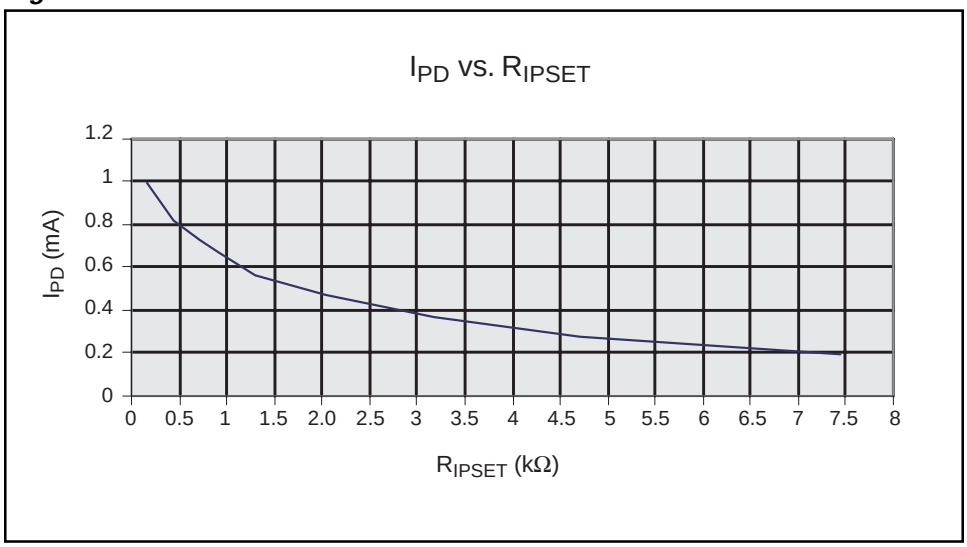
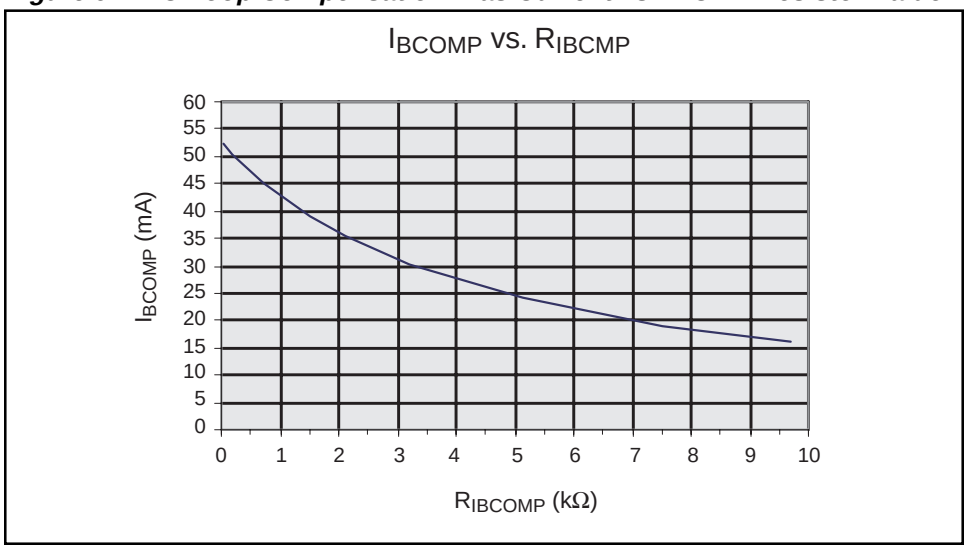


Figure 9. APC Loop Compensation Bias Current vs. IBCMP Resistor Value



Programming t_{DELAY}

$$t_{DELAY} = (100k\Omega)\ (C_{DEL})$$

Timing for Start Up Sequence

Figure 10. DISABLE Unasserted

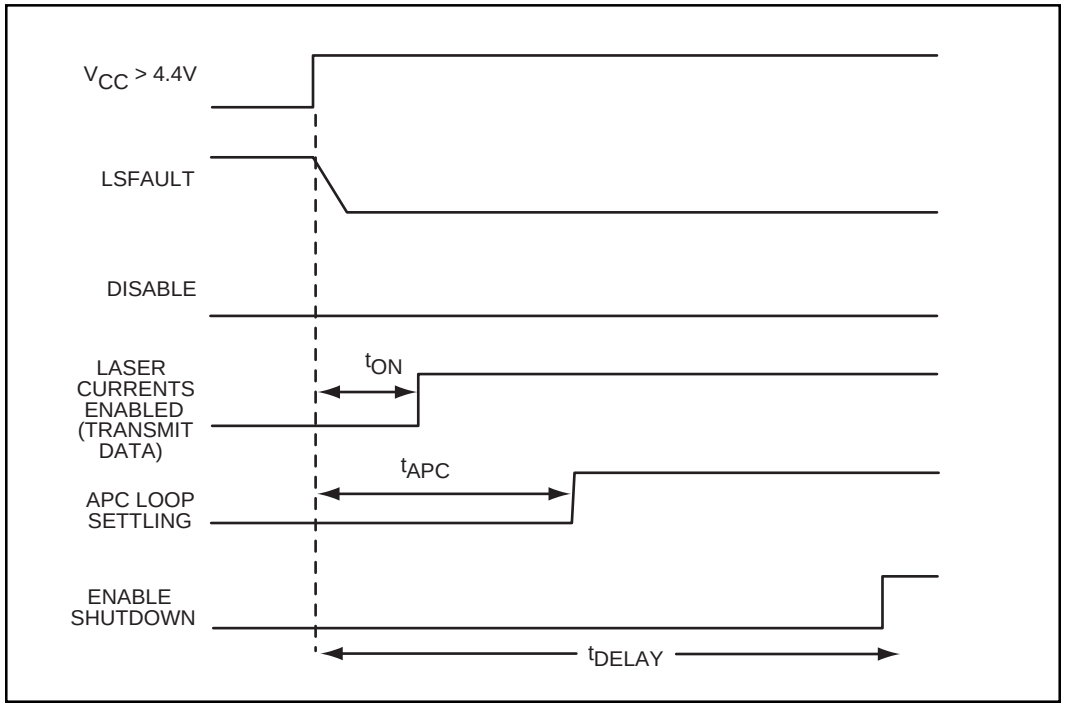
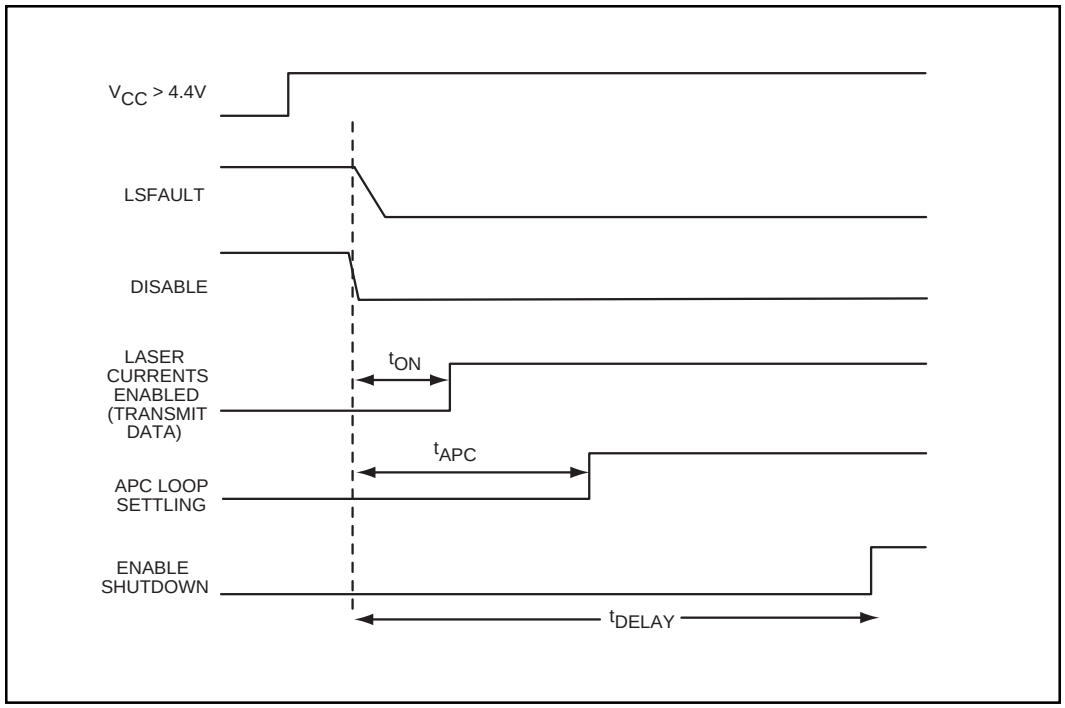


Figure 11. DISABLE Asserted



APPLICATION INFORMATION

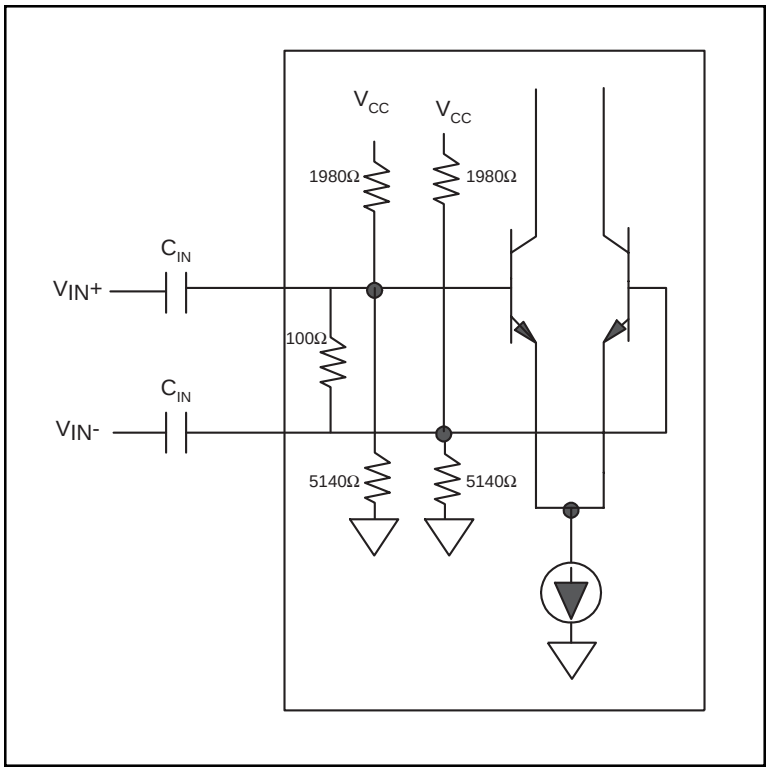
Power Dissipation Across Device

The power dissipation in the package must be kept below 640mW. Quiescent power is 399mW. Therefore, power dissipation due to the laser currents must be kept below 240mW.

Connecting to the Input of S3049

The equivalent input circuit of S3049 is shown in Figure 12. Both DC biasing and 50 ohm line termination have been implemented internally.

Figure 12. S3049 Equivalent Input Circuit for Data and Clock



Typical Operating Characteristics

Figure 13. Supply Current vs. Temperature, I_{MOD} = 0, I_{BIAS} = 0

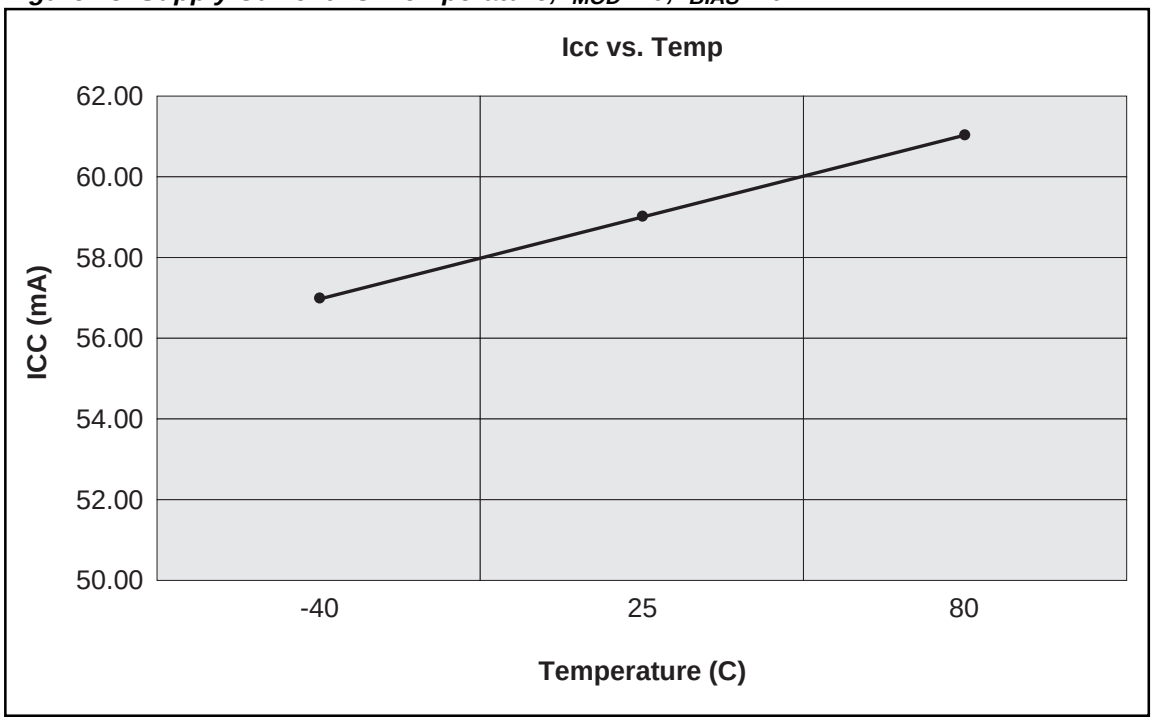


Figure 14. Modulation Current vs. Temperature

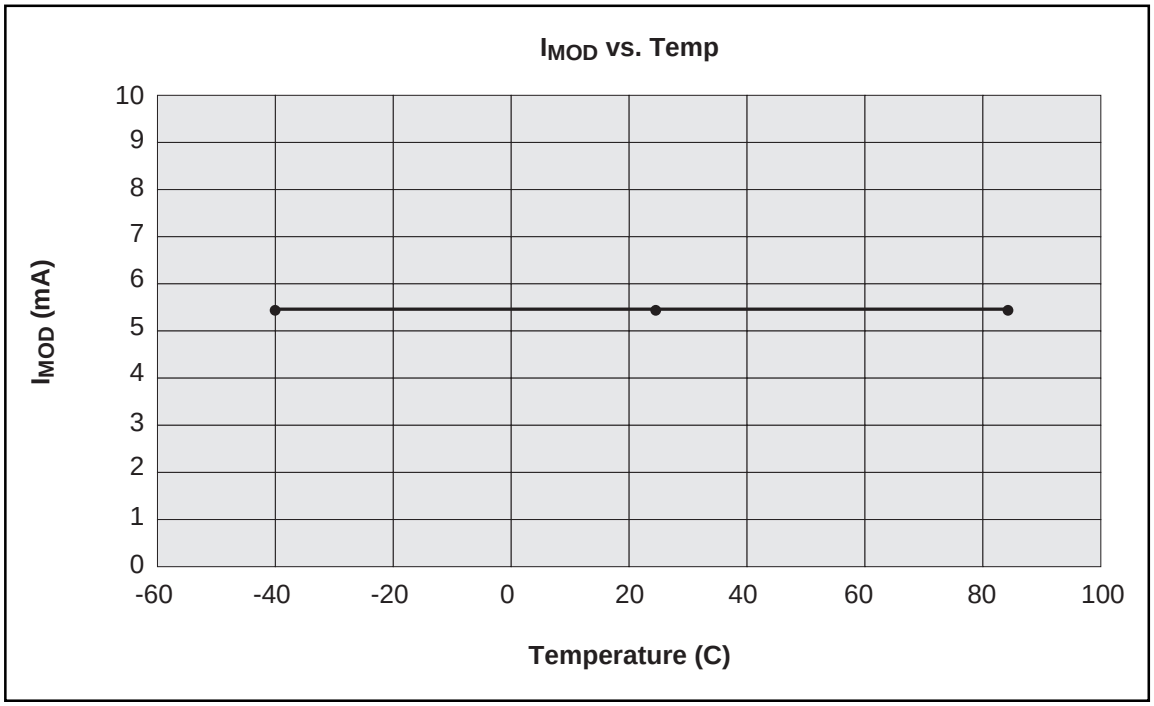
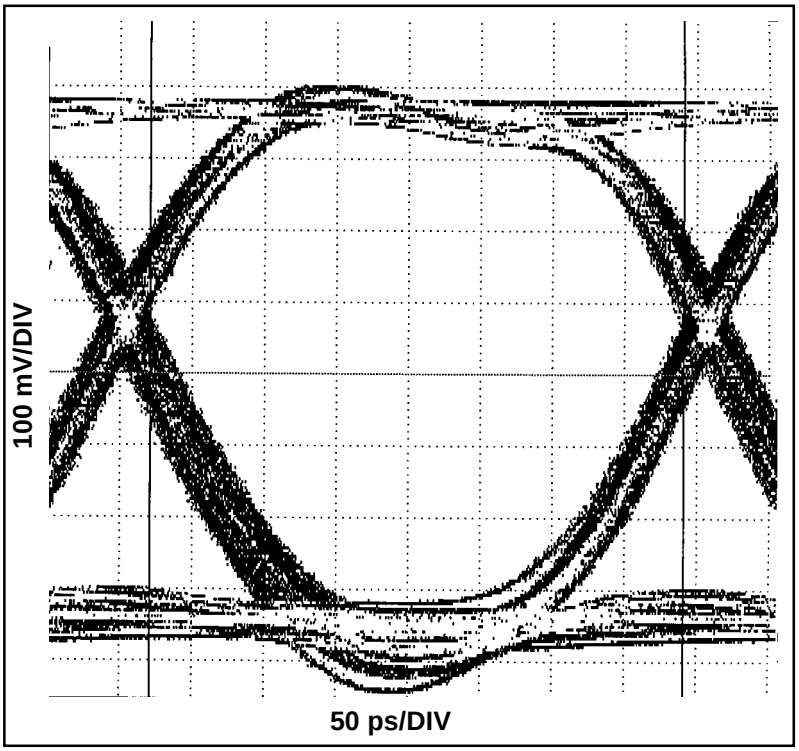
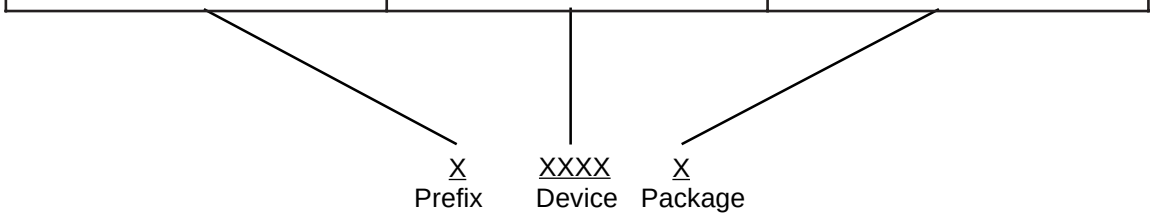


Figure 15. Eye Diagram, I_{MOD} = 30mA, 2.5 Gbps, 2^{23}–1 Pattern



Ordering Information

PREFIX	DEVICE	PACKAGE
S – Integrated Circuit	3049	A – 32 Pin TQFP B – Die



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