SONET/SDH CLOCK RECOVERY UNIT S3040B

FEATURES

- Micro-power Bipolar technology
- Complies with Bellcore, and ITU-T specifications for jitter tolerance, jitter transfer and jitter generation
- On-chip high frequency PLL with internal loop filter for clock recovery
- Supports clock recovery for OC-48/STM-16 (2488.32 Mbit/s) NRZ data
- 155.52 MHz reference frequency
- Lock detect—monitors frequency
- Low-jitter serial interface
- +5 V supply
- 32 TQFP Package

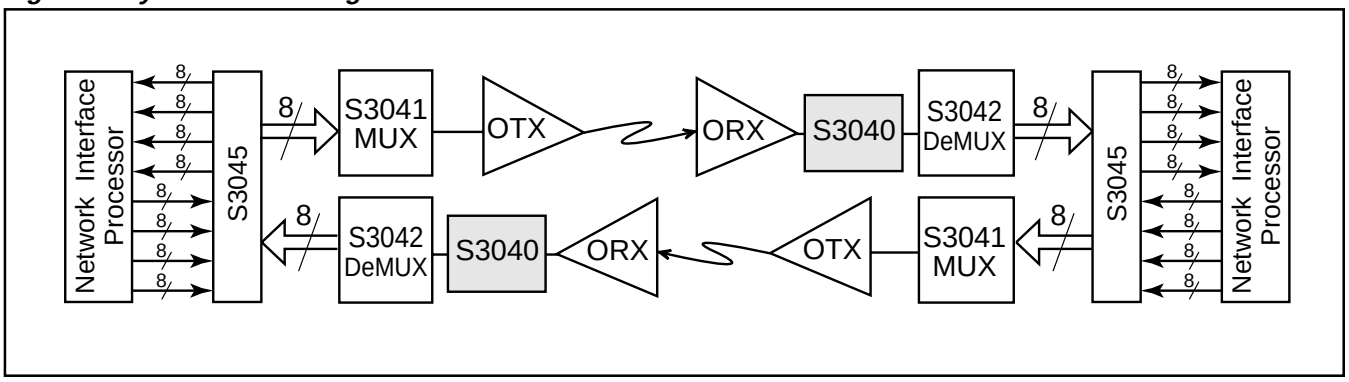
GENERAL DESCRIPTION

The function of the S3040 clock recovery unit is to derive high speed timing signals for SONET/SDH-based equipment. The S3040 is implemented using AMCC's proven Phase Locked Loop (PLL) technology.

The S3040 receives an OC-48/STM-16 scrambled NRZ signal and recovers the clock from the data. The chip outputs a differential bit clock and retimed data.

The S3040 utilizes an on-chip PLL which consists of a phase detector, a loop filter, and a Voltage Controlled Oscillator (VCO). The phase detector compares the phase relationship between the VCO output and the serial data input. A loop filter converts the phase detector output into a smooth DC voltage, and the DC voltage is input to the VCO whose frequency is varied by this voltage. A block diagram is shown in Figure 2.

Figure 1. System Block Diagram



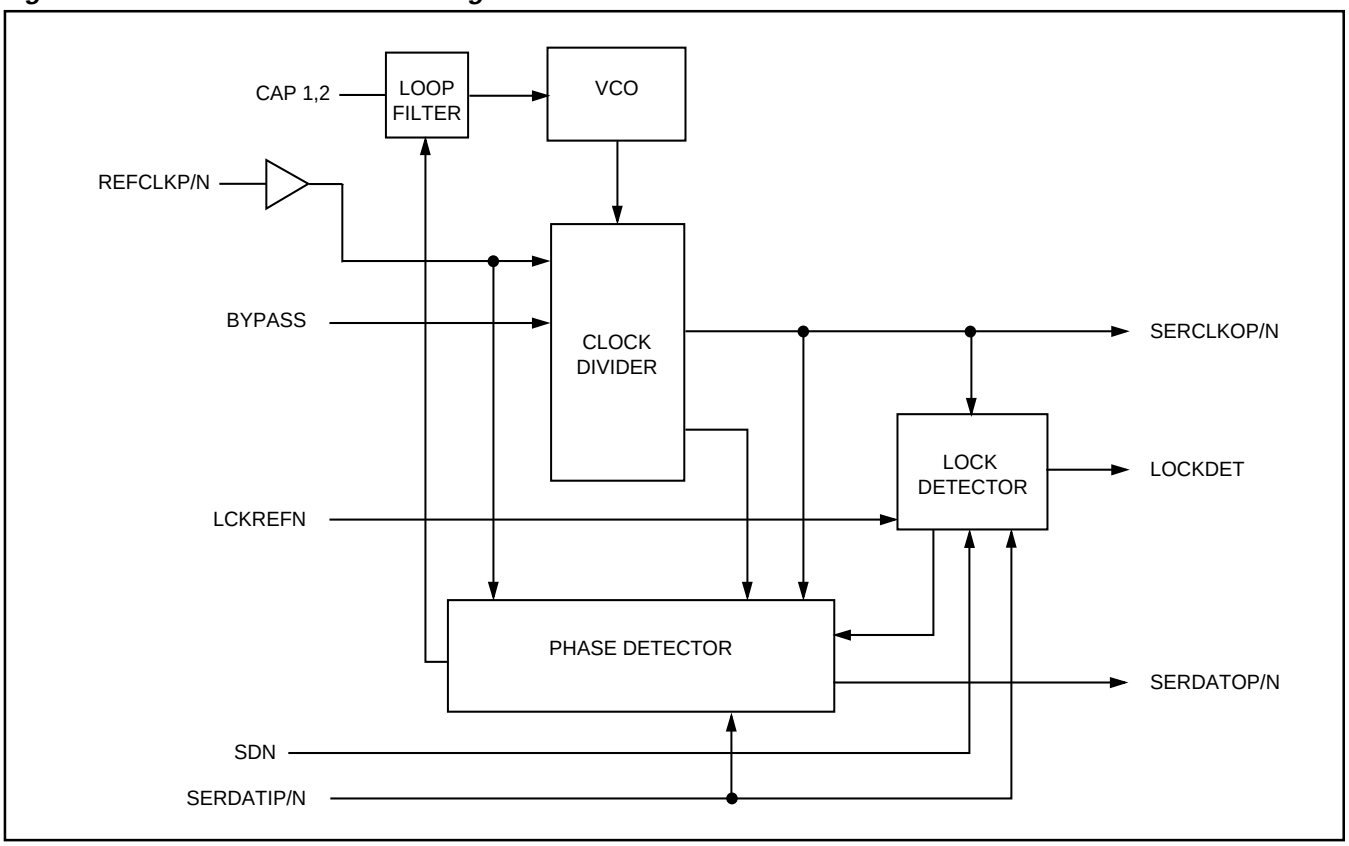
S3040 OVERVIEW

The S3040 supports clock recovery for the OC-48/ STM-16 data rate. Differential serial data is input to the chip at the specified rate and clock recovery is performed on the incoming data stream. An external oscillator is required to minimize the PLL lock time and provide a stable output clock source in the absence of serial input data. Retimed data and clock are output from the S3040.

Table 1. Suggested Interface Devices

Sumitomo	OC-48 Optical Receiver
AMCC S3044	OC-48 DeMUX
AMCC S3042	OC-48 DeMUX

Figure 2. S3040 Functional Block Diagram



S3040 FUNCTIONAL DESCRIPTION

The S3040 clock recovery device performs the clock recovery function for SONET OC-48 serial data links. The chip extracts the clock from the serial data inputs and provides retimed clock and data outputs. A 155.52 MHz reference clock is required for phase locked loop start-up and proper operation under loss of signal conditions. An integral prescaler and phase locked loop circuit is used to multiply this reference to the nominal bit rate.

Clock Recovery

Clock recovery, as shown in the block diagram in Figure 2, generates a clock that is at the same frequency as the incoming data bit rate at the serial data input. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

Frequency stability without incoming data is guaranteed by an alternate reference input (REFCLK) that the PLL locks onto when data is lost. If the frequency of the incoming signal with respect to REFCLKP/N varies by greater than the ppm specified in Table 3, the PLL will be declared out of lock, and the PLL will lock to the reference clock. The assertion of SDN will also cause an out of lock condition.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. This transfer function yields the typical capture time stated in Table 3 for random incoming NRZ data.

The total loop dynamics of the clock recovery PLL yield a jitter tolerance which exceeds the minimum tolerance proposed for SONET equipment by the Bellcore TA-NWT-000253 standard, shown in Figure 4.

Lock Detect

The S3040 contains a lock detect circuit which monitors the integrity of the serial data inputs. If the received serial data fails the frequency test, the PLL will be forced to lock to the local reference clock. This will maintain the correct frequency of the recovered clock output under loss of signal or loss of lock conditions. If the recovered clock frequency deviates from the local reference clock frequency by more than the ppm stated in Table 3, the PLL will be declared out of lock. The lock detect circuit will poll the input data stream in an attempt to reacquire lock to data. If the recovered clock frequency is determined to be within the ppm stated in Table 3, the PLL will be declared in lock and the lock detect output will go active.

CHARACTERISTICS

Performance

The S3040 PLL complies with the jitter specifications proposed for SONET/SDH equipment defined by the Bellcore Specifications: GR-253-CORE, Issue 2, December 1995 and ITU-T Recommendations: G.958 document, when used with differential inputs and outputs.

Input Jitter Tolerance

Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1 dB optical/electrical power penalty. SONET input jitter tolerance requirements are shown in Figure 3. The measurement condition is the input jitter amplitude which causes an equivalent of 1 dB power penalty.

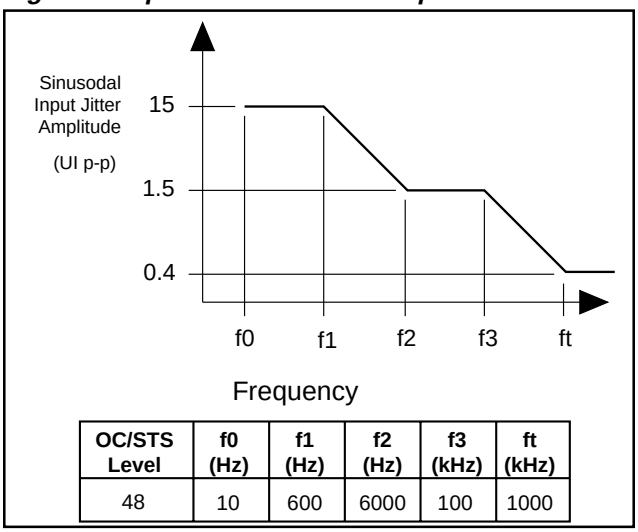
Jitter Transfer

Jitter transfer function is defined as the ratio of jitter on the output OC-N/STS-N signal to the jitter applied on the input OC-N/STS-N signal versus frequency. Jitter transfer requirements are shown in Figure 4. The measurement condition is that input sinusoidal jitter up to the mask level in Figure 3 be applied.

Jitter Generation

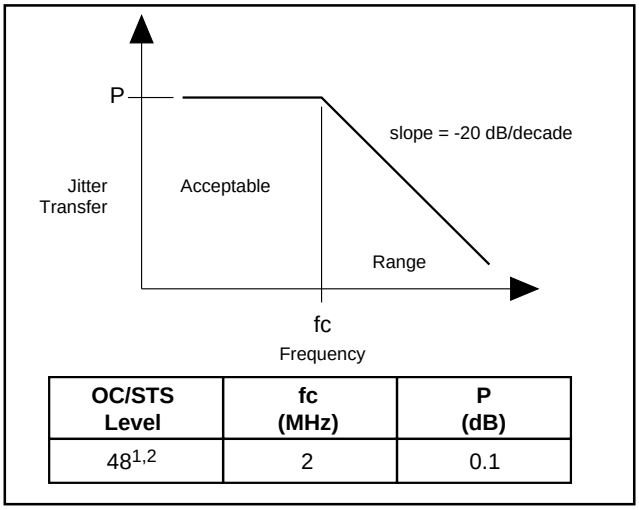
The jitter of the serial clock and serial data outputs shall not exceed 0.01 UI rms when a serial data input with no jitter is presented to the serial data inputs. (See Table 3).

Figure 3. Input Jitter Tolerance Specification



OC/STS Level	f0 (Hz)	f1 (Hz)	f2 (Hz)	f3 (kHz)	ft (kHz)
48	10	600	6000	100	1000

Figure 4. Jitter Transfer Specification



OC/STS Level	fc (MHz)	P (dB)
48[1,2]	2	0.1

1. Bellcore Specifications: GR-253- CORE, Issue 2, December 1995.
2. ITU-T Recommendations: G.958.

Table 2. Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin#	Description
SERDATIP/N	Diff. PECL	I	5,6	Serial Data In. (Internal Termination.) Clock is recovered from the transitions on these inputs.
BYPASS	TTL	I	20	Bypass Enable. Active High. Used during production test to bypass the VCO in the PLL. Tie to ground for normal operation.
SDN	PECL	I	11	Signal Detect. Active Low. A single-ended 10K PECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDN is inactive, the data on the Serial Data In (SERDATIP/N) pins will be internally forced to a constant zero, and the PLL will be forced to lock to the REFCLK inputs. When SDN is active, data on the SERDATIP/N pins will be processed normally.
REFCLKP/N	Diff. PECL	I	8,9	Reference Clock. 155.52 MHz input used to establish the initial operating frequency of the clock recovery PLL and also used as a standby clock in the absence of data, during reset or when SDN is inactive.
CAP1 CAP2		I	28,27	Loop Filter Capacitor. The loop filter capacitor and resistors are connected to these pins. The resistor values are 82 Ω ± 5%. The capacitor value should be 1.0 µF ± 10% tolerance, X7'R dielectric, 50 volt rating is recommended. (See Figure 13.)
LCKREFN	TTL	I	10	Lock to Reference. Active Low. When active, the serial clock output will be forced to lock to the local reference clock input [REFCLK].
SERDATOP/N	CML	O	19,18	Serial Data Out. This signal is the delayed version of the incoming data stream (SERDATI) updated on the falling edge of Serial Clock Out (SERCLKO).
SERCLKOP/N	CML	O	23, 22	Serial Clock Out. This signal is phase aligned with Serial Data Out (SERDATOP/N). (See Figure 7.)
LOCKDET	TTL	O	16	Lock Detect. Clock recovery indicator. Set High when the internal clock recovery has locked onto the incoming data stream. LOCKDET is an asynchronous output.
AVCC	+5V		2, 29	Analog power supply.
AVEE			3,4, 21,30	Analog GND connection.
VCC			12,14, 25	Power Supply.
VEE			13,15, 26	Ground connection connected to exposed heatsink.
NC			1, 7, 17, 24, 31, 32	No connection.

Figure 5. S3040 Pinout.

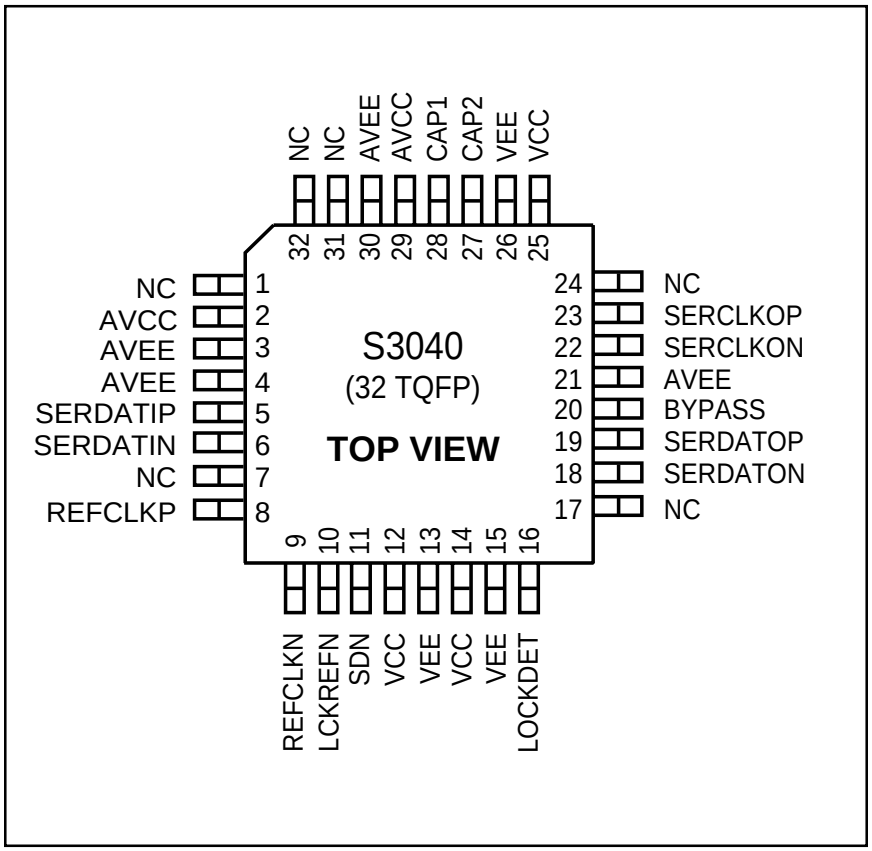
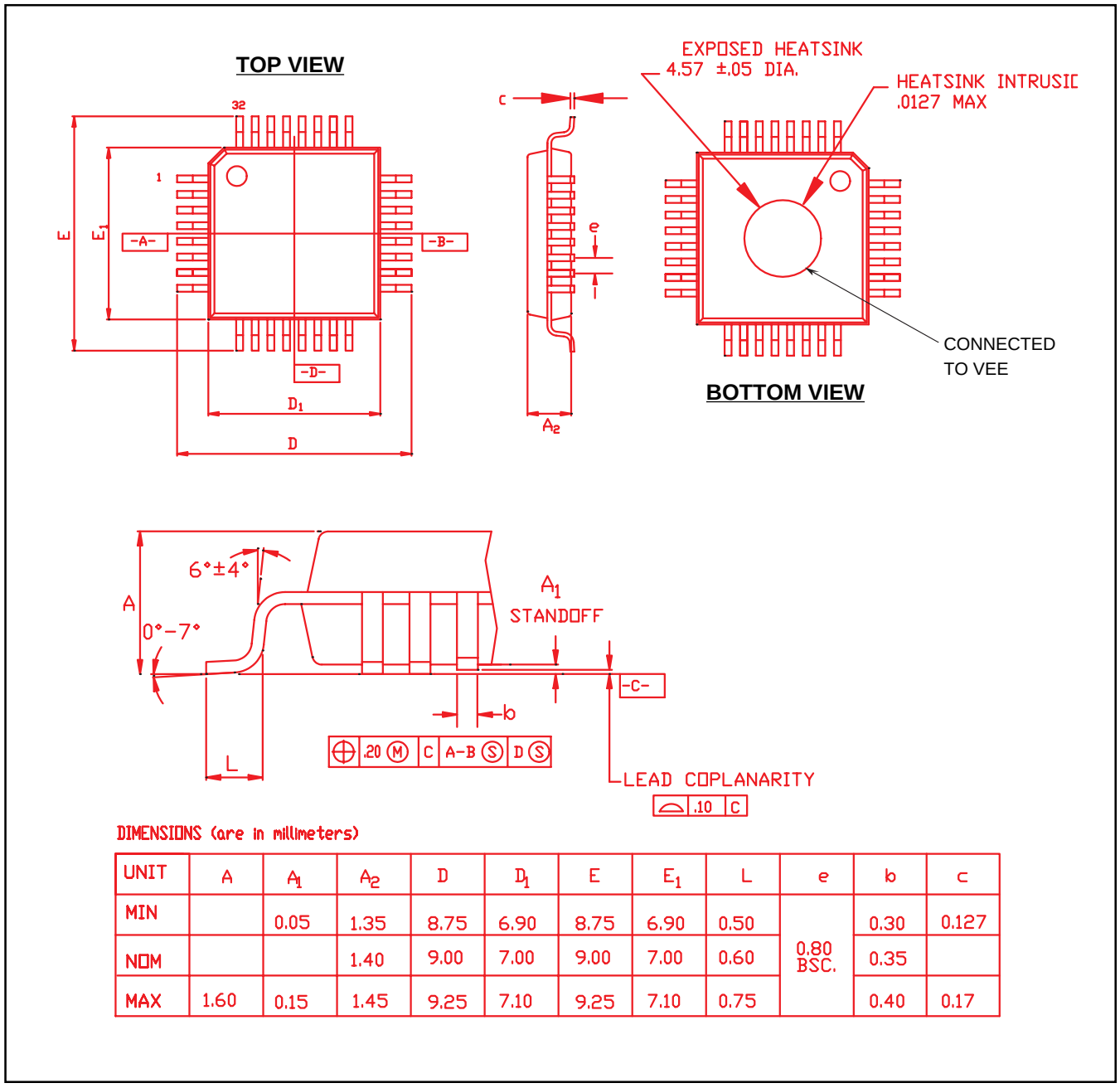


Figure 6. 32 TQFP Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.05	1.35	8.75	6.90	8.75	6.90	0.50	0.80 BSC.	0.30	0.127
NOM			1.40	9.00	7.00	9.00	7.00	0.60		0.35	
MAX	1.60	0.15	1.45	9.25	7.10	9.25	7.10	0.75		0.40	0.17

Note: The S3040 package is equipped with an embedded conductive heatsink on the bottom (board side). Active circuitry and vias should not appear in the area immediately under the package. This heatsink is electrically biased to the VEE potential of the S3040. For optimum thermal management, a foil surface at ground (or VEE if other than ground) is recommended immediately under the package, and connected with multiple vias to the internal plane(s) of similar potential. Thermally conductive epoxy or other conductive interposer can be used to establish a good thermal dissipation path.

Thermal Management

Device	Θja	Θjc
S3040	36˚ C/W with heatsink soldered to ground plane	2˚ C/W

Table 3. Performance Specifications

Parameters	Min	Typ	Max	Units	Conditions
Nominal VCO Center Frequency		2.5 ±12%		GHz	
Data Output Jitter with VCO locked to REFCLK **STS-48** 155.52 MHz Ref. Clk			0.01	UI (rms)	rms jitter, SDN active
Data Output Jitter with VCO locked to SERDATIP/N **STS-48**			0.01	UI (rms)	With no jitter on serial data inputs
Reference Clock Frequency Tolerance	-100		+100	ppm	
Capture Range Lock Range Capture Time		±200 ±12% 32		ppm µsec	With respest to fixed reference frequency
Acquisition Lock Time			16	µsec	Minimum transition density of 20% With device already powered up and valid ref. clk.
Reference Clock Input Duty Cycle	30%		70%	% of UI	
Reference Clock Rise and Fall Times			1.0	ns	20% to 80% of amplitude
CML Output Rise & Fall Times		100	150	ps	20% to 80%, 50 Ω load, 1pF cap
Frequency difference at which out of lock is declared (REFCLK compared to the divided down VCO clock)	340	600	732	ppm	
Frequency difference at which receive PLL is declared in lock (REFCLK compared to the divided down VCO clock)	244	300	366	ppm	
t_{SU} Setup time w.r.t. ↑ SERCLKOP	100			ps	
t_{H} Hold time w.r.t. ↑ SERCLKOP	100			ps	

Table 4. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature under Bias (industrial)	-40		+85	˚C
Ambient Temperature under Bias (commercial)	0		+70	˚C
Junction Temperature under Bias	-10		+130	˚C
Voltage on VCC with Respect to GND	4.75	5.0	5.25	V
Voltage on Any TTL Input Pin	0.0		VCC	V
Voltage on Any PECL Input Pin	VCC -2		VCC	V
ICC Supply Current		220	250	mA

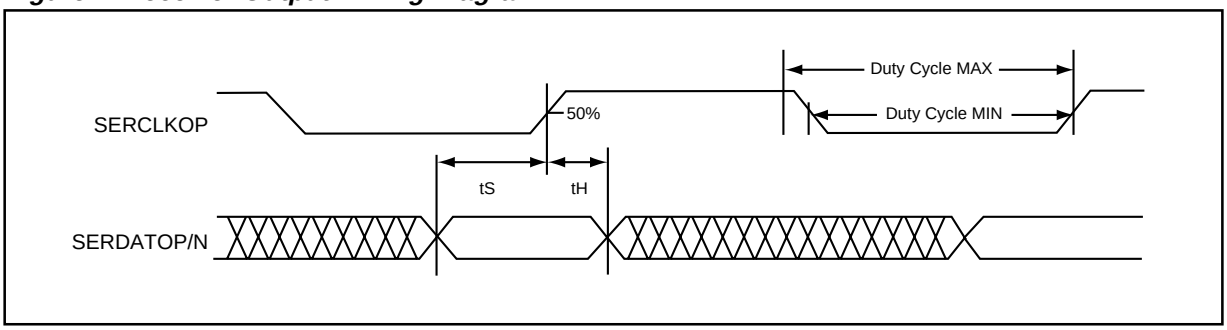
Table 5. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		+150	˚C
Voltage on VCC with Respect to GND	-0.5		+7.0	V
Voltage on any TTL Input Pin	-0.5		+5.5	V
Voltage on any PECL Input Pin	VCC -2.0		VCC	V
TTL Output Sink Current			20	mA
TTL Output Source Current			10	mA

EDS Rating

The S3040 is rated to the following ESD voltages based on the human body model: 1. All pins are rated at or above 1500 V except pin 5, pin 6, pin 27, and pin 28.

Figure 7. Receiver Output Timing Diagram



Note: Setup and hold time is the time in pico seconds from the cross-over point of the reference signal to the cross-over point of the output.

Table 6. Serial Input/Output DC Characteristics[1]

(T_A = -40°C to +85° C, V_{CC} = 5 V ± 5%)

Parameter	Description	Signal Name	Min	Max	Units	Conditions
V_{IL}[2]	Input Low Voltage		V_{CC} -2.00	V_{CC} -1.47	Volts	Guaranteed Input Low Voltage for all single ended inputs
V_{IH}[2]	Input High Voltage		V_{CC} -1.18	V_{CC} -0.80	Volts	Guaranteed Input High Voltage for all single ended inputs
V_{IL}[2]	Input Low Voltage		V_{CC} -2.0	V_{CC} -0.70	Volts	Guaranteed Input Low Voltage for all Differential inputs
V_{IH}[2]	Input High Voltage		V_{CC} -1.70	V_{CC} -0.45	Volts	Guaranteed Input Low Voltage for all Differential inputs
V_{ID}[2]	Input Diff Voltage		40	1000	mV	Guaranteed Input Diff Voltage for all Differential inputs
I_{IL}	Input Low Current	SDN	0	450	uA	V_{CC} = MAX, V_{IL} = Vcc -2 V
		SERDATIP/N	3.0	6.0	mA	V_{CC} = MAX, VDiff = 0.5 V
		REFCLKP REFCLKN	100	450	uA	V_{CC} = MAX, V_{IL} = Vcc -2 V
I_{IH}	Input High Current	SDN	100	500	uA	V_{CC} = MAX, V_{IH} = Vcc -0.80 V
		SERDATIP/N	3.5	6.4	mA	V_{CC} = MAX, VDiff = 0.5 V
		REFCLKP REFCLKN	100	500	uA	V_{CC} = MAX, V_{IH} = Vcc -0.80 V
V_{OL}	Output Low Voltage		V_{CC} -1.4	V_{CC} -0.5	Volts	100 Ω Line to Line
V_{OH}	Output High Voltage		V_{CC} -0.4	V_{CC}	Volts	100 Ω Line to Line
V_{OD}	CML Output single-ended Voltage Swing	SERDATOP/N SERCLKOP/N	280	600	mV	100 Ω Line to Line
V_{OD}	CML Output Diff Voltage Swing	SERDATOP/N SERCLKOP/N	560	1200	mV	100 Ω Line to Line

1. These conditions will be met with no airflow.
2. These input levels provide a zero-noise immunity and should only be tested in a static, noise-free environment.

Table 7. TTL Input/Output DC Characteristics[1]

(T_A = -40°C to +85° C, V_{CC} = 5 V ± 5%)

Parameter	Description	Min	Max	Units	Conditions
V_{IL}[2]	Input Low Voltage		0.8	Volts	Guaranteed Input Low Voltage for all inputs
V_{IH}[2]	Input High Voltage	2.0		Volts	Guaranteed Input Low Voltage for all inputs
I_{IL}	Input Low Current	-1		mA	V_{CC} = MAX, V_{IN} = 0.5 V
I_{IH}	Input High Current		50.0	uA	V_{CC} = MAX, V_{IN} = 2.7 V
I_I	Input High Current at Max V_{CC}		1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V
I_{OS}	Output Short Circuit Current	-40	-5.0	mA	V_{CC} = MAX, V_{OUT} = 0.5 V
V_{IK}	Input Clamp Diode Voltage	-1.2		Volts	V_{CC} = MIN, I_{IN} = -18.0 mA
V_{OL}	TTL Output Low Voltage		0.5	Volts	V_{CC} = MIN, I_{OL} = 4 mA
V_{OH}	TTL Output High Voltage	2.4		Volts	V_{CC} = MIN, I_{OH} = -1.0 mA

1. These conditions will be met with no airflow.
2. These input levels provide a zero-noise immunity and should only be tested in a static, noise-free environment.

Figure 8. +5 V Differential PECL Driver to S3040 Input Direct Coupled Termination

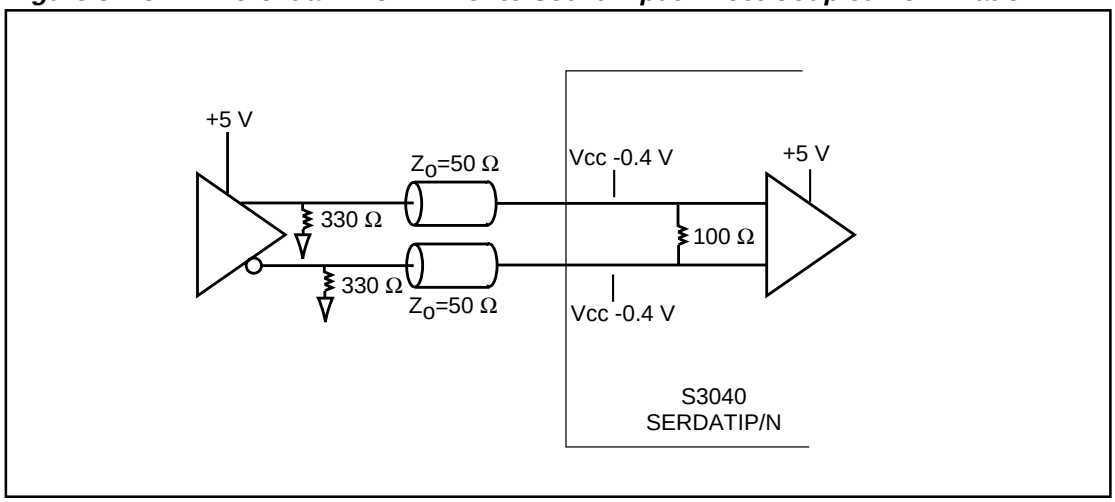


Figure 9. +5 V Differential PECL Driver to S3040 Input AC Coupled Termination

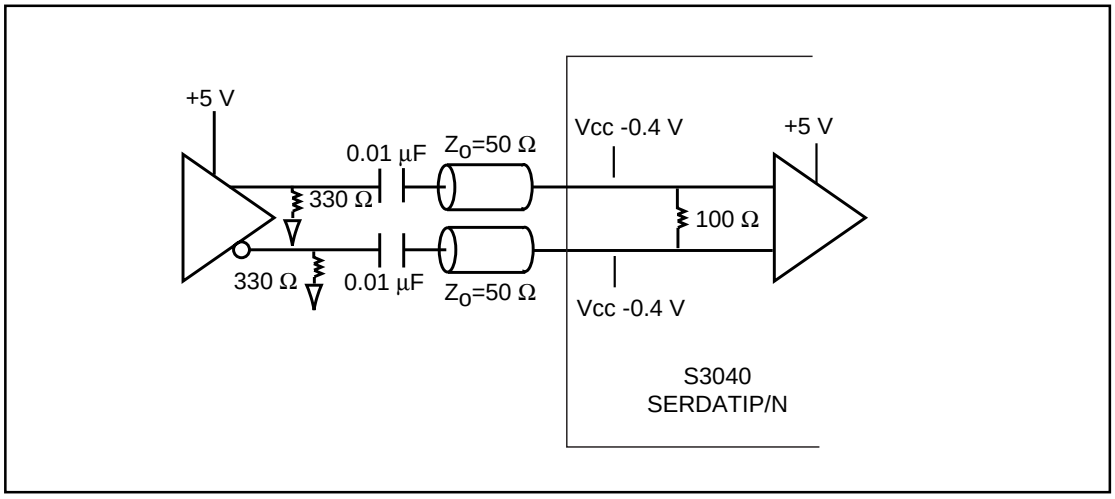


Figure 10. S3040 CML Output Driver to S3042/S3044 Terminations

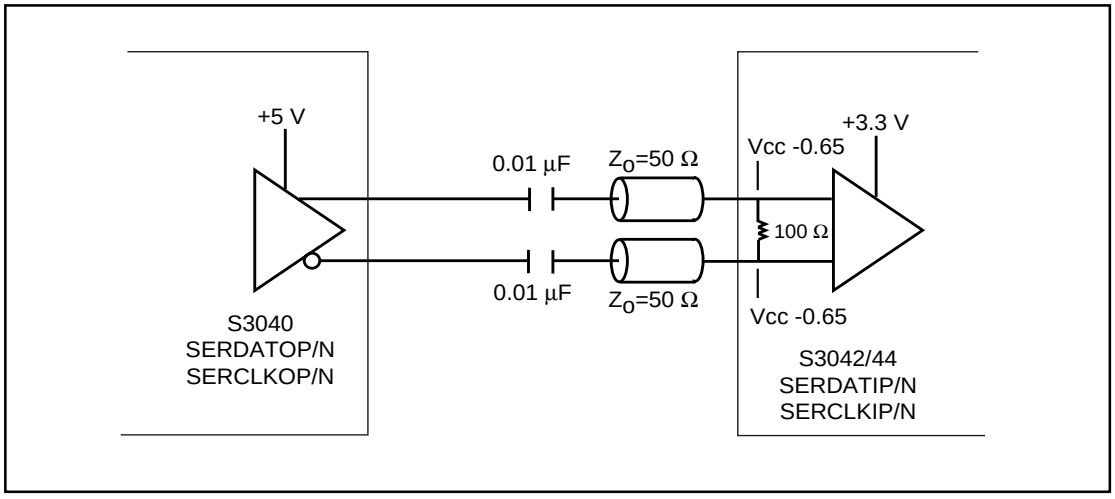


Figure 11. +3.3 V Single Ended LVPECL Driver to S3040 Reference Clock Input AC Coupled Termination

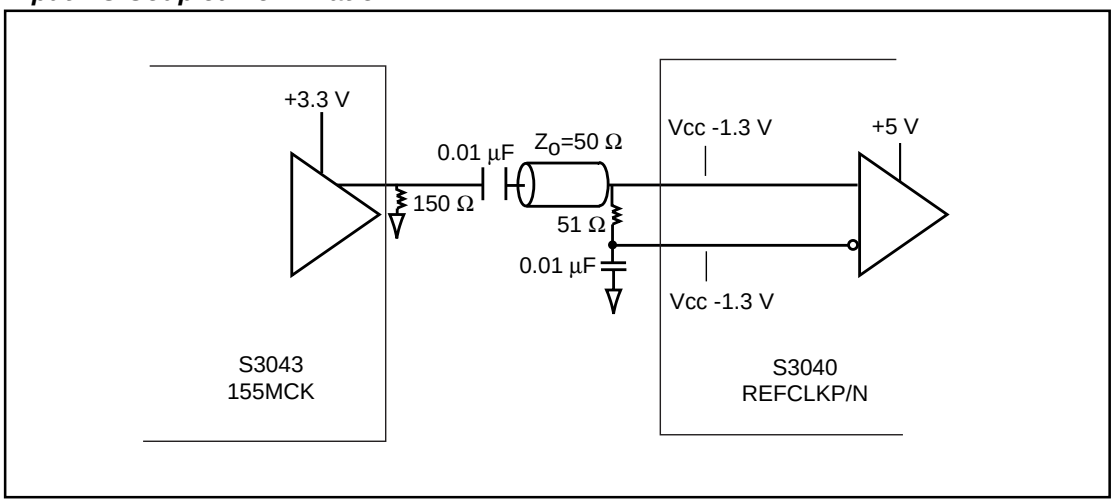


Figure 12. +5 V Differential PECL Driver to S3040 Reference Clock Input AC Coupled Termination

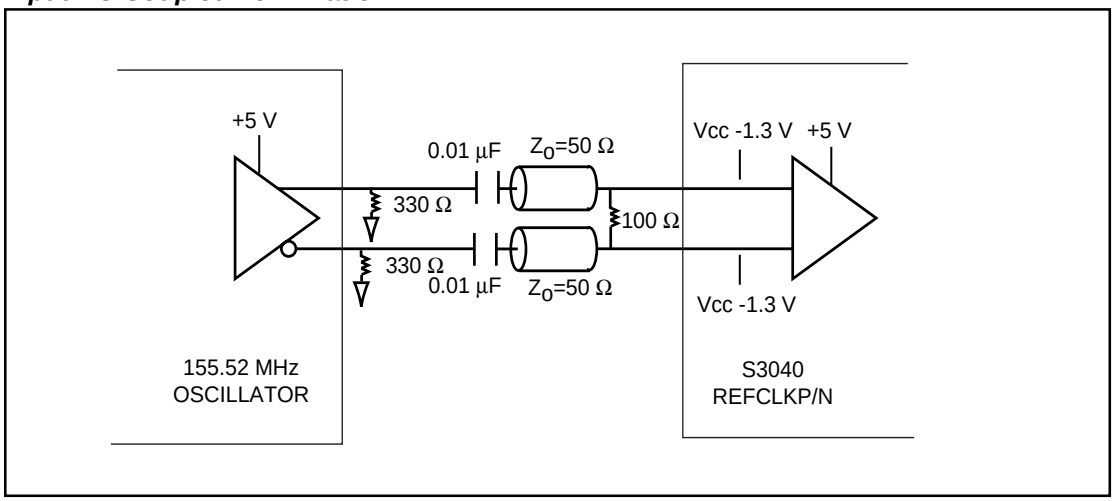
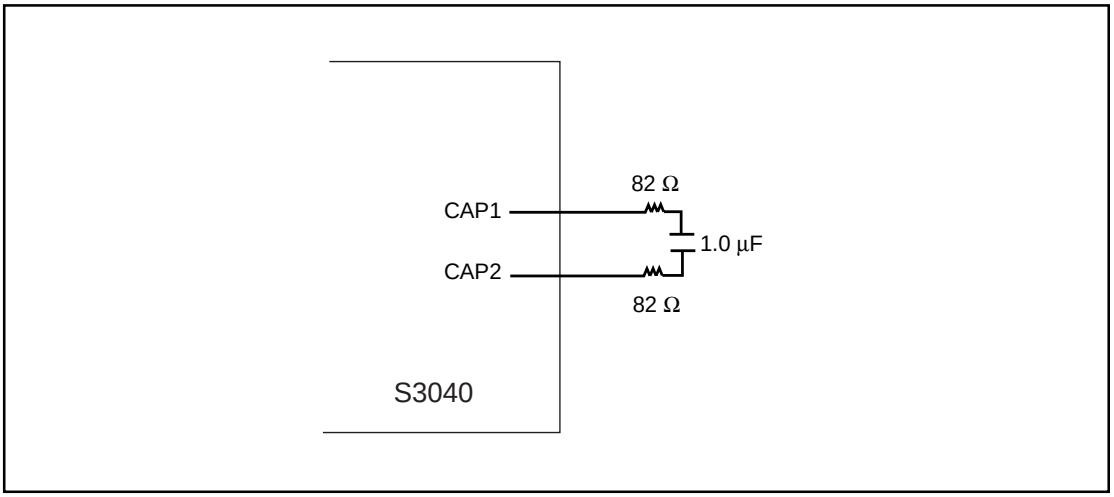


Figure 13. Loop Filter Capacitor Connections



Ordering Information

PREFIX	DEVICE	PACKAGE
S-commercial/ Industrial	3040	B – 32 TQFP

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